

# Low Ohmic contact resistance and high on/off ratio in transition metal dichalcogenides field-effect transistors via residue-free transfer

Ashok Mondal<sup>1,2</sup>, Chandan Biswas<sup>1,\*</sup>, Sehwan Park<sup>1,2</sup>, Wujoon Cha<sup>1</sup>, Seoung-Hun Kang<sup>3</sup>, Mina Yoon<sup>3</sup>,  
Soo Ho Choi<sup>1,2</sup>, Ki Kang Kim<sup>1,2</sup>, and Young Hee Lee<sup>1,2,4,\*</sup>

<sup>1</sup>Center for Integrated Nanostructure Physics, Institute for Basic Science, Sungkyunkwan University,  
Suwon 16419, Republic of Korea

<sup>2</sup>Department of Energy Science, Sungkyunkwan University, Suwon 16419, Republic of Korea

<sup>3</sup>Materials Science and Technology Division, Oak Ridge National Laboratory, Oak Ridge, Tennessee  
37831, United States of America

<sup>4</sup>Department of Physics, Sungkyunkwan University, Suwon 16419, Republic of Korea

\*Email: [chandan@skku.edu](mailto:chandan@skku.edu), [leeyoung@skku.edu](mailto:leeyoung@skku.edu)

## Abstract

**Beyond-silicon technology demands ultrahigh performance field-effect transistors (FETs). Transition metal dichalcogenides (TMDs) provide an ideal material platform, but the device performances such as contact resistance, on/off ratio, and mobility are often limited by the presence of interfacial residues caused by transfer procedures. Here, we show an ideal residue-free transfer approach using polypropylene carbonate (PPC) with a negligible residue coverage of ~0.08% for monolayer MoS<sub>2</sub> in the centimeter scale. By incorporating bismuth semimetal contact with atomically-clean monolayer MoS<sub>2</sub>-FET on h-BN substrate, we obtain an ultralow Ohmic contact resistance  $R_C$  of ~78  $\Omega\text{-}\mu\text{m}$ , approaching the quantum limit, and a record-high on/off ratio of ~10<sup>11</sup> at 15 K. Such an ultraclean fabrication approach could be the ideal platform for high-performance electrical devices using large-area semiconducting TMDs.**

High-performance field-effect transistor (FET) is an essential building block for next-generation semiconductor technologies beyond silicon-based complementary metal-oxide-semiconductor (CMOS)<sup>1</sup>. Three-dimensional (3D) silicon technology suffers from degradation of FET performances beyond sub-3-nm technology node<sup>2</sup>. One-atom thick (~0.7 nm) two-dimensional (2D) transition metal dichalcogenides (TMDs) offer an ideal FET platform and have been investigated intensively during the last decade to achieve high-performance FETs<sup>1</sup>. Nevertheless, practical applications of TMD-based FETs are limited due to wafer-scale integration incapability and fabrication-provoked residues<sup>3,4</sup>.

Recently, monolayer single-crystal TMDs grown by chemical vapor deposition (CVD) without involving grain boundaries are available in wafer-scale and suitable for integrated circuits<sup>5,6</sup>. Such atomically thin fragile TMD materials further require transfer to a desired gate dielectric substrate by facilitating mechanical supporting holder<sup>3</sup>. Traditionally, polymethyl methacrylate (PMMA) is used as a supporting holder for device transfer<sup>3,4</sup>. PMMA leaves notorious insulating residues on TMD surface which often generates mechanical damage to the TMD during transfer<sup>4,7</sup>. As an alternative to PMMA, several other polymers such as polydimethylsiloxane (PDMS), polyvinyl alcohol (PVA), polystyrene (PS),

polycarbonate (PC), ethylene vinyl acetate (EVA), polyvinylpyrrolidone (PVP) and organic molecules including paraffin, cellulose acetate, naphthalene have been proposed as a supporting holder<sup>3,7-9</sup>. Nevertheless, residues and mechanical damages are inevitably introduced during transfer and often degrade FET performances.

Different types of metal contacts have been investigated for TMD FETs<sup>10-19</sup>. Traditionally, titanium (Ti) is used as a low work-function metal contact for n-type MoS<sub>2</sub> on SiO<sub>2</sub> gate dielectric. The presence of a Schottky barrier and metal-induced gap states at the Ti-MoS<sub>2</sub> interface poses high contact resistance, low on/off ratio, Fermi level pinning, and poor mobility<sup>20</sup>. Indium metal is introduced in MoS<sub>2</sub>-SiO<sub>2</sub> FET to remove Fermi level pinning<sup>10,21</sup>. This leaves nearly Ohmic contact but the practical implementation could be limited due to low-temperature deposition requirement<sup>10,21</sup>. Recently, Weyl semimetal bismuth (Bi) contact is introduced for low contact resistance<sup>20</sup>. Nevertheless, the contact resistance is almost twice the quantum limit presumably owing to the PMMA-residue left-over at the interface.

Our aim is to search for a residue-free supporting holder for wafer-scale ultraclean transfer and to further demonstrate the state-of-the-art device performances including Ohmic contact resistance, high current on/off ratio, and on-current. Here, we show a residue-free transfer of CVD-grown TMD samples using polypropylene carbonate (PPC) as a supporting holder which leaves negligible residue coverage of ~0.08% on the TMD surface compared to traditional PMMA (~35%). PPC was previously used as a stamping holder in the typical dry-transfer process<sup>22,23</sup>. However, the stamping technique is suitable for the monolayer flake size of as small as 30-40  $\mu\text{m}$ <sup>23,24</sup>. A larger TMD flake size transferred by the conventional stamping technique introduces wrinkling, mechanical damage, and transfer inhomogeneity. A conventional stamping technique cannot be implemented for CVD-grown large samples for integrated circuits. A wafer-scale, residue-free wet-transfer process is deemed necessary for electronics integration.

Here we introduce a residue-free wet-transfer approach in which PPC-enabled transfer can address supporting holder contamination and flake wrinkling in the large-area homogeneous transfer of CVD-TMDs. FET device fabricated by PPC method with CVD-grown monolayer MoS<sub>2</sub> reveals Ohmic contact resistance of  $R_C \sim 78 \Omega\text{-}\mu\text{m}$  close to the quantum limit due to the absence of interfacial residues between MoS<sub>2</sub> and semimetal Bi. An ultrahigh current on/off ratio of  $\sim 10^{11}$  at 15 K was also achieved using the h-BN substrate. Our device exhibits state-of-the-art FET performances among all other previously reported literature values.

### **Advantages of residue-free transfer technique**

CVD-grown monolayer TMD flakes can be transferred using a traditional PMMA supporting holder (see Methods and Supplementary Fig. 1a)<sup>3,7-9</sup>. Similarly, PPC as a supporting holder was developed in this study to transfer CVD-grown monolayer MoS<sub>2</sub> (Supplementary Fig. 1b, 2-3). The complete removal of PMMA supporting holder is a major obstacle in the community to date<sup>3,25-27</sup>. For example, very thin PMMA residues (<20-30 nm thickness) exhibit low optical contrast/visibility and induce mechanical damage to the transferred 2D flakes<sup>3,8,9,25-27</sup>. PMMA residues remain more prominently in 2D heterostructure fabrication, in which mechanical damage to the top layer is often observed in previous reports<sup>28,29</sup>. Figure 1a shows a schematic and corresponding optical micrograph (lower panel) of the TMD heterostructure (bottom TMD1: WSe<sub>2</sub>, top TMD2: WS<sub>2</sub>) fabricated using conventional PMMA transfer method<sup>29</sup>. Interfacial PMMA

residue at TMD1/TMD2 interface (black arrows in Fig. 1a) emerged from TMD1 transfer and was optically invisible. After the removal of the top PMMA holder, the top TMD2 often suffers from mechanical damage (for example, crumbled flake shown in Fig. 1b). In contrast, this problem can be resolved by using the PPC-assisted transfer method. Here, PPC leaves negligible residues on the top of TMD1, TMD2, and at the interface, confirmed by the optical micrograph shown in Fig. 1c and Supplementary Fig. 1c (no crumbled flake).

The absence of PPC residues was further confirmed by atomic force microscopy (AFM). We chose monolayer MoS<sub>2</sub> as a typical TMD for residue coverage and further used for FET analysis later due to i) relatively higher carrier density ( $n_{2D}$  at  $V_g = 0$  V) among TMDs, ii) used as a benchmarking TMD material for FETs, and iii) standard semiconducting TMD material for contact resistance studies in previous literature<sup>12–20</sup>. PPC residues were negligibly present (after PPC holder removal) on MoS<sub>2</sub> as shown in optical image (Fig. 1d) and AFM topography (Fig. 1e) at high-resolution (Fig. 1f). AFM images were analyzed to quantify residue coverage as shown in Extended Data Fig. 1a–e with a marginal PPC residue coverage of  $\sim 0.08 \pm 0.0065\%$  (Extended Data Fig. 1b,e and Supplementary Note 1). This is well contrasted with PMMA residues with ( $\sim 35 \pm 0.0059\%$ ) coverage on MoS<sub>2</sub> (see Extended Data Fig. 1a,c). Similar behavior was observed on the SiO<sub>2</sub> substrate, where PPC residue was negligible compared to PMMA ( $\sim 43 \pm 0.0061\%$  coverage shown in Fig. 1g–i and Extended Data Fig. 1a,d). The roughness of the PPC-transferred sample (RMS  $\approx 0.66$  nm shown in Fig. 1j) was close to the monolayer MoS<sub>2</sub> thickness ( $\sim 0.7$  nm shown in Extended Data Fig. 1f), suggesting an ultraclean residue-free surface, in contrast with PMMA-transferred samples (RMS  $\approx 5.6$  nm). The roughness of PPC and PMMA residues on the SiO<sub>2</sub> substrate in Fig. 1k was similar to those of MoS<sub>2</sub> in Fig. 1j.

Eliminating PMMA residues from the TMD surface is a challenging process due to the high reactivity of the carbonyl group (C=O) in PMMA, which manifests strong adsorption energy on the 2D material surface<sup>7</sup>. The issue of PMMA residues on 2D materials is well-known problem in the community<sup>3,30</sup>. In order to understand the underlying causes of the variation in PMMA and PPC (Extended Data Fig. 2a–c) residues on the MoS<sub>2</sub> surface, we conducted a theoretical study employing density functional theory (DFT), as shown in Extended Data Fig. 2 and Supplementary Note 2. Carbonyl group of PMMA trimer on MoS<sub>2</sub> monolayer has higher adsorption energy (258 meV/cell) than PMMA backbone (101 meV/cell) from LDA calculations (Extended Data Fig. 2d). In PPC trimer, however, carbonyl group yields lower adsorption energy (91 meV/cell) than backbone (258 meV/cell), resulting in low adsorption energy in PPC-carbonyl than PMMA-carbonyl. These results are consistent across different exchange-correlation functionals in the DFT, including van der Waals correction schemes on PBE and LDA functional (see Extended Data Fig. 2e and f). For PMMA, significant charge transfer occurs when the highly reactive carbonyl group is close to MoS<sub>2</sub>, leading to strong adsorption. In PMMA, carbonyl group has two C=O bonds involving charge transfer and dipole moment, whereas PPC has a single C=O bond in proximity to the MoS<sub>2</sub> surface. This leads to stronger adsorption energy in PMMA than that of PPC. Insulating residues are known to increase contact resistance in electrical devices. This increase carrier and phonon scatterings and introduce doping effects in 2D materials<sup>3</sup>. Consequently, intrinsic 2D material properties such as electron mobility, thermal conductivity, and threshold voltage degrade drastically upon device performances<sup>3</sup>. Furthermore, wrinkles were significantly reduced in the PPC transfer process presumably due to higher Young's modulus by one order of magnitude stiffer than that of PMMA<sup>3,31,32</sup>.

The insulating nature of residues was investigated by using conductive AFM (C-AFM) measurements. A platinum-coated tip was used for contact mode scanning of monolayer MoS<sub>2</sub> transferred onto 50 nm-thick Pt substrate. Residue-free PPC-transferred MoS<sub>2</sub> sample shows uniform current distribution (Fig. 2a), which is in good contrast with the scattered spots (arrows) on PMMA-transferred MoS<sub>2</sub> (Fig. 2b). The mean resistance ( $R_{\text{mean}} \approx 1.5 \text{ G}\Omega$ ) of PPC-transferred sample was lower than that ( $R_{\text{mean}} \approx 4.6 \text{ G}\Omega$ ) of PMMA-transferred sample. The resistance profiles were extracted arbitrarily from PPC and PMMA (dashed lines) samples to compare resistance variations (Fig. 2c). The PPC-transferred MoS<sub>2</sub> sample is rather uniformly distributed and shows low resistance variations (red), suggesting residue-free uniform electrical properties. In contrast, some spots with high resistance as high as  $\sim 95 \text{ G}\Omega$  was observed on top of the PMMA residues.

Photoluminescence (PL) characterization was performed with three samples; i) as-grown MoS<sub>2</sub> (without precursor cleaning), ii) PMMA-transferred MoS<sub>2</sub> (after precursor cleaning), and iii) PPC-transferred MoS<sub>2</sub> (after precursor cleaning). The CVD-grown TMD materials inevitably introduce some remaining metal precursors during CVD growth<sup>33,34</sup>, which can be removed after transfer<sup>33,34</sup>. PL spectrum of PPC-transferred monolayer MoS<sub>2</sub> shows standard A-exciton near 1.88 eV and B-exciton near 2.02 eV under low excitation power (135  $\mu\text{W}$ ) (Fig. 2d)<sup>35</sup>. By increasing excitation power to 10.5 mW (Fig. 2e), the PPC sample exhibits significantly high PL intensity,  $\sim 20$  times higher than the PMMA sample. Power-dependent PL intensity was also plotted in Fig. 2f-h (and Supplementary Fig. 5) with different samples. PL peaks of the as-grown sample emerged from excitation power of  $\sim 0.4 \text{ mW}$  ( $P_{\text{th}}$  shown in Fig. 2f) and attributed to the remaining precursors, as illustrated in AFM 3D topography (inset) and optical micrograph (Supplementary Fig. 4a). Similar  $P_{\text{th}}$  value was obtained from PMMA sample (Supplementary Fig. 4b). Although precursors were removed during the transfer, the  $P_{\text{th}}$  value remained same due to the emergence of PMMA residue (Fig. 2g). In contrast,  $P_{\text{th}}$  value from PPC sample was remarkably improved to 70  $\mu\text{W}$  (Fig. 2h). The enhanced PL intensity was attributed to the absence of PPC residues (Supplementary Fig. 4c). In contrast, PL signal was reduced due to the absorption from precursors and PMMA residues.

### Ultralow contact resistance

We next investigate electrical performances of residue-free MoS<sub>2</sub> FET using a top gate to elucidate the effect of residues with PMMA and PPC (Fig. 3a). Five sets of device types were compared: i) PPC-transferred Weyl semimetal Bi contact FET on h-BN substrate (Device1, PPC-Bi: h-BN/MoS<sub>2</sub>/h-BN), ii) that on SiO<sub>2</sub> substrate (Device2, PPC-Bi: SiO<sub>2</sub>/MoS<sub>2</sub>/h-BN), iii) PPC-transferred Ti contact FET on SiO<sub>2</sub> substrate (Device3, PPC-Ti: SiO<sub>2</sub>/MoS<sub>2</sub>/h-BN), iv) PMMA-transferred Bi contact FET on SiO<sub>2</sub> substrate (Device4, PMMA-Bi: SiO<sub>2</sub>/MoS<sub>2</sub>/h-BN), and v) PMMA-transferred Ti contact FET on SiO<sub>2</sub> substrate (Device5, PMMA-Ti: SiO<sub>2</sub>/MoS<sub>2</sub>/h-BN). Figure 3b shows contact resistance extracted from the conventional transfer-length method (TLM) on monolayer MoS<sub>2</sub> FET<sup>13,20</sup>. The contact resistance in Device1 was  $\sim 78 \text{ }\Omega\text{-}\mu\text{m}$  at 15 K ( $V_{\text{g}} = 12 \text{ V}$ ), lower than  $\sim 92 \text{ }\Omega\text{-}\mu\text{m}$  in Device2 with SiO<sub>2</sub> substrate (Supplementary Table 1).  $R_{\text{C}}$  in Device1 was slightly increased to  $\sim 111 \text{ }\Omega\text{-}\mu\text{m}$  at room temperature, which is the lowest among other devices. Similar behavior of contact resistance was also shown with  $V_{\text{g}} = 0 \text{ V}$ , although contact resistances of all the devices were slightly high due to low carrier density at  $V_{\text{g}} = 0 \text{ V}$  (Extended Data Fig. 3). Such a low contact resistance is attributed to residue-free interfacial contact between Weyl semimetal Bi and MoS<sub>2</sub> to overcome the Fermi level pinning, and h-BN substrate to minimize substrate scattering.

PPC-Bi contact on SiO<sub>2</sub> substrate (Device2) shows a linear I<sub>d</sub>-V<sub>d</sub> relationship to a large drain voltage of up to 2.5 V, independent of the temperature, confirming Ohmic contact behavior (Fig. 3c, Supplementary Fig. 6 and 7a-c). The R-T shows non-linear metallic behavior (inset) similar to the previous report<sup>20</sup>. The Schottky barrier height ( $\Phi_B$ ) was extracted from a typical Arrhenius plot<sup>20,36</sup> (Fig. 3d). PMMA-Ti contact device shows a negative slope ( $\Phi_B = 33$  meV) whereas, the PPC-Bi device shows a nearly constant  $\Phi_B$  slope at low temperature (<50 K) and a positive slope at high temperature. This suggests the Arrhenius transport model is inapplicable to Bi contact which is similar to the previous report<sup>20</sup>. Furthermore, it does not satisfy T<sup>2</sup> transport (ideal thermionic emission model) shown in Supplementary Fig. 7d. The nonlinearity (N) can be extracted from the I<sub>d</sub>-V<sub>d</sub> which verifies zero SBH (N = 0)<sup>20</sup>. At room temperature, nonlinearity was close to zero for both Bi and Ti contact samples. The nonlinearity increased (N ≠ 0) with decreasing temperature in the PMMA-Ti sample (Device5), shown in Fig. 3e. Meanwhile, the PPC-Bi contact sample (Device2) shows N=0 in all temperatures. This confirms Ohmic contact in the PPC-Bi device.

Figure 3f demonstrates the benchmark with the state-of-the-art R<sub>C</sub>-n<sub>2D</sub> (2D carrier density) in different metal contacts used in various semiconductor technologies for monolayer MoS<sub>2</sub>-FET<sup>10-19,37</sup>. Bi MoS<sub>2</sub>-FET (Device1) exhibits the lowest R<sub>C</sub> (~78 Ω-μm) at 2D carrier density, n<sub>2D</sub> ≈ 1.1 × 10<sup>13</sup> cm<sup>-2</sup> at 15 K. The contact resistance was slightly decreased at higher n<sub>2D</sub>. All Bi contact devices show significantly lower R<sub>C</sub> (yellow region) compared to conventional metal contacts (grey region) used in this study (Ti) and literature<sup>10-19</sup>. At zero V<sub>g</sub> (n<sub>2D</sub> ≈ 1.5 × 10<sup>12</sup> cm<sup>-2</sup> black arrow in Fig. 3f), R<sub>C</sub> reached close to the theoretical quantum limit<sup>38,39</sup> (dashed line) of 66 Ω-μm.

### Ultrahigh on/off ratio field-effect transistor

Figure 4a,b demonstrate the transfer characteristics (I<sub>d</sub>-V<sub>g</sub>) of the Bi contact and Ti contact devices for comparison. PPC-Bi contact FET on h-BN substrate (Device1) showed an ultrahigh on/off ratio of 3.2 × 10<sup>9</sup> at 300 K (Supplementary Fig. 8). On/off ratio was slightly reduced in PPC-Bi contact FET on SiO<sub>2</sub> substrate (Device2) due to the substrate-induced charge scattering. In contrast, in PMMA-Bi FET on SiO<sub>2</sub> substrate (Device4), on/off ratio was significantly reduced to 2.2 × 10<sup>6</sup> by three orders of magnitude (Fig. 4a, Supplementary Fig. 9) due to the transfer-provoked PMMA residues. When Ti was used as a contact, the contact resistance was as high as ~10<sup>5</sup> Ω-μm (Supplementary Table. 1). The effect of residues dominated in the PMMA sample, nevertheless PPC slightly increases the on/off ratio of 10<sup>6</sup> (Fig. 4b and Supplementary Fig. 10-11). Temperature-dependent transfer characteristics were compared for Bi and Ti contact devices (Fig. 4c,d). The elevated current with decreasing temperature in the PPC-Bi FET device (Fig. 4c) was similar to the previous report<sup>20</sup>, and opposite to the PPC-Ti device (Fig. 4c inset) due to the high contact resistance of Ti electrode<sup>40,41</sup>. Interestingly, the residue-free PPC-Bi contact FET on the h-BN substrate (Device1) shows an ultrahigh on/off ratio ~10<sup>11</sup> at 15 K (Fig. 4d, Supplementary Fig. 8). The temperature-dependent current variation (black arrow) in h-BN substrate (Device1) sample was lower (Fig. 4d inset) than SiO<sub>2</sub> substrate sample (Device2) due to the reduced charge scattering and low contact resistance. Figure 4e summarizes on/off ratios at two temperatures (15 and 300 K) for all Bi-contact samples. At room temperature, the h-BN-based PPC-Bi device (Device1) shows a consistently high on/off ratio compared to SiO<sub>2</sub>-based devices fabricated with PPC transfer (Device2) as well as with PMMA transfer (Device4). This trend is similar for PPC-Bi samples (Device1) at 15 K but an ultrahigh on/off ratio of 1.4 × 10<sup>11</sup> was reached ( see Supplementary Fig. 6, 8, and 9).

Figure 4f compares two-probe (2P) mobility ( $\mu_{FE}$ ) of MoS<sub>2</sub> FETs with Bi and Ti contacts. PPC-Ti-contact device (black) showed the lowest mobility due to high  $R_C$  and SBH compared to Bi-contact devices. The highest mobility was 19.2 cm<sup>2</sup>/Vs at 300 K in the PPC-Bi contact device on the h-BN substrate (Device1). The mobility was reduced marginally to 7.6 cm<sup>2</sup>/Vs in PPC-Bi contact (blue) on the SiO<sub>2</sub> substrate (Device2) due to carrier scattering from SiO<sub>2</sub> substrate<sup>42,43</sup>. PMMA-Bi-contact device (Device4) on SiO<sub>2</sub> substrate exhibited much lower mobility due to the high  $R_C$  from the residues in the metal-TMD interface. The high  $R_C$  effect on mobility became clear in the four-probe mobility measurements shown in Fig. 4g. No significant mobility difference was observed between four-probe and two-probe in the PPC-Bi device (Device2), implying the low  $R_C$  effect. In contrast, two-probe mobility was lower than the four-probe mobility attributed to the high  $R_C$  effect in the PPC-Ti contact device (Device3). In addition to four-probe mobility, four-probe resistance was also examined for all devices (Extended Data Fig. 4). PPC-Bi device (red) shows the lowest  $R_{4P}$  ( $\sim 7.8 \times 10^5 \Omega$ ) followed by PMMA-Bi ( $\sim 1.9 \times 10^8 \Omega$ ), PPC-Ti ( $\sim 4.9 \times 10^8 \Omega$ ), and PMMA-Ti ( $\sim 8.7 \times 10^9 \Omega$ ) devices.

### Benchmark with other semiconductor technologies

Figure 5a compares the on/off ratio with  $R_C$  of the semimetal Bi contact (PPC-Bi, PMMA-Bi) with different metal contacts including In, Ag, Au, Ni, and Cr in the literature (Extended Data Table 1). It was clear to see that the reduction of  $R_C$  below 0.2 k $\Omega$ - $\mu\text{m}$  sharply elevates the on/off ratio (yellow region). PMMA-Bi device (Device4) exhibited comparable device performance with the previous report<sup>20</sup>. We note that the FET device performance in previous report<sup>20</sup> was limited due to PMMA residues between Bi and MoS<sub>2</sub>, leaving the charge scattering in the MoS<sub>2</sub> channel from the gate dielectric substrate (SiN<sub>x</sub>, SiO<sub>2</sub>) and open-atmospheric effects. In contrast, Bi-contact MoS<sub>2</sub>-FET fabricated using the residue-free PPC wet-transfer method (PPC-Bi, Device2) gave rise to improving  $R_C$  ( $\sim 112 \Omega$ - $\mu\text{m}$ ) with nearly one order of magnitude higher on/off ratio ( $\sim 10^9$ ). The device performance was further improved in the state-of-the-art device (PPC-Bi h-BN, Device1) using low carrier scattering in an h-BN double-encapsulated MoS<sub>2</sub> channel at room temperature and 15 K up to  $R_C \sim 78 \Omega$ - $\mu\text{m}$  with an on/off ratio of  $\sim 10^{11}$ .

The maximum on-current ( $I_{on-max}$ ) versus on/off ratio is a critical benchmark of high-performance FET devices for signal processing<sup>44,45</sup>. Figure 5b demonstrates  $I_{on-max}$ -on/off ratio benchmark in different semiconductors such as thin metal oxide (ITO), MoS<sub>2</sub>, metal oxides (IGZO, ZnO), and black phosphorus (BP)<sup>44,46-62</sup>. PPC-Bi contact device on the h-BN substrate (Device1) shows an ultrahigh on/off ratio  $\sim 10^{11}$  (Fig. 4e, Supplementary Fig. 8) and  $I_{on-max} \approx 1.4 \text{ mA}/\mu\text{m}$  at 15 K (see Supplementary Fig. 7b), superseding all existing materials. The  $I_{on-max}$  slightly reduced in PPC-Bi on SiO<sub>2</sub> substrate (Device2) to  $\approx 1.2 \text{ mA}/\mu\text{m}$  at 15 K (Supplementary Fig. 7c). It should be noted that all Bi contact devices show Ohmic contact nature (Supplementary Table 1) independent of the presence of residues. Nevertheless, FET device performance was significantly limited in PMMA-Bi Device4 due to the presence of carrier scattering from insulating PMMA residues (Supplementary Fig. 12). Residue-free Bi-contact FETs based on other TMD (such as WS<sub>2</sub>) show Ohmic conduction (Supplementary Fig. 13) with a higher on/off ratio ( $\sim 2.1 \times 10^9$ ) compared to PMMA residue-based WS<sub>2</sub>-FET ( $\sim 10^7$ )<sup>20</sup>. On the contrary, residue-free Bi contact MoS<sub>2</sub>-FET (PPC-Bi, Device1 and Device2) exhibited ultrahigh FET device performance outperforming earlier reports (Fig. 5). These results highlight that the residue-free monolayer MoS<sub>2</sub> FET performance can supersede other 2D and 3D materials reported earlier.

## Conclusions

In summary, our demonstrated MoS<sub>2</sub>-FETs establish a new benchmark with low R<sub>C</sub> of  $\sim 78 \pm 12 \text{ } \Omega\text{-}\mu\text{m}$  and ultrahigh on/off ratio of  $\sim 10^{11}$ . Residue-free semimetal Bi contact with the top and bottom encapsulation of monolayer MoS<sub>2</sub> results in such an ultrahigh FET performance. Moreover, this process was developed for CVD-grown TMD for wafer-scale clean transfer (Supplementary Fig. 14-16) with low adsorption energy of the PPC on the TMD surface (Extended Data Fig. 2, Supplementary Note 2, Supplementary Fig. 17) and could be easily implemented for large-scale integrated circuit technologies.

## Acknowledgements

This work was supported by the Institute for Basic Science of Korea (IBS-R011-D1) and Advanced Facility Center for Quantum Technology. A.M. and C.B. acknowledge Dr. Pramod Ghising for the scientific discussion. Authors acknowledge Sung Gyu Lee for the training of the C-AFM. Theory work was supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, Materials Sciences and Engineering Division (M.Y.) and by the U.S. Department of Energy (DOE), Office of Science, National Quantum Information Science Research Centers, Quantum Science Center (S.-H.K.) and this research used resources of the Oak Ridge Leadership Computing Facility at the Oak Ridge National Laboratory, which is supported by the Office of Science of the U.S. Department of Energy under Contract No. DE-AC05-00OR22725 and resources of the National Energy Research Scientific Computing Center, a DOE Office of Science User Facility supported by the Office of Science of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231 using NERSC award BES-ERCAP0024568. K.K.K. acknowledges support from the Basic Science Research (2022R1A2C2091475) and Next-generation Intelligence Semiconductor Program (2022M3F3A2A01072215) through the National Research Foundation of Korea (NRF), which is funded by the Ministry of Science, ICT & Future Planning.

## Author Contributions Statement

C.B. and Y.H.L. supervised the project. A.M., C.B. proposed and developed the project. A.M., C.B. and Y.H.L. designed the experiments. A.M. carried out the device fabrication, transfer of materials, and performed the all-electrical characterization supervised by C.B. W.C. and A.M. measured the C-AFM, AFM respectively. All AFM data analysis was performed by W.C, A.M., and C.B. S.P., S.H.C contributed to the growth of materials. TEM measurements and analysis carried out by A.M., C.B., S.H.C. and K.K.K. The DFT calculations were performed by S.H.K., M.Y. A.M., C.B. and Y.H.L wrote the manuscript. A.M. and C.B. analyzed all the data. All authors verified the manuscript.

## Competing Interests Statement

The authors declare no competing interests.

### Figure Legends/Captions:

**Fig. 1 | Residue-free PPC transfer vs traditional PMMA transfer.** **a,b,c**, Schematic (top panel) and optical micrograph (bottom panel) of a typical TMD heterostructure fabrication (**a**) before, (**b**) after the top PMMA supporting-holder removal, (**c**) after PPC supporting holder removal (see Supplementary Fig. 1 for complete process). Optically invisible PMMA residue stays between TMD1/TMD2 interface (for example, WSe<sub>2</sub>/WS<sub>2</sub>), as highlighted by the black arrow. The top TMD2 flake exhibits poor adhesion to the bottom TMD1 due to the interfacial PMMA residue and suffers from crumbling and structural damage. In contrast, TMD heterostructures fabricated using the PPC method show no structural damage, superior adhesion, and good interfacial contact. **d,e**, Optical micrograph (**d**) and AFM topography (**e**) PPC-transferred monolayer MoS<sub>2</sub>. **f**, High-resolution AFM topography (selected black box region in **e**) with negligible PPC residues (coverage  $\approx 0.08\%$ ). **g,h,i**, Optical micrograph (**g**), AFM topography (**h, i**) of PMMA-transferred MoS<sub>2</sub> film. The PMMA residue coverage was 35.2% on MoS<sub>2</sub> surface and 42.6% on SiO<sub>2</sub> substrate. **j,k**, AFM height profiles (from dotted lines in **f, i**) for PMMA and PPC-transferred MoS<sub>2</sub> and SiO<sub>2</sub> substrate. The PPC-transfer method (**f**) exhibits a flat height profile (RMS  $\approx 0.66$  nm) compared to PMMA transfer (RMS  $\approx 5.62$  nm extracted from **i**).

**Fig. 2 | Electrical and optical effect of the residues.** **a,b**, Conducting AFM topography (top panel) and current mapping of the monolayer MoS<sub>2</sub> transferred by (**a**) PPC ( $V_{\text{bias}} = 0.1$  V) and (**b**) PMMA ( $V_{\text{bias}} = 1$  V) methods under atmospheric conditions. **c**, Average resistance (R) profile comparison on MoS<sub>2</sub> taken from the colored dashed line in **a, b**. PMMA residues show high resistance peaks. The R peak highlights the resistance increase (arrows) from the PMMA residues (black arrows in **b**) on the MoS<sub>2</sub> surface. In contrast, the PPC transfer method results in uniformly flat resistance distribution. **d,e**, PL spectra of the monolayer MoS<sub>2</sub> under low (**d**) and high (**e**) excitation power (532 nm) in as-grown, PMMA, and PPC samples. Negligible residue in the PPC samples exhibited a very high PL intensity. **f,g,h**, Excitation power dependent PL intensity mapping of the as-grown (**f**), PMMA (**g**), and PPC (**h**) transferred samples (identical color scale). The presence of precursor residue (**f**-inset) in the as-grown and PMMA residue (Fig. 1h) results in a similar power threshold ( $P_{\text{th}}$ ) of  $\sim 0.4$  mW. In contrast, the PPC sample shows a significantly low  $P_{\text{th}}$  of  $\sim 70$   $\mu$ W under identical PL measurement conditions due to the residue-free PPC transfer method.

**Fig. 3 | Ultralow contact resistance in monolayer MoS<sub>2</sub>.** **a**, Schematic model of MoS<sub>2</sub> FET device fabricated using PMMA (top panel shows residue in the metal-MoS<sub>2</sub> interface), compared to PPC (bottom panel) methods. PMMA method leaves residues between metal contact and MoS<sub>2</sub> surface (black arrows), resulting in device performance degradation. On the contrary, the PPC method exhibits negligible residues, and device performance improves significantly due to the absence of transfer process-induced residue. **b**,  $R_C$  extracted for Bi contact devices using transfer-length method (TLM) for Device1, Device2, and Device4. Device image (top inset) and magnified y-intercepts ( $2R_C$  in bottom inset) show the lowest  $R_C$  value ( $\sim 78$   $\Omega$ - $\mu$ m) in Device1 at 15 K. **c**, Temperature-dependent output characteristics ( $I_d$ - $V_d$ ) of Device2 (R-T plot in the inset). **d**, Arrhenius plots of Bi and Ti contact devices. Bi contact (PPC-Bi, PMMA-Bi) shows clear ohmic contact behavior ( $\Phi_B = 0$  at low temperature) compare to Schottky contact ( $\Phi_B = 33$  meV) in Ti contact device (PMMA-Ti). **e**, Nonlinearity ( $N = (d^2I_d/dV_d^2)/2(dI_d/dV_d)$ ) for PPC-Bi and PMMA-Ti contacts ( $V_d$  dependent N shown in the inset).  $N = 0$  in the PPC-Bi confirms ohmic contact between Bi and MoS<sub>2</sub><sup>20</sup>. **f**, Benchmark of  $R_C$  vs.  $n_{2D}$  in MoS<sub>2</sub> FET using different metal contacts for various semiconductor

technologies<sup>10–19,37</sup>. The black dashed line represents the quantum limit of ( $R_C \approx 0.026 (n_{2D})^{-0.5}$ ) as calculated in previous literature<sup>38,39</sup>.

**Fig. 4 | Ultrahigh on/off ratio in MoS<sub>2</sub> FET. a,b**, Transfer characteristics ( $I_d$ - $V_g$ ) comparison between (a) Bi contact devices (Device1, Device2, Device4), Device performance was improved by using h-BN substrate (Device1) instead of SiO<sub>2</sub> (Device2). (b) Ti contact devices (Device3, Device5) at 300 K and  $V_{ds} = 0.5$  V. **c**, Temperature-dependent  $I_d$ - $V_g$  between Bi and Ti (inset) contacts. **d**,  $I_d$ - $V_g$  of the PPC-Bi device on h-BN (Device1) and SiO<sub>2</sub> (Device2, inset) substrates at the chosen temperature of  $T = 15$  and 300 K. **e**, On/off ratio vs.  $T$  plot for the Bi contact devices (PPC and PMMA). Bi contact device (Device1) shows an ultrahigh on/off ratio of  $1.4 \times 10^{11}$  at 15 K due to residue-free interfacial contact and low charge scattering from the h-BN substrate. **f**, Two-probe field effect mobility ( $\mu_{FE}$ ) comparisons between Bi and Ti contact devices (PPC and PMMA). PPC-Bi contact shows much higher  $\mu_{FE}$ . **g**, Two-probe and four-probe mobility for Bi and Ti contact devices at 300 K. Almost similar  $\mu_{FE}$  values between 2-probe and 4-probe suggested insignificant  $R_C$  effect.

**Fig. 5 | Benchmark of ultra-clean large-area monolayer MoS<sub>2</sub>-FET. a**, Benchmark of on/off ratio vs.  $R_C$  in MoS<sub>2</sub> FET compared to different metal contacts used in semiconductor technologies<sup>10–13,16,17,20,63–66</sup>. **b**, Benchmark of the maximum on-current ( $I_{on-max}$ ) vs. on/off ratio of the MoS<sub>2</sub> FET ( $L_{CH} = 200$  nm) for PPC-Bi contact compared to black phosphorus (BP), MoS<sub>2</sub>, metal oxides, and thin metal oxides FETs described in the literature<sup>44,46–62</sup>. PPC-Bi contact on the h-BN substrate (Device1) exhibited the highest on/off ratio and  $I_{on-max}$  among all other devices.

## References

1. Liu, C. *et al.* Two-dimensional materials for next-generation computing technologies. *Nat. Nanotechnol.* **15**, 545–557 (2020).
2. Jung, S.-G., Kim, J.-K. & Yu, H.-Y. Analytical Model of Contact Resistance in Vertically Stacked Nanosheet FETs for Sub-3-nm Technology Node. *IEEE Trans. Electron Devices* **69**, 930–935 (2022).
3. Watson, A. J., Lu, W., Guimarães, M. H. D. & Stöhr, M. Transfer of large-scale two-dimensional semiconductors: challenges and developments. *2D Mater.* **8**, 032001 (2021).
4. Zhang, S. *et al.* Wafer-scale transferred multilayer MoS<sub>2</sub> for high performance field effect transistors. *Nanotechnology* **30**, 174002 (2019).
5. Lee, J. S. *et al.* Wafer-scale single-crystal hexagonal boron nitride film via self-collimated grain formation. *Science* **362**, 817–821 (2018).
6. Li, T. *et al.* Epitaxial growth of wafer-scale molybdenum disulfide semiconductor single crystals on sapphire. *Nat. Nanotechnol.* **16**, 1201–1207 (2021).
7. Leong, W.S. *et al.* Paraffin-enabled graphene transfer. *Nat. Commun.* **10**, 1–8 (2019).
8. Zhang, T. *et al.* Clean Transfer of 2D Transition Metal Dichalcogenides Using Cellulose Acetate for Atomic Resolution Characterizations. *ACS Appl. Nano Mater.* **2**, 5320–5328 (2019).

9. Wang, P. *et al.* High-Fidelity Transfer of Chemical Vapor Deposition Grown 2D Transition Metal Dichalcogenides via Substrate Decoupling and Polymer/Small Molecule Composite. *ACS Nano* **14**, 7370–7379 (2020).
10. Wang, Y. *et al.* Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. *Nature* **568**, 70–74 (2019).
11. Cui, X. *et al.* Low-Temperature Ohmic Contact to Monolayer MoS<sub>2</sub> by van der Waals Bonded Co/h-BN Electrodes. *Nano Lett.* **17**, 4781–4786 (2017).
12. Kim, C. *et al.* Fermi Level Pinning at Electrical Metal Contacts of Monolayer Molybdenum Dichalcogenides. *ACS Nano* **11**, 1588–1596 (2017).
13. English, C. D., Shine, G., Dorgan, V. E., Saraswat, K. C. & Pop, E. Improved Contacts to MoS<sub>2</sub> Transistors by Ultra-High Vacuum Metal Deposition. *Nano Lett.* **16**, 3824–3830 (2016).
14. Das, S., Chen, H.-Y., Penumatcha, A. V. & Appenzeller, J. High Performance Multilayer MoS<sub>2</sub> Transistors with Scandium Contacts. *Nano Lett.* **13**, 100–105 (2013).
15. English, C. D., Smithe, K. K. H. & Pop, E. Approaching Ballistic Transport in Monolayer MoS<sub>2</sub> Transistors with Self-aligned 10 nm Top Gates. In *Proc. 2016 IEEE International Electron Devices Meeting (IEDM)* 131–134 (IEEE, 2016).
16. McClellan, C. J., Yalon, E., Smithe, K. K. H., Suryavanshi, S. V. & Pop, E. High Current Density in Monolayer MoS<sub>2</sub> Doped by AlO<sub>x</sub>. *ACS Nano* **15**, 1587–1596 (2021).
17. Smithe, K. K. H., Suryavanshi, S. V., Muñoz Rojo, M., Tedjarati, A. D. & Pop, E. Low Variability in Synthetic Monolayer MoS<sub>2</sub> Devices. *ACS Nano* **11**, 8456–8463 (2017).
18. Guimarães, M. H. D. *et al.* Atomically Thin Ohmic Edge Contacts Between Two-Dimensional Materials. *ACS Nano* **10**, 6392–6399 (2016).
19. Smets, Q. *et al.* Ultra-scaled MOCVD MoS<sub>2</sub> MOSFETs with 42nm contact pitch and 250μA/μm drain current. in *2019 IEEE International Electron Devices Meeting (IEDM)* 23.2.1–23.2.4 (2019).
20. Shen, P.-C. *et al.* Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **593**, 211–217 (2021).
21. Kim, B.-K. *et al.* Origins of genuine Ohmic van der Waals contact between indium and MoS<sub>2</sub>. *Npj 2D Mater. Appl.* **5**, 1–10 (2021).
22. Kinoshita, K. *et al.* Dry release transfer of graphene and few-layer h-BN by utilizing thermoplasticity of polypropylene carbonate. *Npj 2D Mater. Appl.* **3**, 22 (2019).
23. Frisenda, R. *et al.* Recent progress in the assembly of nanodevices and van der Waals heterostructures by deterministic placement of 2D materials. *Chem. Soc. Rev.* **47**, 53–68 (2018).
24. Schranghamer, T. F., Sharma, M., Singh, R. & Das, S. Review and comparison of layer transfer methods for two-dimensional materials for emerging applications. *Chem. Soc. Rev.* **50**, 11032–11054 (2021).
25. Wood, J. D. *et al.* Annealing free, clean graphene transfer using alternative polymer scaffolds. *Nanotechnology* **26**, 055302 (2015).
26. Zhang, L. *et al.* Damage-free and rapid transfer of CVD-grown two-dimensional transition metal dichalcogenides by dissolving sacrificial water-soluble layers. *Nanoscale* **9**, 19124–19130 (2017).
27. Van Ngoc, H., Qian, Y., Han, S. K. & Kang, D. J. PMMA-etching-free transfer of wafer-scale chemical vapor deposition two-dimensional atomic crystal by a water soluble polyvinyl alcohol polymer method. *Sci. Rep.* **6**, 33096 (2016).

28. Lu, F., Karmakar, A., Shahi, S. & Einarsson, E. Selective and confined growth of transition metal dichalcogenides on transferred graphene. *RSC Adv.* **7**, 37310–37314 (2017).
29. Yue, Y., Feng, Y., Chen, J., Zhang, D. & Feng, W. Two-dimensional large-scale bandgap-tunable monolayer  $\text{MoS}_{2(1-x)}\text{Se}_{2x}$ /graphene heterostructures for phototransistors. *J. Mater. Chem. C* **5**, 5887–5896 (2017).
30. Lin, Z. *et al.* Controllable Growth of Large-Size Crystalline  $\text{MoS}_2$  and Resist-Free Transfer Assisted with a Cu Thin Film. *Sci. Rep.* **5**, 18596 (2015).
31. Jiang, G., Feng, J., Zhang, M., Zhang, S. & Huang, H. Structure, and thermal and mechanical properties of poly(propylene carbonate) capped with different types of acid anhydride via reactive extrusion. *RSC Adv.* **6**, 107547–107555 (2016).
32. Gao, J. *et al.* A promising alternative to conventional polyethylene with poly(propylene carbonate) reinforced by graphene oxide nanosheets. *J. Mater. Chem.* **21**, 17627–17630 (2011).
33. Choi, S. H. *et al.* Water-Assisted Synthesis of Molybdenum Disulfide Film with Single Organic Liquid Precursor. *Sci. Rep.* **7**, 1983 (2017).
34. Chang, M.-C. *et al.* Fast growth of large-grain and continuous  $\text{MoS}_2$  films through a self-capping vapor-liquid-solid method. *Nat. Commun.* **11**, 3682 (2020).
35. Chen, F., Wang, L., Wang, T. & Ji, X. Enhanced local photoluminescence of a multilayer  $\text{MoS}_2$  nanodot stacked on monolayer  $\text{MoS}_2$  flakes. *Opt. Mater. Express* **7**, 1365 (2017).
36. Xu, S. *et al.* Universal low-temperature Ohmic contacts for quantum transport in transition metal dichalcogenides. *2D Mater.* **3**, 021007 (2016).
37. Chhowalla, M., Jena, D. & Zhang, H. Two-dimensional semiconductors for transistors. *Nat. Rev. Mater.* **1**, 1–15 (2016).
38. Allain, A., Kang, J., Banerjee, K. & Kis, A. Electrical contacts to two-dimensional semiconductors. *Nat. Mater.* **14**, 1195–1205 (2015).
39. Jena, D. 2D crystal semiconductors: Intimate contacts. *Nat. Mater.* **13**, 3 (2014).
40. Choi, W. *et al.* Low-temperature behaviors of multilayer  $\text{MoS}_2$  transistors with ohmic and Schottky contacts. *Appl. Phys. Lett.* **115**, 033501 (2019).
41. Li, X.-X. *et al.* Gate-controlled reversible rectifying behaviour in tunnel contacted atomically-thin  $\text{MoS}_2$  transistor. *Nat. Commun.* **8**, 970 (2017).
42. Knobloch, T. *et al.* The performance limits of hexagonal boron nitride as an insulator for scaled CMOS devices based on two-dimensional materials. *Nat. Electron.* **4**, 98–108 (2021).
43. Chan, M. Y. *et al.* Suppression of thermally activated carrier transport in atomically thin  $\text{MoS}_2$  on crystalline hexagonal boron nitride substrates. *Nanoscale* **5**, 9572–9576 (2013).
44. Li, S. *et al.* Nanometre-thin indium tin oxide for advanced high-performance electronics. *Nat. Mater.* **18**, 1091–1097 (2019).
45. Daus, A. *et al.* High-performance flexible nanoscale transistors based on transition metal dichalcogenides. *Nat. Electron.* **4**, 495–501 (2021).
46. Wu, S. H. *et al.* Performance boost of crystalline in-Ga-Zn-O material and transistor with extremely low leakage for IoT normally-off CPU application. *In VLSI Symp. Tech. Dig.* T166–T167 (2017).
47. Lyu, R.-J., Shie, B.-S., Lin, H.-C., Li, P.-W. & Huang, T.-Y. Downscaling Metal—Oxide Thin-Film Transistors to Sub-50 nm in an Exquisite Film-Profile Engineering Approach. *IEEE Trans. Electron Devices* **64**, 1069–1075 (2017).

48. Wu, S. H. *et al.* Extremely low power c-axis aligned crystalline In-Ga-Zn-O 60 nm transistor integrated with industry 65 nm Si MOSFET for IoT normally-off CPU application. In *2016 IEEE Symposium on VLSI Technology* 1–2 (2016).
49. Matsuda, S. *et al.* 30-nm-channel-length c-axis aligned crystalline In-Ga-Zn-O transistors with low off-state leakage current and steep subthreshold characteristics. In *2015 Symposium on VLSI Technology (VLSI Technology)* T216–T217 (2015).
50. Matsubayashi, D. *et al.* 20-nm-Node trench-gate-self-aligned crystalline In-Ga-Zn-Oxide FET with high frequency and low off-state current. in *2015 IEEE International Electron Devices Meeting (IEDM)* 6.5.1-6.5.4 (2015).
51. Kobayashi, Y. *et al.* Scaling to 50-nm C-axis aligned crystalline In-Ga-Zn oxide FET with surrounded channel structure and its application for less-than-5-nsec writing speed memory. In *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers* 1–2 (IEEE, 2014).
52. Lin, H.-C., Shie, B.-S. & Huang, T.-Y. 100-nm IGZO Thin-Film Transistors With Film Profile Engineering. *IEEE Trans. Electron Devices* **61**, 2224–2227 (2014).
53. Lyu, R.-J. *et al.* Film profile engineering (FPE): A new concept for manufacturing of short-channel metal oxide TFTs. in *2013 IEEE International Electron Devices Meeting* 11.2.1-11.2.4 (2013).
54. Xiong, X. *et al.* High Performance Black Phosphorus Electronic and Photonic Devices with HfLaO Dielectric. *IEEE Electron Device Lett.* **39**, 127–130 (2018).
55. Si, M., Yang, L., Du, Y. & Ye, P. D. Black phosphorus field-effect transistor with record drain current exceeding 1 A/mm. in *2017 75th Annual Device Research Conference (DRC)* 1–2 (2017).
56. Yang, L. *et al.* How Important Is the Metal–Semiconductor Contact for Schottky Barrier Transistors: A Case Study on Few-Layer Black Phosphorus? *ACS Omega* **2**, 4173–4179 (2017).
57. Li, T. *et al.* High field transport of high performance black phosphorus transistors. *Appl. Phys. Lett.* **110**, 163507 (2017).
58. Li, K.-S. *et al.* MoS<sub>2</sub> U-shape MOSFET with 10 nm channel length and poly-Si source/drain serving as seed for full wafer CVD MoS<sub>2</sub> availability. in *2016 IEEE Symposium on VLSI Technology* 1–2
59. Liu, Y. *et al.* Pushing the Performance Limit of Sub-100 nm Molybdenum Disulfide Transistors. *Nano Lett.* **16**, 6337–6342 (2016).
60. Nourbakhsh, A. *et al.* 15-nm channel length MoS<sub>2</sub> FETs with single- and double-gate structures. in *2015 Symposium on VLSI Technology (VLSI Technology)* T28–T29 (2015).
61. Yang, L., Lee, R. T. P., Rao, S. S. P., Tsai, W. & Ye, P. D. 10 nm nominal channel length MoS<sub>2</sub> FETs with EOT 2.5 nm and 0.52 mA/μm drain current. in *2015 73rd Annual Device Research Conference (DRC)* 237–238 (2015).
62. Yang, L. *et al.* High-performance MoS<sub>2</sub> field-effect transistors enabled by chloride doping: Record low contact resistance (0.5 kΩ·μm) and record high drain current (460 μA/μm). in *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers* 1–2 (2014).
63. Li, W. *et al.* High-Performance CVD MoS<sub>2</sub> Transistors with Self-Aligned Top-Gate and Bi Contact. in *2021 IEEE International Electron Devices Meeting (IEDM)* 37.3.1-37.3.4 (2021).
64. Kang, K. *et al.* High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity. *Nature* **520**, 656–660 (2015).
65. Chee, S.-S. *et al.* Lowering the Schottky Barrier Height by Graphene/Ag Electrodes for High-Mobility MoS<sub>2</sub> Field-Effect Transistors. *Adv. Mater.* **31**, 1804422 (2019).

66. Smithe, K. K. H., English, C. D., Suryavanshi, S. V. & Pop, E. Intrinsic electrical transport and performance projections of synthetic monolayer MoS<sub>2</sub> devices. *2D Mater.* **4**, 011009 (2016).
67. Zhang, Y. *et al.* Influence of the linkage type between the polymer backbone and side groups on the surface segregation of methyl groups during film formation. *Soft Matter* **11**, 9168–9178 (2015).
68. Hirata, T., Matsuno, H., Tanaka, M. & Tanaka, K. Surface segregation of poly(2-methoxyethyl acrylate) in a mixture with poly(methyl methacrylate). *Phys. Chem. Chem. Phys.* **13**, 4928–4934 (2011).

## Methods

### PPC and PMMA transfer methods for monolayer TMDs.

The CVD-grown monolayer MoS<sub>2</sub> was transferred by using the PPC (Sigma-Aldrich) and PMMA (Sigma-Aldrich) by wet transfer method. First, PPC was spin-coated (6000 rpm, 1min) onto as-grown monolayer TMD samples and subsequently baked in atmospheric condition at 90 °C on a hotplate for 1min., The films were then released from SiO<sub>2</sub>/Si growth substrate by etching in a concentrated hydrofluoric acid (HF) solution at room temperature. The PPC/TMD stacks were picked up, rinsed with deionized water (several times) and then transferred onto the target substrate. After transfer, the film was dried using an N<sub>2</sub>. Finally, the sample was gradually immersed in a beaker of anisole (Sigma-Aldrich) for 10 min to remove PPC, followed by rinsing in a beaker of acetone, IPA and ethanol. Afterward, the sample was allowed to dry in N<sub>2</sub> gas until complete solvent evaporation. For PMMA transfer, monolayer TMDs were transferred in the same manner as PPC transfer for monolayer TMDs. PMMA was spin-coated at 3500 rpm for 1 min onto the as-grown monolayer TMD sample. The sample was then baked in atmospheric condition at 150 °C on a hot plate for 1 min. Finally, the PMMA support layer was dissolved by the gradual immersion in a beaker of acetone for 20 min, followed by the gradual immersion in IPA, and ethanol.

### PPC transfer methods for heterostructure TMDs.

The freestanding PPC/TMD stacks were picked up (after the above wet transfer) by a cleaned PET sheet with a hole as shown in supplementary Fig. 1c. After that, the PPC/TMD stack was transferred to a dry transfer holder (leaving TMD on the outside surface). Dry transfer holder with PPC/TMD film was placed on the hot plate at 90 °C, for few seconds to dry excess moisture. Subsequently, two TMDs were aligned and transferred at room temperature. The temperature of the sample stage was raised up to 90 °C for 2 min to completely separate the PPC film from the metal dry transfer holder. Finally, the remaining PPC film is removed by immersing in anisole for 5-10 min.

### Device fabrication.

The standard electron-beam (e-beam) lithography was used to pattern the source/drain contacts with PMMA e-beam resists (950 PMMA A4). An UHV sputter system was employed for depositing 20 nm Bi (deposition rate 1 nm/min) and 50 nm Au capping layer (deposition rate 5 nm/min) at  $\sim 10^{-7}$  torr, followed by a 10 – 20 min lift-off process in acetone at room temperature. Ti/Au (2/50 nm) electrodes were used for the top gate electrode. We fixed channel widths (3  $\mu$ m) for all FET devices. The channel length ( $L_{CH}$ ) was varied from 200 nm to 1  $\mu$ m for the TLM measurements. No chemical doping and annealing were

performed on all FET devices. All electrical transport measurements were performed in a vacuum ( $10^{-6}$  –  $10^{-7}$  torr) in a Lakeshore cryogenic probe station by using a semiconductor characterization system (Keithley 4200-SCS). h-BN (~15 – 20 nm) was used for top gate dielectrics in all FET studies.

**Data availability**

The data that support the findings of this study are available from the corresponding author upon reasonable request.

**Additional information**

**Supplementary information** The online version contains supplementary material available at

