FERMILAB-CONF-23-182-PPD
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The CMOS Pseudo-Thyristor: A Zero-Static Current Discriminator Circuit

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ABSTRACT: A very low power discriminator circuit for pixelized detectors, called the Pseudo-Thyristor is described in this document. It is a positive feedback topology using regular PMOS and NMOS field-effect transistors (FET's) with zero static current. When a small charge is injected into the circuit, it flips rapidly due to the positive feedback and outputs a logic transition for further digitization. Simulation shows that in a 65 nm process, it is possible to achieve a detecting threshold below 5 fC while maintain the average power consumption below 10 micro-Watts when the hit occupancy is < 10% for 40 MHz operation.

KEYWORDS: Front-end electronics for detector readout; Solid state detectors; Timing detector

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This work was produced by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11359 with the U.S. Department of Energy, Office of Science, Office of High Energy Physics. Publisher acknowledges the U.S. Government license to provide public access under the DOE Public Access Plan DOE Public Access Plan

1. Introduction

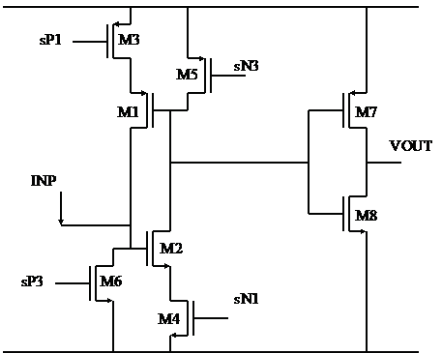
In contemporary high energy physics detectors, pixelized detectors, either silicon detectors or Low-Gain Avalanche Detectors (LGADs) [1-3] are widely used for tracking, timing or calorimeters. As the number of detector elements or pixels continues to increase towards the future, much lower power consumption of the front-end circuits is desired. In some applications, power consumptions as low as 10 micro-Watts per channel are desired. In typical architecture today, amplifier-based discriminators consume about 1 milli-Watts power for 65-180 nm CMOS fabrication processes and this is a factor of 100 higher than what's desired in the future. To reduce the power consumption by up to two orders of magnitude, new approaches are required. The Pseudo-Thyristor proposed here is a novel CMOS discriminator circuit with zero static current with the potential to have ultra-low power consumption.

We chose a circuit scheme with positive feedback (which is rarely used in analog frontend circuits) for fast switching between the OFF and the ON states that operates like a thyristor. However, unlike a thyristor that needs a static current to maintain the ON state, our circuit consumes zero static currents for both the ON and the OFF states as in regular CMOS digital circuits. For this reason, we name the circuit as Pseudo-Thyristor Discriminator. In this documents, the circuit design of the pseudo-thyristor discriminator is described in Section 2 and simulation results are shown in Section 3, followed by a conclusion in Section 4.

2. Design of the Pseudo-Thyristor Discriminator

2.1 Circuit Diagram

Figure 1 illustrates the circuit diagram of the pseudo-thyristor discriminator. The entire circuit is constructed with regular PMOS and NMOS field-effect transistors (FET's) in TSMC 65 nm process.



FET	W (nm)	L (nm)
M1	200	130
M2	200	60
M3	1000	130
M4	500	130
M5	5000	60
M6	5000	60
M7	4000	130
M8	120	60

Figure 1. Circuit diagram of the pseudo-thyristor discriminator and transistor sizes

The core of the circuit consists of a pair of PMOS (M1) and NMOS (M2) FET's whose drain and gate terminals are cross connected to form a positive feedback loop. At standby condition, external control signals sP1=LO and sN1=HI which cause M3 and M4 in the ON state while sP3=LO and sN3=HI, causing M6 and M5 in the OFF state. After initialization, both M1 and M2 are in the OFF state, i.e., the gate of M1 (and the drain of M2) is in the HI state while the gate of M2 (and the drain of M1) is in the LO state. When a small amount of electric charges (typically several femto-Coulombs) is injected via INP port into the NMOS (M2) gate, after the M2 gate is

charged beyond the threshold voltage, both the M2 and M1 are turned from the OFF to the ON state. Due to positive feedback, the switching process is fast with relatively large instantaneous currents that charge the gates of the FET's in a short amount of time. Once in the ON state, both M1 and M2 are conductive and the gates of M1 and M2 are kept in the LO and HI voltage levels, respectively, which maintain both transistors in the ON state until the next reset period. Compared to the conventional current comparators such as Traff's circuit or its variants [4], this circuit does not consume any static power because it only turns on when there is sufficient charge accumulated at the gate of M2. Hence, it significantly reduces the power consumption of the discriminator circuit in applications with relatively low hit rate.

During the reset period, sP3 is turned to the HI level while sN3 is turned to the LO level causing both M6 and M5 becoming conductive. The gates of M1 and M2 are discharged to the HI and the LO voltage levels, respectively, which force both of them to go the OFF state. To prevent shorting power rail that cause large current when M5 and M6 become conductive before M1 and M2 are turned off, transistors M3 and M4 are added and controlled by sP1 and sN1 signals. The sP1 and sN1 are flipped slightly earlier than sP3 and sN3 so that they can cut off current paths before M6 and M5 are turned on. Therefore, the detailed resetting process takes several small steps: (1) M3 and M4 are turned from the ON to the OFF state, (2) M5 and M6 from the OFF to the ON state, (3) M1 and M2 from the ON state to the OFF state, (4) M3 and M4 from the OFF state back to the ON state, (5) M5 and M6 from the ON state back to the OFF state. After resetting, M1 and M2 remain the OFF state until external charges injected into the gate of M1.

The pair of transistors M7 and M8 form an inverting buffer to drive circuits in later stages.

2.2 Design Considerations

Cautions must be taken during the design of the pseudo-thyristor discriminators. During the standby condition, M1 and M2 in Figure 1 are both in the OFF state. The OFF state leakage current of a transistor may charge the gate of the other one which may cause the transistor pair to go to the ON state spontaneously via positive feedback if the one of the gates is charged above the conductive threshold. To prevent the transistor pair from spontaneous state changing, the length of M1 is chosen to be relatively large so that it can be turned off as completely as possible. Transistors M5 and M6, on the other hand, are designed to provide small leakage currents to maintain M1 and M2 in the OFF state.

In standby condition, the transistor M8 is in the ON state, the leakage current through its gate is not negligible, especially in IC chips fabricated with deep nano-meter processes. The length and width of M8 are chosen to be relatively small and the leakage current of M8 is to be balanced with the OFF state leakage current through the M5 drain.

With appropriate sets of the transistor lengths and widths, as shown in Figure 1, the circuit is able to remain in standby condition indefinitely.

3. Simulation Results

The operations of the pseudo-thyristor discriminator is simulated in schematic-level with TSMC 65 nm process technology.

3.1 An Application Example

An application example of the pseudo-thyristor discriminator interfacing with a current source is studied and the circuit diagram is shown in Figure 2.

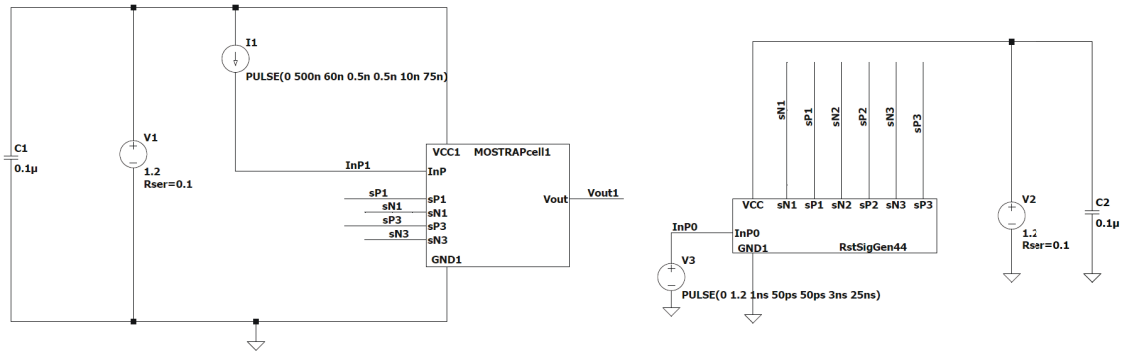


Figure 2. Circuit diagram of the application of pseudo-thyristor discriminator interfacing with a current source.

The current source I1 emulates the input from the frontend circuit that generates a short (~10 ns) pulse with a total charge approximately 5fC. The input current is fed into the pseudo-thyristor discriminator in the subcircuit MOSTRAPcell1 block with circuit diagram as shown in Figure 1.

The block RstSigGen44 contains a set of inverters and converts the input pulse (InP0) into the control signals sN1, sP1, sN3 and sP3 for the reset process as described in previous section. In this example, the reset pulse is a 40 MHz periodic signal that emulates resetting the circuits every beam crossing for detectors operating in LHC environment. In fact, the resetting pulse may also be a delayed version of the output logic level, so that the circuit can operate in a self-trigger, self-resetting mode, which we will discuss later.

The voltage supplies V1 and V2 with some internal resistance are bypassed with capacitors. Note that the values of the resistance and capacitance are not realistic and they are chosen solely for the purpose of measuring the power consumptions of different parts of the circuit conveniently.

3.2 Operations of the pseudo-thyristor discriminators

The simulation is based on an application in a collider with a 40 MHz beam crossing as described in Figure 2. The reset pulses generated by V3 in Figure 2 repeat in 25 ns periods with about 3 ns in the HI state. The external current input is emulated with current source I1 that produces pulses up to 500 nA for about 10 ns, resulting in a total input charge approximately 5 fC.

The reset pulses and the signal input pulses are plotted in the top pane in Figure 3.

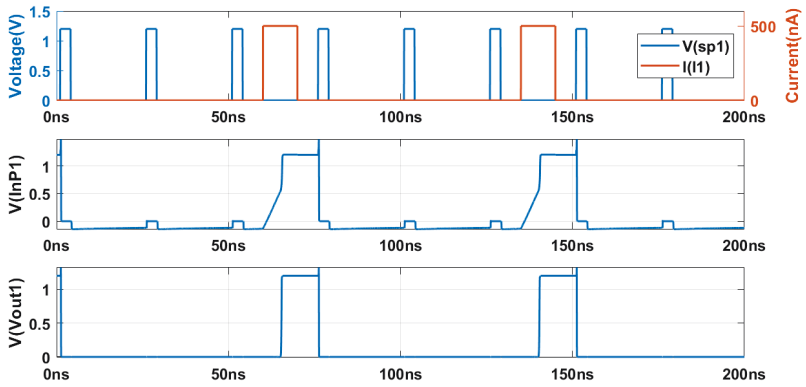


Figure 3. Simulation of the operations of the pseudo-thyristor discriminators

The middle pane shows the voltage at the node InP1 (V(InP1)). The output of the current source in Figure 2 charge up the gates of M2 in Figure 1. When V(InP1) exceeds the threshold voltage of M2, the positive feedback in the discriminator speeds up the charging speed of InP1 until V(InP1) reaches VDD. V(InP1) stays at VDD until the reset at the end of each beam crossing.

The bottom pane shows the Vout1 of the pseudo-thyristor discriminator (V(Vout1)). It has a sharp leading edge because of the gain of inverter and thus it can be used to provide timing information.

3.3 Flipping threshold under PVT variations

The Monte-Carlo (MC) simulation result of the flipping threshold including the process and mismatch variations is shown in Figure 4, with a mean (μ) of 2.7 fC and a standard variation (σ) of 0.21 fC. Since the flipping voltage is mostly related to the threshold voltage of the NMOS and the input capacitance, the temperature and voltage variations have less significant effect on the flipping threshold compared to the process and mismatch variations, as shown in Figure 4. With ±10% variation on VDD (from 1.08 V to 1.32 V), the variation on the flipping threshold is less than 1%. For temperature varying from -40 °C to 80 °C, the flipping threshold changes by 15%.

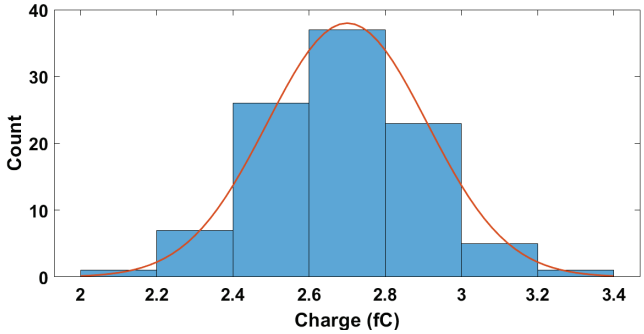


Figure 4. Flipping threshold with process and mismatch variations (100 points MC simulation)

In the future work, multiple techniques can be utilized to provide a sufficient calibration range to cover the variation of flipping threshold. The voltage controlled capacitor can be utilized to vary the input capacitance and hence to calibrate the flipping threshold. The threshold voltage of the input NMOS (M2) can also be calibrated by changing the V_{SB} of M2 via controlling the bulk voltage.

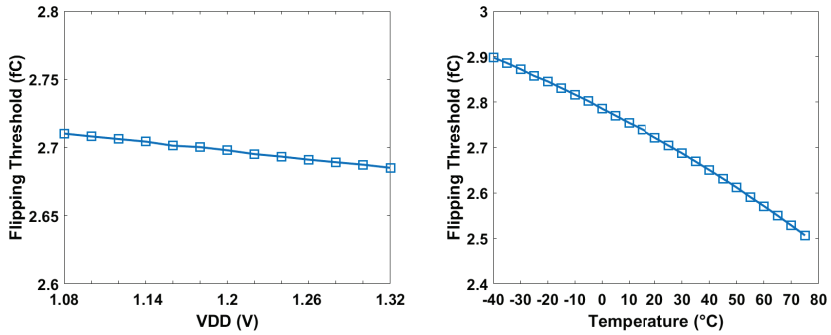


Figure 5. Flipping threshold versus supply voltage (left) and temperature (right)

3.4 Power Consumptions

The bottom pane in Figure 4 shows the currents flowing through the voltage supplies V1 and V2 which reflect the power consumptions in different parts of the circuit in schematic-level.

In static state, the current flowing through the pseudo-thyristor discriminator is very small as in regular CMOS logic circuits. From the trace of I(V1), the current flowing through power supply V1, one can see a current pulse due to the flipping operations with an sufficient injected charge. The peak of I(V1) is about 1.5 μA (with the effect of the bypass capacitor and internal resistance), and the average over a short time interval (75 ns in this case) is approximately 0.3 μA. The power consumption in this extreme case (33% hit occupancy) is roughly 0.4 μW.

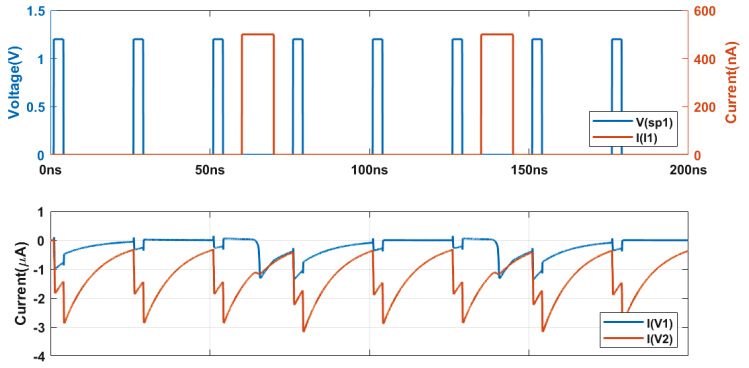


Figure 6. Simulation of the current of the pseudo-thyristor discriminator

The trace I(V2) is the current through the power supply V2, which powers the block RstSigGen44 that produces pulses for resetting process. The peak of this trace is around 3 μA and the average is about 1.3 μA with an average power consumption of about 1.6 μW, which should be acceptable for many applications. Note that this "service" circuit consumes dominating portion of the power in the entire circuit since resetting processes are repeated in all beam crossings.

If a self-trigger self-reset scheme is utilized, the reset operation only happens when a flip is detected at the output of discriminator. In this scheme, neglectable power is consumed when no hit is detected. In real applications with pixelized detector, hit occupancy is typically <1% and therefore, the overall power consumption of the discriminator (including the self-triggered reset generation block) is less than 0.1 μW.

4. Conclusion and outlook

A very low power consumption discriminator circuit, pseudo-thyristor discriminator is presented in this document. Simulation results show that it consumes much less than 10 μW/channel in ASIC chips fabricated with TSMC 65 nm process.

The positive feedback employed in the circuit helps reach a fast switching speed with a very simple topology. The CMOS structure ensures that current paths are cut off at both the ON and the OFF states resulting in zero static current, while during the switch process, relative high currents flowing through the transistors bring them into a high conductivity region to fulfill the speed requirements.

It is worth to mention that positive feedback processes are present in amplifications inside natural materials for charged particle detections, such as in gaseous detectors. The frontend circuit utilizing well-controlled positive feedback can be viewed as an extension beyond the interaction of the charged particle with detecting materials.

Acknowledgments

This work has been authored by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11359 with the US Department of Energy, Office of Science, Office of High Energy Physics.

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