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Special Collection: Wide- and Ultrawide-Bandgap Electronic Semiconductor Devices

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ABSTRACT

The drain current temperature dependence is an efficient way to determine the channel temperature in semiconductor devices; however, it has been challenging to use due to the potential interference of trapping effects. A trapping tolerant method is proposed, illustrated here for Ga_2O_3 MOSFETs, making *in situ* temperature measurements possible, allowing a thermal resistance of 59 K·mm/W to be measured in Ga_2O_3 MOSFETs. However, neglecting the effect of trapping causes an error of ∼15% in the channel temperature measured using the drain current. 3D simulations show that the measured channel temperature is the average temperature value between source and drain contact.

β-Gallium oxide (β-Ga_2O_3) is attracting great interest for power electronic devices, such as Schottky barrier diodes (SBDs)[1,2] and field-effect transistors (FETs)[3] due to its high bandgap energy of ∼4.9 eV (Ref. 4) and expected electrical breakdown strength of 8 MV/cm.[5] However, the anisotropic low thermal conductivity of β-Ga_2O_3 of 13–27 W/m K, depending on crystallographic direction,[6–8] compared to GaN (230 W/m·K) and SiC (490 W/m·K),[9] makes efficient heat removal in Ga_2O_3-based devices more challenging than for competing technologies. The resulting high device temperature can lead to premature device failure, including failure induced by Schottky contact degradation[10] and crystal defect generation.[11] Therefore, an accurate assessment of the channel temperature in Ga_2O_3-based devices under different operating conditions is very important to optimize thermal management and determine their mean time to failure (MTTF).

Numerous methods have been used to measure the temperature in Ga_2O_3 devices. Raman nano-particle thermometry measurement[12,13] employs nano-particles to determine the surface temperature of the sample. However, it requires specialist equipment. Apart from Raman thermography, other optical measurements, such as infrared[14] and chip-level transient thermoreflectance (TTR),[15] have been employed. Electrical parameter based temperature measurement methods have been studied, e.g., on GaN[16] or Ga_2O_3.[17] The electrical parameters employed, such as the forward Schottky junction voltage[18] and PN junction voltage,[19] are straightforward to use; in particular, the equipment needed is readily available in an electrical testing laboratory. However, many of these methods are based on pulsed measurements, which must employ a heating quiescent bias point with little trapping,[13,17] or it will be impacted by trapping effects,[20] potentially causing erroneous temperature measurements.

In this work, we propose a drain current based trapping tolerant method for device temperature measurement. A pre-trapping process was introduced to ensure that the measured change in drain current is predominantly temperature driven. Simulations were performed to study the relationship between the extracted temperature and the temperature distribution in the device.

Samples used in this work have a 1.2 μm-thick unintentionally doped (UID) epilayer grown by ozone MBE on a Fe-doped semi-insulating-Ga_2O_3 (010) substrate.[21] The channel layer was defined by selective-area Si^+ ion implantations at multiple energies with a plateau concentration of 3×10^{17} cm^{-3}, forming a 0.3-μm-deep box-like profile. Source and drain Ohmic regions were implanted with a Si-doping of 5×10^{19} cm^{-3}. Capless implant activation annealing was performed at 950 °C for 30 min in N_2 ambient. An 0.9-μm-thick undoped Ga_2O_3 layer was under the channel. The Ohmic electrode was composed of a Ti/Au metal stack. 20 nm Al_2O_3 and 0.4 μm SiO_2 were used as the gate dielectric, deposited by a plasma atomic layer deposition and chemical

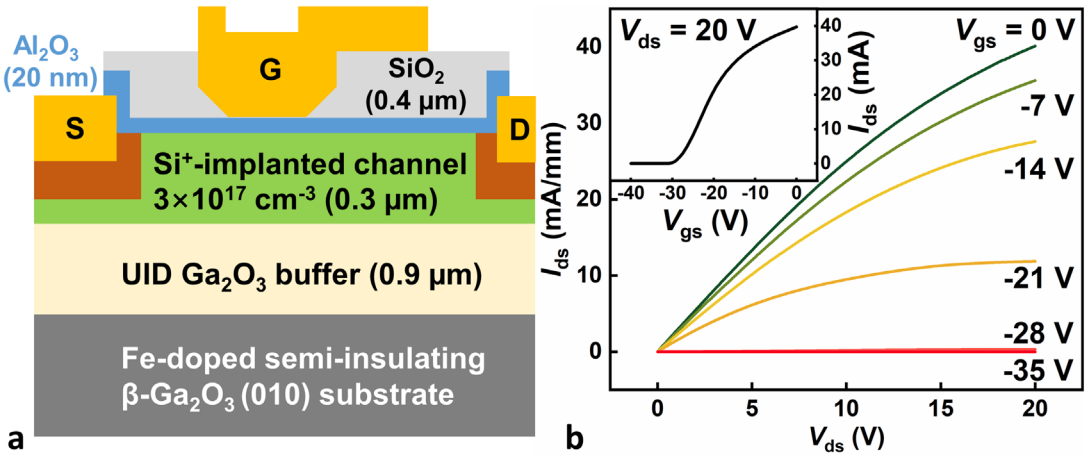

FIG. 1. (a) Schematic of the transistor. (b) The electrical characteristics of the transistor.

vapor deposition. CF_4 RIE gate recess through the SiO_2 was followed by depositions of Ti (3 nm)/Pt (12 nm)/Au (280 nm) for the gate electrode and Ti/Au for a gate-connected field plate. The transistor was an annular (circular) structure with the gate length, gate width, gate-source spacing, and gate-drain spacing of 2, 500, 5, and 15 μm, respectively (Fig. 1).

Figure 2 illustrates the principle of the measurement technique: (1) pre-trapping step: a bias was applied for 3 s to fill traps, here $V_{gs} = -14$ V and a $V_{ds} = 50$ V (a semi-on state with high drain bias); this bias condition efficiently fills traps. This step is used to suppress the change in the trapping during the subsequent on-state operation when temperature will be determined and minimizes the impact of traps on the temperature measurement. (2) Cooling: as the semi-on state will cause self heating, a 3-s-long cooling process is used to dissipate the heat, which was induced during the pre-trapping process. This period chosen is dependent on the time constant of the traps present in the devices. (3) Heating pulse: the device is switched on for 1.6 s—this is the condition device temperature is to be determined of; 1.6 s enables the device to reach steady state temperature;[22] different bias conditions were used to determine the channel temperature rise

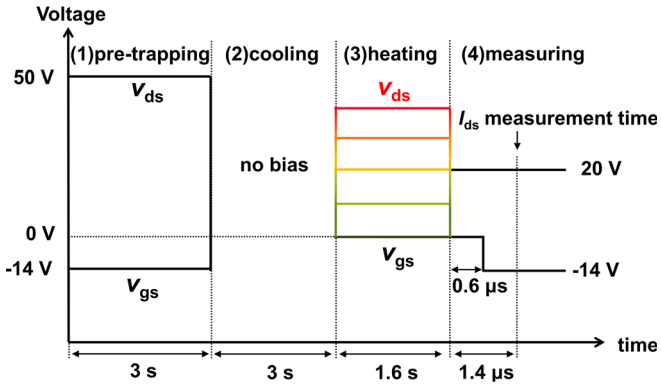

FIG. 2. Measurement sequence: (1) pre-trapping step, (2) cooling period, (3) phase after which device temperature should be measured, i.e., heating period, and (4) device temperature measurement phase.

as a function of power dissipation. (4) Measuring temperature: a bias of $V_{ds} = 20$ V and $V_{gs} = -14$ V was applied (semi-on, minimal self heating), and the temperature-dependent drain current was measured. The V_{gs} was changed 0.6 μs after V_{ds} to be able to observe the respective current though such delay is not necessarily needed. The drain current was measured 1.4 μs after (3), considering that the thermal time constant of Ga_2O_3 is on the order of about the ms-level,[22] the measured temperature will be in first approximation equal to the steady state temperature (3). Prior to these measurements, temperature calibration of the drain current was performed using the method described at different baseplate temperatures but applying $V_{ds} = 0$ V during (3), i.e., no self heating.

If most traps remain occupied after cooling, trapping effects are suppressed during the measuring pulse after heating, i.e., the drain current is only affected by the temperature rise. It is, therefore, important to quantify how much de-trapping occurs during the cooling step: The temperature measurement sequence previously described in Fig. 2 was used, but with I_{ds} measured during three extra 100-μs-long $V_{ds} = 10$ V, $V_{gs} = 0$ V pulses before pre-trapping, immediately after pre-trapping, and after the 3-s-long cooling phase, measuring $I_{ds} = 10.8$, 8.6, and 8.9 mA, respectively. There is 2.2 mA reduction in I_{ds} during the pre-trapping step, but only a 0.3 mA recovery during the 3-s-long cooling phase. This means that the majority of traps remains filled after the cooling period. The chosen cooling time should be long enough to dissipate heat after the pre-trapping pulse, but shorter than the de-trapping time constant.

Figure 3(a) shows the measured transient I_{ds} of the Ga_2O_3 MOSFET at various power densities, with the current change visible when V_{gs} and V_{ds} are stepped during the temperature measurement phase (4). Figure 3(b) shows I_{ds} values measured at the time point shown in Fig. 3(a), as a function of power dissipation. Figure 3(c) shows the temperature calibration made using a hot plate, from which $k_1 = -0.046$ mA/K is determined. During calibration, V_{ds} and V_{gs} are 0 V so that no power is dissipated during the "heating" phase, and the channel temperature ($T_{channel}$) equals the ambient temperature T_{amb}. The measurement shown in Fig. 3(d) for the active transistor uses the relationship: $T_{channel} = (k_2/k_1)P_{diss} + T_{amb}$. The thermal resistance is $R_{th} = k_2/k_1 = 59$ K·mm/W, determined from the slope in Fig. 3(d).

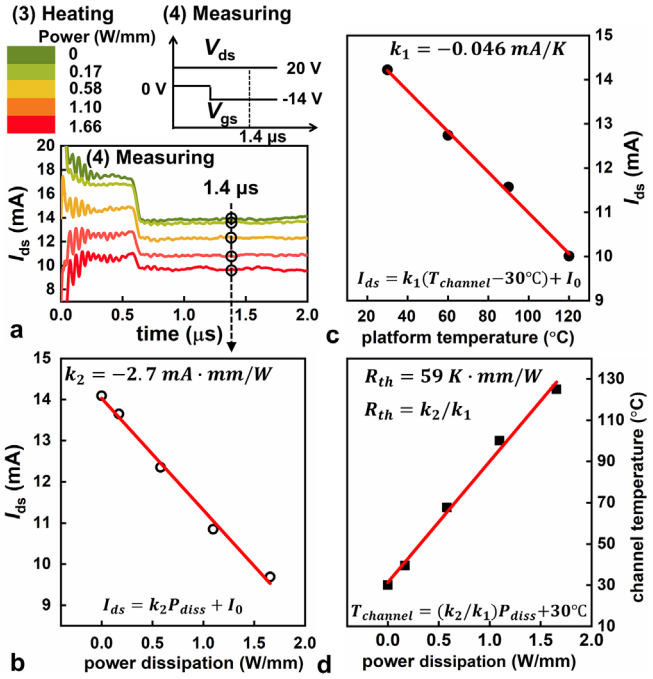

FIG. 3. (a) Drain current during the measuring phase (4) as function of time at various power dissipations applied during (3). (b) Extracted dependence between measured drain current 1.4 μs after stepping V_{ds} in (4) and electrical power density applied in (3). The ambient temperature is 30 °C. (c) Temperature calibration with the device in non-powered state, as a function of platform temperature. (d) Extracted dependence of temperature on power density and the corresponding thermal resistance.

To further demonstrate that pre-trapping mitigated the effect of trapping on the drain current temperature measurement, measurements were repeated using the same power dissipation (~0.59 ± 0.02 W/mm), but with different drain and gate bias voltages, shown in Table I. Temperature rise should be almost identical in each case, though trapping effects will be different under the pulsed electrical conditions to measure temperature. There is a significant 2.5 mA variation in I_{ds} (15%) without performing the pre-trapping, corresponding to a 53 °C measured temperature error. In contrast, when the pre-trapping step is included, the measured temperatures are identical within the experimental uncertainty, for all bias voltages. This highlights that trapping effects have been mitigated and confirms that the pre-trapping and cooling conditions are appropriately chosen for the devices studied here.

ANSYS 3D finite element thermal simulations were used to predict the transistor temperature distributions at each of the measurement conditions. An axisymmetric model was employed for this circular structure with anisotropic thermal conductivity for Ga_2O_3. Temperature dependent thermal conductivities of $29 \times (300/T)^{1.27}$ W/m·K and $13.7 \times (300/T)^{1.12}$ W/m·K were used for out-of-plane [010] and in-plane [001] directions.[23] The Channel Joule heating distribution was obtained from a drift-diffusion model simulated using Silvaco ATLAS as in Ref. 22. Figure 4(a) shows a comparison of measured temperatures and simulation, and (b) shows the simulated transient peak channel temperature. In general, the simulated average source-drain temperature rise is close to the measured value, illustrating that the electrical method measures an average over the whole device periphery; this is consistent what has been reported for electrical temperature measurements on other technologies, such as GaN, e.g., in Ref. 24. The temperature-dependent thermal conductivity of Ga_2O_3 leads to a temperature-dependent R_{th}, whereas the measurement analysis assumes, for simplicity, a fixed R_{th} value, causing a difference at high power dissipation.

The simulated peak channel temperature thermal resistance is 88 K·mm/W, i.e., 27% higher than the measured average temperature. For comparison, the peak R_{th} simulated here is identical to the peak channel thermal resistance of 88 K·mm/W measured using Raman nano-thermometry on a similar size transistor,[12] albeit with somewhat different transistor layout. Regarding the simulated transient response of the transistor, the thermal time constant is ~3 ms and much greater than the 1.4 μs measurement delay in (4), confirming that cooling can be neglected for the measurement parameters used here.

In conclusion, we proposed a trapping tolerant method for electrical based temperature measurements of Ga_2O_3 MOSFETs. We introduced a pre-trapping process to minimize the effect of trapping on temperature measurements. A thermal resistance of 59 K·mm/W was measured. 3D thermal simulations confirmed that an average temperature rise across the whole device periphery is measured. This

TABLE I. A comparison between temperature measurements with and without the pre-trapping pulse.

			Heating (1.6 s)				
	Pre-trapping (3 s)	Cooling (3 s)	V_{gs} (V)	V_{ds} (V)	Power density (W/mm)	Measured I_{ds} (mA) ($V_{gs} = 0$ V, $V_{ds} = 20$ V)	Measured temperature rise (°C)
Without pre-trapping	NaN	NaN	0	16.5	0.60	17.2	24
			−13	18	0.58	17.2	24
			−20	28	0.61	16.0	49
			−23	44	0.58	14.7	77
With pre-trapping	$V_{gs} = -14$ V $V_{ds} = 50$ V	No bias	0	20	0.58	12.4	34
			−13	22	0.60	12.5	35
			−20	28	0.59	12.5	35
			−23	44	0.57	12.5	35

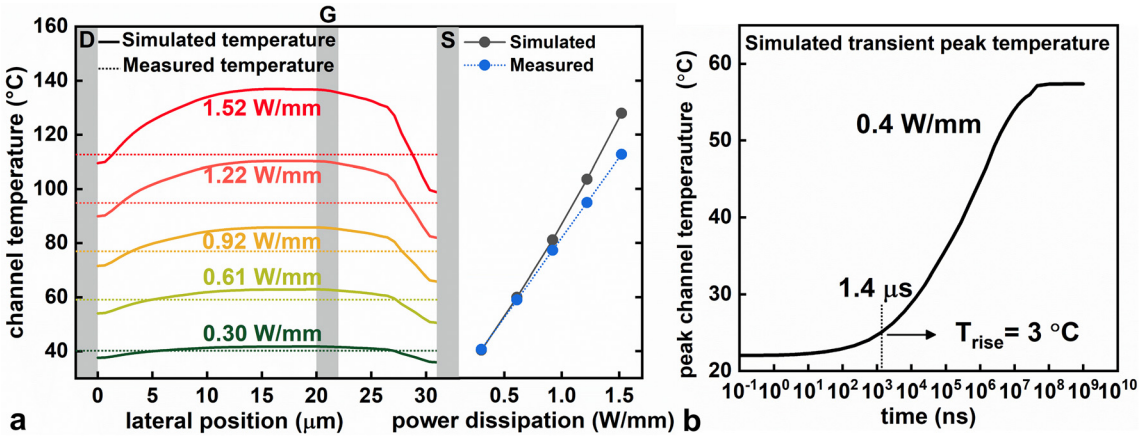

FIG. 4. (a) Comparison between simulated channel temperature profiles and measured temperature (calculated by $R_{th} \times P_{diss} + T_{amb}$, $R_{th} = 59\,\mathrm{K\,mm/W}$). The right black line and symbols are the simulated average channel temperature. (b) Simulated transient peak channel temperature with the device operated at 0.4 W/mm. In the time of 1.4 μs after switching the device on, there was only 3 °C temperature change.

temperature measurement method could also be used to overcome the impact of trapping effects on electrical thermal measurement in other Ga_2O_3-based, or even other technologies (GaN, etc.), by choosing pre-trapping, heating, and measurement pulse lengths appropriate to the trap time and thermal time constants of the device under test.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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