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Effect of oxide layer growth conditions on radiation detection performance of Ni/SiO_2/epi-4H-SiC MOS capacitors

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Abstract – High resolution radiation detection has been demonstrated using Ni/SiO_2/n-4H-SiC metal-oxide-semiconductor vertical capacitors fabricated using highly crystalline 4H-SiC epilayers. The oxide layers have been grown thermally using two different approaches: i) in-air, and ii) oxygen-ambience oxidation. The devices fabricated using the former method exhibited dark currents one order of magnitude higher than that in the latter. The observed difference has been attributed to the back-contact series resistance and capacitance. Regardless of the difference in the device parameters, detectors prepared using both the methods exhibited very high energy resolution of ≤ 0.5% for 5486 keV alpha particles emitted by a ^{241}Am radioisotope. Capacitance mode deep level transient spectroscopic studies revealed similar type of electrically active defects along with $Z_{1/2}$ and EH_5 deep level defects. The DLTS scans also revealed positive polarity peaks in both the types of devices which indicate emission from minority carrier trap centers. The activation energy corresponding to the peak was found to be ~1.2 eV which has been assigned to HK3 defects responsible for hole trapping in 4H-SiC. The possibility of appearance of the positive peak due to non-negligible impedance of the back-contact has been ruled out based on the observation that the centroid of the observed peak did not change with detectors having different device parameters.

Keywords: B2. 4H-Silicon carbide (4H-SiC), B3. Metal-oxide-semiconductor (MOS) capacitor, A3. Epitaxial layer, A1. Defects, A1. Minority carrier traps, A1. Deep level transient spectroscopy (DLTS).

1. Introduction

Owing to the excellent combination of physical properties such as wide bandgap (WBG), low on-state resistance and high breakdown voltages, 4H-SiC offers power losses much lower than that experienced in silicon power devices [1]. In addition, 4H-SiC is a radiation hard material which can withstand high temperatures and chemically corrosive environments, making it suitable for applications in harsh environments such as extra-terrestrial and deep space mission, nuclear core reactors, particle accelerators, and laser generated plasma environments [2] [3] [4] [5] [6] [7]. During the last decade, the advances in the growth of epitaxial 4H-SiC has led to the achievement of extraordinary crystalline quality with ultralow micropipe density and electrically active deep defect concentrations [8] [9] [10] [11]. Deep level defects can lead to charge trapping or recombination leading to deterioration of carrier mobility and lifetime which largely affects the charge transport of any electronic or optoelectronic device [12] [13]. Micropipe, a structural defect, is basically a hollow-core threading screw dislocations (TSDs) which are known to induce device failures and reliability issues [14] [15] [16].

Another key advantage of 4H-SiC is that its highly stable native oxide is silicon dioxide (SiO_2), which makes it compatible with the mature silicon processing techniques [17]. Metal-oxide-semiconductor (MOS) devices fabricated on 4H-SiC promise high performance compared to silicon MOS devices under extreme high voltages, high frequencies, and high temperatures [18] [19] [20]. However, presence of

residual carbon on the SiO_2/4H-SiC interface following oxidation, leads to a density of interface trapped charge which is order of magnitudes higher than that observed in Si/SiO_2 interface [21] [22]. The high density of interface trapped charge leads to instability in the threshold voltage which at present is the biggest challenge for wide scale commercialization of 4H-SiC MOS based devices [1] [17].

Apart from power electronics applications, 4H-SiC epitaxial layers have been demonstrated to perform as high-resolution radiation detection [23] [24] [25] [26] [27]. Recently, Ni/SiO_2/4H-SiC MOS devices have also been demonstrated as excellent radiation detectors [28] [29]. Junction based detectors are generally metal-semiconductor (MS) structures operating under reverse bias. MS structures however does not offer optimized electrical characteristics because of the Fermi level pinning related to the metal induced gap states near the interface. An interfacial oxide layer unpins the Fermi level as well as offer additional quantum barrier to the charge carriers thereby improving the electrical properties of the junction [17]. Dry thermal oxidation of 4H-SiC is an economical choice of deposition of SiO_2 layer compared to sophisticated techniques like atomic layer deposition (ALD) which, nevertheless, has demonstrated improvement in electrical performance of SiO_2/4H-SiC MOS capacitors [17]. In the present work, SiO_2 layers have been grown on 20 and 50 μm thick n-type 4H-SiC epitaxial layers using two dry thermal oxidation approaches viz., in-air thermal oxidation and oxygen-flow thermal oxidation. The Ni/SiO_2/4H-SiC MOS capacitors have been characterized electrically using current-voltage and capacitance-voltage measurements. The radiation detection performances of the devices have been evaluated and compared in terms of energy resolution. The MOS detectors have been studied using capacitance mode deep level transient spectroscopy (C-DLTS) to identify the electrically active defects that defines the energy resolution.

2. Experimental Details

2.1. Device fabrication

Fig. 1(a) shows a schematic of the Ni/SiO_2/n-4H-SiC vertical MOS capacitor device structure fabricated on n-type 4H-SiC epitaxial layers. The 4H-SiC epilayers have been grown on the (0001) face of highly conductive bulk 4H-SiC (0.015-0.028 Ω.cm) substrates 4° off-cut towards the $\langle 11\bar{2}0 \rangle$ direction. A 1 μm thick buffer layer with a carrier concentration of 10^{18} cm^{-3} was included between the 4H-SiC bulk substrate and the epilayer. The wafers were diced in square shapes with 8 mm edge length. The diced wafers were RCA cleaned [30] to remove organic residues accumulated during post-growth processing. Dilute hydrofluoric acid (HF) etching was done for 1 min to remove the native oxide (SiO_2) layer in order to ensure similar initial surface conditions among differently prepared devices. Thermal oxidation has been performed in a GSL – 1100X tubular horizontal furnace at 1000 °C either in air or under oxygen flow. In-air oxidation was chosen for one of the 20 μm thick epilayer wafers henceforth known as A-SiC-20. For the oxygen-ambient oxide growth, high purity oxygen gas was flown through a quartz tube containing a 20 μm and a 50 μm thick epilayer device placed inside the furnace. The 20 μm and the 50 μm devices, prepared using oxygen ambience oxide growth, will be designated as O-SiC-20 and O-SiC-50. The oxygen flow rate was set to ~8 mL/min using a flow meter for the wafers oxidized in oxygen ambience. The 4H-SiC wafers were inserted in the furnace, following which it was heated to 1000 °C at a ramp rate of 10 °C/min. The oxidation temperature and the ramp rate has been kept same for both in-air and oxygen-ambient growth conditions. For the sake of reproducibility and comparison with various samples oxidized separately, the location of the sample inside the furnace during the oxidation procedure has been precisely maintained. Following the completion of the thermal oxidation, 25 nm thick circular ($\emptyset = 3.8$ mm) nickel contacts have been deposited on the top of the epilayer side (Si-face) to form the gate contact and 100 nm thick of 6×6 mm^2 square nickel (Ni) contact was deposited on the bottom (C-face) surface to form the bulk (back) contact. The Ni depositions have been carried out using a Quorum

Q150T DC sputtering unit. The photograph of a finished Ni/SiO_2/n-4H-SiC vertical MOS capacitor device used in this study is shown in Fig. 1(b).

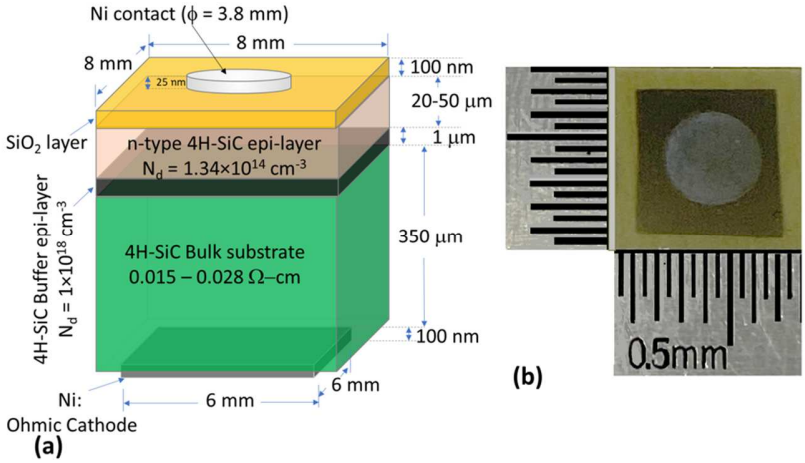

Figure 1. (a) Schematic of the Ni/SiO_2/n-4H-SiC vertical MOS capacitor structure fabricated on an n-type 4H-SiC epilayer. **(b)** A fabricated Ni/SiO_2/n-4H-SiC vertical MOS capacitor.

2.2. Electrical Characterization and Deep Level transient Spectroscopy

Current-voltage (*I-V*) measurements have been carried out using a Keithley 237 source-measure unit with the devices mounted inside an electromagnetic interference (EMI) shielded box. Capacitance-voltage (*C-V*) and the capacitance mode deep level transient spectroscopic measurements were carried out using a SULA DDS-12 DLTS system equipped with a 1 MHz capacitance meter unit. Both the *I-V* and *C-V* measurements were carried out by applying the bias to the top Ni contact. For the temperature variation in the C-DLTS measurements, the MOS capacitors were mounted inside a Janis VPF 800 LN_2 cryostat controlled by a Lakeshore LS335 temperature controller. The DDS-12 DLTS system was equipped with 12 choices of digital rate windows and allows simultaneous recording of DLTS spectra with 4 rate window settings in a single temperature scan. The device was kept at a quiescent bias V_r = -12 V prior to the electrical pulsing to V_p= 0 for trap filling. The filling pulse width was set to 2 ms to ensure saturated trap filling and repeated each 50 ms.

2.3. Device Radiation Response Characterization

The radiation detection performance of the MOS devices were examined from the pulse height spectra (PHS) acquired using an Americium-241 (^{241}Am) radioactive source emitting α particles with primarily three energies viz. α_1= 5486, α_2 = 5443, and α_2 = 5388 keV with emission rates of 85%, 14%, and 1%, respectively. A standard benchtop alpha spectrometer comprising a charge sensitive Amptek A250CF pre-amplifier, an Ortec 572 spectroscopy preamplifier, and a Canberra Multiport II multichannel analyzer has been used for the PHS acquisition. The MOS detectors were placed inside an EMI shielded box which has been continually evacuated during the PHS acquisition to minimize the scattering of alpha particles with air molecules before reaching the detector window. The alpha spectrometer was calibrated using an absolute calibration method described elsewhere [31].

3. Results and Discussions

3.1. Electrical Characterization

The variation of gate leakage currents measured as a function of positive and negative gate bias V_g are shown in Fig. 2(a) and (b), respectively. All the three devices exhibited leakage currents under negative gate bias that are suitable for high-resolution and high efficiency (charge collection) radiation detection applications. Radiation detectors which exhibit high leakage currents at bias voltages optimized for the maximum charge collection offers poor energy resolution primarily due to the increase in white parallel noise [32]. The dark current densities measured under negative gate bias for the MOS capacitors O-SiC-20 and O-SiC-50, both grown in oxygen ambient, have been observed to be consistently lower by at least an order of magnitude compared to that measured for A-SiC-20 (in-air oxidation). The forward bias characteristics (Fig. 2(a)) for both the 20 µm thick epilayer devices resembled to that of a metal-semiconductor Schottky barrier diode. The surface barrier heights and the diode ideality factors were found from the linear region of the ln$I$ vs V_g plots following a thermionic emission model [33]. The surface barrier height and the diode ideality factor were calculated to be 1.33 eV and 2.78 for A-SiC-20, respectively and the same for the O-SiC-20 were found to be 1.35 eV and 2.35. The positive bias *I-V* characteristic for the 50 µm thick epilayer device did not reveal any linear region suitable for the application of the above model. Since the barrier heights of both the 20 µm thick epilayer devices are same, the observed difference in the dark current corresponding to the negative gate bias is most likely due to the different series resistances from the back contact. As because, the back contact is deposited after the oxide layer is grown, the back contact impedance is non-negligible and is supposed to vary due to the different rate of growth of the oxide layer in the case of two approaches.

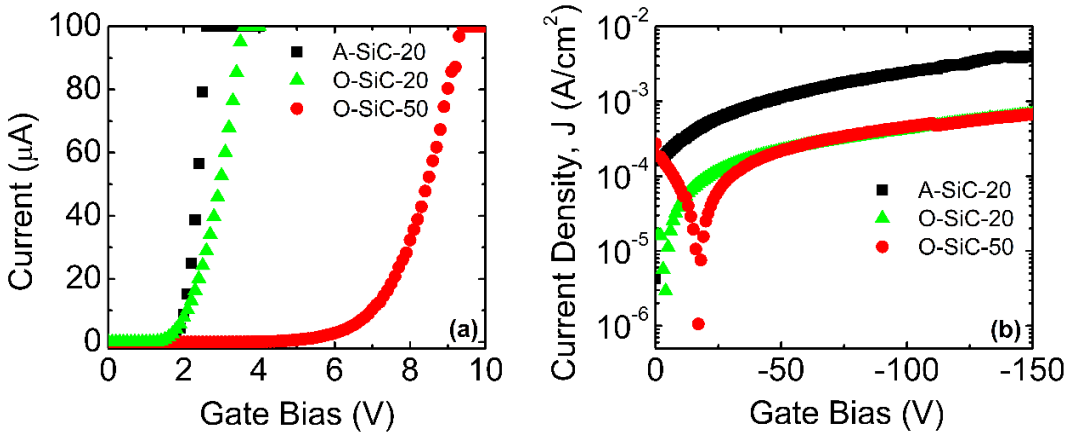

Figure 2. Variation of device current as a function of positive gate bias **(a)** and current density as a function of negative gate bias **(b)** for 20 µm (A-SiC-20 and O-SiC-50) and 50 µm (O-SiC-50) thick Ni/SiO_2/n-4H-SiC vertical MOS capacitor measured at room temperature and under dark.

The variation of MOS capacitance vs negative gate voltage, as shown in Fig. 3(a) revealed a nature obtained for Schottky diodes under reverse bias. The Mott-Schottky plots showed a linear relation between the $\frac{1}{C^2}$ and the gate bias V_g as shown in Fig. 3(b). The effective carrier concentrations, N_{eff}, were determined from the linear fit to the Mott-Schottky plots following Eq. 1 given below.

$$\frac{1}{C^2} = \frac{2}{q\epsilon_{4H-SiC}N_{eff}}\left(V_{bi} - V_g\right) \quad (1)$$

where, q is the elementary charge of an electron, ϵ_{4H-SiC} is the electrical permittivity of 4H-SiC, and V_{bi} is the built-in potential. The N_{eff} values were calculated to be 1.3×10^{14}, 1.0×10^{14} and 1.2×10^{14} cm^{-3} for the A-SiC-20, O-SiC-20, and O-SiC-50, respectively. Although the effective carrier concentration has

been found to be similar, the capacitance of the MOS device fabricated using the epilayer with oxide layer grown in-air was found to be higher by several factors at any given gate bias compared to the devices with the oxide layer grown in oxygen ambience.

The comparison of the above *I-V* and *C-V* characteristics from the different devices reveals that the gate current and the junction capacitance are widely different between the devices with in-air and oxygen ambience grown oxide layer. In general, the observed difference could be due to the difference in bulk device parameters such as the series and shunt resistance, back contact capacitance of the diode etc., or the interfacial parameters such as junction capacitance, barrier height, density of interfacial states etc. However, the above arguments tend to incline the reason behind the observe differences towards the difference in bulk properties such as different series resistance, and back contact capacitance. The drawn inference will be useful to identify the positive DLTS peaks, described later in this article, as minority carrier trap related.

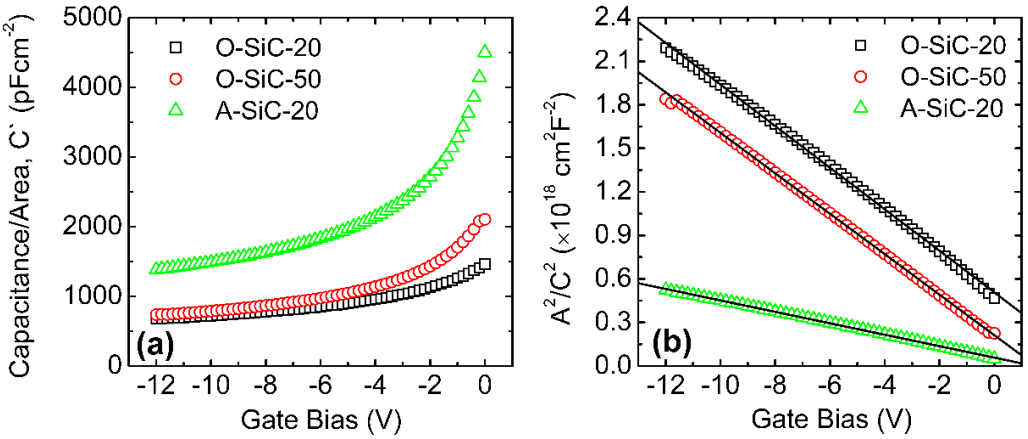

Figure 3. (a) Variation of capacitance per unit area as a function of negative gate bias for the Ni/SiO_2/n-4H-SiC vertical MOS devices. **(b)** The corresponding Mott-Schottky plots. The solid lines are the linear fit to the experimental data.

3.2. Radiation Detection

Fig. 4 (a) and (b) show the ^{241}Am alpha pulse height spectra for the A-SiC-20 and the O-SiC-50 MOS detector, respectively at optimized gate bias voltages of -40 V. Since the effective doping concentration of both these devices are almost same, the depletion widths at a certain negative gate bias are expected to be the same. Once the depletion width approaches the maximum penetration depth or range of the 5486 keV alpha particles in 4H-SiC (~18 μm), all the radiation induced charge carriers are generated within the depletion width a condition where the charge collection efficiency almost always approaches the optimum value [28] [32] [34]. The depletion width achieved by the above detectors at -40 V gate bias was calculated to be ~14 μm. As the depletion width is less than the range of the alpha particles in the present case, a fraction of the charge pairs will be created in the neutral region of the 4H-SiC epilayer. However, since the minority carrier diffusion length is very high in these epilayers, most of the holes generated in the neutral region manage to diffuse to the depletion region and adds to the charge collection efficiency [32]. Hence, the optimized bias for both the detectors were found to be below the bias needed to deplete the detectors to a width equaling the range of the alpha particles. The detector performance has been seen to saturate beyond -40 V and the effect of leakage current or device capacitance was found to be negligible even at gate bias voltages as high as -200 V. The optimized shaping time for the spectroscopy amplifier was found to be 2 μs for both the detectors. Under the optimized bias and shaping time the

detectors have been seen to resolve all the primary alpha particles —5388, 5443, and 5486 keV—with a percentage energy resolution of less than 0.5 % FWHM for the 5486 keV peak. To determine the energy resolution of the detection system, the partially resolved peaks were deconvoluted using multiple Gaussian fit to obtain the width of the peaks in terms of full width at half maximum (FWHM). The FWHM of the alpha peak has been expressed as percentage of the actual energy (5486 keV) to calculate the percentage energy resolution of the detector at that energy. The observed energy resolution of the O-SiC-50 MOS detector is even better than that observed in our previously reported Schottky barrier detector fabricated on similar 50 µm thick 4H-SiC epilayer [8].

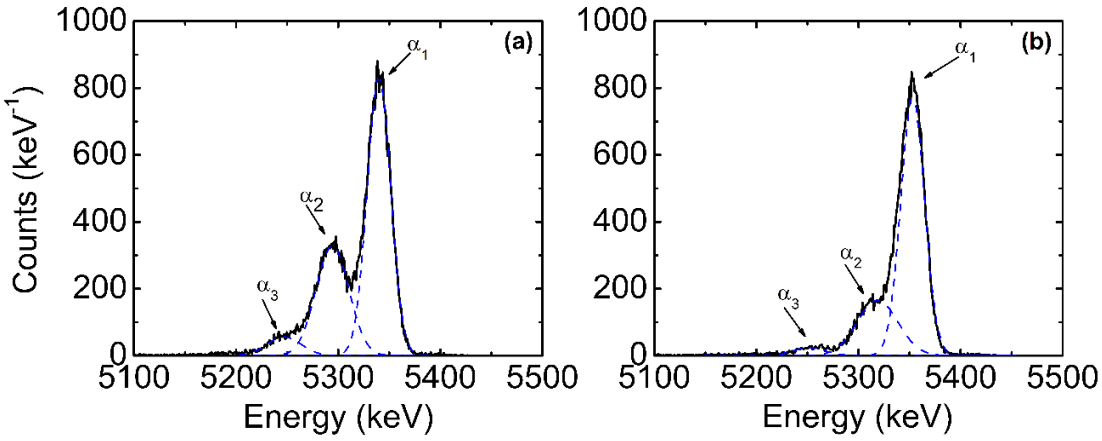

Figure 4. Pulse height spectra obtained for the Ni/SiO_2/n-4H-SiC vertical MOS detectors A-SiC-20 **(a)** and O-SiC-50 **(b)** exposed to a ^{241}Am source. The dashed lines are the multiple Gaussian fits used to calculate the centroid and width of the partially resolved peaks.

3.3. Defect Level Transient Spectra Analyses

Capacitance mode DLTS measurements were carried out on the Ni/SiO_2/n-4H-SiC vertical MOS devices for detecting and identifying the defect centers that degrade the device performance. Deep level transient spectroscopy is a technique that studies the emission rates of carriers from trap centers using thermal scans [35]. As is evident from the *C-V* measurements presented in Section 3.1, the device capacitance exhibited a behavior similar to that of a reverse biased diode which is ideal for capacitance mode DLTS measurements. In a typical capacitance mode DLTS measurement the signal is defined as the change in the capacitance (ΔC) measured within a rate window $\Delta\tau$ on a capacitance transient obtained from the device followed by the termination of a trap filling pulse. The emission rate e_n, the capture cross-section σ_n and the location of the trap energy level within the bandgap ΔE are related as shown in Eq, 2 below. They are plotted using Eq. (2) given below,

$$e_n/T^2 = (\sigma_n \langle v_{th} \rangle N_c/g)e^{-\Delta E/kT} \quad (2)$$

where, $\langle v_{th} \rangle$ is the mean thermal velocity of electrons and g is the degeneracy of the trap level. A typical DLTS thermal scan shows peaks at different temperatures on a ΔC vs temperature plot corresponding to each resolvable trap center. The DLTS thermal scans are generally repeated for different rate window ($\Delta\tau = 1/e_n$) settings. The variation of the peak positions with different rate windows are used to obtain Arrhenius plots from which the capture cross-section and the activation energy of a particular defect can be calculated. The traps concentration N_t has been extracted using Eq. (3) below.

$$N_t = 2\left(\frac{\Delta C(0)}{C_0}\right) N_{eff} \tag{3}$$

where, $\Delta C(0)$ is the change in depletion capacitance, and C_0 is the steady-state capacitance.

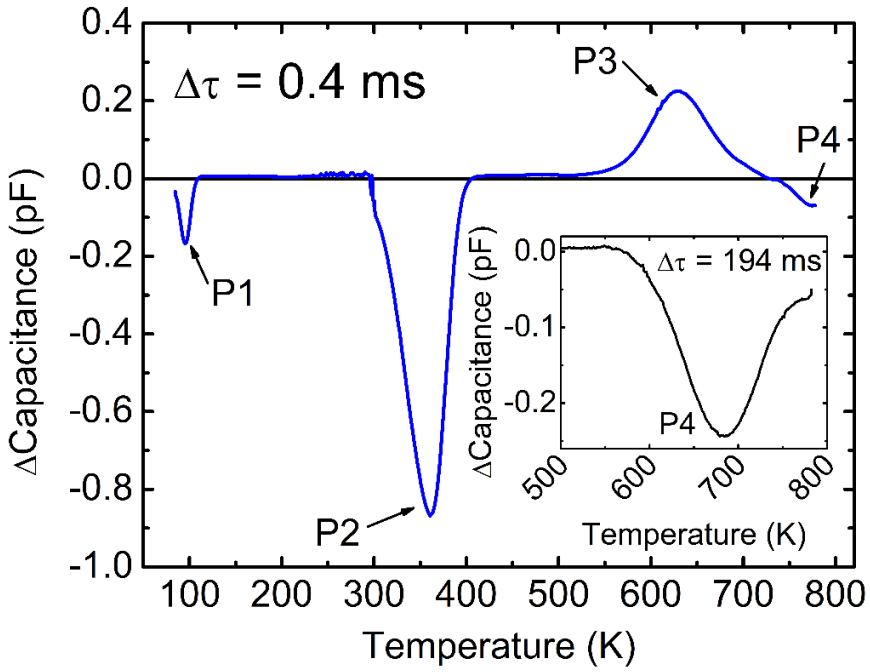

Figure 5. DLTS spectrum for A-SiC-20 MOS device in the temperature range 80 – 800 K obtained using a rate window $\Delta\tau = 0.4$ ms. The peak P4, partly visible in the given scan range, has been shown in the inset using a higher rate window at which it fully evolved.

Figure 5 shows the DLTS spectrum for the MOS devices A-SiC-20 obtained in the thermal scan range 80 – 800 K for a single rate window setting $\Delta\tau = 0.4$ ms. At least four peaks (P1 through P4) were observed in the thermal scans. The peak P4 did not evolve fully in the scan shown in Fig. 5, however, full peak formation has been observed using higher rate window settings as shown in the inset. Figure 6 shows the DLTS plot obtained for the MOS devices O-SiC-50. At least 5 peaks (P1 through P5) have been observed for the MOS capacitor A-SiC-50 with 50 µm thick epilayer. Several rate window settings have been used for both the detectors to record the DLTS spectra in order to obtain the Arrhenius plots for each trap related peak. The Arrhenius plots obtained for all the detected peaks for A-SiC-20 and O-SiC-50 are shown in Fig. 7(a) and (b), respectively. The trap parameters extracted from the DLTS spectra of the MOS devices A-SiC-20 and O-SiC-50 are listed in Table 1.

The three peaks P1, P2, and P4 out of 4 observed in the DLTS scan of the device A-SiC-20 shown in Fig. 5, are the commonly observed trap related peaks in 4H-SiC epilayers. The peak P1 with an activation energy of 0.13 eV corresponds to titanium impurity Ti(h) commonly identified as the triply ionized titanium acceptor (Ti^{3+}) lodged at the hexagonal Si lattice sites [36] [37] [38]. The peak P2 corresponds to an activation energy of 0.73 eV and is attributed to $Z_{1/2}$ center. The $Z_{1/2}$ center has been established as the major lifetime killing defect in 4H-SIC [39]and has been identified as either silicon and carbon vacancy complexes ($V_{Si} + V_C$), or antisite complexes ($C_{Si} + Si_C$) pairs, or a pair of an antisite and a vacancy of different atoms [40] [41] [42]. The activation energy corresponding to the peak P4 has been calculated as 1.30 eV which is close to EH_5 trap center reported to be located approximately 1.1 eV below the conduction band edge [43] [44]. EH_5 trap center has been identified as carbon clusters. Defect levels

related to chlorine impurity *Ci*1 in 4H-SiC has been reported to have activation energy equal to 1.34 eV [43], however it is unlikely to find chlorine impurities in detectable quantities in the present epilayers. Peaks similar to P1, P2, and P4 has also been identified in the MOS capacitor O-SiC-50 labelled as T2, T3, and T5. An additional peak T1 with an activation energy of 0.17 eV has also been detected in O-SiC-50. The trap related to T1 has been identified as the Ti(c) which is Ti impurity lodged in a cubic Si lattice site [36] [37] [38].

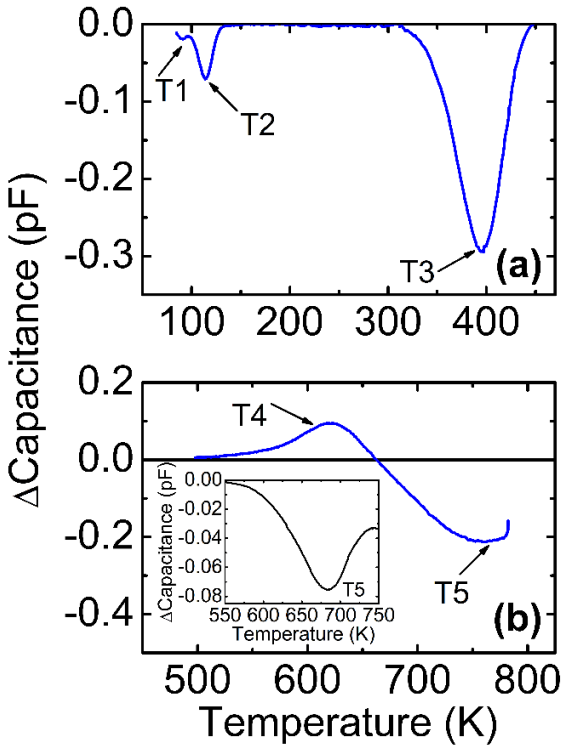

Figure 6. DLTS spectra for Ni/SiO_2/n-4H-SiC vertical MOS detectors O-SiC-50 obtained in the temperature range 84 - 450 K **(a)** and 500 - 750 K **(b)**. The fully formed peak T5 is shown for a higher rate window within the inset.

The above-mentioned peaks P1, P2, P4 and T1, T2, T3, T5 are all negative peaks as can be seen in the DLTS spectra presented in Figs. 5 and 6. A negative peak in capacitance deep level transient spectrum indicates that the corresponding defect is a majority carrier trap center and hence the activation energy gives the energy positions of the trap levels measured from the conduction band edge. The peaks P3 and T4, however, are observed to be positive with activation energies 1.27 and 1.22 eV, respectively. In capacitance mode DLTS, a positive polarity peak indicates emission from minority carrier trap centers. Populating minority carriers using electrical pulsing, as has been done in this case, is however unlikely for Schottky type junction devices under normal circumstances, because of the insignificant injection of minority carriers during the trap filling using electrical pulsing. Nevertheless, in the case of Schottky diodes with back Ohmic contacts having non-negligible impedance, it has been demonstrated that capacitance mode DLTS scans can exhibit spurious positive peaks which may not be related to any trap center [45] [46]. However, minority carrier trap-related positive peaks have been reported by others in electrically pulsed p-type GaAsN Schottky devices without intentional injection of minority carriers wherein the contribution of the back contact has been ruled out [47]. The spurious peaks are supposed to change their position depending on the series resistance and the equivalent capacitance of the back contact though [45]. The positive DLTS peaks observed in the present study for both the devices have

been found to exist in the same position on the temperature scale of the DLTS spectra and yield same activation energies albeit having widely different device capacitance and series resistance as observed from the *I-V* and *C-V* measurements. Hence, the observed positive peaks have been considered to be appearing most likely from the minority (hole) traps present in the 4H-SiC epilayers. The activation energies corresponding to the positive peaks P3 and T4 in A-SiC-20 and O-SiC-50, respectively has been found to be 1.27 and 1.22 eV. Incidentally, primary hole traps designated as HK3 center (related to carbon vacancies) with activation energy 1.27 eV has been reported in p-type 4H-SiC layers [48] [49], [50]. Hence, the observed positive DLTS peak has been identified as the HK3 center which is a hole trap most likely related to carbon vacancies.

Table I. Trap parameters obtained from the capacitance mode DLTS measurements of A-SiC-20 and O-SiC-50 MOS detector.

Peak	ΔE (eV)	σ_n (10^{-15} cm^2)	N_t (10^{12} cm^{-3})	Possible Trap Identity
P1	$E_c - 0.13$	0.20	1.18	Ti (h)
P2	$E_c - 0.73$	27.7	6.26	$Z_{1/2}$
P3	$E_v + 1.27$	7.23	1.48	HK3
P4	$E_c - 1.30$	0.03	1.24	EH_5
T1	$E_c - 0.15$	90.4	0.17	Ti (h)
T2	$E_c - 0.17$	4.44	0.61	Ti (c)
T3	$E_c - 0.68$	7.02	2.55	$Z_{1/2}$
T4	$E_v + 1.22$	0.3	0.14	HK3
T5	$E_c - 1.11$	0.003	0.56	EH_5

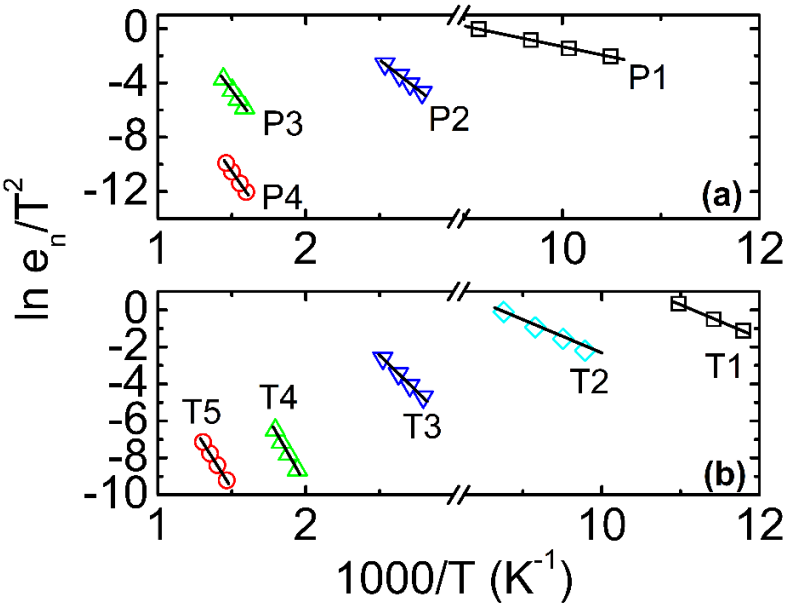

Figure 7 The Arrhenius plots corresponding to DLTS peaks presented in Figs. 5 and 6 for the Ni/SiO_2/n-4H-SiC vertical MOS detectors A-SiC-20 **(a)** and O-SiC-50 **(b)**.

4. Conclusions

Metal oxide semiconductor (MOS) capacitor structures have been realized by growing SiO_2 layers on detector-grade highly crystalline 20 μm thick n-type 4H-SiC epilayers by thermal oxidation. A 25 nm thick nickel layer has been used as the metallic gate contact which also facilitates efficient charged particle detection. The difference in device behavior between two approaches for growing the SiO_2 layers viz. in-air oxidation and oxygen-ambient oxidation, has been studied. Current-voltage and capacitance voltage characteristics suggested that while the junction properties (barrier height and diode ideality factor) and the effective doping concentration remain almost similar in the devices fabricated using the two different techniques, the difference in device properties such as the back contact capacitance and the back contact series resistance results in the observed difference of device current and capacitance. A similar MOS capacitor has been fabricated on a 50 μm thick 4H-SiC epilayers and oxygen ambient grown oxide layer. The 20 and 50 μm devices with oxygen-ambience oxide layer behaved very similarly in terms of device current and capacitance. The radiation response of the MOS capacitor devices have been tested in terms of energy resolution using a ^{241}Am alpha source. The 20 μm device with in-air grown oxide layer and the 50 μm thick 4H-SiC epilayers and oxygen ambient grown oxide layer both exhibited high energy resolution of ≤ 0.5% for 5486 keV alpha particles. The energy resolution of the 50 μm MOS device is better than our previously reported resolution of 0.8% obtained using a 50 μm Ni/n-4H-SiC Schottky barrier diode. The electrically active defects responsible for partly defining the energy resolution of these devices have been studied using capacitance mode DLTS measurements. The DLTS spectra showed the presence of similar majority carrier defects regardless of the oxide growth procedure which is expected as DLTS gives information on the bulk defects. The DLTS spectra also showed the presence of a minority carrier trap center located ~1.2 eV above the valence band edge. The presence of minority carrier related peaks in capacitance mode DLTS is not generally observed with electrical trap-filling pulse (as has been used in this case). The role of back contact in the appearance of the positive polarity DLTS peak has been ruled out as both the devices with different device parameters showed the presence of the peak at the same temperature. The study finds that radiation detection using a MOS capacitor type device might exhibit better energy resolution and prompts to launch investigation to understand the device physics behind such observation.

Acknowledgment

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