Coupled-DC Module-Based Photovoltaic System With Power Mismatch-Tolerated Modulation

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Abstract

This article presents a coupled-DC power module-based cascaded multilevel converter integrating utility-scale photovoltaic (PV) generations (coupled-DC-link power module (CDPM)-PV). CDPM-PV inherits merits such as modular structure, distributed maximum power point tracking (MPPT), direct distribution grid access, from cascaded H-bridge-based PV (CHB-PV) system. But, it supplies more flexible power routes than CHB-PV, through coupling different DC-links. Power routes are intended for enlarging the entire operating range including conditions of active power mismatch arising from nonideal elements such as partial shading and parameter variations. The system construction with its self-balancing principle is first introduced. Switching states for different operating regions are then derived based on the principle of easing implementation. Based on these, a modulation strategy including initial switching pattern selection and coordinated power routing is proposed to allow module-mismatches. Operating ranges are also analyzed and compared with conventional CHB-PV. Simulation results of a 3-MW/13.8-kV system developed in MATLAB/Simulink platform, and experiment results based on a 2.4-kW/311-V setup are presented and have demonstrated that the CDPM-PV topology with proposed modulation strategy can not only ride through a larger range of module mismatches, but also improve solar power utilization and system efficiency owing to noncompromised MPPT.

Index Terms

Cascaded photovoltaic (PV) systems, coupled-DC module, modulation, module mismatch

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1. Introduction

Facilitated by the energy internet concept, utility-scale distributed energy resources (DER) such as wind farms, photovoltaic (PV) power stations, electric vehicle charging stations, energy storage power stations, etc., interacting with a medium- or high-voltage (MV/HV) distribution grid are growing in a rapid way [1]–[6]. Power electronics converters are enhancing efficiency and power density of the whole integrated DER system. Especially, cascaded H-bridge (CHB) has recently gained considerable attention due to its advantages in terms of modularization, extendibility, and minimization of power semiconductors. CHB can extract maximum power from DER, allow advised optimal charging/discharging for batteries, and allow the access of different kinds distributed loads as well. It has been widely applied in different places and is still a converter of great potential.

CHB-based photovoltaic (CHB-PV) generation system interacting with MV/HV power grid is a typical utility-scale DER application [7]–[10], which is the sequential combination of CHB, HVDC/high-frequency alternating current (HFAC), a high-frequency transformer (HFT) with phase-shift inductor and HFAC/low-voltage direct current (LVDC). Thanks to the extra power stages, HV insulation can be achieved, i.e., leakage current loop can be cut off easily [7]. Nevertheless, being susceptible to diversities in operating environment, manufacturing, etc., active power on modules will not be uniform consequently, which can cause DC-link voltage imbalance and even disturb the system stability. And in three-phase level, power imbalance issue can be introduced. The module power mismatch is the hurdle to the wide application of CHB-PV [11]–[15].

A severe module mismatch is likely to run a cascaded PV system at over-modulation risk. The DC voltage utilization rate has been defined as the index that indicates the degree allowing module-mismatch [15]–[18]. The utilization rate is lower, the degree is higher. Hence, a DC-voltage over-designed system is possible to handle some light module-mismatch conditions. In the early studies such as [4], [11], [15], [16], and [19]–[21], DC voltage difference is used as the error and a simple P or PI controller is adopted to adjust the modulation index for each module. Modulation indexes on modules are redistributed. But they cannot exceed the upper limit inherited from conventional phase-shifted pulse width modulation (PS-PWM)/level-shifted pulse width modulation (LS-PWM). The improvement is still limited. To further develop the module-mismatch operating ability, a reactive power compensation strategy is used. Nevertheless, the reactive power would occupy a rather amount of the system capacity and introduce considerable copper loss. Therefore, Wang *et al.* [18] proposed an improved LS-PWM modulation that can realize square modulation for certain modules, thus has larger DC voltage utilization rates, which releases the reactive power requirement. However, its modulation process requires frequent voltage-sorting actions and considerable switching events. Power hardware organizing can also help to mitigate the module-mismatch issues. Achanta et al. [22] proposed a very flexible three-phase PV power plant structure.

The three-phase imbalance problem is well addressed. However, the module-mismatch inside each phase leg still exists and requires further consideration.

In this article, a cascaded coupled-DC module-based PV (coupled-DC-link power module (CDPM)-PV) system is presented for the first time, inspired by the fact that more goals can be achieved through improving system topology. Actually, in recent years, there emerge some multilevel topologies that provide the option to connect modules in not only series, bypass, but also parallel, like the back-to-back full-bridge (B2B-FB) [23], the double full-bridge (DFB) [24], the semi-full-bridge (SFB) [25], the double half-bridge (DHB) [26], and the three switch (TS) converter [27]. These topologies are possible for more flexible power exchange between modules. However, they have some operational differences that affect their coherence when used in different systems, and are never found in PV applications. This article combines such topology complexity with the features of utility scale PV system, and develops more degrees of freedom for better control and operation. Compared with CHB-PV, the improvement is replacing H-bridge (HB) with CDPMs. The interphase power imbalance issue can be solved in the similar way to CHB-PV. Inner each phase, the power module supplies more flexible power routes through coupling different DC-links. Power exchanging on each two neighboring ports becomes an autonomous process due to the CDPMs, which will discard reactive power compensation, lighten the overdesign degree, save voltage sorting burden, and reduce switching actions. The bidirectional switches equipped in each CDPM can also enhance the system redundancy, especially at conditions of switch failures. The above features upgrade the PV system in terms of efficiency, reliability, and operating range. This article focuses on the inner-phase power mismatch tolerating modulation strategy for CDPM-PV.

The rest of this article is organized as follows. Section II introduces the configuration of a two-stage grid-connected cascaded PV system with CDPMs. This is followed by the analysis of equivalent model and self-balancing principle for CDPM. In Section III, switching states for CDPM are first derived. Focally, initial switching pattern selection is explained. Based on the above analysis, an improved modulation is proposed to achieve the optimal switching pattern selection. Lastly, the overall control structure is presented to cooperate with the proposed modulation strategy. To validate the proposed technologies, the simulation results using MATLAB/SIMULINK based on a 3-MW/13.8-kV platform and the experimental results on a 2.4 kW/311-V prototype are presented in Sections IV and V, respectively.

2. Construction of Coupled-DC-Link Module-Based PV System

A. System Construction

The proposed PV system consists of a cascaded multilevel converter stage and multiple dual-active-bridge (DAB) stages forming segmented PV accessing ports. Similar as CHB-PV, the DABs are selected to achieve HV insulation, wide-range DC/DC voltage boosting and distributed

maximum power point tracking (MPPT) for the PV arrays. The HV DC side of each DAB associates with a CDPM DC-link. Topology of such a star-configured CDPM-PV system is depicted in Fig. 1. The cascaded multilevel converter stage fulfills the requirements of grid codes while delivering desirable active power to the grid. Each DC-link voltage is stabilized at a constant value. This configuration inherits the advantages of traditional CHB-PV systems [15]– [22], [28]–[31], such as applicability to MV/HV situations, independent MPPT for segmented PV arrays, no propagation of twice-the-line-frequency ripple power into the PV arrays, reduced ground leakage current, better insulation, etc. But it supplies more power routes, also more control degrees of freedom.

B. Equivalent Model of CDPMs

Considering the three legs to be balanced, the analysis will be focused onto one leg, i.e., phase a, which has its own modulation system. And in the following analysis, the phase information is omitted for simplicity. Two copies of half-bridges and one bidirectional bridge constitute a CDPM. The CDPM is the building block for the proposed PV system and featured by coupled-DC-link structure, as illustrated in Fig. 1(b). Adjacent DC-links are possible to interact with each other through the CDPM. Besides, the PV system needs two terminal half-bridges to access grid and to connect with a common neutral point. The left terminal half-bridge [grid-connected, HB^G in Fig. 1(a)] and the right terminal half-bridge [neutral point-connected, HB^N in Fig. 1(a)] can be integrated as a whole, named as a terminal H-bridge (T-HB). As such, an arm with N modules contains $N-1$ CDPMs and one T-HB. Each CDPM bridges two PV-generating units, while the T-HB serves as the terminals between each leg and the AC grid. The adjacent CDPMs (or one CDPM and one T-HB) can be dynamically configured in series, bypass, or parallel configurations. Take a two-module system (one CDPM and one T-HB), for example. Let the sign combination of i_g and v_r be $\{i_g > 0,\ v_r > 0\}$, where i_g is the grid current and v_r is the total AC terminal voltage. Positive directions of i_g and v_r are defined with Pattern 1 in Fig. 2. Driving S_1 (or S_1 and S_4) and S_7 (or S_7 and S_{10}) will result in Pattern 1(or Pattern 2). During Pattern 1 and Pattern 2, the modules operate in bypass status and series status, respectively. Based on Pattern 1, driving both S_4 and S_6 instead of S_7 alone will result in Pattern 3. Pattern 3 makes the two modules operate in parallel interconnection statuses. And Pattern 3 has the same contribution to the phase voltage reproducing as State 1. Therefore, the parallel state will not change the arm output voltage and can replace bypass states from this perspective. Based on Pattern 2, driving S_6 in instead of S_7 will result in Pattern 4. Similarly, Pattern 4 makes the two modules operate in parallel interconnection statuses as well.

The series and bypass states are equivalent to those of CHB-PV, while the parallel state is unique for the proposed CDPM-PV. It couples adjacent DC-links and splits solar power into different streams across multiple modules. Nonetheless, the mentioned “parallel” does not mean two DC-links are exactly paralleled with each other. Taking Pattern 4 for example, such a state can be

actually divided into two statuses by the sign of ($v_{dc1} - v_{dc2}$), where v_{dc1} and v_{dc2} are, respectively, the left and the right capacitor voltages. Assuming $v_{dc1} > v_{dc2}$, the equivalent circuit can be shown in Fig. 3(a), where some transistors are omitted for simplicity. The diode D_5 withstands a reverse voltage $v_{dc1} - v_{dc2}$ and thus makes the current on D_5 become zero, i.e., $i_{sp1} = 0$. In this way, the grid current will discharge the capacitor C_{dc1} until $v_{dc1} = v_{dc2}$. Such a status is illustrated in Fig. 2, named as Status 1 of Pattern 4. On the other hand, if the voltages yield $v_{dc1} < v_{dc2}$, the equivalent circuit is shown in Fig. 3(b). Instead, the diode D_8 withstands a reverse voltage $v_{dc2} - v_{dc1}$ and thus makes $i_{sp2} = 0$. The grid current will discharge the capacitor C_{dc2} instead, until $v_{dc2} = v_{dc1}$. Such a status is also illustrated in Fig. 2, named as Status 2 of Pattern 4. It is easy to see that the capacitor with larger voltage will be discharged until its DC voltage is equal to the one of another capacitor during the whole interval of Pattern 4.

Similarly, Pattern 3 has an equivalent circuit shown in Fig. 3(c) when $v_{dc1} > v_{dc2}$. The diode D_5 will withstand a reverse voltage $v_{dc1} - v_{dc2}$ and the grid current charges the capacitor C_{dc2}. At the same time, the grid current discharges the capacitor C_{dc1}. The two actions are consistent with each other, in terms of the final achievement of $v_{dc2} = v_{dc1}$. However, for the condition of $v_{dc1} < v_{dc2}$, both DC-links will be bypassed. To produce an expected charge/discharge process, Pattern 5 can be employed, as shown in Fig. 2. Its equivalent circuit is shown in Fig. 3(d), where the grid current charges the capacitor C_{dc1} and discharges the capacitor C_{dc2} until $v_{dc1} = v_{dc2}$. By proper usage of Pattern 3 and Pattern 5, the capacitor with smaller voltage can be charged until its DC voltage is equal to the one of another capacitor. This process is caused by the difference between adjacent DC-link voltages. Note that, there is no circulating current between the two DC-links owing to diodes' unidirectional current flows. This is similar for each of other sign combinations of i_g and v_r, i.e., $\{i_g > 0 \text{ and } v_r < 0\}$, $\{i_g < 0 \text{ and } v_r < 0\}$, and $\{i_g < 0 \text{ and } v_r > 0\}$.

The above voltage difference-leading mechanism will guarantee an interval during which the involved DC-links charge/discharge each other to convergent voltage values. Such a "self-balancing" process happens once the capacitor voltages meet corresponding relationships. Extension of the "self-balancing" mechanism to a system with more than two modules is also straightforward. Take a four-module system (one T-HB and three CDPMs), for example. The DC-link voltages have the sorting sequence as $v_{dc1} < v_{dc3} < v_{dc4} < v_{dc2}$. All modules work at the Level 0 states. Fig. 4 illustrates the reconstructed single-phase leg. The fourth DC-link is charging the third one. The third DC-link is discharging the second one. At the same time, the second DC-link is charging the first one while the grid is discharging the fourth one. It is actually a chain "self-balancing" reaction from the perspective of each phase leg.

In the above, the system construction and its equivalent model for self-balancing mechanism are explained. A corresponding modulation would help to settle the best use of such a mechanism. In the following, general voltage levels are first introduced to represent the modules' contributions to the reproducing of total AC terminal voltage. Switching states are then redefined and rearranged,

in order to facilitate the modulation implementation process. During the modulation process, switching patterns are carefully selected in order to guarantee the initial voltage balancing and enlarge the operating range suffering from solar power mismatch. The details are presented in the following.

3. Modulation Strategy

A. Switching States Derivation

Patterns 2–5 can be decomposed into two parts as shown in Fig. 5. The left is about the T-HB, while the right is about the CDPM. Inspired by the voltage-level definition of conventional HB, the contribution levels of T-HB during Pattern 3 (or Pattern 5) and Pattern 4 (or Pattern 2), can be regarded as 0 and +1, respectively.

The normal state, Pattern 2, forms a +2 terminal voltage level. For the self-balancing states, i.e., Pattern 3 (or Pattern 5) and Pattern 4, the total terminal voltage levels are, respectively, 0 and +1. Since the total terminal voltage level is the superposition of both modules' levels, the contribution level of the CDPM during Pattern 2 should be considered as +1. Similarly, the contribution level during Pattern 3 (or Pattern 5) and Pattern 4 should be considered as 0 as well. From the capacitor charging/discharging perspective, during Pattern 2, the grid current discharges both capacitors. During Pattern 3 (or Pattern 5), the grid current charges the lower voltage capacitor and discharges the one with higher voltage value. During Pattern 4, the grid current discharges the capacitor with higher voltage. All the above self-balancing states contribute to capacitor voltage balancing. In conclusion, as long as the bidirectional bridge affects, the capacitor voltages would tend to be balanced.

Next, it is necessary to divide the switching states based on their contribution to establishing the total AC terminal voltage. According to the sign combinations of i_g and v_r, four operating regions (represented by the variable of N_{region}) can be divided as shown in Fig. 6. Inner each operating region, the proposed modulation provides three alternative switching states contributing to the AC voltage superposition for each CDPM/T-HB. Switching states combinations of CDPMs and T-HB are derived as listed in Fig. 6.

Fig. 6(a) shows the states that can directly reveal the ON/OFF switches in the four regions for CDPM, while Fig. 6(b) illustrates the states for T-HB. The capacitors take their parts in the establishing of the total AC terminal voltage. All the states fall into three categories: 1) "Level +1" means that the coupled capacitors contribute a voltage that has the same polarity with v_r; 2) "Level −1" means that the coupled capacitors contribute a voltage that is in opposite direction with v_r; and 3) "Level 0" means a self-balancing path between the coupled capacitors and a near free-wheeling path at the grid side. The values +1, −1, 0 are also known as "contribution levels." All of the

switching states are illustrated in Fig. 7. A_1, B_1, C_1, and D_1 are nonzero states for CDPM, while E_1, F_1, G_1, and H_1 are nonzero states for T-HB. Their contribution levels are varied by regions. For example, during Region I, levels of A_1 and B_1 are, respectively, +1 and −1. Instead, during Region III, they are −1 and +1.

Different from the conventional modulation strategies for CHB [16]–[18], paths of CDPM are alternative during the "Level 0" case. The flowing of grid current is led by the capacitor voltage differences. If the voltage on the right capacitor is larger than the left one, the current will flow through the bidirectional bridge instead of the power line connecting AC terminals. Hence, the "Level 0" states, i.e., AB_0 and CD_0, bypass the DC-links from the grid, but will charge the lower voltage DC-links or discharge the higher voltage DC-links. The resulted self-balancing ability is one remarkable advantage of the CDPM-PV system. Normally, a "Level 0" state and a "Level +1" state are enough to reproduce an expected AC output voltage. As such, the modulation works at a loss-reducing mode. The "Level −1" states serving as extended ones would increase modulation complexity. Nonetheless, it supplies more degrees of freedom, in terms of DC-links charging/discharging possibilities.

Note that more power paths are produced and many switching states are newly defined. Selection of switching patterns is more flexible compared with traditional LS-PWM/PS-PWM. The management of switching patterns will be discussed in Sections III-B–III-E.

B. Initial Switching Pattern Selection

A simplified switching pattern ($i_g > 0$) graph sketching the charging/discharging routings can be deduced as shown in Fig. 8. In Fig. 8, a DC-link node (negative or positive) is represented by a triangle symbol ("▲"). A bottom node has lower potential than its neighbor top node unless they are connected together. Two linked nodes share the same potential level. A capacitor is represented by a circle symbol ("●"). If a capacitor is between two bottom nodes or two top nodes, it will be bypassed. If a capacitor is placed between a left-bottom node and a right-top node, it will be charged. If a capacitor is placed between a right-bottom node and a left-top node, it will be discharged. Two neighbor nodes' potential difference is the voltage of capacitor in-between. To express the low to high orders, the capacitor voltages are remarked with variables of v_{dcl1} , v_{dcl2} , ... , v_{dclN} , where $(l_1, l_2, \dots, l_N) \in (1, 2, \dots, N)$ and $l_1 /= l_2 /= \cdots /= l_N$. Note that, v_{dcl1} , v_{dcl2} , ... , v_{dclN} have been sorted from low to high already. It illustrates a reconstructed single-phase leg of a voltage difference flag array of $l_2 l_1 l_4 l_3$ that means $v_{dc1} = v_{dcl2}$, $v_{dc2} = v_{dcl1}$, $v_{dc3} = v_{dcl4}$, and $v_{dc4} = v_{dcl3}$. The pattern graph can be extended easily and is a straightforward way to make clear the charging/discharging status for a system that has three or more power modules.

By employing self-balancing (Level 0) states, a capacitor can be charged if its voltage is lower than both the neighbor ones, or a capacitor can be discharged if its DC voltage is higher than both

the neighboring ones. Therefore, to make the best use of the self-balancing states, the modules can be first divided into two groups named as "0^{u}" and "0_{d}," referring to the principle: the DC voltages for modules in "0^{u}" are larger than the ones in "0_{d}." An easy way is to put half modules into Group "0^{u}" and another half into "0_{d}." For a four-module system, all the six grouping possibilities according to voltage sorting are listed in Table I. For the #1 and #2 conditions, assigning all the modules with self-balancing states is enough to achieve the expected charging/discharging purposes for all the capacitors. For the rest four conditions, "Level +1" or "Level −1" states are utilized. Since the "Level +1/−1" states can link a bottom node with a top one (see Fig. 8), they change the capacitors' voltage potentials. Taking the #3 condition, for example, the capacitor C_{dc1} is previously bypassed. Once #2 CDPM has a "Level +1" state, the capacitor C_{dc1} turns to be discharged. Similarly, the capacitor C_{dc3} is previously bypassed. Once the state of #4 CDPM is changed to a "Level −1" state, the capacitor C_{dc3} can be charged.

Through the above analysis, it can be concluded that if the left side of a "0^{u}" module (# *j* module) is standing another "0^{u}" module, the # *j* module should be assigned a "Level +1" state. In a similar way, if the right side of a "0_{d}" module is standing another "0_{d}" module, the # *j* module should be assigned a "Level −1" state. Otherwise, the # *j* module should be assigned a self-balancing state (also "Level 0" state). The relationship of the charging/discharging topology with respective to the module grouping is summarized in Table I. Such a relationship also indicates the initial selectable switching patterns (according to a zero AC output voltage level) for different grouping conditions. The above are derived under special conditions, i.e., $i_{g} > 0$, four-module system, half modules in "0^{u}," and half modules in "0_{d}." Nevertheless, it can inspire initial pattern selection for other conditions. The analysis and derivation process is similar and will not be further discussed here. Switching patterns can be previously determined for timely look-up. If initializing the switching states according to the listed states in Table I, it will guarantee the voltage balancing in advance. In the following, switching patterns will be managed in order to reproduce different AC output voltage levels suffering from power-mismatch.

C. Modulation-Coordinated Reconstruction Considering Power Mismatch

A significant advantage of applying self-balancing states and arranging them with an optimal way is that all the DC-link charges can be regulated automatically in a nearly analog way, instead of acting at switching period intervals, which helps to distribute the total charges timely in spite of power mismatch. In a further way, the active power distribution ratios sorted from low to high as r_{Pk1} , r_{Pk2} , ... , r_{PkN} are considered in the implementation process. Note that (k_1, k_2, ..., k_N) ∈ (1, 2, ... , *N)* and $k_1 \neq k_2 \neq \cdots \neq k_N$. In the proposed modulation strategy, logic variables F_{misj} (j = 1, 2, ... , *N)* are used for individual modules to fall into one of the mentioned two groups of "0^{u}" and "0_{d}." In detail, F_{misj} is generated by

$$F_{\mathrm{mis}k_j} = \begin{cases} 0, & r_{Pk_j} \geq 1/N \\ 1, & r_{Pk_j} < 1/N \end{cases} \left(k_j = 1, 2, \ldots, N\right) \tag{1}$$

$F_{\mathrm{mis}kj} = 0$ means #k_j module will enter the group of "0_{d}." Otherwise, #k_j module will enter the group of "0^{u}." In (1), $1/N$ is the average active power ratio of the phase leg. The idea behind (1) is that the low-output modules (which tend to have low DC-link voltages) should be given more chances to be charged by the grid, and the high-output modules (which tend to have high DC-link voltages) should be given more chances to be discharged, which will enhance the system's ability to ride through a higher degree of module mismatches.

Diagram of the overall control system for an individual leg is shown in Fig. 9(a). Note that, three-phase power balance is achieved by using zero-sequence voltage injection. The determination of a proper zero-sequence voltage can refer to [11]. Since control subsystems of the three-phase legs are decoupled through the power-balanced control, only the details of one phase are shown. First, the MPPT is always guaranteed. The perturb and observe (P&O) method is employed due to its simple implementation [32]. The DABs are employed to regulate the PV panel terminal voltages ($v_{\mathrm{pv}\,j}$), in order to track maximum power points. DAB is modulated by the well-known phase-shift modulation (PSM) [33]. To satisfy the DC–DC voltage-boosting requirement and the grid code, the average DC-link voltage is regulated closely by the DC voltage-regulating loop. Then, with decoupled control of the active and reactive currents, the active and reactive components of the expected terminal voltage are generated. Detailed information for voltage/current loops can refer to [18]. The phase leg voltage modulation signal is finally sent to the proposed modulation part.

For the proposed modulation, the calculation of $F_{\mathrm{mis}kj}$ ($j = 1, 2, \ldots, N$) is finished in a digital signal processor s, processes like determination of operating region (N_{region}), calculation of modulation wave duty (d), and overall control are completed in the DSP. Fig. 9(b) illustrates how the modulation is implemented. The main modulation process is completed in a field programmable gate array (FPGA).

Fig. 9(c) is the flowchart. In the initialization stage, modules with label number j ($j = 1, 2, \ldots, N$) smaller than the expected AC voltage for the phase leg are put into "Level +1" states, while those with larger module numbers are put into "Level 0" states. After the initialization, v_{pwm}, N_{region}, $F_{\mathrm{mis}k}$ ($j = 1, 2, \ldots, N$) are sampled. And $v_{\mathrm{dc}\,j}$ ($j = 1, 2, \ldots, N$) are sampled and sorted. The sampled v_{pwm} at the kth step is then compared with the one at previous step to get $\mathrm{pwm}_{\mathrm{diff}}(k)$, which indicates the direction and amount of the level change. The calculation of $\mathrm{pwm}_{\mathrm{diff}}(k)$ can be expressed by

$$\mathrm{pwm}_{\mathrm{diff}}(k) = \begin{cases} |v_{\mathrm{pwm}}(k)| - |v_{\mathrm{pwm}}(k-1)|, & \text{Region I/ II} \\ |v_{\mathrm{pwm}}(k-1)| - |v_{\mathrm{pwm}}(k)|, & \text{Region III/ IV} \end{cases} \tag{2}$$

Afterward, the subloop in Fig. 9(c) will be initiated once a change of $\mathrm{pwm}_{\mathrm{diff}}$ or N_{region} is

encountered. Modules are classified into Group "0^u" and Group "0_d" according to the different values of F_{misj} ($j = 1, 2, \ldots, N$). A subinitialization is necessary to apply self-balancing states with the principle mentioned in the end of Section III-E. $\text{pwm}_{\text{diff}}(k)$ is updated accordingly. A recurring process is then executed to bring $\text{pwm}_{\text{diff}}(k)$ to zero, so that $v_{\text{pwm}}(k)$ is realized.

If $\text{pwm}_{\text{diff}}(k) < 0$, a sequence of switching events is first generated for Group "0_d" modules only, in which some modules will be switched from "Level 0" states to "Level −1" states. If this alone cannot bring $\text{pwm}_{\text{dif}\,f}(k)$ to zero, then some modules in Group "0^u" will be switched from "Level +1" states to "Level 0" states. If this still cannot bring $\text{pwm}_{\text{diff}}(k)$ to zero, then some modules in Group "0^u" that have already been put in "Level 0" states will be switched to "Level −1" states. For Region I/III, modules with lower DC voltages are to be switched first, while for Region II/IV, modules with higher DC voltages are to be switched first.

On the other hand, if $\text{pwm}_{\text{diff}}(k) > 0$, a switching sequence involving modules in both Group "0^u" and Group "0_d" will be generated, in which some modules will be switched from "Level 0" to "Level +1" or from "Level −1" to "Level 0." For Region I/III, modules with higher DC voltages are to be switched first, while for Region II/IV, modules with lower DC voltages are to be switched first. Besides, the "Level 0" modules in Group "0^u" will be switched first (to "Level +1" states). If this cannot bring $\text{pwm}_{\text{diff}}(k)$ to zero, then some modules in Group "0_d" will be switched from "Level −1" states to "Level 0" states. If the above still cannot bring $\text{pwm}_{\text{diff}}(k)$ to zero, then some modules in Group "0_d" that have already been put in "Level 0" states will be switched to "Level +1" states. After a complete execution of the subloop, the gating signals are finally updated.

D. Discussion on the Switching Events and Conduction Loss

In each region, conventional LS-PWM provides two alternative switching states contributing to the superposition of AC voltage for one module. One state provides a path for the grid to charge/discharge the DC link of the module. The other state provides a freewheeling path at the grid side. Similar to conventional LS-PWM, two states in each region are enough for the proposed modulation to reproduce the expected AC voltage of CDPM-PV. Another significant advantage of such state derivation considering the polarity of i_g is that the number of switching events can be minimized by arranging the states aforementioned properly. If A_1 and AB_0 are assigned in Region I [see Fig. 6(a)] for CDPM, a transition two states involves only two switching events (one turning-on and another turning-off). The number is same for other regions if with state assignment listed in Fig. 6(a). The similar conclusion applies to the T-HB [see Fig. 6(b)]. Its transition number between adjacent states is also 2.

Note that, there is a third state ("Level −1") for each region. Such a state is introduced to further increase the module-mismatch riding-through ability. "Level +1" and "Level 0" states are, hence, called basic states, while "Level −1" states are the extended states. Combinations of switching

states have been derived as listed in Fig. 6. A transition between an extended state and its adjacent state also involves only two switching actions. For example, a transition between A_1 and B_1 in Region I involves only two turning-on actions or two turning-off actions. The same number applies to the transition between C_1 and D_1. It demonstrates that the switching event number is not increased although more semiconductors are employed.

On the other hand, the conduction loss lies on operating currents and the amount of switches sustaining. Actually, the amount of acting switches for each CDPM state is same to the one of CHB in terms of the same voltage level. If supposing the same power rating, the conduction loss for our proposed structure would be similar as the conventional ones. Hence, the efficiency for the proposed topology will not be compromised.

E. Discussion on the Module-Mismatch Range

The charges for each capacitor can be estimated by using simulations with the proposed modulation strategy and a fixed capacitor voltage relationship, i.e., $v_{dc1} = v_{dcl1} < v_{dc2} = v_{dcl2} < v_{dc3} = v_{dcl3} < v_{dc4} = v_{dcl4}$. The discharge ratios [per unit, r_{dchlj} *(j = 1, 2, 3, 4)*] by the grid in terms of modulation index are shown in Fig. 10. The operating ranges can be represented by using the ratio difference between the largest and lowest ones, i.e., $\Delta r_{dch} = r_{dchl4} - r_{dchl1}$. Six scenarios are considered, as listed in Table II. Five of them belong to the proposed modulation. They are different in module grouping. The rest one is about CHB-PV using LS-PWM.

As shown in Fig. 10, for all of the six scenarios, lower modulation indexes mean larger operating ranges. This conclusion is consistent with ones in early literatures [19], [22], [28]. For Scenario #1, modules are intently placed into Group "0^u." For Scenario #5, all the modules fall into Group "0^d." It is not hard to find the ranges of these two scenarios are very close. For Scenario #2, the module #l_1 (with the lowest capacitor voltage) gets distinguished and classified into Group "0^d." For Scenario #4, the module #l_4 (with the highest capacitor voltage) is the only one left in Group "0^u." Operating ranges for Scenario #2 and Scenario #4 are almost same. The two modules, #l_1 and #l_4 are, respectively, assigned the highest charging ratio and the highest discharging ratio. For Scenario #3, the modules in the two groups are half and half. Its operating range is middle among all five scenarios from Scenario #1–#5. Lastly, the CHB-PV scenario (Scenario #6) is supplied as a comparison, shown in Fig. 10(f). Obviously, the operating range of this conventional way is the lowest. The operating ranges are directly displayed in Fig. 11.

As shall be seen, the mismatch operating range of the CDPM-PV can be twice the CHB-PV one with LS-PWM. That is to say, CDPM-PV provides higher tolerating degree of module power mismatch compared with conventional CHB-PV with LS-PWM. Considering that LS-PWM bears significant importance for the energy-balancing capacity compared with PS-PWM [34], [35], the

same conclusion can apply to the CHB-PV using PS-PWM.

4. Simulation Verification

To explore the performance of the proposed techniques including the converter topology and its power mismatch-tolerated modulation strategy, a simulation model of a 3-MW/13.8-kV three-phase CDPM-based modular cascaded PV system is set up on a MATLAB/ SIMULINK platform.

In the system, four CDPMs per each leg, including one T-HB and three normal CDPMs, are connected in series to directly interact with a 13.8-kV (line voltage rms vaule) MV AC grid, just making each CDPM's DC-link a 3.0-kV MV DC bus. Each MV DC bus associates with one solar power port. A DAB is located in-between, so as to achieve voltage boosting and HV insulation. PV panels harvest solar radiation in the unity of a string. The string is capable of forming a 0–600-V DC port voltage (the voltage value is varied with different irradiances, temperatures, and even different dust accumulation conditions). MPPT for each PV string is independent with each other and holds for the whole time interval. Parameters of the simulation system are concluded in Table III.

Fig. 12 shows the three-phase simulation results including four scenarios listed in Table IV. The waveforms from top to bottom are, respectively, about grid voltages, grid currents, active power injected to the grid, CDPM DC-link voltages, and zero-sequence voltage. Zoomed-in three-phase waveforms of the steady state are shown at the right side of Fig. 12. During the whole simulation interval, the three-phase balancing control takes effect on the coordination for three-phase legs. To focus analyses on the (inner-phase) module power mismatch, the three legs are supposed to have duplicated module power distribution status. The zero-sequence voltage contains only third harmonics (see v_{zs} in Fig. 12), which is used to enhance the linear modulation range for each individual leg.

The simulation results of phase-a are highlighted in Fig. 13. The zooming waveform for each scenario is shown in Figs. 14(a), 15(a), and 16(a), respectively. Waveforms of the currents flowing through bidirectional bridges are intentionally added in Figs. 14(a), 15(a), and 16(a) to verify the beneficial impact of the reproduced power paths on routing the mismatched solar power. Furthermore, the switching times are counted in real-time, and displayed with other waveforms.

Note that, the simulation results of CHB-PV are also supplied in Figs. 14–16 for comparisons. The two conventional carrier-based modulation methods, i.e., PS-PWM and LS-PWM, are considered. Simulation parameters in CHB-PV are same with CDPM-PV ones listed in Table III.

As shown in Fig. 13, all solar ports are first processing rated power absorption. The MPPT control is enabled and each module harvests maximum power through the segmented PV arrays. The soft-

start process lasts for 0.2 s (from 0 to 0.2 s). At 0.2 s, the active power harvested by the four modules, P_{pv1a}– P_{pv4a}, changes from 0 to 250 kW (1.0 p.u.). Accordingly, the active power to grid, P_{ga}, increases to 1 MW. And the grid current magnitude, I_{ga}, increases to 174 A. Since the symmetrical active power can equalize the output voltage among modules, there is no over-modulation occurring, and grid currents have good qualities, as shown in Fig. 15(a) (before 0.5 s). At 0.5 s, #2, #3, and #4 modules keep 250-kW solar power inputs, but the one of #1 module reduces to a very low value, i.e., 25 kW (0.1 p.u.), due to different irradiation degrees. For CHB-PV using PS-PWM [see Fig. 14(b)], it takes a long transient interval to return to steady operation. The overshoot of DC voltages is very large (about 10%), which is likely to trigger over-voltage protection. Furthermore, the grid current is suffering from severe distortion with total harmonic distortion (THD) of 36.17%. Obviously, it cannot meet the grid code requirements. For CHB-PV using LS-PWM, the current quality is acceptable (the THD is 2.82%). But the DC voltage of #1 module has an opposite variation trend, i.e., it keeps fast decreasing due to solar power shortage, as shown in Fig. 14(c). In contrast, for CDPM-PV [see Fig. 14(a)], power mismatch shows little impact on its steady operation. The current quality is good (THD is 2.78%). The DC voltages are well balanced and regulated at the reference value of 3 kV.

At 0.8 s, the solar power of #1 module recovers to 120 kW (0.48 p.u.). The one of #2 module also changes to 120 kW (0.48 p.u.). As shown in Fig. 15(b), the unsymmetrical active power still degrades the operation performance for the CHB-PV using PS-PWM, i.e., the DC voltage difference is as large as 0.2 kV, THD of the grid current is 33.46%. The condition for the CHB-PV using LS-PWM is better, but still has a large DC voltage difference. And such a difference is likely to get larger as time goes on, as shown in Fig. 15(c). In contrast, the dynamic performance of grid current, point of common coupling (PCC) voltage, and individual DC voltages of CDPM-PV can be seen in Fig. 15(a). It takes about five cycles to bring the system back to be steady operation. As seen from the bottom set of waveforms in Fig. 15(a), active power taken by the bidirectional bridges changes. That is the reason why the system can return to the steady operation although active power distribution among the four modules is still unsymmetrical.

To further verify the proposed topology, Case 3 with solar powers for #1, #2, and #3 modules changing to 165 kW (0.66 p.u.) happens at 1.1 s. As shown in Fig. 16(b), the DC voltage tracking performance is still not satisfied (the peak to difference is as high as 100 V and still has the increasing trend) for the conventional CHB-PV using PS-PWM. While for CHB-PV using LS-PWM, such a module mismatch is well tolerated, which means LS-PWM can allow a considerable degree of power mismatch, as shown in Fig. 16(c). While for the CDPM-PV, the grid current still has good quality and THD is less than 5%. The four DC voltages are always converged, as shown in Fig. 16(a). Validity of the proposed topology and its power mismatch-tolerating modulation is verified in this simulation.

5. Experimental Results

To further verify the effectiveness of proposed techniques, a downscaled CDPM-PV prototype is built up, as shown in Fig. 17. Parameters of the prototype is summarized in Table V. It contains a DSP + FPGA control board, configurable power modules, reactive components, PV emulators (DC–DC converters and programmable DC power supplies) and measuring/recording instruments. On the main control board, a Cyclone IV FPGA (EP4CE40F23C8N) receives the modulating signals from a TI DSP (TMS320F28346) and performs the pulsewidth modulation. Based on modular design, the main circuit of CDPM-PV is constituted by four identical PV power units. The driving pulses of semicondctors are generated by the main control board and transferred to each power unit by optical fibers.

At the PV emulator sides, the capacitor value, the input voltage, and the switching frequency are, respectively, 2200 μF, 80 V, and 15 kHz. Control loops for the CDPMs and DC–DC converters and determination of the reactive power are implemented with the DSP. The DSP also prepares the necessary data for modulation, including region judging, determination of $F_{\mathrm{mis}kj}$ (j = 1, 2, 3, and 4), and generation of v_{pwm}. The main part of the modulation is accomplished in the FPGA.

In the experiments, five mismatch scenarios as listed in Table VI are considered. Case #1 is the balanced condition with each module running at rated power, while other cases are with different degrees of power mismatch. Fig. 18 shows the experimental results from the power balance condition to various power mismatch conditions. Waveforms from top to bottom are, respectively, about the grid voltage, the capacitor voltages, the grid current, and the current on #2 bidirectional bridge (i_{bi}, numbering of bidirectional bridges can refer to Fig. 4). During the module power balance condition, all the modules operate at the rating power point, i.e., the power value is 520 W. Note that the experimental environment is not perfect since the gird is not that strong, i.e., its THD is as high as 2.38%. Nevertheless, the proposed system can work well under such a weak grid. THD of the grid current is 3.56%. Moreover, the four capacitor voltages are balanced with each other. Pulse-shape current flows through the bidirectional bridge. Positive current value means the power is transferring from #3–4 modules to #1–2 modules. Negative current value means the opposite power transfer direction. As seen from Fig. 18(a), the positive current part is nearly symmetrical with the negative one. Such a shape means the active power exchanging between #1–2 modules and #3–4 modules is almost 0.

When the power of #1 module decreases to 0.125 p.u. (65 W), the shape of the bidirectional bridge current changes [see Fig. 18(b)]. Power is transferred from #3–4 modules to #1–2 modules, in order to achieve DC voltage balance. More obviously, after powers of both the #1 and #2 modules decrease to 0.364 p.u. (195 W), negative part of i_{bi} is almost disappeared, as shown in Fig. 18(c). Similar bidirectional bridge current shape applies to case #4 where powers of all the #1–2 and #4 modules decrease to 0.538 p.u. (280 W). The experiment result is shown in Fig. 18(d). Obviously,

the parallel states are employed during these cases. And the bidirectional bridges split solar power into different streams across multiple modules and allow module power mismatch. It demonstrates that the proposed CDPM-PV and its modulation strategy work well for different degrees of module power mismatch.

Fig. 19 further illustrates the experimental results for another module-mismatch case (Case #5). In this case, there are also two low-power modules (the value is 0.364 p.u.) and two high-power modules (the value is 1 p.u.). The different thing is that the total power on #1–2 modules is equal to the one of #3–4 module. At this time, the power transfer through the #2 bidirectional bridge is not necessary. As expected, there is no current flowing through the bidirectional bridge. It demonstrates that the utilization of parallel states is adjustable within different power mismatch situations, in order to avoid unnecessary switching events.

Finally, a special experiment is made with Cases #3 and #4 to highlight the performance of the proposed modulation strategy, i.e., Case #3 with all zero $F_{\text{mis}\,j}$ (j = 1, 2, 3, 4) and Case #4 with all zero $F_{\text{mis}\,j}$ (j = 1, 2, 3, 4) are considered. The results are shown in Fig. 20(a) and (b). Now, the voltage balancing is not fully activated although the bidirectional bridges can transfer some power. Hence, the balancing effect is limited. As shown in the left half of Fig. 20(a), the two DC-link voltages deviate from the reference value. And the difference between maximum and minimum voltages is 6.5 V for case #3 (7% of the reference value). After considering the real-time power mismatch, i.e., calculating $F_{\text{mis}\,j}$ according to (1) and updating switching states with the principle in Section III-C, the DC voltages converge to the reference value as shown in the right half of Fig. 20(a). The similar conclusion applies to Case #4 (the gap increases from 2.5 to 7.3 V). Moreover, the peak DC voltage values with subinitial process are also higher for both cases. It demonstrates that the modulation-coordinated reconstruction considering real-time power mismatch is critical for CDPM-PV to tolerate module power mismatch.

6. Conclusion

Cascaded multilevel converter is a promising candidate for modern utility-scale PV generation accessing MV power system. Concerning the fact that the active power flows are dominated by different operating conditions, PV modules are not likely to be matched. This study proposes a novel CDPM-PV topology based on CDPMs. By choosing the most suitable switching patterns for each CDPM, this topology provides an alternative view in flexible and efficient power routing for cascaded utility-scale PV systems. Compared with conventional CHB-PV with LS-PWM or PS-PWM, this CDPM-PV provides higher tolerating degree of module power mismatch, i.e., the range can be twice the CHB-PV one. The simulation and experiment results demonstrate that by employing the proposed techniques, the tradeoff between operating power range and performance in face of module power mismatch is finally alleviated.

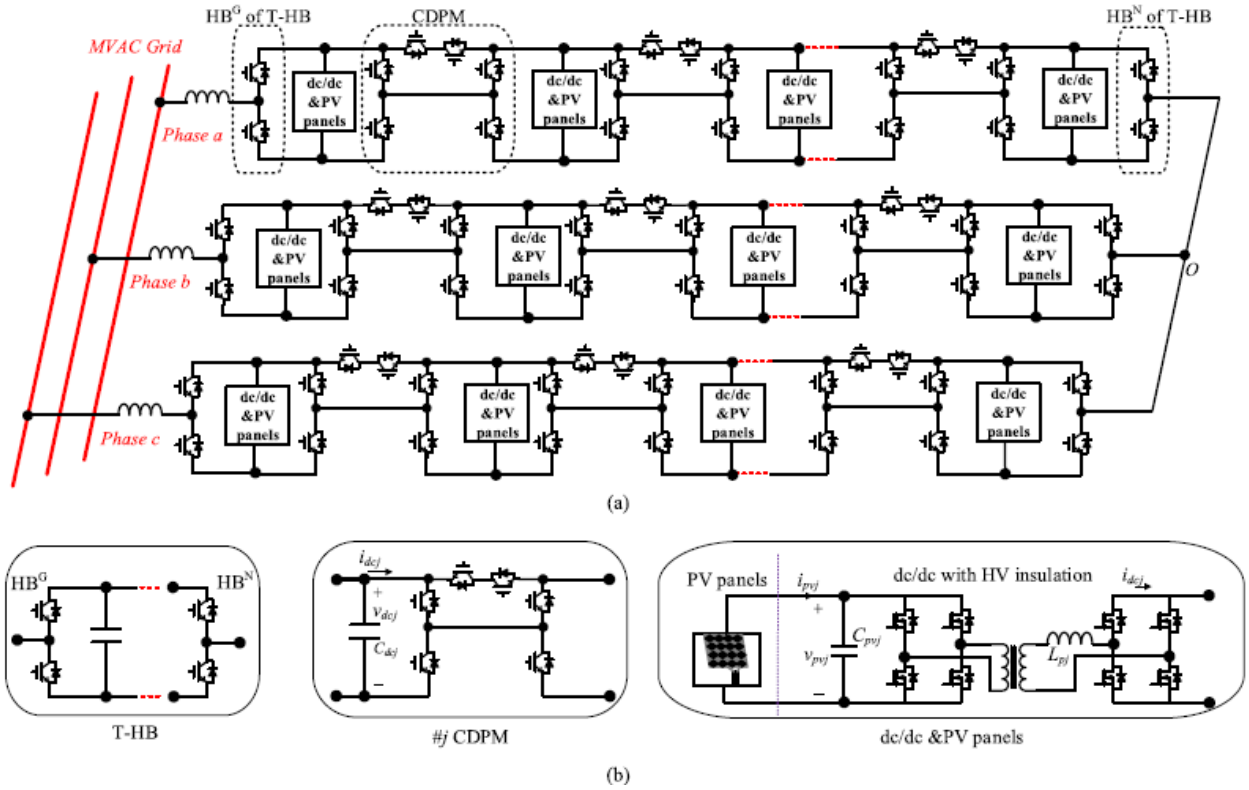


Figure 1. Two-stage, grid-interacted, cascaded coupled-DC-link-module converter-based PV system: (a) three-phase structure and (b) structure of the terminal half-bridges, coupled-DC-link modules, and DC/DC and PV panels for PV applications.

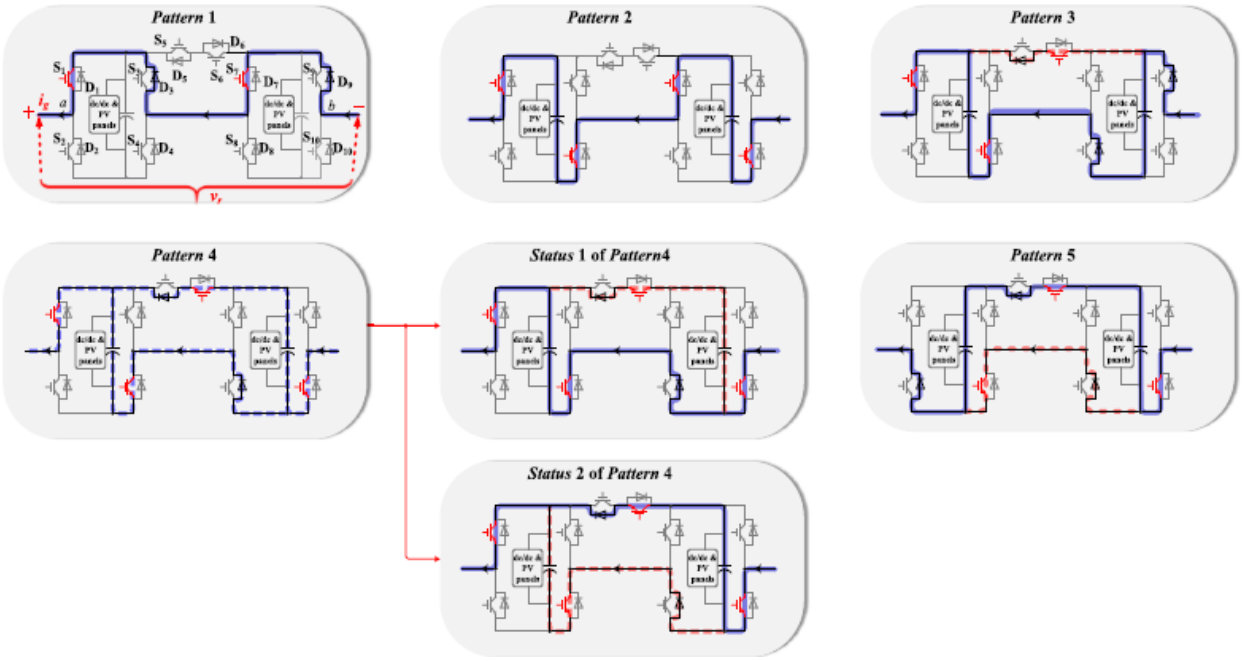


Figure 2. Switching patterns for a two-module CDPM-PV system.

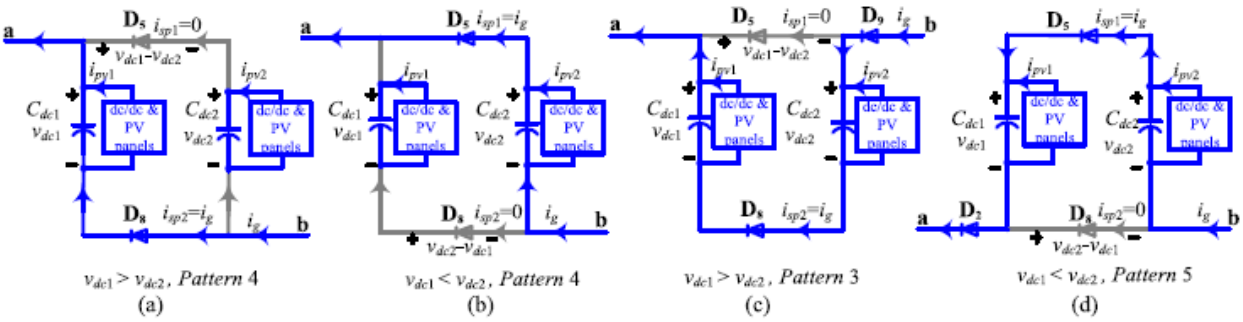


Figure 3. Equivalent circuits illustrating the self-balancing mechanism. (a) Equivalent circuit of Pattern 4 when $v_{dc1} > v_{dc2}$. (b) Equivalent circuit of Pattern 4 when $v_{dc1} < v_{dc2}$. (c) Equivalent circuit of Pattern 3 when $v_{dc1} > v_{dc2}$. (d) Equivalent circuit of Pattern 5 when $v_{dc1} < v_{dc2}$.

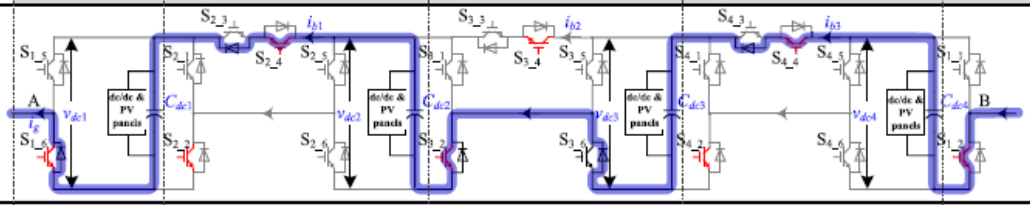
Power module #	Left of #1 module (T-HB)	#2 module (#1 CDPM)	#3 module (#2 CDPM)	#4 module (#3 CDPM)	Right of #1 module (T-HB)
Contribution Level	Level 0	Level 0	Level 0	Level 0	Level 0
Equivalent circuit					
Charging Status	*Charging* C_{dc1}	*Discharging* C_{dc2}	*Charging* C_{dc3}	*Discharging* C_{dc4}	/
Bi-directional bridge #	/	#1 Bi-directional bridge	#2 Bi-directional bridge	#3 Bi-directional bridge	/

Figure 4. Equivalent circuit illustrating the charging/discharging status of a four-module CDPM-PV system.

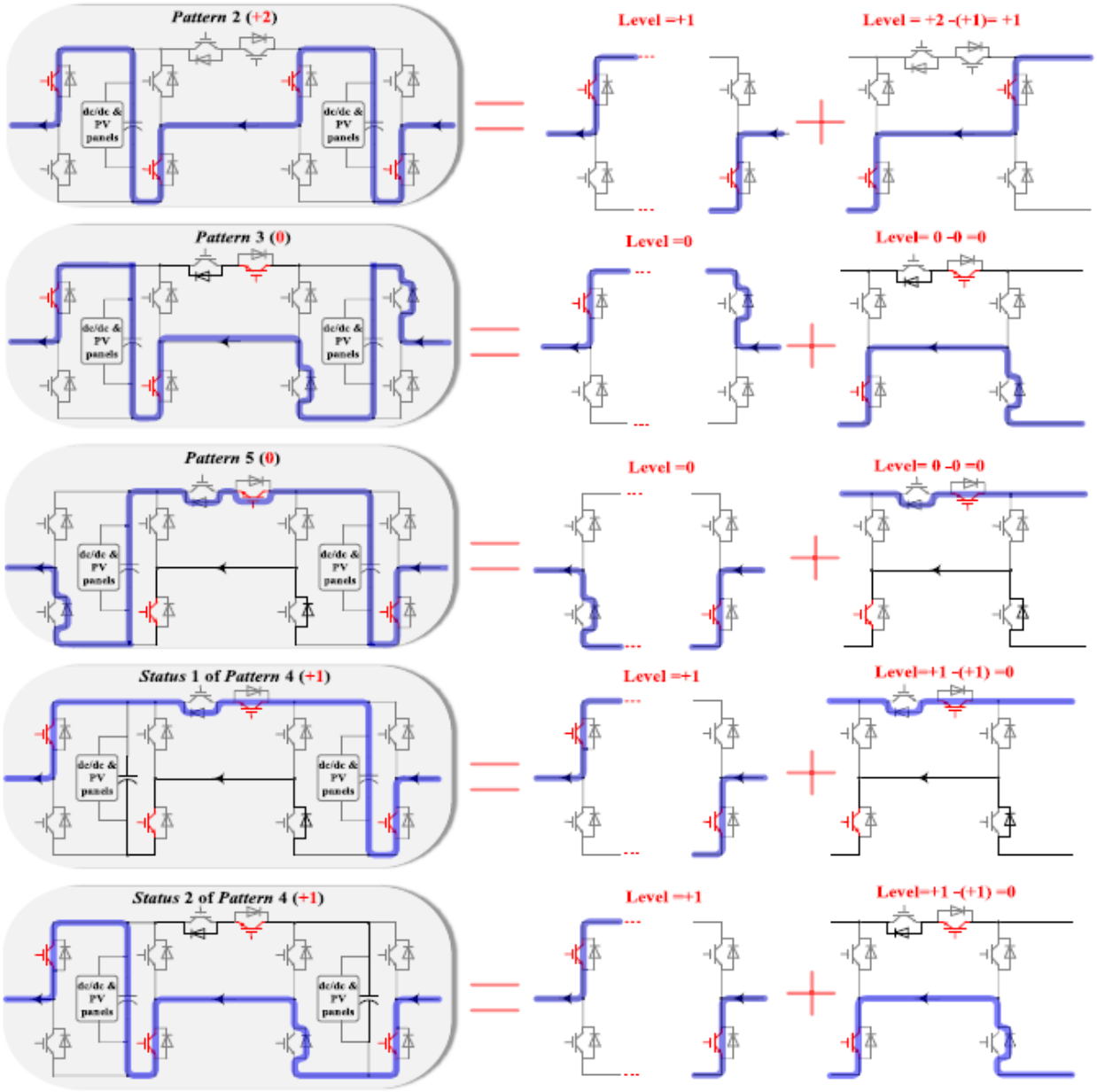


Figure 5. Switching states derivation diagram.

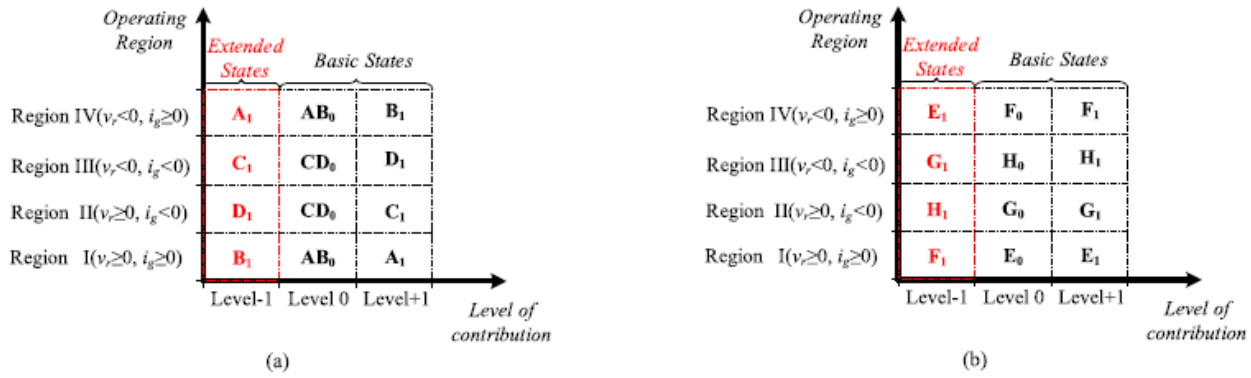


Figure 6. Assignment of switching states for the proposed modulation: (a) states assignment for CDPM and (b) states assignment for T-HB.

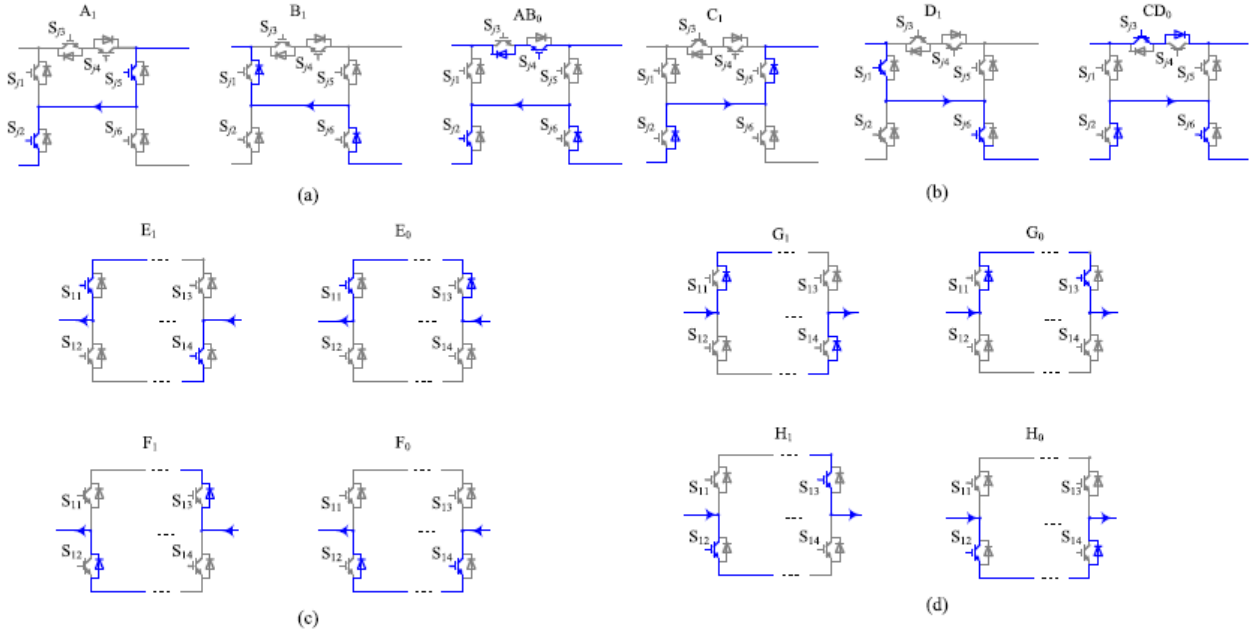


Figure 7. Switching states clarified in different regions: (a) switching states for CDPM (# *j)* during Region I/IV; (b) switching states for CDPM (# *j)* during Region II/III; (c) switching states for T-HB during Region I/IV; and (d) switching states for T-HB during Region II/III.

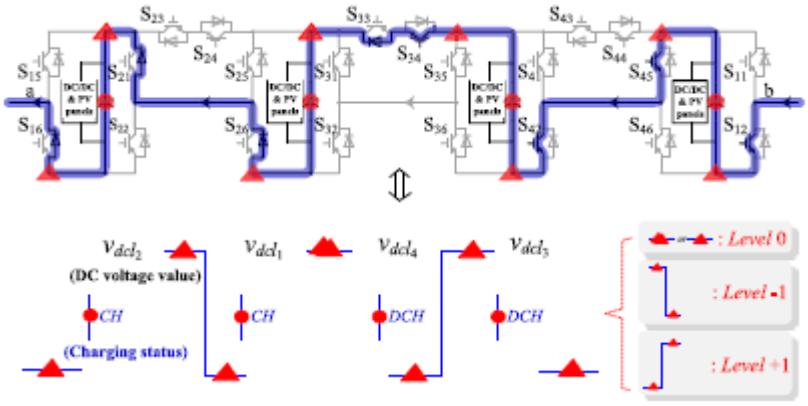


Figure 8. Simplified switching pattern graph sketching the charging/discharging routings.

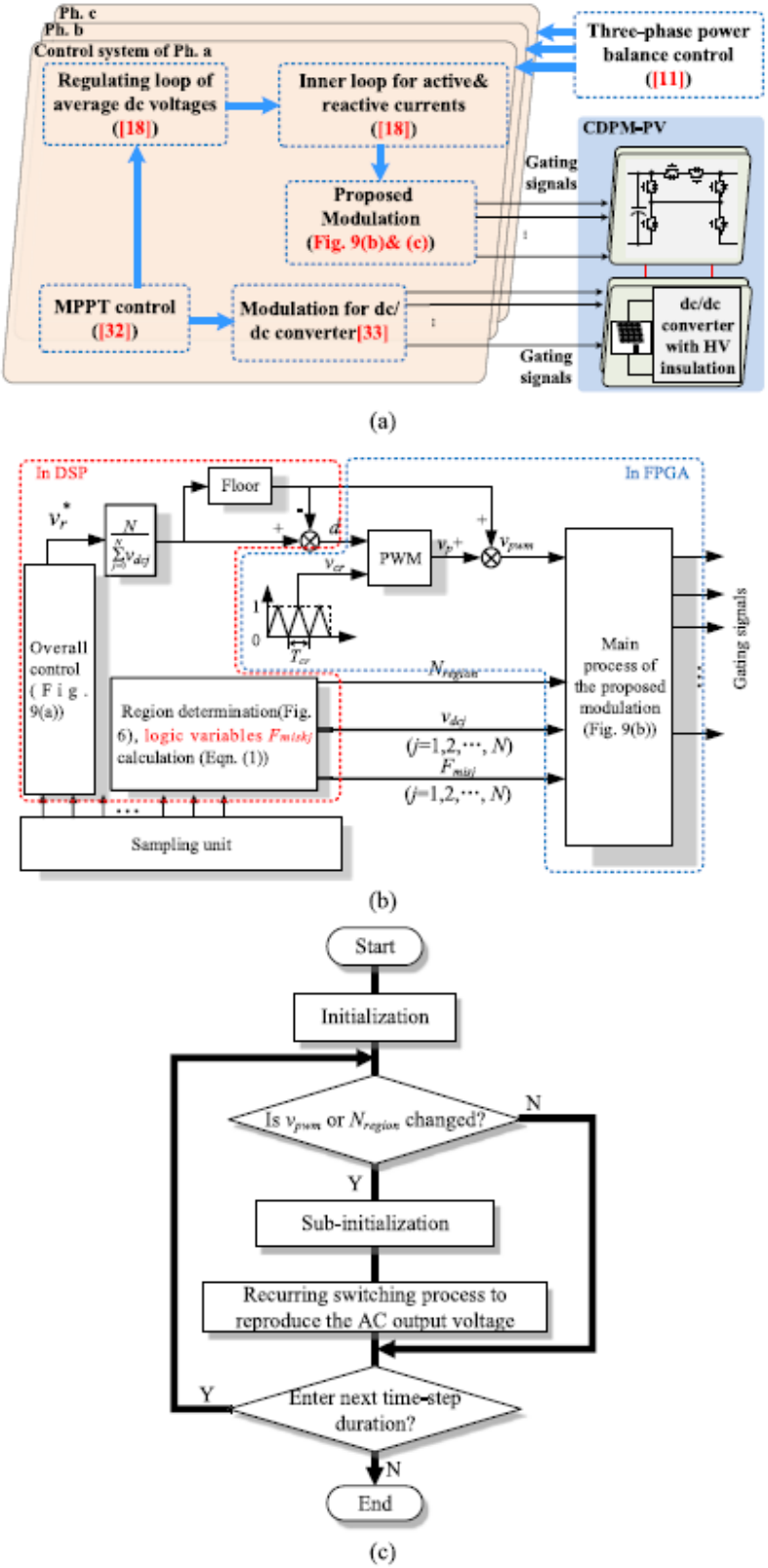


Figure 9. Implementation diagram of the proposed modulation strategy: (a) overall control structure; (b) modulation assignments; and (c) flowchart of the main process.

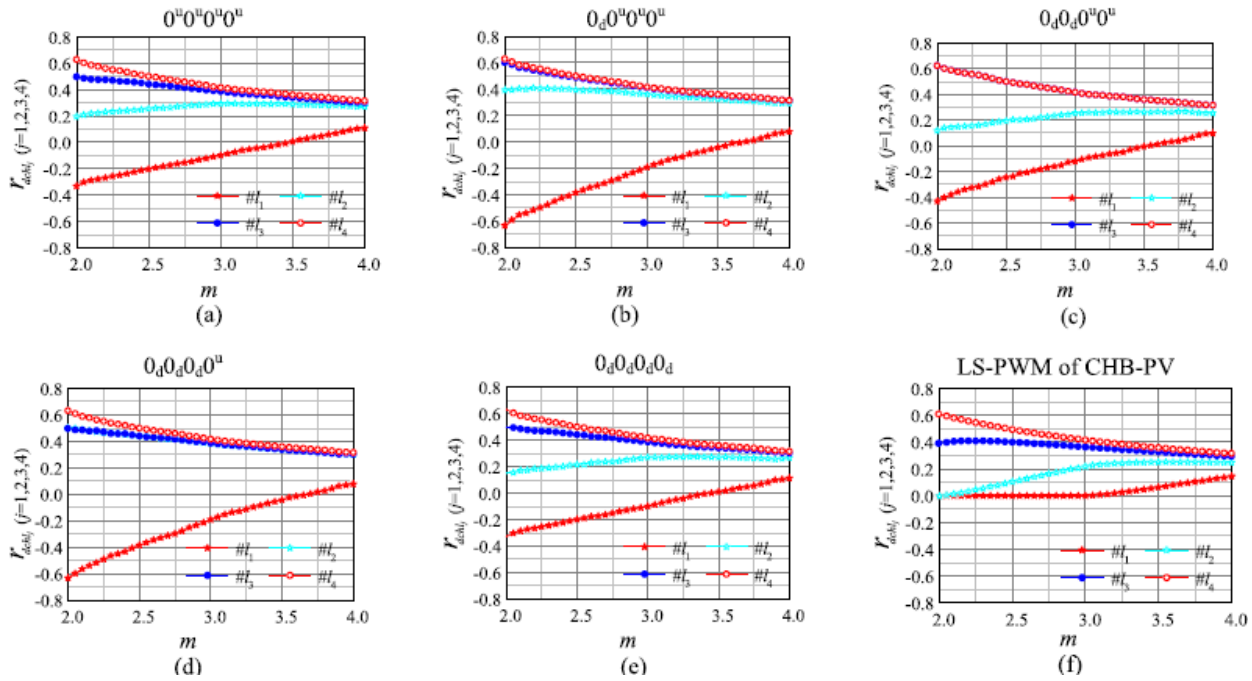


Figure 10. Operating range comparison for different cases: (a) scenario #1; (b) scenario #2; (c) scenario #3; (d) scenario #4; (e) scenario #5; and (f) scenario #6.

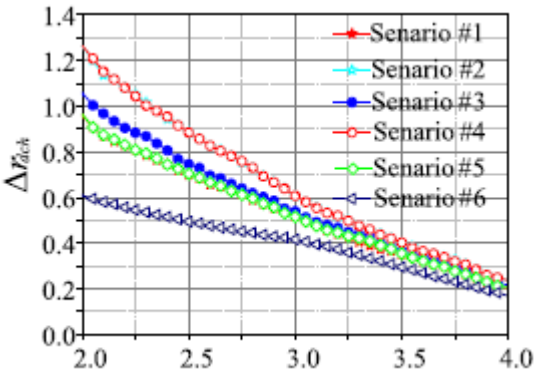


Figure 11. Operating ranges of all the six scenarios.

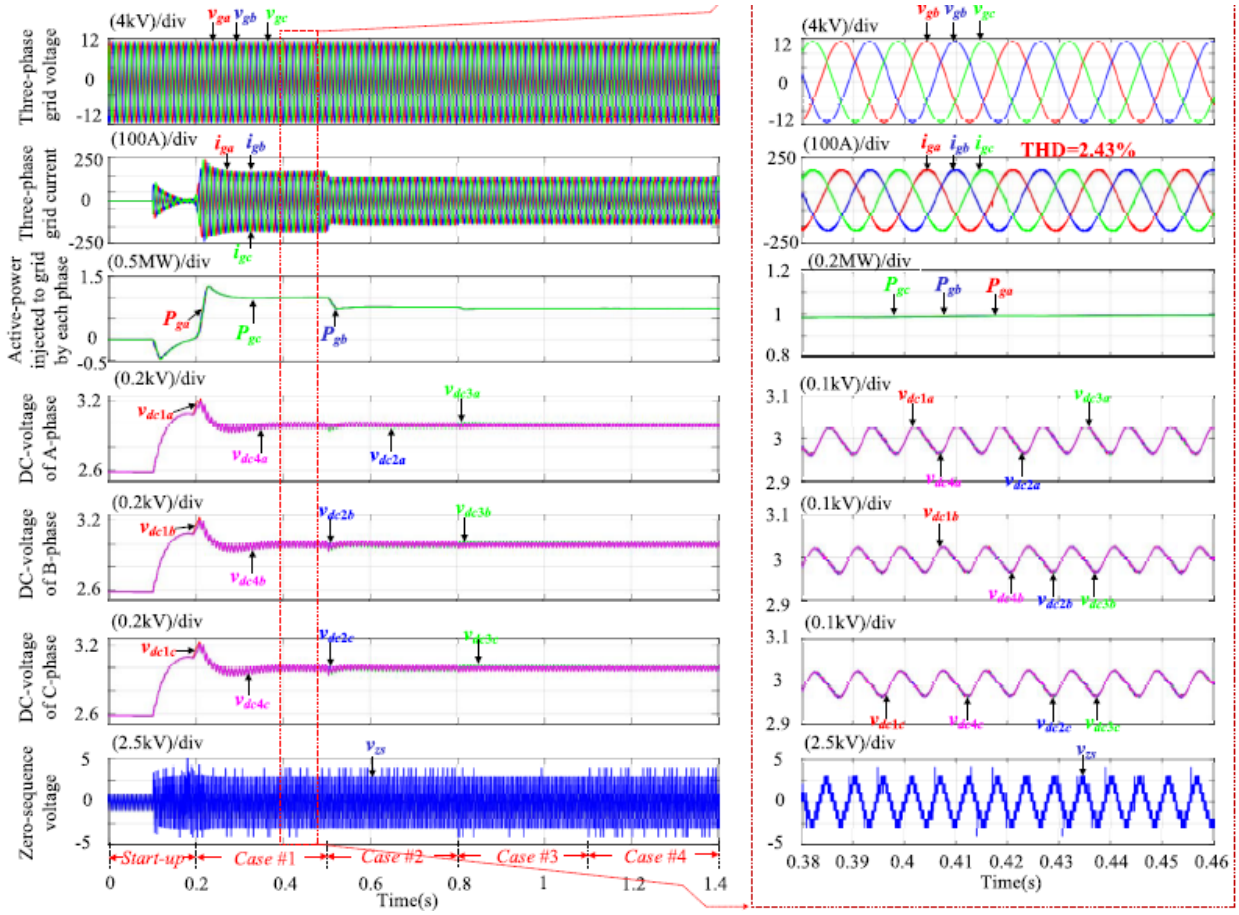


Figure 12. Three-phase simulation results including scenarios of 1) normal modulation (from 0 to 0.5 s); 2) module-mismatch #2 case (from 0.5 to 0.8 s); 3) module-mismatch #3 case (from 0.8 to 1.1 s); and 4) module-mismatch #4 case (from 1.1 to 1.4 s).

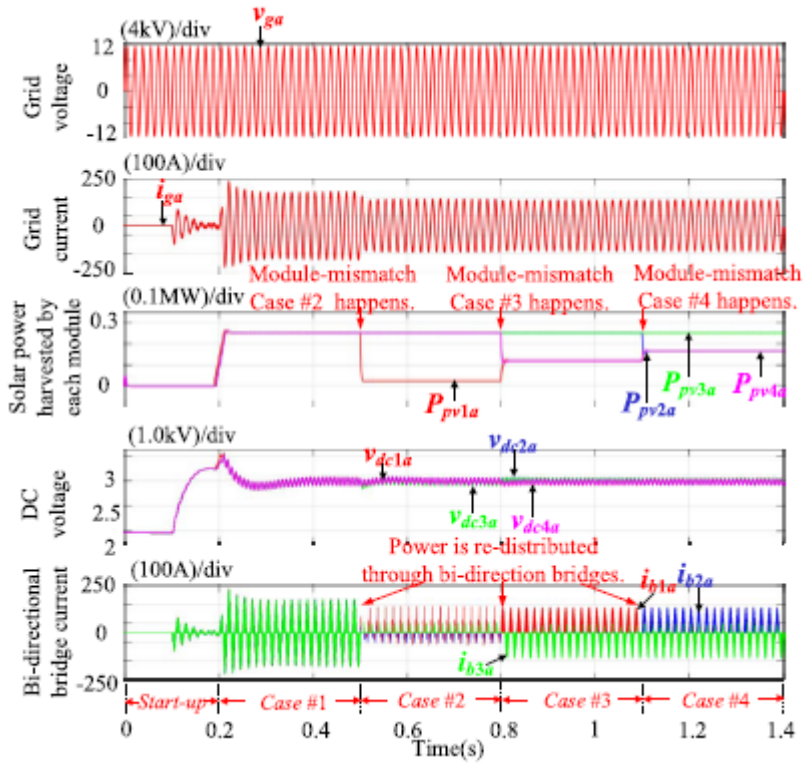


Figure 13. Simulation results of phase leg a during the whole time interval.

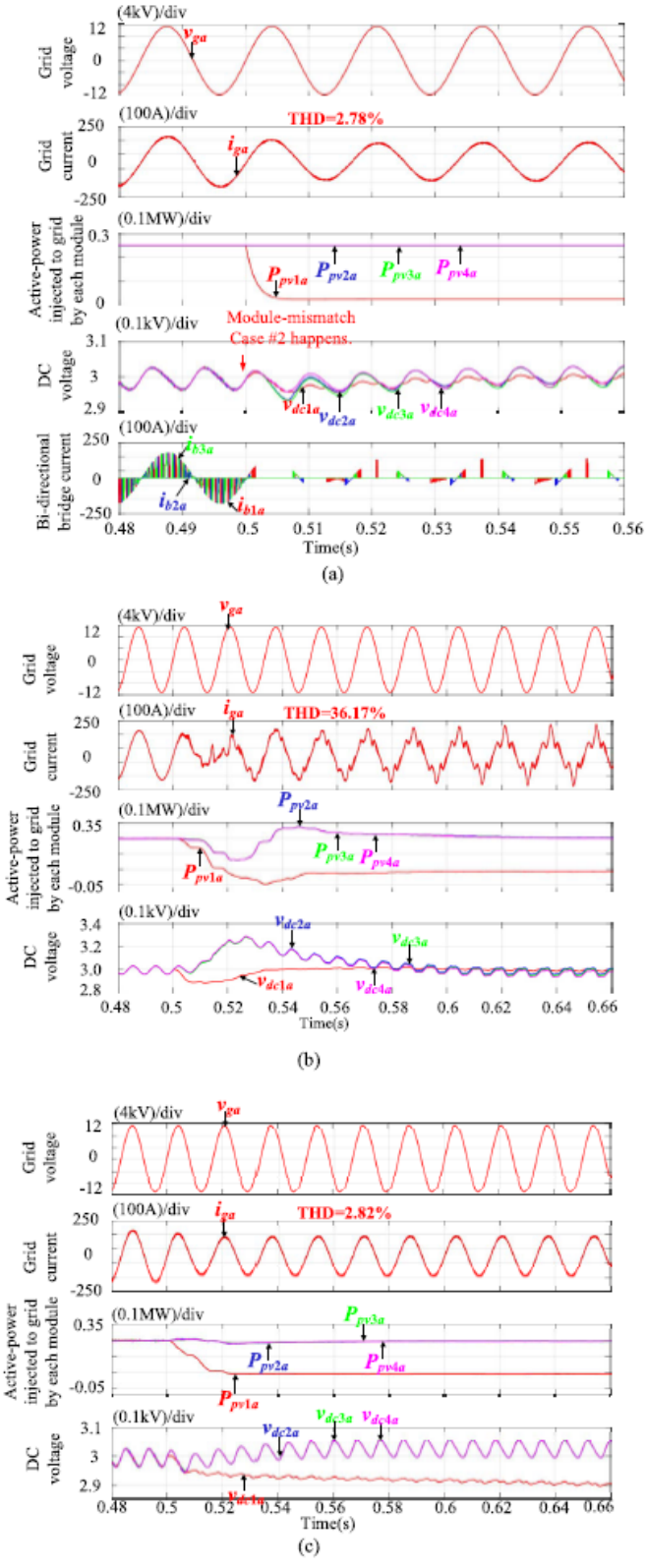


Figure 14. Zooming-in simulation results from Case #1 to Case #2: (a) CDPM-PV; (b) CHB-PV using PS-PWM; and (c) CHB-PV using LS-PWM.

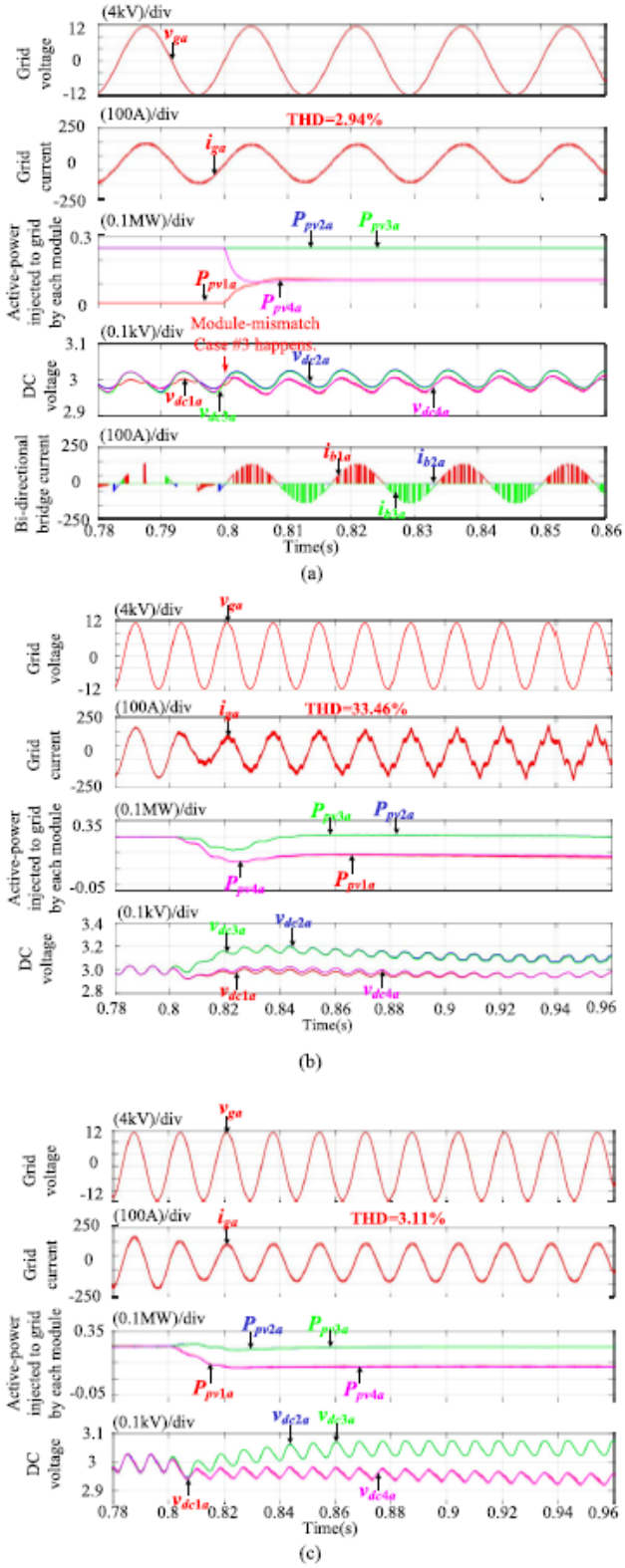


Figure 15. Zooming-in simulation results from Case #2 to Case #3 of CHB-PV using LS-PWM for comparison: (a) CDPM-PV; (b) CHB-PV using PS-PWM; and (c) CHB-PV using LS-PWM.

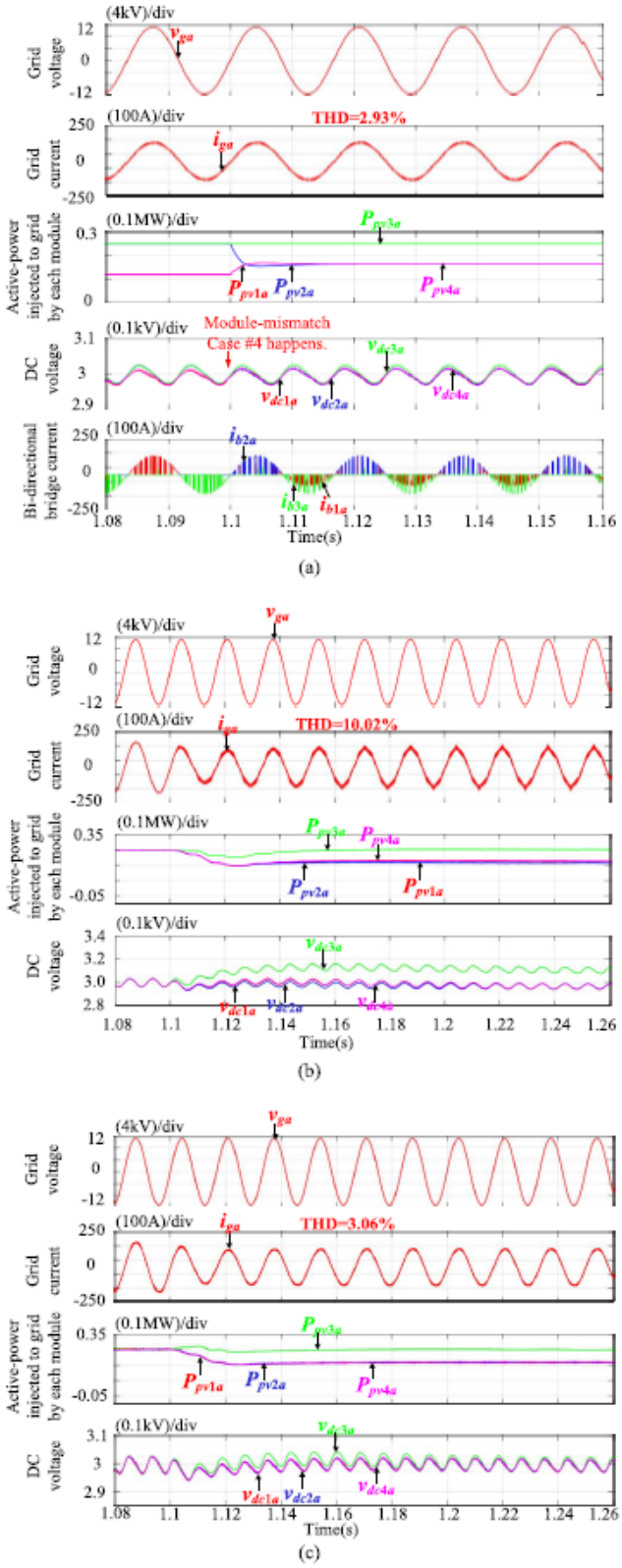


Figure 16. Zooming-in simulation results from Case #3 to Case #4: (a) CDPM-PV; (b) CHB-PV using PS-PWM; and (c) CHB-PV using LS-PWM.

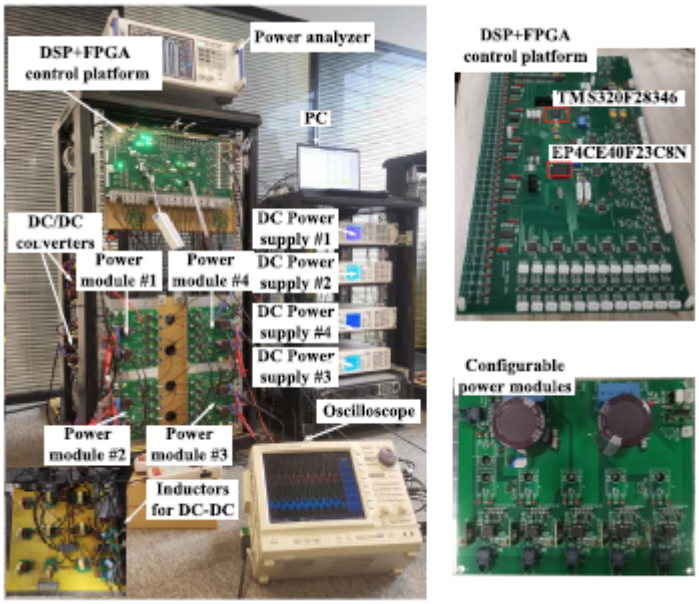


Figure 17. Laboratorial CDPM-PV system hardware prototype including four cascaded 2.4-kW power modules.

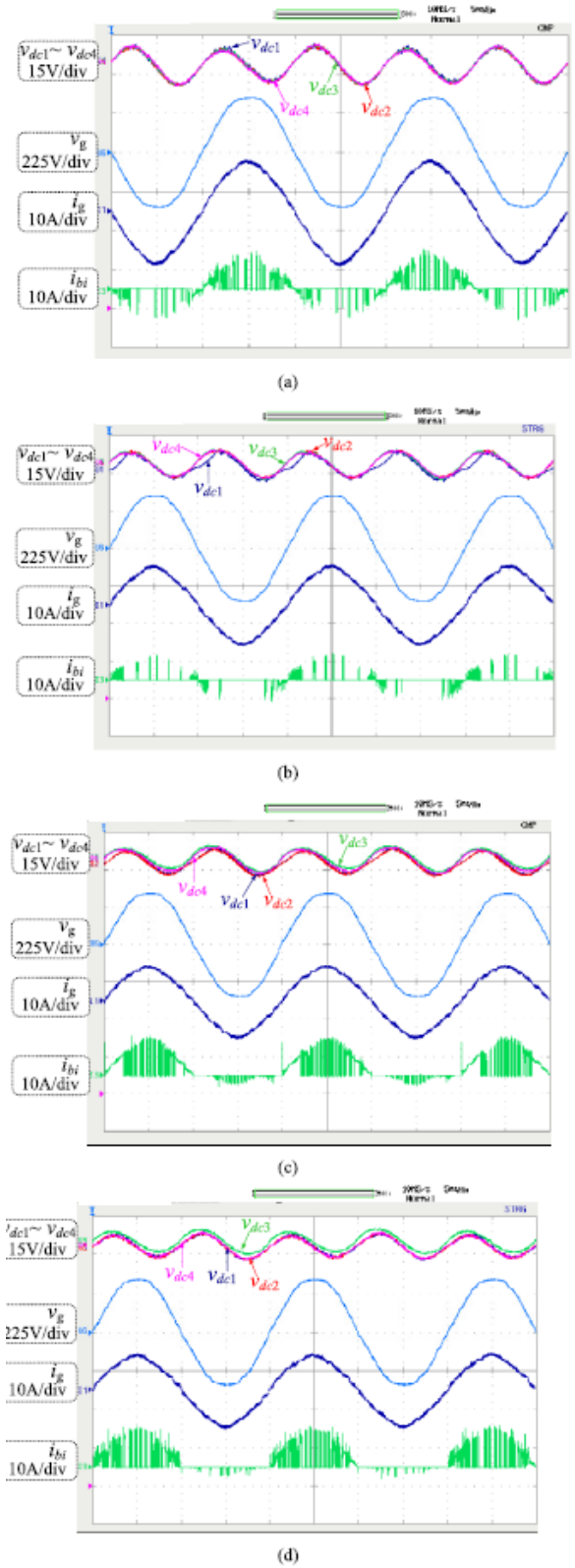


Figure 18. Experimental results for different cases: (a) Case #1; (b) Case #2; (c) Case #3; and (d) Case #4.

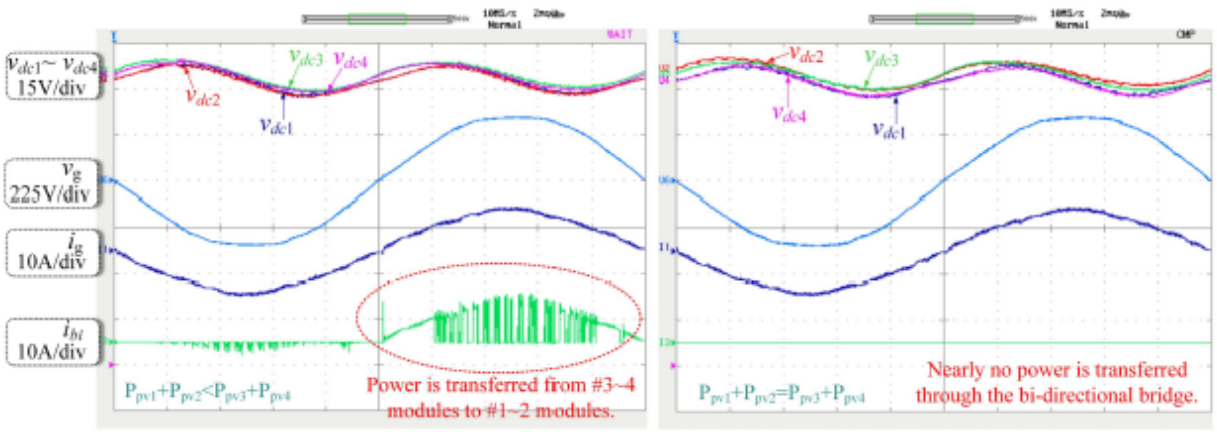


Figure 19. Experimental results comparison between Case #4 and Case #5.

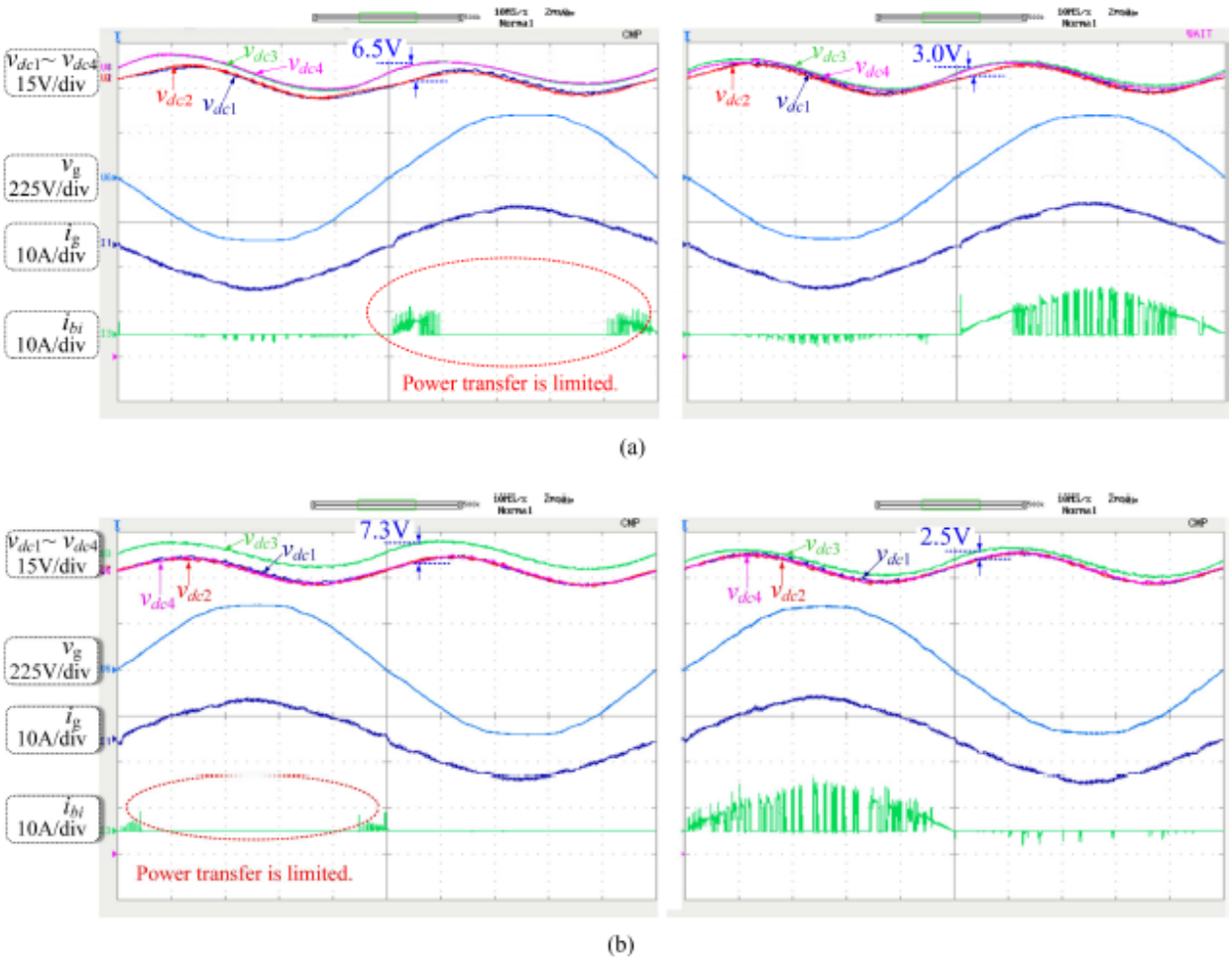


Figure 20. Experimental results to verify the effect of initial switching pattern selection process: (a) Case #3 and (b) Case #4.

Table I. Relationship of the charging/discharging topology with respective to the module grouping.

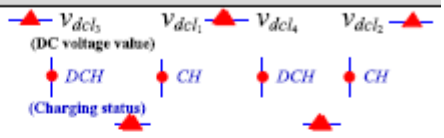
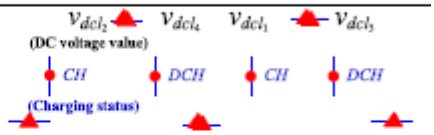
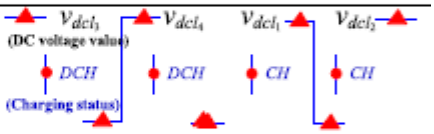
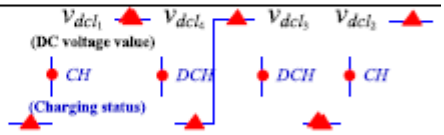
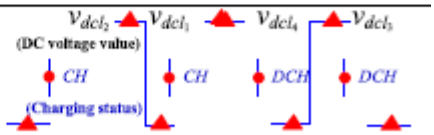
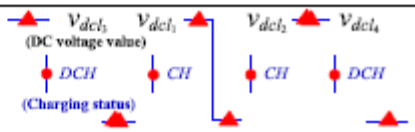
#	Grouping according to the voltage sorting	Grouping after the initializing process	Charging/ discharging Topology
1	$0^{a}\ 0_{d}\ 0^{a}\ 0_{d}$	$0^{a}\ 0_{d}\ 0^{a}\ 0_{d}$	
2	$0_{d}\ 0^{a}\ 0_{d}\ 0^{a}$	$0_{d}\ 0^{a}\ 0_{d}\ 0^{a}$	
3	$0^{a}\ 0^{a}\ 0_{d}\ 0_{d}$	0^{a} +1 0_{d} -1	
4	$0_{d}\ 0^{a}\ 0^{a}\ 0_{d}$	-1 0^{a} +1 0_{d}	
5	$0_{d}\ 0_{d}\ 0^{a}\ 0^{a}$	0_{d} -1 0^{a} +1	
6	$0^{a}\ 0_{d}\ 0_{d}\ 0^{a}$	+1 0_{d} -1 0^{a}	

Table II. Scenarios for operating range comparison.

#1	All the 4 modules in Group "0^{a}"
#2	3 modules in Group "0^{a}", 1 in Group "0_{d}"
#3	2 modules in Group "0^{a}", 2 in Group "0_{d}"
#4	1 module in Group "0^{a}", 3 in Group "0_{d}"
#5	All the 4 modules in Group "0^{d}"
#6	CHB-PV using LS-PWM

Table III. System parameters in the simulation.

Parameters		Symbol	Value
Grid (per phase)	Rated power	P_r	1MW
	Phase voltage (peak value)	v_g	11.27kV
Coupled-dc-link power modules	Rated power per CDPM	P_{rcdpm}	250kW
	Number	N	4
	Capacitor Voltage	v_{dcj}	3kV
	dc-link Capacitor	C_{dcj}	2200μF
	Filter Inductance	L_f	5mH
	Switching Frequency	f_{sw}	2.5kHz
Dual-active-bridges	Rated power per DAB	P_{rdab}	250kW
	Number	N_{dab}	4
	LVdc Capacitor	C_{pvj}	940μF
	LVdc Bus Voltage	v_{pvj}	576V
	Switching Frequency	f_{dab}	30kHz
	HFT Ratio	n_h	6:1
	Leakage Inductance	L_p	100μH

Table IV. Solar power harvested by modules in the simulation.

Case / Module	#1	#2	#3	#4
1	1.00 p.u.	0.10 p.u.	0.48 p.u.	0.66 p.u.
2	1.00 p.u.	1.00 p.u.	1.00 p.u.	0.66 p.u.
3	1.00 p.u.	1.00 p.u.	1.00 p.u.	1.00 p.u.
4	1.00 p.u.	1.00 p.u.	0.48 p.u.	0.66 p.u.
$F_{mpk,a}$ / $F^{2}_{mpk,a}$	0000	0111	0011	0001

Table V. Parameters of the CDPM-PV prototype.

Symbol	Value
P_{rated}	2.4kW
Q_{rated}	2.4kVar
v_g (peak value/ frequency)	311V/ 50Hz
N	4
v_{dcj}	92V
v_{pvj}	80V
C_{dcj}	940μF
C_{pvj}	2200uF
L_f	5mH
f_{sw_cdpm}	2.5kHz
f_{sw_dc}	15 kHz

Table VI. Solar power harvested by modules in the experiment.

Case / Module	#1	#2	#3	#4	#5
1	1.00 p.u.	0.125 p.u.	0.364 p.u.	0.538p.u.	0.364p.u.
2	1.00 p.u.	1.00 p.u.	0.364 p.u.	0.538p.u.	1.00 p.u.
3	1.00 p.u.	1.00 p.u.	1.00 p.u.	1.00 p.u.	1.00 p.u.
4	1.00 p.u.	1.00 p.u.	1.00 p.u.	0.538p.u.	0.364p.u.

References

1. C. Sun, M. Zhu, X. Zhang, J. Huang, and X. Cai, "Output-series modular DC–DC converter with self-voltage balancing for integrating variable energy sources," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11321–11327, Nov. 2020.
2. M. A. Rahman, M. R. Islam, K. M. Muttaqi, and D. Sutanto, "Data-driven coordinated control of converters in a smart solid-state transformer for reliable and automated distribution grids," *IEEE Trans. Ind. Appl.*, vol. 56, no. 4, pp. 4532–4542, Aug. 2020.
3. S. D'Silva, M. Shadmand, S. Bayhan, and H. Abu-Rub, "Towards grid of microgrids: Seamless transition between grid-connected and islanded modes of operation," *IEEE Open J. Ind. Electron. Soc.*, vol. 1, pp. 66–81, 2020.
4. B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1722–1731, Mar. 2015.
5. A. Ghias, P. Jose, and V. G. Agelidis, "A novel control method for transformerless H-bridge cascaded STATCOM with star configuration," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1189–1202, Mar. 2015.
6. L. Wang, D. Zhang, Y. Wang, B. Wu, and H. S. Athab, "Power and voltage balance control of a novel three-phase solid-state transformer using multilevel cascaded H-bridge inverters for microgrid applications," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3289–3301, Apr. 2016.
7. W. Liang, Y. Liu, B. Ge, and X. Wang, "DC-link voltage balance control strategy based on multidimensional modulation technique for quasi-Z-source cascaded multilevel inverter photovoltaic power system," *IEEE Trans. Ind. Informat.*, vol. 14, no. 11, pp. 4905–4915, Nov. 2018.
8. W. Mao *et al.*, "Research on power equalization of three-phase cascaded H-bridge photovoltaic inverter based on the combination of hybrid modulation strategy and zero-sequence injection methods," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9337–9347, Nov. 2020.
9. K. Wang, R. Zhu, C. Wei, F. Liu, X. Wu, and M. Liserre, "Cascaded multilevel converter topology for large-scale photovoltaic system with balanced operation," IEEE Trans. Ind. Electron., vol. 66, no. 10, pp. 7694–7705, Oct. 2019.
10. S. Yang et al., "Quantitative comparison and analysis of different power routing methods for single-phase cascaded H-bridge photovoltaic grid-connected inverter," IEEE Trans. Power Electron., vol. 36, no. 4, pp. 4134–4152, Apr. 2021.
11. Y. Yu, G. Konstantinou, B. Hredzak, and V. G. Agelidis, "Power balance of cascaded H-bridge multilevel converters for large-scale photovoltaic integration," IEEE Trans. Power Electron., vol. 31, no. 1, pp. 292–303, Jan. 2016.
12. Y. Zhang, Y. Yu, F. Meng, and Z. Liu, "Experimental investigation of the shading and mismatch effects on the performance of bifacial photovoltaic modules," IEEE J. Photovolt.,

vol. 10, no. 1, pp. 296–305, Jan. 2020.
13. A. Lashab et al., “Cascaded multilevel PV inverter with improved harmonic performance during power imbalance between power cells,” IEEE Trans. Ind. Appl., vol. 56, no. 3, pp. 2788–2798, May 2020.
14. M. Wang et al., “Harmonic compensation strategy for single-phase cascaded H-bridge PV inverter under unbalanced power conditions,” IEEE Trans. Ind. Electron., vol. 67, no. 12, pp. 10474–10484, Dec. 2020.
15. L. Liu, H. Li, and Y. Xue, “Control strategies for utility-scale cascaded photovoltaic system,” in Proc. IEEE Energy Convers. Congr. Expo., Raleigh, NC, USA, Sep. 2013, pp. 2391–2397.
16. L. Liu, H. Li, Y. Xue, and W. Liu, “Reactive power compensation and optimization strategy for grid-interactive cascaded photovoltaic systems,” IEEE Trans. Power Electron., vol. 30, no. 1, pp. 188–202, Jan. 2015.
17. C. Wang, K. Zhang, J. Xiong, Y. Xue, and W. Liu, “An efficient modulation strategy for cascaded photovoltaic systems suffering from module mismatch,” IEEE J. Emerg. Sel. Topics Power Electron., vol. 6, no. 2, pp. 941–954, Jun. 2018.
18. C. Wang, K. Zhang, J. Xiong, Y. Xue, and W. Liu, “A coordinated compensation strategy for module mismatch of CHB-PV systems based on improved LS-PWM and reactive power injection,” IEEE Trans. Ind. Electron., vol. 66, no. 4, pp. 2825–2836, Apr. 2019.
19. L. A. Tolbert, F. Z. Peng, T. Cunnyngham, and J. N. Chiasson, “Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles,” IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 1058–1064, Oct. 2002.
20. Z. Du, B. Ozpineci, and L. M. Tolbert, “Modulation extension control of hybrid cascaded H-bridge multilevel converters with 7-level fundamental frequency switching scheme,” in Proc. IEEE Power Electron. Spec. Conf., Orlando, FL, USA, Jun. 2007, pp. 2361–2366.
21. Z. Du, L. M. Tolbert, B. Ozpineci, and J. N. Chiasson, “Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter,” IEEE Trans. Power Electron., vol. 24, no. 1, pp. 25–33, Jan. 2009.
22. P. K. Achanta, B. B. Johnson, G.-S. Seo, and D. Maksimovic, “A multilevel DC to three-phase AC architecture for photovoltaic power plants,” IEEE Trans. Energy Convers., vol. 34, no. 1, pp. 181–190, Mar. 2019.
23. S. M. Goetz, A. V. Peterchev, and T. Weyh, “Modular multilevel converter with series and parallel module connectivity: Topology and control,” IEEE Trans. Power Electron., vol. 30, no. 1, pp. 203–215, Jan. 2015.
24. K. Ilves, F. Taffner, S. Norrga, A. Antonopoulos, L. Harnefors, and H.-P. Nee, “A submodule implementation for parallel connection of capacitors in modular multilevel converters,” IEEE Trans. Power Electron., vol. 30, no. 7, pp. 3518–3527, Jul. 2015.
25. S. Heinig et al., “Implications of capacitor voltage imbalance on the operation of the semi-full-bridge submodule,” IEEE Trans. Power Electron., vol. 34, no. 10, pp. 9520–9535, Oct. 2019.

26. Z. Li, R. Lizana F., S. Sha, Z. Yu, A. V. Peterchev, and S. M. Goetz, “Module implementation and modulation strategy for sensorless balancing in modular multilevel converters,” IEEE Trans. Power Electron., vol. 34, no. 9, pp. 8405–8416, Sep. 2019.
27. R. Lizana F. et al., “Modular multilevel series/parallel converter for bipolar DC distribution and transmission,” IEEE J. Emerg. Sel. Topics Power Electron., vol. 9, no. 2, pp. 1765–1779, Apr. 2021.
28. A. Tani, M. B. Camara, and B. Dakyo, “Energy management in the decentralized generation systems based on renewable energy— Ultracapacitors and battery to compensate the wind/load power fluctuations,” IEEE Trans. Ind. Appl., vol. 51, no. 2, pp. 1817–1827, Mar. 2015.
29. M. Coppola, F. Di Napoli, P. Guerriero, D. Iannuzzi, S. Daliento, and A. Del Pizzo, “An FPGA-based advanced control strategy of a grid-tied PV CHB inverter,” *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 806–816, Jan. 2016.
30. H. Iman-Eini, J.-L. Schanen, S. Farhangi, and J. Roudet, “A modular strategy for control and voltage balancing of cascaded H-bridge rectifiers,” *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2428–2442, Sep. 2008.
31. F.-S. Kang, S.-J. Park, S. E. Cho, C.-U. Kim, and T. Ise, “Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power systems,” *IEEE Trans. Energy Convers.*, vol. 20, no. 4, pp. 906–915, Dec. 2005.
32. N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, “Optimization of perturb and observe maximum power point tracking method,” *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 963–973, Jul. 2005.
33. F. An, W. Song, B. Yu, and K. Yang, “Model predictive control with power self-balancing of the output parallel DAB DC–DC converters in power electronic traction transformer,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 1806–1818, Dec. 2018.
34. J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, “Energy-balance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 98–111, Jan. 2013.
35. P. Sochor and H. Akagi, “Which is more suitable to a modular multilevel SDBC inverter for utility-scale PV applications, phase-shifted PWM or level-shifted PWM?” in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Milwaukee, WI, USA, Sep. 2016, pp. 1–7.