Economic and Embodied Energy Analysis of Integrated Circuit Manufacturing Processes

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Abstract

Integrated circuits (ICs) are the fundamental microelectronic building blocks of typical information and communication technology (ICT) devices such as laptops and smartphone. With the emergence of faster and cheaper low-power ICs for the growing ICT market, there is a limited information on their manufacturing energy and economic impacts owing to the lack of recurrent upgradation of proprietary IC manufacturing process data. Economic and life cycle energy assessments (LCAs) of IC manufacturing and assembly processes were conducted using the latest bill of materials (BOM) manufacturing data in a state-of-the-art IC manufacturing cost software tool developed by IC Knowledge, LLC. IC manufacturing cost was estimated to be \$1.00-\$59.00/cm^2;

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the high-end cost represents the most advanced 3D NAND IC technology with the Wafer Level Chip Scale Package cost of \$4/cm^2. Total cumulative energy demand (CED) estimates of IC manufacturing using the OpenLCA software ranged from 9 to 38 MJ/cm^2 or 56 to 235 BJ/month with the largest share (~ 75%) from on-site energy. The IC manufacturing CED is projected to increase with the progress in IC technology node, which has increased by more than two times for technology node evolution from 110 to 14 nm. Furthermore, the representative detailed BOM data were considered to reduce the CED uncertainties of the estimated standard deviation of 35%-42%.

Keywords: Economic assessment; life cycle assessment; information and communication technology electronics; integrated circuits

Glossary

Acronym	Full form	Acronym	Full form
AI	artificial intelligence	LCA	life cycle assessment
ArF	argon fluoride lithography	LCI	life cycle impact
ArFi	argon fluoride Immersion lithography	MPU	microprocessor unit
BOM	bill of materials	MSDS	material safety declaration sheet
CO2	carbon dioxide	MAE	mean average error

CED	cumulative energy demand	NAND	Not AND – a Boolean operator and logic gate used in non-volatile storage technology
CMP	chemical mechanical polishing	nm	nanometer
CMOS	Complementary metal oxide semiconductor	PC	personal computer
COO	cost-of-ownership	PET	polyethylene terephthalate
DRAM	dynamic random-access memory	QFP	quad flat package
EIO	economic input-output	RMSE	root mean square error
FCBGA	flip chip ball grid array	SI	supplemental information
GHG	greenhouse gases	TSSOP	thin shrink small outline package
GDP	gross domestic product	WLCSP	wafer level chip scale package
GPU	graphics processing unit		

GSD	geometric standard deviation		
ICK	IC Knowledge, LLC		
IC	integrated circuit		
ICT	information and communication technology		

1. Introduction

The global demand and use of information and communication technology (ICT) devices are gradually increasing especially with the recent advances in smart and sustainable manufacturing (Terry, Nagapurkar and Das 2020). The ICT sector includes the manufacturing and service industries that capture, transmit and display data electronically; it comprises devices such as smartphones, television, personal computers (PCs), radios, servers, monitors, and printers. The annual global expenditure on these devices by the end of 2023 is forecasted to be $5.8 trillion, exhibiting an annual increase of 6.5% since 2020 (IDC 2020). The ICT sector significantly affects the global economy and environment with carbon dioxide (CO_2) emissions that were projected to reach 1.43 Gigatonnes (CO_2 eq.) in 2020 (The Climate Group 2008).

Life cycle assessments (LCAs) have been used to assess ICT environmental effects by computing the embodied energy performance of electronic devices over their entire life cycle, beginning from raw material acquisition, and extending to manufacture and use phases, including their end of life. Malmodin et al. conducted a comprehensive macro-LCA analysis of global ICT devices to estimate the carbon footprint, assuming that all the products in a single product group were identical and possessed equal carbon emissions (Malmodin and Moberg 2010). For instance, all devices in the PC category were assumed to possess an average carbon footprint of 360 kg CO_2-eq for the manufacturing phase. In reality, similar PCs may have different environmental footprints as revealed by device manufacturers, depending on the assumed manufacturing process technology and its production year. For example, the carbon footprint of a Lenovo PC (Lenovo 2019) was twice that of a Dell PC (Dell 2010).

Several single product-based life cycle studies, such as by Maga et al. revealed that using a server-based computer instead of a desktop PC would reduce greenhouse gas (GHG) emissions by nearly 65% during the entire life cycle of the PC, with the

largest contribution originating from the material and extraction life phases (Maga, Hiebel and Knermann 2013). Babbit et al. developed a bill of materials (BOM) for each device from a similar product-based teardown study of electronic products such as PCs, Blu-ray players, and drones (Babbitt, et al. 2019).

Recently published LCAs of ICT products on CO_2 emissions and embodied energy effects have been limited and therefore do not reflect recent technology advancements in the semiconductor industry. A relatively recent and widely referenced integrated circuit (IC)-level analysis (Boyd 2009) estimated the GHG emissions, primary energy use, acidification potential, and other impact factors of various ICs, such as dynamic random-access memory (DRAM), Not And (NAND) memory, and microprocessor units (MPUs). DRAM ICs are typically used for data storage, like 2D NAND and 3D NAND ICs, whereas MPU ICs are used for performing data calculations and processing. A drawback of Boyd's analysis is that the BOM refers to the IC manufacturing processes pertaining to 57 and 130 nm technology nodes, which are now obsolete (since 2010) and are no longer used to manufacture ICs. Typically, the IC technology node (denoted by nanometers) indicates its circuit generation and manufacturing process. The smaller the technology node (nm), the more recent the manufacturing process. In 2017, Kline et al. reported that the IC manufacturing energy has gradually increased over time, with a rise of nearly 60% from technology nodes of 130 to 32 nm owing to effects on life cycle by the doubling of the IC transistor count every 2 years (i.e., Moore's law) (Kline, Parshook and Johnson, et al. 2017). This work was subsequently expanded by Kline et al. in 2018 to incorporate a newer technology node of 7 nm. The authors concluded that the manufacturing energy nearly doubled for a 7 nm technology node with respect to 130 nm complementary metal-oxide-semiconductor (CMOS) logic IC (Brunvand, Kline and Jones 2018). These energy

99 estimations were performed by Kline et al. through their self-developed predictive tool,
100 'GreenChip', that considered various IC parameters such as architecture, core count,
101 cache size, main memory, and solid-state storage capacities for different technology
102 nodes (Kline, Parshook and Ge, et al. 2019). Despite estimating the energy consumption
103 during each step of CMOS IC manufacturing process, the GreenChip did not consider
104 the detailed BOM used in IC manufacturing process, so it excluded the materials'
105 embodied energy. Furthermore, GreenChip also excluded the energy and materials
106 consumption of packaging IC products.
107 The drawbacks of the previously described product-based teardown approach
108 can be overcome by using an IC semiconductor-level approach. ICs such as logic,
109 DRAM, microprocessors, and microcontrollers are common semiconductor building
110 blocks of all ICT devices whose increasing progress has revolutionized the performance
111 of final ICT products. Another reason to emphasize the significance of an IC/chip-level
112 LCA is that the remaining discrete electronic components within an ICT product such as
113 resistors, capacitors, diodes, switches, and coils, have considerably smaller carbon
114 footprints than the ICs (Okrasinski and Chalkley 2020).
115 This work focuses on Logic, Memory, and MPU ICs because of their major
116 share (63%) in the total global semiconductor market of $414 billion in 2019
117 (Semiconductor industry association (SIA) 2020). The combined share of discrete,
118 analog, optoelectronics, sensors, and other semiconductor devices was small at 37%;
119 therefore, these semiconductors were not considered in the presented work.
120 A few studies have also focused on economic analysis of ICs. An analytical
121 economic analysis approach, "cost-of-ownership" (COO), was developed by Sematech
122 based on detailed mathematical equations (SEMI 1996). The COO-based model
123 considered the direct (e.g., material, equipment, labor) and indirect costs (e.g., utility,

insurance, contingency) associated with a semiconductor facility. Currently, detailed economic analysis methodologies do not focus on material costs incurred in IC manufacturing and assembly. Although such an analysis can be complex because a lack of industry's proprietary information, it could be conducted using IC cost estimation tools developed by IC Knowledge, LLC (ICK), which estimate a wide range of IC costs with consideration of a detailed BOM in IC manufacturing (IC Knowledge 2020).

The current research focus is on the economic and life cycle cumulative energy demand (CED) estimation of a wide range of the latest IC types at the level of wafer and packaging. In this study, a detailed IC ICK cost estimation tool provided the necessary detailed BOM life cycle impact (LCI) data for the IC life cycle energy analysis. LCI data harmonization for current IC manufacturing and assembly processes was conducted using the ICK tool and published data. A CED Monte Carlo uncertainty analysis of IC manufacturing and assembly was considered to quantify the uncertainty impacts.

2. Materials and Methods

In this section, the methodologies for an IC economic analysis and energy LCA approach are described. As depicted in Figure 1, the economic and energy analyses focused on materials and energy used at the IC manufacturing and assembly life cycle stages, whereas the life cycle use phase energy was considered only to a limited extent for a representative IC device to demonstrate its importance to the overall IC life cycle energy use. The detailed information regarding the cost simulation models is given in the supplemental information (SI) document.

The step-by-step economic and energy methodology used in the analysis is illustrated in Figure 2. In the first two steps, costs and BOM were generated using the ICK tool followed by literature harmonization of the proprietary and missing materials

used. In the third step, an LCA was conducted to compute the embodied energy using the OpenLCA software, and results were compared with those available in literature.

2.1 IC Wafer and Packaging Manufacturing—Generic Process Overview

Depending on the IC types, the manufacturing process can be incredibly complex, with more than 400 process steps at the initial wafer and final IC packaging (Plummer, Michael and Peter 2000). A brief overview of these steps is provided in the SI document (see S1 Figure, SI). At the final IC assembly manufacturing stage, an initial wafer is encapsulated inside a semiconductor material to prevent mechanical damage and corrosion. The generic IC assembly process can be broadly classified into the following three stages: wafer sorting, package assembly, and product testing (see Figure S2, SI). The exact process varies with the packaging type such as plastic–lead frame, plastic–ball grid array (BGA), hermetic (ceramic), and others.

2.2 Economic Analysis of IC Manufacturing and Assembly

ICs can be broadly classified as data storage or data processing depending on the end-use function. ICs such as NAND and DRAM are used for data storage and memory applications whereas logic and MPU ICs are used for data processing and calculations. Logic and MPU ICs are the “brains” in any electronic device and comprise multiple processors within them. They can perform a variety of operations in applications such as mathematical calculations, gaming, photo editing, and media streaming. The data storage operation is performed by ICs such as NAND and DRAM. DRAM is a type of volatile memory IC and stores short term or temporary data that is being processed. As soon as the external power is disconnected from the circuit, the memory stored in DRAM is lost. This type of memory loss does not occur in NAND ICs, which are non-volatile ICs. Unlike DRAM ICs, NAND ICs are used for long term memory storage

typically used for various applications, such as storage of photos, videos, and files. DRAM and 2D NAND ICs are planar in structure or possess horizontal density scaling, whereas 3D NAND ICs possess horizontal and vertical density scaling. The addition of memory cells in a vertical direction in 3D NAND ICs increases the storage capacity and density of the IC.

In this work, analyses focused on five IC types: 2D NAND, 3D NAND, DRAM, logic-foundry, and logic-MPU, with each IC possessing a similar technology node of ~20 nm. Table 1 provides the technical inputs and process assumptions for each IC types. The technical inputs for each IC type differed in the number of photomasks, manufacturing steps, and equipment.

Using cost models developed by the ICK software tool, LCI data including the BOM and energy, were generated for the manufacturing of different IC types. The BOM for IC manufacturing comprised of approximately 235 distinct materials, but in the subsequent energy LCA, only the top 25 materials ranked in order of decreasing costs (US dollar per wafer) were included. Together, these 25 materials represented nearly 80% of the total materials costs of the entire BOM. In addition to power consumption of process equipment (15 kWh/photomask), the electricity consumption for non-process tools was assumed be 12.27 kWh/photomask (Wang, et al. 2016) (Applied Materials 2015).

2.3 IC assembly—Cost modeling methodology and input assumptions

Tremendous growth has occurred in the development of a wide range of different IC packaging types, and four commonly used types were considered for this analysis: Flip chip ball grid array (FCBGA), Quad flat package (QFP), Wafer level chip scale package (WLCSP), and thin shrink small outline package (TSSOP) (see Table 2). The selection of a packaging type is complex and depends on different IC attributes

198 such as its physical dimensions, number of electrical connections and die attach method.
199 Additionally, the selection criteria also depend on other factors such as external
200 operating conditions, power dissipation and cost. For instance, the size of the FCBGA
201 package is 30 times greater than that of the WLCSP. The number of electrical
202 connections are different for these packages because the FCBGA package possesses 40
203 times more connections than the WLCSP. The QFP and TSSOP are older IC packaging
204 types that were developed in the 1970s and 1980s whereas the FCBGA and WLCSP are
205 newer packaging types designed closer to the 2000s.
206 In this work, the technical inputs (see Table 2) were entered into the ICK
207 assembly model to generate the BOM. The BOM estimation procedure for each
208 packaging types was similar to IC manufacturing. For each packaging type (see Table
209 2), a BOM of 74 materials was generated by the ICK assembly model, of which only
210 the top 10 most expensive materials with nearly 95% share of the total material costs of
211 each packaging type were considered for the IC energy analysis. The electricity
212 consumption for each packaging type was assumed to be 0.34 kWh/cm^2 of the package
213 (MCTC 1993).
214 The CED impact of equipment used in IC manufacturing and assembly is
215 beyond the scope of this work. Furthermore, the materials and energy consumed in IC
216 manufacturing and assembly presented in this work were aggregated at the level of IC
217 manufacturing and assembly. The disaggregation of materials with respect to each step
218 of IC manufacturing and assembly can be done in the ICK software tool, but because of
219 proprietary concerns, it is not depicted here. The disaggregation of energy consumed
220 with respect to each step of IC manufacturing and assembly is not possible in the ICK
221 software tool. Such information is challenging to procure and may only exist with IC
222 manufacturers (e.g., Intel, Micron, TSMC). Owing to such data unavailability and

proprietary issues, granular examination of materials and energy consumed with respect to IC manufacturing and assembly steps is beyond the scope of this work.

2.4.1 IC manufacturing—LCA

Similar to the IC economic analysis, five IC types (2D NAND, 3D NAND, DRAM, logic-foundry, and logic-MPU) with each IC possessing a similar technology node (~20 nm) were considered for the IC energy LCA. CED was estimated for each IC type assuming the location of their manufacturing facility to be in the United States. CED was used as an indicator of environmental performance because it is made up of direct and indirect energy use throughout the life cycle of the product, which includes the energy consumed during extraction, manufacturing, and disposal of the raw and auxiliary materials (Huijbregts, et al. 2006). The US electricity grid mix based on the 2019 grid distribution for electricity use was assumed to be 38.4% natural gas, 23.5% coal, 19.7% nuclear, 17.9% renewables, and 0.5% oil. (EIA 2020).

The BOM generated by the ICK model included only material trade names rather than exact names to protect intellectual property rights. (Kim, et al. 2018). For instance, instead of specifying the exact chemical names for the top coating material used in argon fluoride immersion (ArFi) lithography, a trade name—ArFi top coating material—was specified. Lithography processes such as ArFi, KrF and KrFi, employ an ultraviolet laser that uses a mixture of noble gases such as Argon, Krypton or Xenon in addition to halogen gases (e.g., fluorine, chlorine) to etch out patterns and marks on the semiconductor wafers.

To include most major trade-specific materials that contribute to LCI data necessary for LCA, data harmonization was critical to exact material names that are available in LCI databases such as Ecoinvent, GaBi, and others (Murphy 2003) (Kim, et al. 2018) (OECD 2015) (Williams, Ayres and Heller 2002). For instance, ethyl lactate

248 was substituted for the ArFi top coating material because harmonization analysis
249 revealed it to be the most used chemical for top coating materials in ArFi lithography.
250 The exact chemical names were not proxy chemicals but were actual chemicals used in
251 IC manufacturing processes. Stochiometric information was used in cases for missing
252 chemicals in LCI databases (Hischier 2005). OpenLCA software was used to estimate
253 the manufacturing CED for five IC types. All analysed ICs had a similar technology
254 node of ~20 nm and were manufactured in the United States. However, the BOM data
255 generated via the ICK tool and harmonization process were not sensitive to the
256 manufacturing location but was sensitive to the IC type (e.g., logic, MPU, 2D NAND)
257 and their technology node (nm). Therefore, even though the semiconductors were
258 manufactured in countries other than the United States, the BOM data will largely
259 remained unaffected. The electricity grid mix can differ significantly with respect to
260 manufacturing location; therefore, the magnitude of electrical energy consumed (kWh)
261 was independent of location.

262 *2.4.2 IC assembly process—LCA*

263 The trade-specific materials used in the IC assembly were replaced with
264 commonly used exact chemical names via harmonization of literature data in a similar
265 manner as in an IC manufacturing process (Murphy 2003) (Kim, et al. 2018) (OECD
266 2015) (Williams, Ayres and Heller 2002). However, a BOM comparison of each
267 packaging type with corresponding manufacturer material safety declaration sheets
268 (MSDSs) revealed some missing materials. For instance, tin was not considered in the
269 BOM list that was generated by the ICK assembly model, although it was listed in the
270 MSDS for QFP, FCBGA and WLCSP packaging types (Lattice Semiconductor 2020a)
271 (Lattice Semiconductor 2020b) (Melexis 2020) (Microchip 2020). In such cases,
272 missing materials along with their respective quantities were added to the final BOM

list. For materials identical to those listed in manufacturer MSDSs based on the top-down or teardown approach, the higher material quantity from the bottom-up ICK assembly model was considered in the final BOM to include manufacturing material losses. Using this hybrid methodology ensured that all the materials consumed in the IC assembly process were considered. Similar to IC manufacturing, the IC assembly LCI data was also developed using the harmonized BOM and the commercial Ecoinvent v3.5 database (Wernet, et al. 2016). OpenLCA software was used for the final CED estimation of various IC assembly packaging types.

2.4.3 IC manufacturing and assembly—Monte Carlo uncertainty analysis

Uncertainty is pervasive in an LCA and can be generally attributed to input data, temporal data, geographical factors, model development, or LCA boundary (Williams, Weber and Hawkins 2009). Omission of an uncertainty analysis may result in reduced confidence in the LCA results because quantifications of uncertainty fundamentally affect LCA studies.

In this work, the temporal uncertainty attributed to technological and process improvements was addressed in the DRAM technology node analysis. Geographical uncertainty was excluded in this work because the manufacturing of semiconductors was assumed to be only performed in the US. The LCA results will differ significantly if the manufacturing country is varied because this affects the electricity grid mix. For instance, the CO_2 emission factor of electricity produced in the United States is 0.45 kg CO_2 eq./kWh but for China and Europe it is 0.67 kg CO_2 eq./kWh and 0.55 kg CO_2 eq./kWh respectively. This variance is the result of a different mix of electricity sources in these countries. For instance, in 2020, the United States generated nearly 25% of its electricity via coal, whereas China and Europe generated 65% and 15% of their electricity via coal, respectively (Argonne National Laboratry (ANL) 2021).

Data uncertainty in the BOM has been addressed in this work via Monte Carlo Analysis which is one of the most widely used methods to assess BOM uncertainty in LCA. Monte Carlo simulation, a type of stochastic analysis, was performed to analyse the uncertainty in the input parameters on the values of the output vector, CED. The BOM (input parameters) of each IC comprised of nearly 40 components. Specifying uncertainty or probability distribution for each component and computing its effect on CED would be computationally intensive and prohibitively time consuming. Therefore, to simplify the analysis, in the case of ICs only five BOM components were specified for a probability distribution, and their selection was based on each component's degree of influence on the output value (CED). In the case of ICs (e.g., 2D NAND, 3D NAND), the top five contributors to CED were chosen, whereas in the case of IC packaging types (e.g., QFP, TSSOP), only the top two CED contributors were chosen. The number of iterations was assumed to be 100 for each IC type (Heijungs 2020), and the uncertainty analysis based its input parameters on the IC BOM that comprises of nearly 33 materials. The probability distribution function for each of the input parameters was assumed to be a logarithmic normal distribution owing to its suitability in CED computations and its wide usage as a default distribution regarding the Ecoinvent LCI database (Ivanov, et al. 2019) (Muller, et al. 2018). For simplicity, the coefficient of variation (geometric standard deviation [GSD]) was also assumed to be identical for all IC and packaging types at 1.7, and the input parameters were assumed to be statistically independent from one another (Ciroth, et al. 2019).

2.4.4 Sensitivity Analysis Considering Technology Node of ICs

Typically, the IC technology node indicates its circuit generation and manufacturing process. The smaller the technology node (nm), the smaller, faster, and efficient the ICs. The typical technology node of a DRAM IC was 130 nm in 2001,

whereas in 2020, the technology node of manufactured ICs was around 20 nm. Any change in node can significantly affect the materials and energy inventory (BOM) of the IC manufacturing process, thereby influencing the LCA.

To demonstrate the effect of a technology node on the CED, the technology node of a DRAM IC was varied from 110 to 14 nm, and its CED was computed for each node using OpenLCA. BOMs for each technology nodes were generated using ICK software and literature harmonization and were subsequently inserting into OpenLCA to determine the CED. The process assumptions used for technology node analysis are depicted in SI Table S4. In this work, the Ecoinvent v3.5 LCI database was used to conduct LCA.

2.4.5 Estimating the use-phase energy consumption of DRAM IC

The use-phase energy consumption was estimated only for the DRAM IC type while excluding other IC types. The memory device developed in 2017 was assumed to be the 2 GB DDR4 Micron DRAM (9 × 13.2 mm, FCBGA package, 78 ball) (Micron 2020). Because the physical dimensions and number of electrical connections of the DRAM-FCBGA package were observed to be different from those shown in the FCBGA package (see Table 2), a new LCI was generated using the ICK assembly tool. The technology node of the DRAM IC in this package was assumed to be 19 nm because this node is currently being manufactured by IC fabrication facilities worldwide. The LCI of IC manufacturing and assembly was then inserted into OpenLCA, and the CED was computed using the Ecoinvent v3.5 database. To compute use-phase electricity consumption, the use profile of a DRAM device was assumed to be that of a business user. The business user uses the DRAM device for 8 h/day in a 70% active state for 5 days/week and 50 weeks/year with 70% power supply efficiency. The DRAM device's lifetime was assumed to be 3 years (i.e., 6,000 h). (Boyd 2009).

The DRAM use phase energy consumption was based on a business user using a laptop or desktop with an embedded DRAM IC, but consumption can be considerably different if the DRAM is being used in the cloud or a data center.

3.0 Results and Discussion

3.1 Material Flow Analysis of IC Manufacturing and Assembly Processes

3.1.1 IC manufacturing—Material flow analysis

The LCI for each IC type with a technology node of ~20 nm is illustrated in SI Table S1. The BOM includes only the top 25 materials sorted by cost out of nearly 240 materials available from the ICK model. Excluding the amount of water and silicon wafer, the total material used was 0.50–0.90 kg/cm^2; the highest amount was required for 3D NAND, and the lowest for 2D NAND. The range of material used can be attributed to a difference in the total number of manufacturing process steps, including the amount of corresponding materials use (see SI Table S1). Within the total material flow values, the nitrogen gas share was observed to be the highest at 90%. A high share of nitrogen was expected because it is used as a bulk gas in most manufacturing steps (Boyd 2009) (Williams, Ayres and Heller 2002). The average share of nitrogen usage within process tools was observed to be 18% whereas the remaining usage was attributed to non-process tools and equipment. Within process tools, nitrogen was used mostly in wet cleaning processes to clean wafers and prevent particle contamination.

Aside from nitrogen, the component flow of other chemicals and materials was observed to depend on the IC type being manufactured. For instance, even though the quantity of cerium oxide required to produce 3D NAND and logic IC were negligible, the amounts required to manufacture DRAM and 2D NAND were 4.13×10^{-3} and 2.76×10^{-3} kg/cm^2 respectively. These values can be attributed to cerium oxide primarily

being used in chemical mechanical polishing (CMP) steps. Six CMP steps were used in manufacturing DRAM and 2D NAND ICs, which was nearly twice that observed in the case of 3D NAND and logic IC manufacturing.

3.1.2 IC assembly—Material flow analysis

The material demand estimates for the four IC package types were based on the hybrid data harmonization approach by integrating IC manufacturer data (MSDSs) with the ICK model results (see SI Table S2). The broad materials list categorization within each packaging type that is commonly used in industry market reports (SEMI 2020) is depicted in SI Table S2 for four packaging types. SI Table S2 lists 25 components that are consumed in each packaging type. The materials flow was observed to depend primarily on the IC packaging type. For instance, the total material demand per package cross-sectional area of the QFP and WLCSP was observed to be nearly 1.2 and 1.7 times that of the TSSOP, respectively. Furthermore, the individual materials within each package material flow were observed to be significantly different. For instance, the demand of Polyethylene terephthalate (PET) for use as a substrate material in the case of chip scale packages (WLCSP and FCBGA) was observed to be 2.16×10^{-3} and 6.32×10^{-5} kg/cm^2, respectively. In the case of lead frame–based packages (QFP and TSSOP), there was no demand for PET, which was expected because PET is typically present in build-up film layers of chip scale packages. The build-up films are typically a characteristic of chip scale packages (FCBGA and WLCSP) and are absent in lead frame–based packages (TSSOP and QFP). Therefore, the PET demand was observed to be zero in the TSSOP and QFP.

One characteristic feature of lead frame packages such as TSSOP and QFP is their use of C194 material as a metal lead-frame body, comprising metals such as copper, iron, zinc, and phosphorus, unlike relatively more recent chip scale WLCSP and

FCBGA packages. Copper is used in WLCSP and FCBGA packages as a substrate material but not as a leadframe material as observed in the case of lead-frame packages.

3.1.3 Sensitivity analysis of DRAM IC with respect to its technology node

The material demand sensitivity by amount and type to various IC generations or technology nodes for a DRAM IC was also considered. SI Table S3 lists 29 components with their corresponding consumption amounts according to their technology node (nm). The results suggest that the process electricity and material use increase as the number of mask layers increases with decreasing IC technology node. Energy (e.g., electricity, natural gas) and material consumption are directly proportional to the number of photomasks used in the IC manufacturing process. From an IC physical standpoint, fewer technology nodes translate into smaller size and improved performance because of a higher number of discrete components such as transistors and resistors. In the case of packing more small components in an IC, the manufacturing process more complex with an increased number of photomasks and process steps resulting in increased material and energy consumption.

3.2 Economic Analysis—Assessment of Material Costs in IC Manufacturing and Assembly

3.2.1 IC manufacturing—Materials cost in BOM

The materials in the BOM generated by the ICK model were categorized into seven major classifications commonly used in the semiconductor industry markets (SEMI 2020). Figure 3 presents the detailed results of the material categorization along with the IC manufacturing costs for each IC wafer type.

The average IC manufacturing costs were observed to be nearly ~\$3/cm^2; with the highest costs were observed for 3D NAND at ~ \$5/cm^2, followed by logic-foundry,

logic-MPU, DRAM, and 2D NAND (in descending order of costs). Relatively higher manufacturing IC costs were observed for 3D NAND and logic-foundry wafers because of their high depreciation costs, which were nearly 17 times higher than those observed for 2D NAND, DRAM, and logic-MPU. The depreciation costs were mainly dependent on the age of each facility. A newer facility has newer equipment, which possess approximately two-thirds of the total annual depreciation costs. Because 3D NAND and logic-foundry were manufactured in newer facilities (i.e., built in 2018 and 2013, respectively), they had higher depreciation costs than 2D NAND, DRAM, and logic-MPU facilities, which were built in 2002 (see Table 1).

The relative material were not significantly different among various ICs, although remaining costs varied considerably particularly in case of 3D NAND and Logic-Foundry ICs(Figure 3). For all IC types, nearly one-third of the total material costs were attributed to silicon and photoresist ancillaries. Within the silicon category, the cost was attributed to the initial front-end 300 mm silicon wafer. Silicon costs for 2D NAND, 3D NAND, and DRAM ICs were identical because of the use of a polished 300 mm wafer as dictated by their process requirements. However, in the case of logic ICs (foundry and MPU), the process required the use of epitaxial 300 mm wafers in place of polished wafers. The cost of epitaxial wafers is almost twice that of polished wafers because of the deposition of a monocrystalline silicon layer on a polished wafer. Therefore, the silicon costs of logic ICs were observed to be twice those of other ICs.

The category of photoresists ancillaries contributes to an average share of nearly one-third of total material costs of all ICs (see Figure 3). Within photoresist ancillaries, the cost share of materials differed according to IC types. For instance, the cost share of Disilane within photoresist ancillaries was 42% in the case of 3D NAND, whereas it was 19% in the case of DRAM, and 5% in the case of 2D NAND. Disilane is typically

used in IC manufacturing as a gas that is deposited on silicon wafer surfaces. Owing to numerous gas deposition steps in the 3D NAND manufacturing process, the share of Disilane costs was observed to be the largest as compared with other 2D NAND and DRAM ICs. For logic ICs (foundry and MPU), the largest share of costs was in carbon spin-on materials at nearly one-third of the total share. During the etching step of an IC manufacturing process, the carbon spin-on materials form a hard mask over the silicon wafer substrate, which increases the photoresists' selectivity to the substrate. Owing to many etching process steps in the case of logic ICs compared with other ICs, its cost share was also high.

3.2.2 IC assembly—Materials cost in BOM

Figure 3 lists the relative total IC assembly costs along with material cost within each IC packaging type for materials and other remaining categories in terms of unit costs of the FCBGA packaging. The total IC assembly costs were observed to be highest for the WLCSP at ~ \$4.00/cm^2 because of high class testing and material costs whose shares in total costs were nearly 37% each. Excluding the WLCSP, the average assembly cost for other packaging types was ~ \$1.00/cm^2, including for the TSSOP (Figure 3). The contribution of material costs to total IC assembly costs was low for TSSOP, QFP and WLCSP types at 4% each whereas for the FCBGA, it was 43%. Because the physical characteristics and assembly process of each packaging type differ significantly, the LCIs also differ considerably, thereby affecting the contribution of material costs. For all packaging types, the average contribution of other IC assembly categories, such as wafer sorting and class testing to total IC assembly costs were observed to be 20% and 37%, respectively.

With respect to other packaging types, the highest substrate cost was observed for the FCBGA package at ~ \$0.540/cm^2 owing to the high use of materials such as

polypropylene, bisphenol A, aluminium, and aluminium oxide in the substrate. The wire bonding costs for the FCBGA and WLCSP were negligible because of the use of solder balls for electrical connections in place of gold wires, as was also observed for the TSSOP and QFP. Consequently, the share of wire bonding costs in total material costs for the QFP and TSSOP was nearly 50%. Furthermore, the average share of lead-frame costs within total material costs was revealed to be nearly 40% for such packages. On the contrary, the lead-frame costs were non-existent for the FCBGA and WLCSP because of their non–lead-frame construction.

3.3 LCA of IC Manufacturing and Assembly Processes

3.3.1 IC manufacturing—CED

Figure 4 presents CED estimates by various IC types using the BOM embodied energy based on the Ecoinvent database v3.5 in OpenLCA. Although the IC manufacturing processes differed, the top five contributors to CED were observed to be identical: electricity, natural gas, nitrogen, magnesium, and silicon wafer. For all IC types, the average contribution of utility (electricity and natural gas) to the total CED was observed to be largest at 75%, followed by nitrogen at 13% and magnesium at 4%. The on-site energy consumption (electricity and natural gas) contributed to nearly three quarters of the net IC manufacturing CED, and the remaining share was from materials. The highest CED was observed in the case of DRAM IC as shown by its high utility footprint, whereas the lowest was observed in the case of 2D NAND because of its low utility consumption. Because the utility consumption is assumed to be directly proportional to the number of photomasks used, CED is also directly proportional to the number of photomasks used in the IC manufacturing process. Although nitrogen content accounted for nearly 90% of all materials requirements (see SI Table S1), its average

share within material CED was only 51% because the CED intensity of nitrogen is 6.44 MJ/kg. The CED intensity is low relative to other BOM materials such as magnesium and silicon wafer with corresponding CED intensities of 1,235 and 6,366 MJ/kg, respectively.

3.3.2 IC assembly—CED

Figure 4 depicts the CED (MJ/cm^2) for four packaging types (TSSOP, QFP, FCBGA, and WLCSP). The highest CED was observed in the case of the TSSOP owing to its high use of gold as a wire bonding material. Although gold constituted a small share (0.42%) in the TSSOP total material demand (see SI Table S2), its share in the total CED was nearly 72%, which can be attributed to gold's high CED intensity (244,554 MJ/kg). Similarly, in the case of QFP, gold made up 0.13% of the total material demand (see SI Table S2), thus contributing to nearly half of its total CED share. However, in the case of the FCBGA and WLCSP, tin solder balls were used for electrical connection purposes with a low CED intensity (316 MJ/kg) instead of gold wires; therefore, their share of the total CED was negligible for these two package types. Unlike the IC manufacturing phase, the assembly phase had a share of on-site energy consumption (electricity) that varied widely between 26% and 93% according to packaging types owing to differences in materials used. For instance, the TSSOP share of on-site energy consumption was low at nearly 26% owing to the use of Gold in the packaging process that possessed a significant CED footprint, as stated earlier. However, the WLCSP share of on-site energy consumption was high at 93% owing to the use of materials that possessed low CED footprints.

3.3.3 Sensitivity analysis of DRAM IC CED with respect to its technology node

The variation of CED was computed as illustrated in Figure 5 with respect to DRAM's technology node and its respective market introduction year. The CED dependence on node was similar to that shown by materials and energy requirement—the lower the node or more recent the technology year, the higher the CED value. CED is directly proportional to the number of materials and amount of energy consumed, which are directly proportional to the number of photomasks and are therefore inversely proportional to technology node. For example, 50% fewer photomasks were used for the 110 nm node, which translated to 50% lower requirements of electricity, natural gas, and nitrogen, which resulted in a 50% lower CED compared with the 14 nm node. Within each node, the utility (electricity, natural gas) had the largest CED share of nearly 75%, and the remaining share was attributed to materials. Within materials, the share of nitrogen was nearly 50%, whereas the shares of magnesium, silicon wafer, and other materials were 16.67% each.

With the passage of time, the DRAM's technology node has become smaller owing to the smaller feature size that houses smaller and more efficient transistors. However, its manufacturing CED footprint is consequently increasing (Figure 5) with the decrease in technology nodes, which indicates that as the DRAM IC is becoming more advanced, its manufacturing process is consuming increasingly more energy.

A comparison by Boyd of CED estimates for similar technology nodes of DRAM ICs indicated a 24% higher value for a 57 nm technology node than that of a 68 nm node(Boyd 2009). Conversely, a study by Williams et al. showed the CED of a 120 nm node to be 30% lower than that of a 110 nm node(Williams, Ayres and Heller 2002). These differences in CED values can be attributed to different LCI assumptions in addition to different impact factor modeling methods used. For instance, the number of LCI materials from Williams et al. and Boyd were found to be nearly twice as those

543 considered in this work regarding a DRAM IC (Williams, Ayres and Heller 2002)
544 (Boyd 2009). Furthermore, both studies used the economic input-output (EIO)–based
545 modeling approach to compute CED, whereas a process data–based LCA modeling
546 approach was used for analyses conducted in this work. The macro level EIO based
547 LCA approach typically estimates materials, energy, and emissions from activities in a
548 specific sector of the national economy, whereas a micro level process-based LCA
549 approach focuses on the itemized materials, energy, and emissions information of a
550 specific process.

551 *3.3.4 IC manufacturing and assembly—Uncertainty analysis using Monte Carlo*
552 *simulation*

553 In the case of IC manufacturing processes, the uncertainty in the value of CED
554 was computed after specifying the lognormal distribution to the following five input
555 parameters, which were also the top five contributors to CED: electricity, natural gas,
556 nitrogen, magnesium, and silicon wafer. The results of the uncertainty analysis (Figure
557 6) indicate that for all ICs, the CED value varied considerably because of uncertainty in
558 the five input values. The average standard deviation was observed to be 12 MJ/cm^2 (or
559 35% of the mean CED value), suggesting that the uncertainty in the five input
560 parameters would considerably affect CED. These uncertainty results strongly depended
561 on the chosen input value of GSD of 1.7. Any changes to the values of GSD will
562 significantly affect the uncertainty results.

563 For IC packaging types, the uncertainty in input parameter values and their CED
564 effects were also quantified using Monte Carlo simulations (see Figure 6). Variation in
565 the top two CED contributors for each packaging type considerably affected results, as
566 evidenced by the standard deviation values. The average standard deviation was

567 revealed to be considerable at 1.26 MJ/cm^2, which is nearly 42% of the respective
568 packaging type's average CED value.

569 *3.3.5 Estimating the use phase of DRAM IC*

570 The use-phase CED of DRAM IC was computed to be 19 MJ/cm^2, assuming the
571 device is being used for 8 h/day in a 70% active state for 5 days/week and 50
572 weeks/year with 70% power supply efficiency. The share of the use-phase CED
573 footprint in the total life cycle was nearly 28%, whereas the manufacturing and
574 assembly shares were estimated to be 66% and 5%, respectively, for a representative 2
575 GB DDR4 Micron DRAM IC LCA considered. The IC use-phase energy share is
576 sensitive to the number of daily operating hours of the device. For instance, a simple
577 sensitivity analysis revealed that halving the daily usage to 4 h/day diminishes the use
578 phase share in the total life cycle to 16%. Conversely, doubling or tripling the daily
579 usage would boost the use phase share to 44% and 54%, respectively, thereby causing
580 the use phase to possess the largest CED footprint of all life cycle phases.

581 *3.3.6 Comparison of IC life cycle results with literature*

582 Figure 7 shows a comparison of the total life cycle CED of a DRAM device in
583 the existing limited literature studies and indicates values 1.5 times higher than values
584 found by Boyd(Boyd 2009), and 3.3 times higher than values found by Williams et al.
585 (Williams, Ayres and Heller 2002). Most of the discrepancy in CED values was
586 attributed to the IC manufacturing phase, although negligible differences were observed
587 in the remaining life cycle phases of silicon wafer, IC assembly, and IC use. The large
588 difference in the IC manufacturing phase can be attributed to the difference in DRAM
589 manufacturing technology nodes, LCIs, and CED computation methods. For instance,
590 the IC technology node assumed by Williams et al. (Williams, Ayres and Heller 2002)

591 and Boyd (Boyd 2009) were outdated since they belonged to manufacturing years 2002
592 (110 nm node) and 2010 (57 nm node), respectively. As shown in the DRAM
593 technology node analysis, CED strongly depends on manufacturing year and technology
594 node. Furthermore, the number of LCI materials in this study was almost half of those
595 observed in the studies by Williams et al. (Williams, Ayres and Heller 2002) and Boyd
596 (Boyd 2009). Finally, this study used a process-data based LCA estimation method
597 compared with the EIO method used in other studies. Together, these differences
598 contributed to a significant difference in CED estimates.
599 Figure 8 shows a CED comparison of similar IC packages (summation of IC
600 manufacturing and assembly phases) with the GaBi commercial LCA database (GaBi
601 2020). The figure indicates a considerable difference in CED values because of
602 dissimilarities in the number of photomasks used in the respective IC manufacturing
603 processes. For example, although the technology nodes and packaging types of the
604 WLCSP 2D NAND flash IC were identical (45 nm) in GaBi database and this work, the
605 CED estimate from the GaBi database was almost double the estimate in this work
606 because of the 20% more photomasks being used in the GaBi database. Similarly, CED
607 for a 20 nm WLCSP logic IC in the GaBi database was observed to be 23% lower than
608 the value estimated in this work because of the 14% fewer photomasks used in the GaBi
609 database. As stated previously, the BOM values strongly depend on the total number of
610 photomasks used in the IC manufacturing process, and they are directly correlated to IC
611 CED.
612 The difference in CED values of the GaBi database and this work were also quantified
613 using error metrics. Assuming the reference baseline as GaBi database values, the root
614 mean square error (RMSE) was found to be 19 MJ/cm^2, and mean absolute error (MAE)
615 was found to be 13 MJ/cm^2. The RMSE and MAE measures how far the estimated

values are from baseline GaBi values. The lower the values of RMSE and MAE, the closer the calculated CED values to the baseline GaBi values. The lowest MAE was observed to be 0.53 MJ/cm^2 in the case of a TSSOP flash IC (45 nm), whereas the highest MAE was observed to be 43 MJ/cm^2 for an FCBGA logic IC (20 nm). Such a large variation in results was expected because even within the GaBi database, CED values vary significantly among similar ICs with similar packaging attributes. For example, within the GaBi database, in the case of MPU ICs with an identical technology node (130 nm) and packaging type (WLCSP), the CED values for the 425 solder ball package (19 × 19 × 1.5 mm) was observed to be 65 MJ/cm^2 and nearly twice that of a 196 solder ball package (12 × 12 × 1.41 mm). Such a variation could be attributed to the difference in the number of solder balls or in the IC manufacturing or assembly process. In general, even for identical packaging types, the IC assembly process can also vary by IC packaging companies. A granular examination of IC manufacturing or assembly process can be challenging because of each manufacturer's proprietary process information and respective trade secrets.

The manufacturing energy of a typical IC exceeds its use-phase energy consumption, and this energy difference becomes larger as the IC becomes smaller and more advanced (i.e., with the reduction of its technology node). Therefore, both the factors—namely, the technology node reduction and the increase in IC demand—will contribute to the increase in the future manufacturing energy demand of the ICs and carbon dioxide emissions. However, the absolute magnitude of these carbon dioxide emissions will determine their impact on climate change. The entire ICT sector, which includes ICs, had a small share of global carbon dioxide emissions of 4% in 2020 and is projected to increase to 6% in 2040 because of the increase in the number of devices used (Belkhir and Elmeligi 2018). However, Belkhir and Elmeligi only adopted a final

product-based carbon footprint analysis while excluding the IC-based approach that considers the effect of technology node on energy and emissions. Such an IC-based analysis can accurately estimate the carbon dioxide emissions of IC manufacturing, which would assist in evaluating their impacts on climate change. This evaluation may be a future expansion of the current work.

Future work and analysis can also focus on emerging artificial intelligence (AI) technologies on smart manufacturing (Terry, Nagapurkar and Das 2020). For instance, most of the existing literature pertaining to AI applications focuses on the software, such as machine learning algorithms (e.g., deep neural networks) while neglecting hardware. However, like software, hardware is fundamental to AI applications. For instance, machine learning algorithms cannot be run without the computational hardware capacity provided by microprocessors. Similarly, graphics processing units (GPU) used in parallel computing implementations of AI. These units use their multicore processors (e.g., application specific ICs) to perform computations that are10 times faster than a typical central processing unit (CPU). A need exists to determine the energy, cost, and carbon footprint of the hardware that serve as a crucial part of AI systems. Such future analyses would not only complement the ongoing AI research but also be advantageous to the successful commercialization of AI technology in smart manufacturing.

4.0 Conclusions

In this work, economic and life cycle analyses of IC manufacturing and assembly processes were conducted for different IC types and their packaging. The economic analysis of IC manufacturing and assembly was conducted for various IC types with a focus on the necessary BOM required for the IC CED analysis using software tools developed by ICK and via harmonization of existing literature studies.

For IC manufacturing, the analysis was conducted for five IC types (2D NAND, 3D NAND, DRAM, logic, MPU) and four IC assembly packaging types (QFP, FCBGA, TSSOP, and WLSCP). IC manufacturing cost was estimated to be \$1.00 - \$59.00/cm^2. The high cost is for the most advanced 3D NAND IC technology with the advanced WLCSP packaging cost of \$4/cm^2.

Equipment and capital costs made up the largest cost share, whereas materials and energy shares were small. The IC manufacturing and assembly costs were \$1.20 - \$5.20/cm^2 with materials share of 22%, whereas the assembly costs were \$0.2 - \$4/cm^2 with materials share of 14%. CED of manufacturing and assembly processes was also estimated using the detailed life cycle inventory data from the IC manufacturing cost models and OpenLCA. Total CED of IC manufacturing and assembly phases using OpenLCA varied widely from 9 to 38 MJ/cm^2, or 56 to 235 BJ/month (based on the estimated 2018 monthly production of 23 million 200 mm wafers and 269 ICs of 100 mm^2 per wafer), with a major share attributed to on-site energy consumption (approximately about three-quarters). These results were also compared with the latest commercial database in GaBi software, which revealed the CED values of ICs to be considerably different because of dissimilarities in manufacturing process assumptions, mainly in the number of photomasks used. MonteCarlo uncertainty analyses of CED results revealed the uncertainty to be considerable because the standard deviation value ranged from 35% to 42% from the mean CED value. A representative CED analysis of a 2 GB DRAM revealed the IC manufacturing phase to be the most energy intensive phase in its life cycle. The phase's share was found to be 66% compared with the use-phase CED share of 28%.

Future work should be focused on estimating embodied energy and carbon dioxide emissions of advanced hardware (e.g., GPUs, ASICs) needed to support

emerging artificial intelligence technologies such as machine learning, deep learning, neural networks, etc.

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CRediT authorship contribution statement

Sujit Das: Conceptualization, Supervision, Writing – review & editing. Prashant Nagapurkar: Methodology, Formal analysis, Writing – First draft, review, editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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834 doi:10.1111/j.1530-9290.2009.00170.x.
835

836 Table 1 Process assumptions in computing Cumulative Energy Demand - CED for each
837 IC type (technology node ~20 nm).

IC type	**2D NAND**	**3D NAND**	**DRAM**	**Logic-foundry**	**Logic-MPU**
Manufacturer	Company A	Company B	Company C	Company D	Company E
Technology node (nm)	16	21	19	20	22
Facility capacity (# wafers per year as a ratio to 2D NAND)	1	0.88	1.03	0.63	0.83
Photomasks (# as a ratio to 2D NAND)	1	1.23	1.48	1.40	1.10
Total process steps (# as a ratio to 2D NAND)	1	1.13	1.55	1.37	1.08
Total equipment (# as a ration to 2D NAND)	1	1.27	1.28	1.33	1.45
Initial built year of facility	2002	2018	2005	2013	2002

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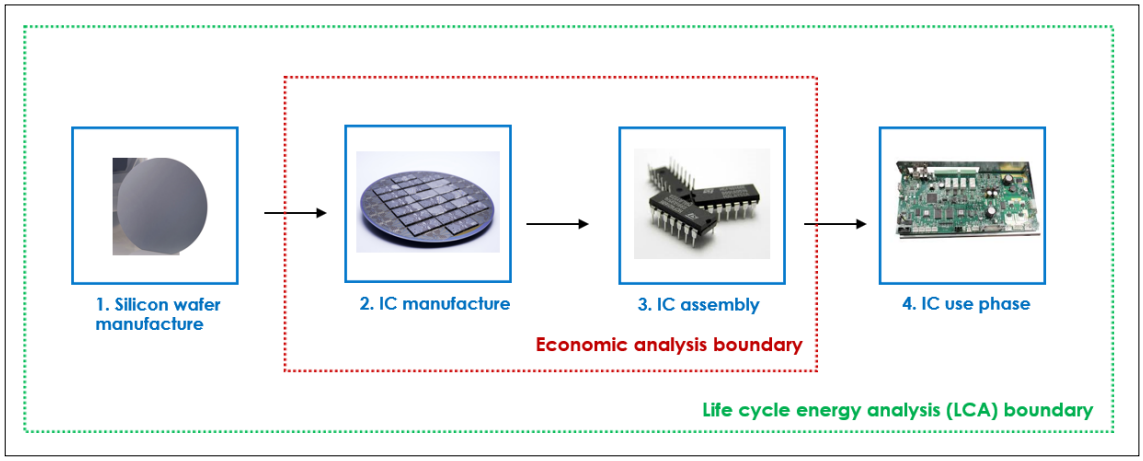
842 Table 2 Major input assumptions to ICK assembly model based on actual
843 manufacturer's safety declaration sheets.

Package type	**FCBGA**	**QFP**	**WLCSP**	**TSSOP**
Manufacturer product reference sheet	Lattice Semiconductor (Lattice Semiconductor 2020a)	Microchip (Microchip 2020)	Lattice Semiconductor (Lattice Semiconductor 2020b)	Melexis (Melexis 2020)
Dimensions (mm)	33 × 33 × 1.4	10 × 10 × 1.4	1.7 × 1.7 × 1.4	4.4 × 9.8 × 0.9
Backgrind wafer thickness (mm)	0.1	0.1	0.1	0.1
Electrical connections (#)	1,020 (solder balls)	44 (gold wire)	25 (solder balls)	28 (gold wire)
Interconnection	Solder balls	Gold wire; length: 1 mil (0.0254 mm)	Solder balls	Gold wire; length: 1 mil (0.0254 mm)
Substrate type	Organic (8 buildup layers)	Metal lead frame (C194 alloy)	Embedded WLCSP	Metal lead frame (C194 alloy)
Die attach	Flip Chip	Epoxy	Epoxy	Epoxy

Net dies from a 300 mm wafer (#)	244	1,476	21,393	3,566
Die efficiency (%)	72.7	92.9	99.5	96.9
Package net weight excluding die (mg)	9,185	331.53	1.35	99.59
Silicon die weight (mg)	215	9.47	1.81	9.41



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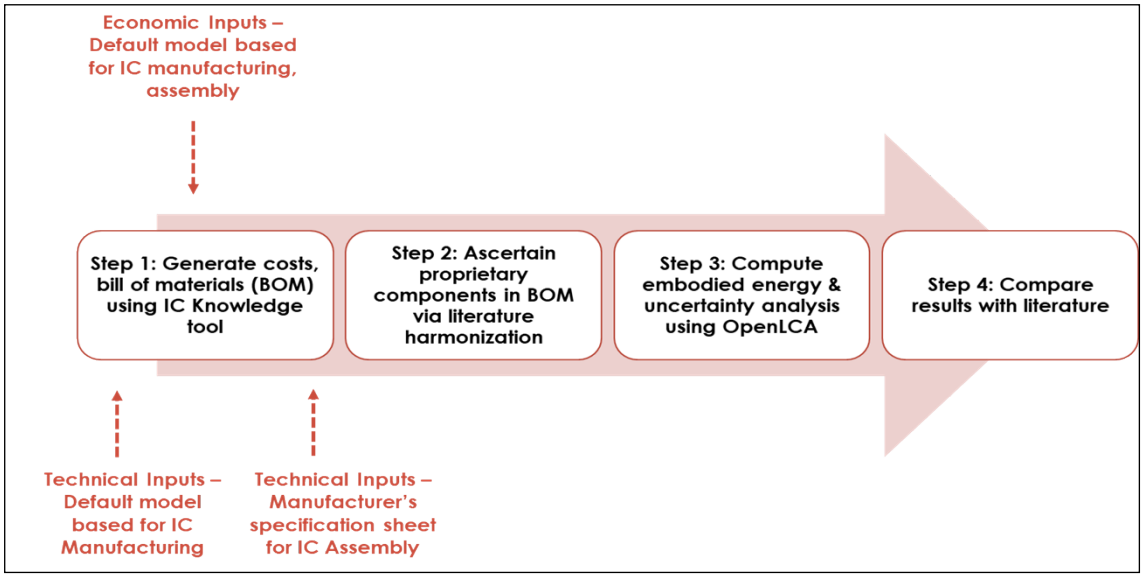
855 *Figure 1 Boundaries for economic analysis and LCA for IC manufacturing, assembly, and use phases*



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857 *Figure 2 Step-by-step methodology for conducting economic and embodied energy analyses for IC manufacturing*
858 *and assembly processes*

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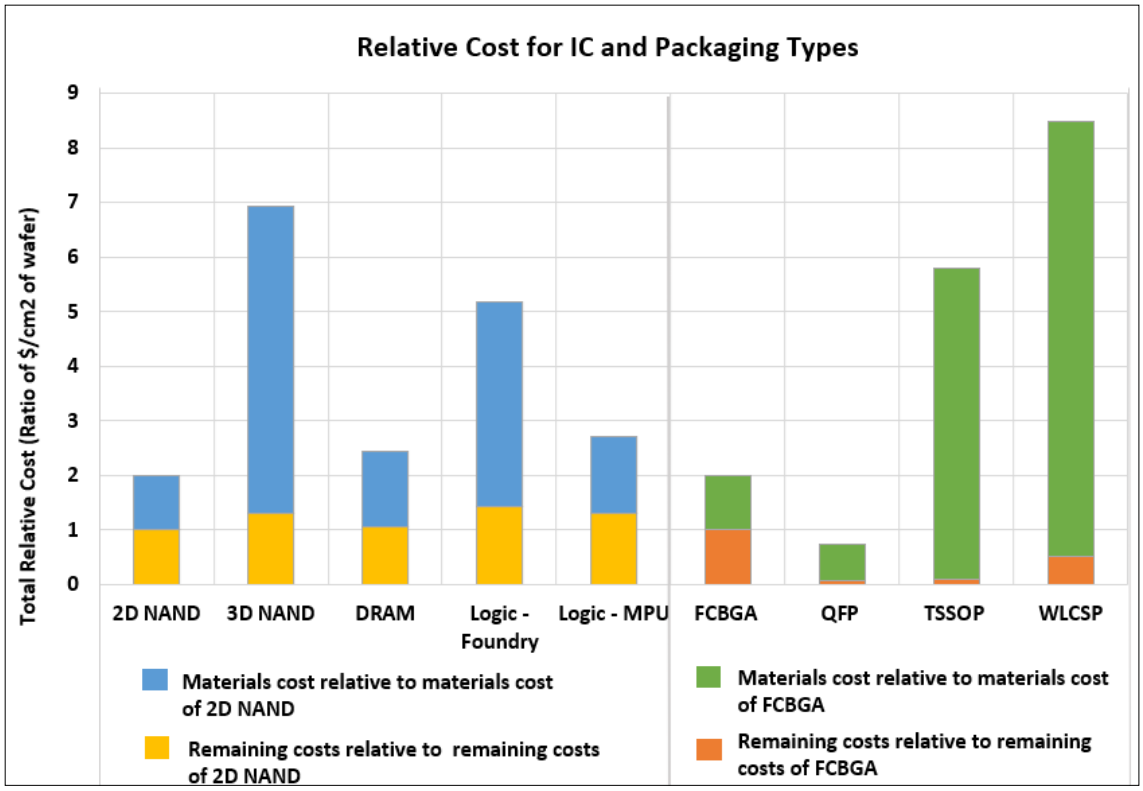


Figure 3 IC manufacturing and assembly costs for materials (e.g., silicon, electronic gases, photoresists) and other remaining categories

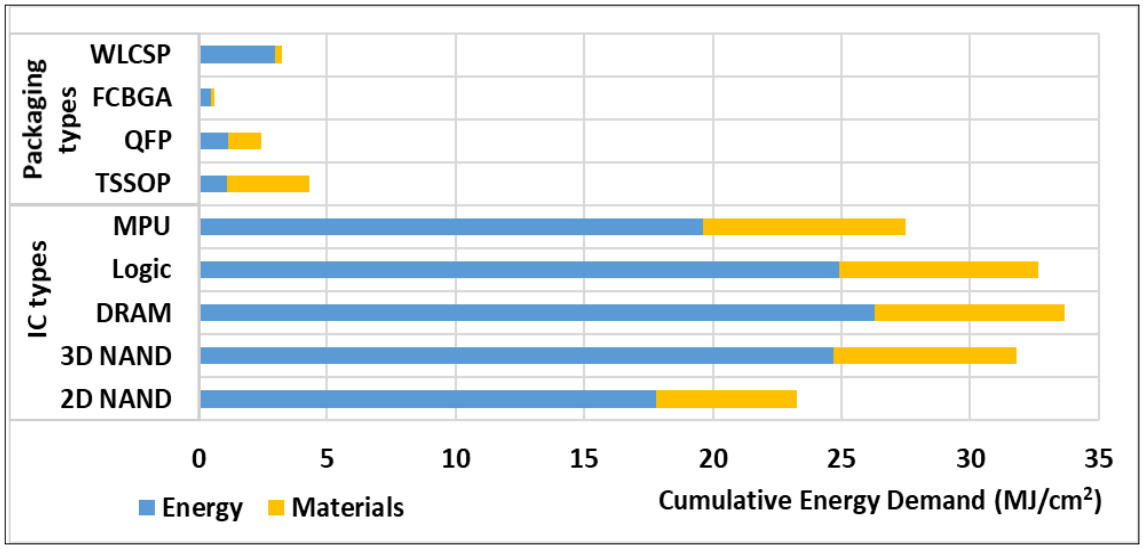
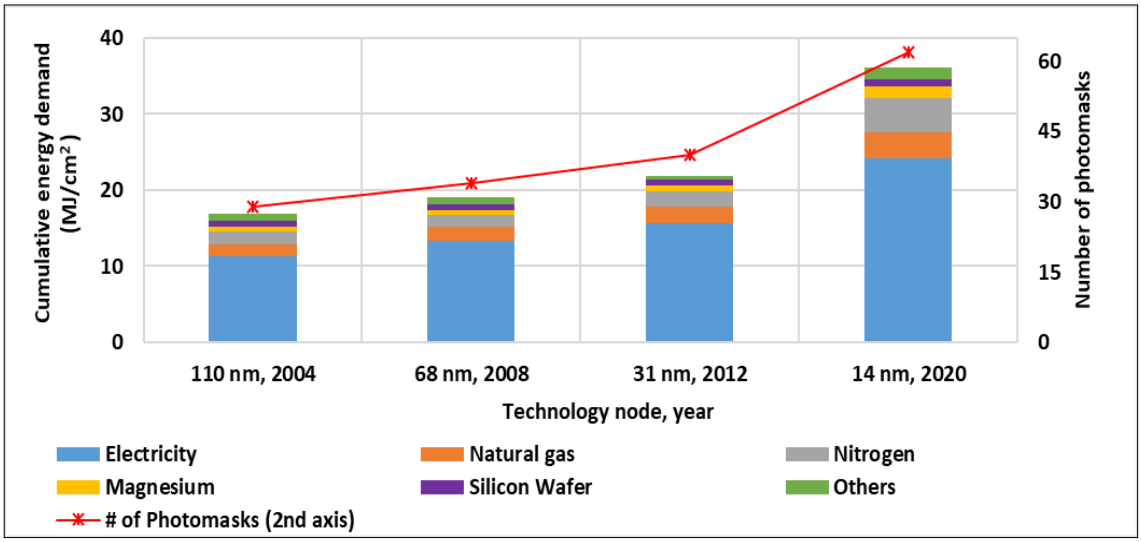


Figure 4 Breakdown of cumulative energy demand - CED (MJ/cm^2) of IC and packaging types



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873 *Figure 5 Variation of Cumulative Energy Demand - CED (MJ/cm²) with respect to DRAM's technology node and*
874 *manufacturing year.*

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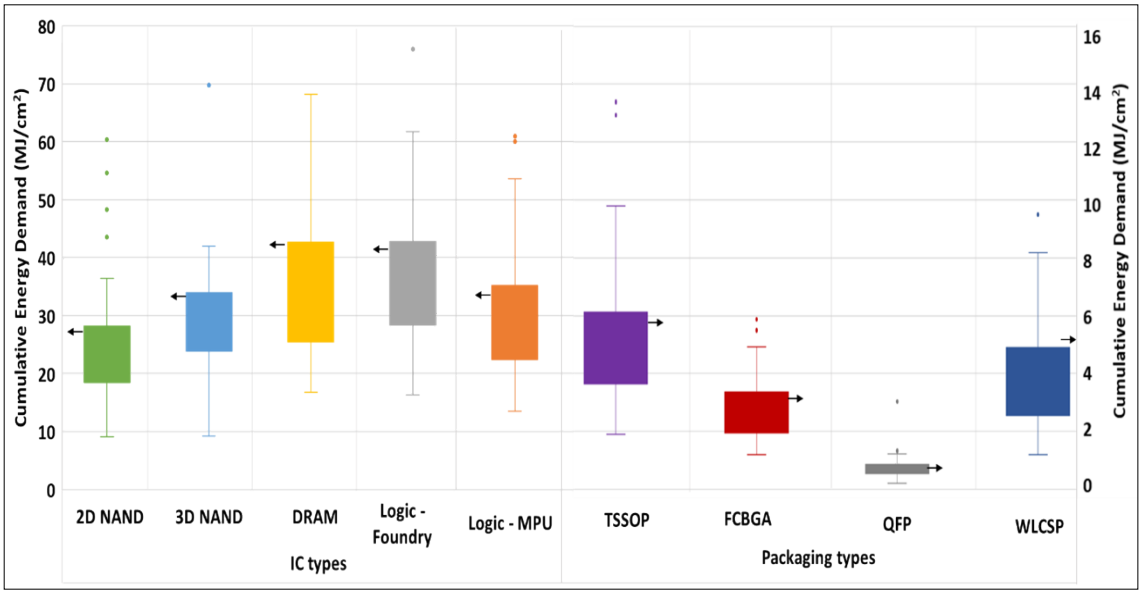

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878 *Figure 6 Uncertainty analysis of IC and packaging types using Monte Carlo simulation*

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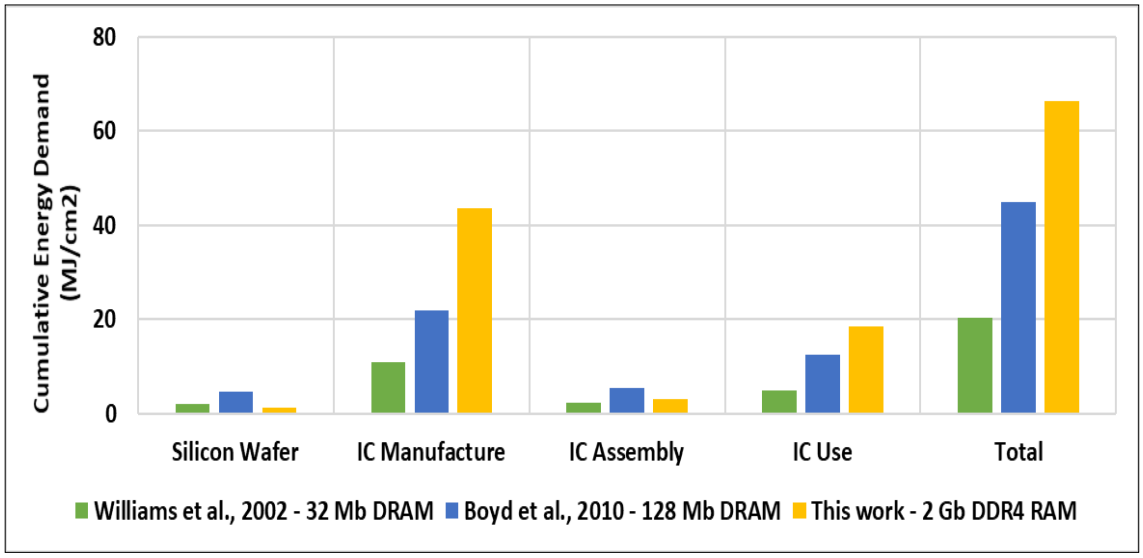

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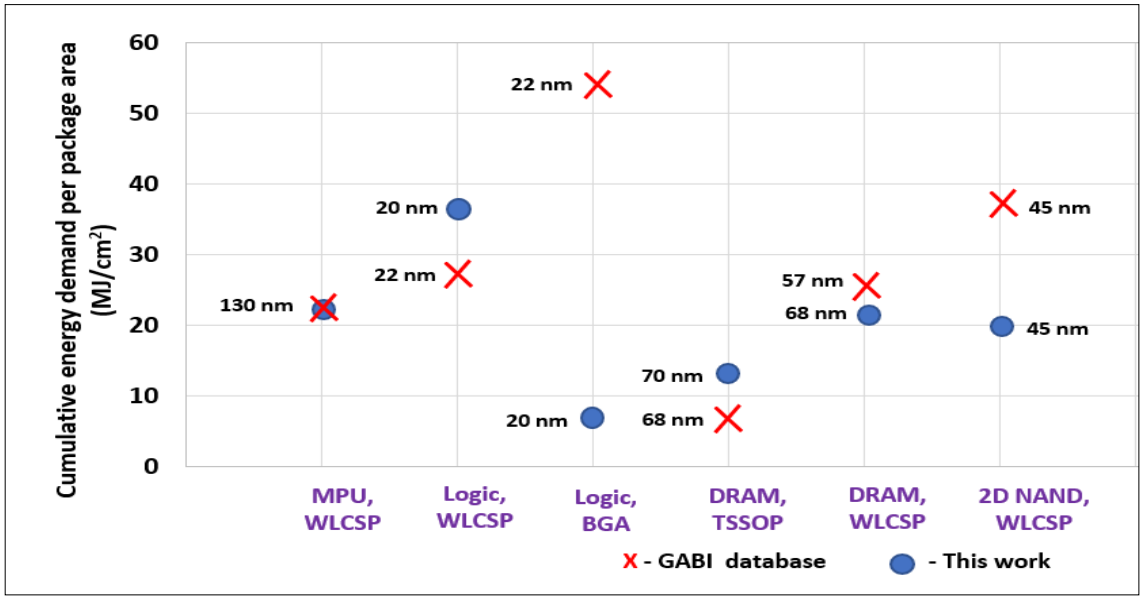
882 *Figure 7 Comparison of Cumulative Energy Demand - CED (MJ/cm2) of a 2 GB DDR4 RAM (20 nm node) with*
883 *literature studies.*



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885 *Figure 8 Comparison of results of the current study with the GaBi database.*

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