Simplified Two-Stage Model Predictive Control for a Hybrid Multilevel Converter with Floating H-Bridge

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***Abstract*—This paper proposes a simplified two-stage model predictive control (ST-MPC) for a hybrid multilevel converter (HMC), which is an active-neutral-point-clamped converter with floating H-bridge (ANPC-H). The objective of the first stage is to select the voltage vector that has the optimal current tracking performance by using a novel geometrical positioning approach in the complex plane. The second stage selects the best switching state among all the available switching states that belong to the same voltage vector obtained in the first stage, to balance dc capacitor voltages and reduce the common mode voltage. The proposed ST-MPC can dramatically reduce the computational burden and ensure the best current tracking by the two-stage structure, such that the execution time is much shorter compared with the conventional MPC. In addition, the geometrical positioning approach in the first stage is generic and can be applicable for any multilevel converters with *N*-level output, thus, this ST-MPC can be applied for both 7- and 9-level operation of the hybrid ANPC-H converter under different dc voltage ratios. Both simulation results and experimental results obtained on a silicon carbide (SiC) hybrid ANPC-H converter prototype validate the feasibility and effectiveness of the proposed ST-MPC strategy.**

***Index Terms*—Active-neutral-point-clamped converter (ANPC), floating H-bridge, hybrid multilevel converter (HMC), model predictive control (MPC).**

I. Introduction

Over the past few decades, various hybrid multilevel converters (HMC) [1]-[14] have been proposed and implemented for different applications, especially for the high-power medium-voltage (MV) applications, such as MV motor drives [5]-[7], renewable energy generation systems [8], electric propulsion aircraft [9], etc. The HMC is usually a combination of one or more types of power electronic building blocks (PEBBs). In particular, one group of HMCs containing cascaded floating H-bridges has been extensively studied [10]-[14], due to its capability of boosting the output voltage [10], [11]. It has the potential for MV grid-tied converter or MV motor drive applications to avoid using high voltage power devices or duplicate PEBBs compared with traditional active neutral-point-clamped (ANPC) converter or T-type converters. Therefore, both the power density and efficiency can be enhanced. More specifically, a hybrid T-type converter with cascaded H-bridge (T-H) is reported in [10], which shares the same features as the ANPC converter with floating H-bridge (ANPC-H) [1], [11]. For these converters, a significant amount of research effort should still be required to develop enhanced control and modulation methods to improve the output power quality and regulate the dc capacitor voltage.

Thanks to the continuous advancement of microprocessors, the model predictive control (MPC) has been increasingly considered as a promising alternative to control the power electronic converters [15]-[20]. The MPC approaches have been proposed and implemented for almost all power electronic applications [20]. Due to their advantages, such as fast dynamic response, the capability of incorporating multiple control objectives, straightforward implementation, and no need for modulator, MPC is much more powerful to tackle the challenge of regulating the dc capacitor voltage in an HMC, compared with traditional linear hierarchical cascade control using multi-carrier pulse-width modulation (MC-PWM) [3], [21], [22].

To ensure the functionality of a power converter, the MPC has to complete a control iteration in the order of tens to hundreds of microseconds. However, the complex multilevel converter topology may lead to an exponentially increased computational burden, which restricts the application of MPC. This is a common challenge for the design of MPC for multilevel converters. For instance, an optimal voltage level MPC for cascaded H-bridge (CHB) converter is proposed in [23], which can reduce the calculation burden from 4^N to $2N+1$, where N is the number of the cascaded H-bridges. An adjacent voltage level MPC is presented in [24], which can also reduce the computational burden but is suitable for scenarios that do not require fast dynamic response. A dc capacitor voltage sorting approach for the modular multilevel converter (MMC) is reported in [25], which can significantly improve the calculation efficiency. In [26], the proposed MPC replaces the time-consuming optimization algorithm by Diophantine equations over the large set of switching combinations to improve the operation efficiency. In [27] and [28], the authors propose a modified sphere decoding algorithm to achieve fast calculation, which reveals significant

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improvement in terms of long-horizon MPC. Furthermore, from the hardware-upgrade point of view, an FPGA based control platform is used for the MPC control of quasi-Z-source inverter in [29], which greatly reduces the control iteration period. However, to control the HMCs, the existing literatures primarily focus on the space vector modulation or MC-PWM [8]-[10], [13], [14]. There is very limited work on the application of MPC for HMCs. In [30], an MPC strategy for an HMC based on ANPC and T-type converter is discussed but only focuses on the single-phase operation without considering computational burden reduction. In addition, the common-mode-voltage (CMV) generated by the fast switching actions of power devices causes common-mode current, which are harmful to the normal operation of converter [31]. Especially for the grid-tied photovoltaic converter and motor drive applications, high CMV can cause problems [32] such as producing over-voltage stresses to the winding insulation, increasing electromagnetic interference and resulting in bearing or leakage current, etc. These problems threaten the motor lifetime [33] and degrade the system reliability [34], [35]. Therefore, the CMV should be reduced simultaneously from the control point of view.

To this end, this paper proposes a solution for the hybrid ANPC-H converter to reduce the computational burden by using a more efficient MPC strategy, namely, a simplified two-stage MPC (ST-MPC), which divides the conventional MPC (C-MPC) into two stages. The first stage selects the voltage vector that has optimal current tracking by geometrical positioning in the complex plane instead of the inefficient exhaustive search algorithm in C-MPC [16], since this geometrical positioning is realized by very simple coordinate transformation and rotation, the computational burden can be dramatically reduced; the objective of the second stage is to evaluate the switching states that satisfy the constraint established by the first stage, i.e., that are subject to the same voltage vector, to select the best one that balances the dc capacitor voltages and reduces the CMV. In this way, not only the operation efficiency is greatly improved, but the best current tracking is guaranteed as well by neglecting the weighting factor for capacitor voltage balancing. The execution time for each control iteration is much shorter compared with the C-MPC. In addition, the geometrical positioning approach in the first stage is generic for an arbitrary multilevel converter with *N*-level output, thus, this proposed ST-MPC can be applied for both 7- and 9-level operation of the hybrid ANPC-H converter under different dc voltage ratios. Both simulation and experimental results on a silicon carbide (SiC) hybrid ANPC-H converter prototype are presented to validate the feasibility and effectiveness of the proposed control strategy.

II. Circuit Analysis

A. Topology Description

Fig. 1 depicts the configuration of the hybrid ANPC-H converter with RL-load, where R and L are the resistance and inductance of the RL-load, u_{dc_1}, u_{dc_2}, u_{dc_a1}, u_{dc_b1}, and u_{dc_c1} are the capacitor voltages of ANPC and H-bridge respectively, i_{dc_1}, i_{dc_2} are the currents of the dc-link capacitors, i_a, i_b, and i_c are the three-phase currents, U_{dc} is the dc-source voltage. The three-level ANPC converter transfers all the active power from the dc-source, while the floating H-bridge serves as a voltage supporting stage, through which only reactive power runs. If the dc voltages are regulated as: $u_{dc\_1} = u_{dc\_2} = U_{dc}/2$, $u_{dc\_a1} = u_{dc\_b1} = u_{dc\_c1} = U_{dc}/4$, the converter output voltage comprises 7 voltage levels: $\pm 3U_{dc}/4$, $\pm U_{dc}/2$, $\pm U_{dc}/4$, and 0; if the dc voltages are maintained as: $u_{dc\_1} = u_{dc\_2} = U_{dc}/2$, $u_{dc\_a1} = u_{dc\_b1} = u_{dc\_c1} = U_{dc}/6$, the converter can output 9 voltage levels: $\pm 2U_{dc}/3$, $\pm U_{dc}/2$, $\pm U_{dc}/3$, $\pm U_{dc}/6$, and 0. It is evident that the hybrid ANPC-H converter possesses the same physical characteristic as the hybrid T-H converter [10]. Furthermore, the operation limitation of this kind of topology is thoroughly investigated in [10] and [12], and thus, will not be discussed in this paper. The working point that is chosen for the simulation and experiment in this paper is within this limitation.

The switching states, output voltage, and charging effects on floating H-bridge capacitor for 7-level operation and 9-level operation are given in Table I and Table II, respectively. v_j are the output voltage levels, S_{ji} are the switching functions of T_{ji}, which have complementary relations as: $S_{j1} = \overline{S}_{j5}$, $S_{j2} = \overline{S}_{j3}$, $S_{j4} = \overline{S}_{j6}$, $S_{j7} = \overline{S}_{j8}$, $S_{j9} = \overline{S}_{j10}$, where $j \in \{a, b, c\}$, $i \in \{1, 2, \ldots, 10\}$. As it can be seen, there are two redundant switching states for output voltage $\pm U_{dc}/4$ under 7-level operation, which have opposite charging effects on floating H-bridge capacitor, and can be used for capacitor voltage balancing, and there are no redundant switching states under 9-level operation, each output voltage level has only one switching state. Note that all the following control analysis is based on 7-level operation, which is also applicable for the 9-level operation.

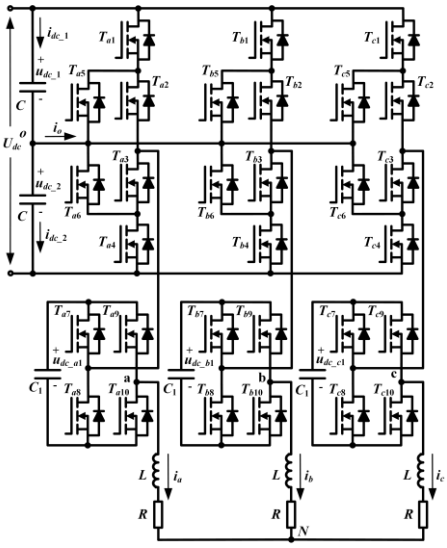


Fig. 1. Topology of the hybrid ANPC-H converter with RL-load.

TABLE I
SWITCHING STATES OF THE HYBRID ANPC-H CONVERTER (7-LEVEL)

Output Voltage (v_j)	S_{jA}	S_{jH}	ANPC			H-bridge		H-bridge Capacitor	
			S_{j1}	S_{j2}	S_{j4}	S_{j7}	S_{j9}	$i_j>0$	$i_j<0$
$3U_{dc}/4$ (3)	1	-1	1	1	0	0	1	-	+
$U_{dc}/2$ (2)	1	0	1	1	0	1	1	0	0
$U_{dc}/4$ (1)	1	1	1	1	0	1	0	+	-
	0	-1	0	1	1	0	1	-	+
0 (0)	0	0	0	1	1	1	1	0	0
$-U_{dc}/4$ (-1)	0	1	0	1	1	1	0	+	-
	-1	-1	0	0	1	0	1	-	+
$-U_{dc}/2$ (-2)	-1	0	0	0	1	1	1	0	0
$-3U_{dc}/4$ (-3)	-1	1	0	0	1	1	0	+	-

TABLE II
SWITCHING STATES OF THE HYBRID ANPC-H CONVERTER (9-LEVEL)

Output Voltage (v_j)	S_{jA}	S_{jH}	ANPC			H-bridge		H-bridge Capacitor	
			S_{j1}	S_{j2}	S_{j4}	S_{j7}	S_{j9}	$i_j>0$	$i_j<0$
$2U_{dc}/3$ (4)	1	-1	1	1	0	0	1	-	+
$U_{dc}/2$ (3)	1	0	1	1	0	1	1	0	0
$U_{dc}/3$ (2)	1	1	1	1	0	1	0	+	-
$U_{dc}/6$ (1)	0	-1	0	1	1	0	1	-	+
0 (0)	0	0	0	1	1	1	1	0	0
$-U_{dc}/6$ (-1)	0	1	0	1	1	1	0	+	-
$-U_{dc}/3$ (-2)	-1	-1	0	0	1	0	1	-	+
$-U_{dc}/2$ (-3)	-1	0	0	0	1	1	1	0	0
$-2U_{dc}/3$ (-4)	-1	1	0	0	1	1	0	+	-

B. Mathematical Model

Using the variables defined in Fig. 1 and assuming that all the dc capacitor voltages are well regulated at their reference values, the mathematical model of the hybrid ANPC-H converter can be given by

$$u_{jo} = L\frac{di_j}{dt} + Ri_j + u_{No} \tag{1}$$

where $j \in \{a, b, c\}$, u_{jo} are the voltage between point j and o, which stand for converter output voltages or pole voltages, u_{No} is equivalent to the CMV u_{cmv}, which can be given by

$$u_{jo} = \frac{U_{dc}}{4}v_j \tag{2}$$

$$u_{cmv} = u_{No} = \frac{1}{3}\left(u_{ao} + u_{bo} + u_{co}\right) \tag{3}$$

where $v_j \in \{-3, \ldots, 0, 1, \ldots, 3\}$. Defining switching functions of ANPC converter and H-bridge as S_{jA} and S_{jH} yields

$$v_j = 2S_{jA} - S_{jH} \tag{4}$$

$$u_{jo} = \frac{U_{dc}}{4}\left(2S_{jA} - S_{jH}\right) \tag{5}$$

where S_{jA} and $S_{jH} \in \{-1, 0, 1\}$, which refers to the negative, zero, and positive output voltage of ANPC converter and H-bridge, respectively.

By applying Clarke's Transformation $\boldsymbol{T_1}$ to (1), the CMV component in mathematical model is neglected as

$$\boldsymbol{u} = L\frac{d\boldsymbol{i}}{dt} + \boldsymbol{i}R \tag{6}$$

where $\boldsymbol{u} = [u_\alpha\ u_\beta]^{\mathrm{T}}$ and $\boldsymbol{i} = [i_\alpha\ i_\beta]^{\mathrm{T}}$, which are converter voltage and phase current vectors in $\alpha\beta$-coordinate respectively, and $\boldsymbol{T_1}$ is defined as

$$\boldsymbol{T_1} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}. \tag{7}$$

The mathematical models of the dc-link and H-bridge capacitors are given by

$$i_{dc\_1} = C\frac{du_{dc\_1}}{dt} \tag{8}$$

$$i_{dc\_2} = C\frac{du_{dc\_2}}{dt} \tag{9}$$

$$S_{jH}i_j = C_1\frac{du_{dc\_j1}}{dt}. \tag{10}$$

The neutral point current can be obtained by subtracting (9) from (8) as

$$i_o = i_{dc\_1} - i_{dc\_2} = C\frac{d\Delta u_{dc}}{dt} \tag{11}$$

where $\Delta u_{dc} = u_{dc\_1} - u_{dc\_2}$, and i_o can be calculated by

$$i_o = H_a i_a + H_b i_b + H_c i_c \tag{12}$$

where variables H_j, which depend on the switching function of the ANPC converter, are defined as

$$H_j = \begin{cases} 1, & S_{jA} = 0 \\ 0, & S_{jA} \neq 0 \end{cases}. \tag{13}$$

Then the discrete-time model of the system can be obtained by applying Euler Forward Approximation to (6), (10), and (11) as

$$\boldsymbol{i}(k+1) = \frac{T_s}{L}\boldsymbol{u}(k) + \left(1 - \frac{RT_s}{L}\right)\boldsymbol{i}(k) \tag{14}$$

$$u_{dc\_j1}(k+1) = S_{jH}\frac{T_s}{C_1}i_j(k) + u_{dc\_j1}(k) \tag{15}$$

$$\Delta u_{dc}(k+1) = \frac{T_s}{C}i_o(k) + \Delta u_{dc}(k) \tag{16}$$

where T_s is the sampling period (or updating period), $\boldsymbol{u}(k)$ and $\boldsymbol{i}(k)$ are the converter output voltage and phase current vector at time instant k, $\boldsymbol{i}(k+1)$ is the predicted phase current vector at time instant $k+1$, $i_j(k)$, $u_{dc\_j1}(k)$, $i_o(k)$, and $\Delta u_{dc}(k)$ are the sampled phase current, capacitor voltage, neutral point current and deviation of the two dc-link capacitor voltages at time instant k, $u_{dc\_j1}(k+1)$ and $\Delta u_{dc}(k+1)$ are the predicted H-bridge capacitor voltages and predicted deviation of the two dc-link capacitor voltages at time instant $k+1$. For the CMV, the $k+1$ instant can be assumed to be equivalent to k instant, based on (3) and (5), the discretized model of CMV can be given by

$$u_{cmv}(k+1) = \frac{1}{3}\left[u_{ao}(k) + u_{bo}(k) + u_{co}(k)\right] \tag{17}$$

where u_{jo} ($j \in \{a, b, c\}$) are converter output voltages at time instant k, which can be given by

$$u_{jo}(k) = \frac{U_{dc}}{4}\left(2S_{jA} - S_{jH}\right). \tag{18}$$

III. Simplified Two-Stage Model Predictive Control

A. ST-MPC Architecture

For the hybrid ANPC-H converter, the conventional MPC (C-MPC) strategy [17] should evaluate totally 9^3 = 729 switching states within one sampling period, which makes it computationally impractical. In addition, to address the trade-off between capacitor voltage balancing and reference current tracking, the weighting factors should be carefully tuned, which may affect the output current quality. To solve these problems, the proposed ST-MPC approach divides the MPC scheme into two stages, i.e., the first stage aims at finding the voltage vector that has optimal current tracking effect, thus, the best current tracking is guaranteed and the weighting factor for capacitor voltage balancing and reference current tracking is neglected, and the second stage selects the optimal switching state among all the switching states that satisfy the constraints set by the first stage, which are subject to the same voltage vector, to balance the dc capacitor voltages and mitigate the CMV. Fig. 2 depicts the overall architecture of the proposed ST-MPC strategy.

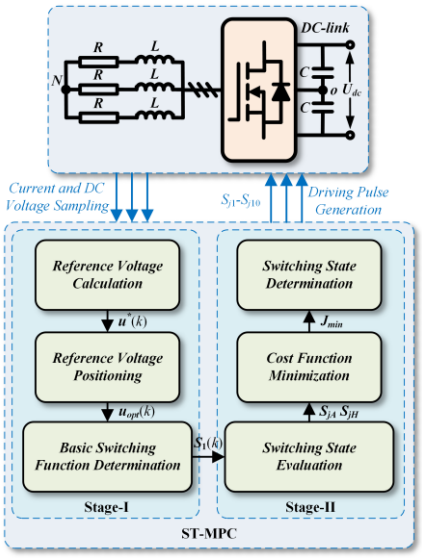


Fig. 2. Overall architecture of the proposed ST-MPC strategy.

B. Stage I: Optimal Voltage Vector Positioning

All the switching states of the hybrid ANPC-H converter form a hexagon with 127 voltage vectors in $\alpha\beta$-coordinate, as shown in Fig. 3 with each dot representing a voltage vector. Each voltage vector has its own impact on current tracking. To determine the optimal voltage vector $\boldsymbol{u}_{opt}(k)$ in terms of the current tracking performance at the time instant k, the following prediction model can be established by replacing predicted current in (15) with reference current $\boldsymbol{i}^*(k+1)$ at the k+1 instant (note that $\boldsymbol{i}^*(k+1)$ can be obtained by Lagrange Extrapolation approach [17]):

$$\boldsymbol{u}^*(k)=\frac{L}{T_s}\boldsymbol{i}^*(k+1)+\left(R-\frac{L}{T_s}\right)\boldsymbol{i}(k) \tag{19}$$

where $\boldsymbol{u}^*(k)$ represents the reference voltage vector that forces the actual current to exactly track the reference current $\boldsymbol{i}^*(k+1)$. Subsequently, Stage I becomes a searching problem, i.e., to search for the voltage vector closest to the reference voltage vector, which is the optimal voltage vector $\boldsymbol{u}_{opt}(k)$.

Fig. 3 demonstrates the space voltage vectors of the hybrid ANPC-H converter along with the reference voltage vector $\boldsymbol{u}^*(k)$ in $\alpha\beta$-coordinate. To simplify the analysis, all the voltage vectors in the $\alpha\beta$-coordinate are converted to per-unit values, i.e., u_{jo} are per-unit values equal to output voltage levels v_j, and $\boldsymbol{u}^*(k)$ is also normalized to per-unit value by $U_{dc}/4$ as $\boldsymbol{u}^*(k) = [V_\alpha\ V_\beta]^T$. As it can be seen, space voltage vectors are divided into six sectors. The optimal voltage vector $\boldsymbol{u}_{opt}(k)$ is the one that the reference voltage vector $\boldsymbol{u}^*(k)$ locates in its surrounding hexagon (SH), which is formed by six vertices that have identical distance to this voltage vector. Therefore, the optimization problem of Stage I is directly transformed into a geometrical positioning problem in the complex plane.

For an arbitrary reference voltage vector which rotates in the complex plane, this geometrical positioning problem can

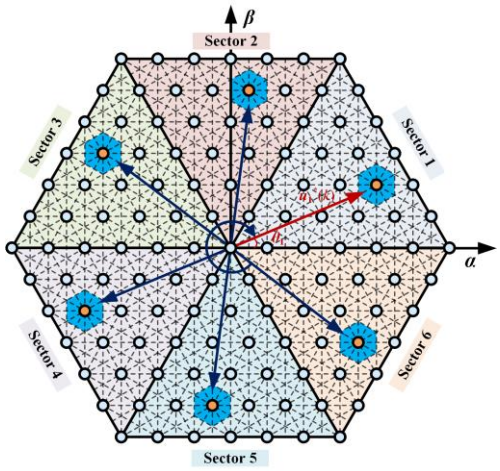


Fig. 3. Rotation of the reference voltage vector in $\alpha\beta$-coordinate.

be equivalently performed in Sector 1 by rotating the reference voltage vectors in other sectors clockwise by multiples of $\pi/3$. Fig. 3 depicts the rotation of the reference voltage vector and its equivalent counterpart in Sector 1. Assuming that the initial angle of the reference voltage vector is in the range $\theta \in [0, 2\pi)$, which can be expressed by

$$\theta=\begin{cases}\arccos\left(V_\alpha\Big/\sqrt{V_\alpha^{\,2}+V_\beta^{\,2}}\right), & V_\beta\ge 0\\ 2\pi-\arccos\left(V_\alpha\Big/\sqrt{V_\alpha^{\,2}+V_\beta^{\,2}}\right), & V_\beta<0\end{cases}. \tag{20}$$

Therefore, the sector number S can be calculated by rounding down function as

$$S=\left\lfloor\frac{3\theta}{\pi}\right\rfloor+1 \tag{21}$$

where the first term on the right means the greatest integer that is not greater than $3\theta/\pi$. The angle and coordinate of an arbitrary reference vector $\boldsymbol{u}^*(k)$ when rotated to Sector 1 can be given by

$$\theta_1 = \theta - \frac{\pi}{3}\left\lfloor \frac{3\theta}{\pi} \right\rfloor \tag{22}$$

$$\begin{cases} V_{\alpha 1} = \sqrt{V_\alpha{}^2 + V_\beta{}^2}\cos\theta_1 \\ V_{\beta 1} = \sqrt{V_\alpha{}^2 + V_\beta{}^2}\sin\theta_1 \end{cases} \tag{23}$$

where $\boldsymbol{u}_1^*(k) = [V_{\alpha 1}\ V_{\beta 1}]$, which refers to the rotated reference voltage vector in Sector 1, θ_1 is the angle in Sector 1.

Then, to obtain an integer coordinate system, the $\alpha\beta$-coordinate is transformed into 120° gh-coordinate [36] by using the following transformation equation:

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{24}$$

$$\begin{bmatrix} g \\ h \end{bmatrix} = \begin{bmatrix} 1 & 1/\sqrt{3} \\ 0 & 2/\sqrt{3} \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \tag{25}$$

where g, $h \in \{-6, \ldots, 0, 1, \ldots, 6\}$, which are the coordinates of the space voltage vectors in 120° gh-coordinate.

Furthermore, to make the vertices of the SH have integer coordinates, the 120° gh-coordinate is transformed into 120° mn-coordinate by rotating the 120° gh-coordinate clockwise by 30°, the transformation equation is given by

$$\begin{bmatrix} m \\ n \end{bmatrix} = \begin{bmatrix} 2 & -1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} g \\ h \end{bmatrix} \tag{26}$$

where m, $n \in \{-12, \ldots, 0, 1, \ldots, 12\}$, which are the coordinates of the space voltage vectors in 120° mn-coordinate. Similarly, the reference voltage vector $[V_{\alpha 1}\ V_{\beta 1}]^{\mathrm{T}}$ in Sector 1 can also be converted to $[V_{g1}\ V_{h1}]^{\mathrm{T}}$ and $[V_{m1}\ V_{n1}]^{\mathrm{T}}$ in 120° gh- and mn-coordinate respectively. In this way, trigonometric functions are replaced by algebraic operation, hence the calculation process is tremendously simplified.

For simplicity, the switching functions of the hybrid ANPC-H converter can be defined as $[S_a\ S_b\ S_c]$, in which $S_j = v_j + 3$, $S_j \in \{0, 1, \ldots, 6\}$. Fig. 4 shows the switching functions and space voltage vectors of Sector 1 in 120° gh- and mn-coordinate. By defining the switching function with the smallest value as the basic switching function of one particular space voltage vector, the other redundant switching functions of this voltage vector can be obtained by integer step-increment of the basic switching function in 120° gh-coordinate. The positioning process can now be performed in two steps as explained in the following paragraphs.

Step 1: Locating in 120° gh-coordinate:

Fig. 5 illustrates the positioning process of the reference voltage vector in 120° gh-coordinate. The basic vector of the reference voltage vector, defined as basic vector in gh-coordinate (BV-GH), can be given by

$$\begin{bmatrix} g_0 \\ h_0 \end{bmatrix} = \begin{bmatrix} \lfloor V_{g1} \rfloor \\ \lfloor V_{h1} \rfloor \end{bmatrix}. \tag{27}$$

Then the basic switching function of this basic vector can be given by $[g_0\ h_0\ 0]$. As it can be seen in Fig. 5(b), the reference

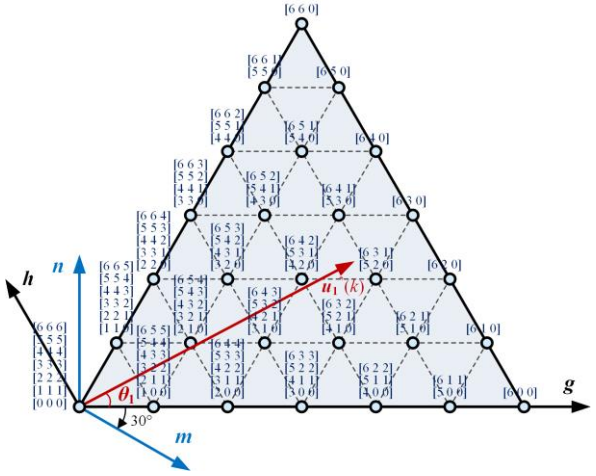
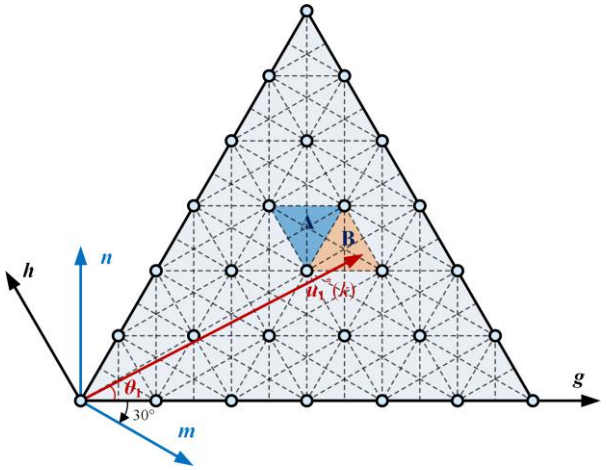
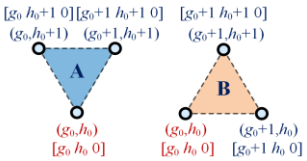


Fig. 4. Switching functions and space voltage vectors in Sector 1.



(a)



(b)

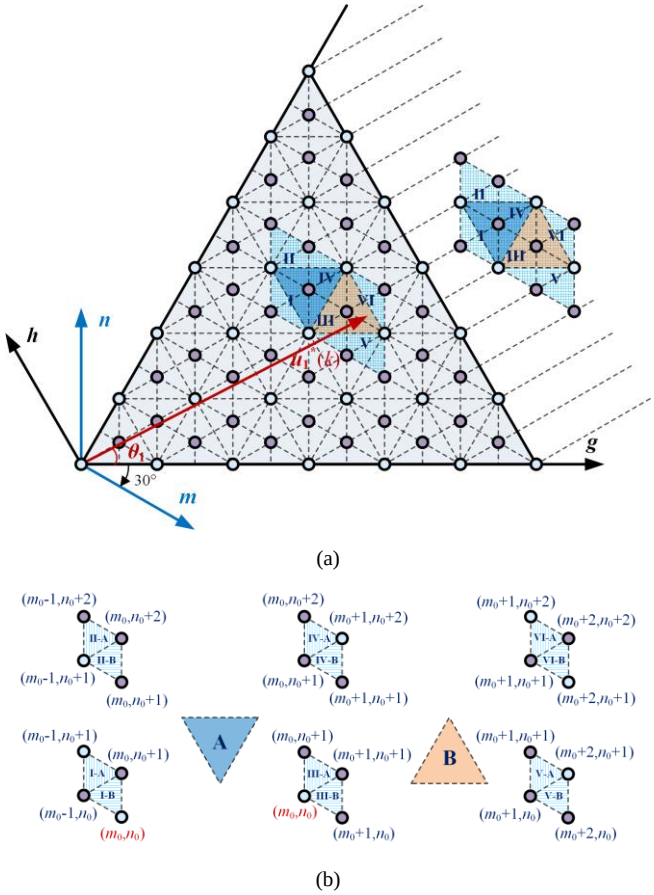
Fig. 5. Reference voltage vector in 120° gh- and mn-coordinate. (a) Space voltage vectors in Sector 1. (b) Two types of switching triangles.

vector possibly locates in either triangle A or B, namely, type A or B, the vertices of which can be obtained by integer step-increment of the basic vector coordinate. These vertices encompass a parallelogram which is composed of triangle A and B. The following criterion can be applied for further positioning of the reference vector:

$$\boldsymbol{u}_1^*(k) \in \begin{cases} \text{A},\ V_{g1} - V_{h1} \le g_0 - h_0 \\ \text{B},\ V_{g1} - V_{h1} > g_0 - h_0 \end{cases}. \tag{28}$$

Step 2: Locating in 120° mn-coordinate:

Fig. 6 illustrates the step 2 of the positioning procedure to locate the reference vector in the 120° mn-coordinate. As illustrated in Fig. 6(a), there are in total six parallelograms (I-



(a)

(b)

Fig. 6. Reference voltage vector in 120° *gh*- and *mn*-coordinate. (a) Space voltage vectors and vectors of the SH vertices in Sector 1. (b) Six types of switching parallelograms.

VI) overlapping with triangle A and B in 120° *mn*-coordinate, whose vertices consist of space voltage vectors and vertices of the SH. The parallelograms I, II, III, and IV overlap with triangle A, while parallelograms III, IV, V, and VI overlap with triangle B. Moreover, the vertices of parallelogram I and VI contain two voltage vectors while the vertices of parallelogram II, III, IV, and V only contain one voltage vectors, which means I and VI belong to two aforementioned SHs and hence more positioning procedure is needed, while II, III, IV, and V belong to one single SH and thus the optimal voltage vector $\boldsymbol{u}_{opt}(k)$ can be directly selected.

In order to get the coordinates of these parallelograms, the BV-GH ($[g_0\ h_0]^{\mathrm{T}}$) of the reference voltage vector should be transformed into 120° *mn*-coordinate by:

$$\begin{bmatrix} m_0 \\ n_0 \end{bmatrix} = \begin{bmatrix} 2 & -1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} g_0 \\ h_0 \end{bmatrix} \tag{29}$$

where $[m_0\ n_0]^{\mathrm{T}}$ is the coordinate of the BV-GH in 120° *mn*-coordinate. As demonstrated in Fig. 6(b), the space vectors of the vertices of the aforementioned parallelogram I-VI in 120° *mn*-coordinate can be readily obtained by integer arithmetic based on $[m_0\ n_0]^{\mathrm{T}}$. Similarly, the basic vector in 120° *mn*-coordinate (BV-MN) can be calculated by rounding down function as

$$\begin{bmatrix} m_1 \\ n_1 \end{bmatrix} = \begin{bmatrix} \lfloor V_{m1} \rfloor \\ \lfloor V_{n1} \rfloor \end{bmatrix}. \tag{30}$$

Therefore, the criterion for determining the parallelograms can be expressed as follows:

if $\boldsymbol{u}_1^*(k) \in$ A,

$$\boldsymbol{u}_1^*(k) \in \begin{cases} \text{I}, & V_{m1} \in (m_0-1, m_0] \,\&\, V_{n1} \in (n_0, n_0+1] \\ \text{II}, & V_{m1} \in (m_0-1, m_0] \,\&\, V_{n1} \in (n_0+1, n_0+2] \\ \text{III}, & V_{m1} \in (m_0, m_0+1] \,\&\, V_{n1} \in (n_0, n_0+1] \\ \text{IV}, & V_{m1} \in (m_0, m_0+1] \,\&\, V_{n1} \in (n_0+1, n_0+2] \end{cases} \tag{31}$$

if $\boldsymbol{u}_1^*(k) \in$ B,

$$\boldsymbol{u}_1^*(k) \in \begin{cases} \text{III}, & V_{m1} \in (m_0, m_0+1] \,\&\, V_{n1} \in (n_0, n_0+1] \\ \text{IV}, & V_{m1} \in (m_0, m_0+1] \,\&\, V_{n1} \in (n_0+1, n_0+2] \\ \text{V}, & V_{m1} \in (m_0+1, m_0+2] \,\&\, V_{n1} \in (n_0, n_0+1] \\ \text{VI}, & V_{m1} \in (m_0+1, m_0+2] \,\&\, V_{n1} \in (n_0+1, n_0+2] \end{cases}. \tag{32}$$

To further locating the reference vector to triangles within the parallelograms, the following criterion can be applied:

$$\boldsymbol{u}_1^*(k) \in \begin{cases} x\text{-A}, & V_{m1} - V_{n1} \le m_1 - n_1 \\ x\text{-B}, & V_{m1} - V_{n1} > m_1 - n_1 \end{cases} \tag{33}$$

where $x \in \{\text{I}, \text{II}, \ldots, \text{VI}\}$.

After the location of the reference vector is determined, the basic switching function $\boldsymbol{S}_1(k)$ of the optimal voltage vector $\boldsymbol{u}_{opt}(k)$ can be expressed according to Fig. 5(b) as

$$\boldsymbol{S}_1(k) = \begin{cases} [g_0\ h_0+1\ 0], & \boldsymbol{u}_1^*(k) \in \{\text{I-A, II}\} \\ [g_0\ h_0\ 0], & \boldsymbol{u}_1^*(k) \in \{\text{I-B, III}\} \\ [g_0+1\ h_0+1\ 0], & \boldsymbol{u}_1^*(k) \in \{\text{VI-A, IV}\} \\ [g_0+1\ h_0\ 0], & \boldsymbol{u}_1^*(k) \in \{\text{VI-B, V}\} \end{cases} \tag{34}$$

where $\boldsymbol{S}_1(k) = [S_{a1}\ S_{b1}\ S_{c1}]$. If $S_{a1} > 6$, as illustrated in Fig. 6(a), which means that the reference vector locates beyond Sector 1 (but still within the first $\pi/3$ angle), then the actual optimal voltage vector must be shifted to the furthest layer of the space voltage vector in Sector 1, which should be the nearest voltage vector to the reference vector. The specific expression for the basic switching function of the optimal voltage vector when $S_{a1} > 6$ can then be given as follows:

if $\boldsymbol{u}_1^*(k) \in$ {I-A, II-B, III-B, IV-B, V-B, VI-A},

$$\boldsymbol{S}_1(k) = \begin{bmatrix} 6 \\ S_{b1} - (S_{a1} - 6) + \lfloor (S_{a1} - 6)/2 \rfloor \\ 0 \end{bmatrix}^{\mathrm{T}} \tag{35}$$

if $\boldsymbol{u}_1^*(k) \in$ {I-B, II-A, III-A, IV-A, V-A, VI-B},

$$\boldsymbol{S}_1(k) = \begin{bmatrix} 6 \\ S_{b1} - \lfloor (S_{a1} - 6)/2 \rfloor \\ 0 \end{bmatrix}^{\mathrm{T}} \tag{36}$$

where the value of S_{a1} and S_{b1} are subject to (35). At this time, if $S_{b1} < 0$, $\boldsymbol{S}_1(k) = [6\ 0\ 0]$; if $S_{b1} > 6$, $\boldsymbol{S}_1(k) = [6\ 6\ 0]$.

Consequently, the reference voltage vector can be positioned wherever it is in the whole complex plane.

The above expressions for basic switching functions can be interpreted as follows: when reference vector is outside of Sector 1, the nearest voltage vector is determined by whether the reference vector locating in the perpendicular zone of the voltage vector stretching to the direction of the coordinate, as depicted in Fig. 6(a). It is noteworthy that the positioning of the reference vector outside of Sector 1 is of great significance especially when the converter works at transient state, when the calculated reference may exceed the boundary of Sector 1. Once the basic switching function in Sector 1 is obtained, the basic switching functions in other five sectors can be easily derived by the relationship exhibited in Table III.

C. Stage II: Switching State Selection

Once the basic switching function $\boldsymbol{S_1}(k) = [S_{a1}\ S_{b1}\ S_{c1}]$ is determined in Stage I, Stage II aims at selecting the optimal switching state, which is subject to the switching function obtained in Stage I, to balance dc capacitor voltage and simultaneously reduce the CMV. This is realized by minimizing the error between desired value and the predicted one. Therefore, the cost functions for MPC Stage II can be given by

$$J_j = \left\| u_{dc\_j1}(k+1) - \frac{U_{dc}}{4} \right\|_2^2 \tag{37}$$

$$J_{dc} = \left\| \Delta u_{dc}(k+1) \right\|_2^2 \tag{38}$$

$$J_{cmv} = \left\| u_{cmv}(k+1) \right\|_2^2 \tag{39}$$

The total cost function J is the summation of the above cost functions:

$$J = J_a + J_b + J_c + J_{dc} + \lambda J_{cmv} \tag{40}$$

where λ ($0 \le \lambda \le 1$) is the weighting factor for CMV. To date, the tuning of weighting factor is still based on heuristic approach. Even though there are several studies available on the weighting factor selection, but still, it is an open question for researchers [18], [19]. Since there is a trade-off between dc capacitor voltage balancing and CMV reduction, the greater λ is, the severer the dc voltage fluctuation is. According to general industry standard [37], the limitation for weighting factor is that the dc capacitor voltage fluctuation ratio should be $\varepsilon \le 5\%$ (ε represents the fluctuation ratio of the H-bridge dc voltage, which is selected as the indicator of the capacitor voltage fluctuation in this paper), which means that when adjusting λ, ε cannot exceed 5%.

The variables at time instant k+1 can be found in (14)-(17). Therefore, the optimization problem can be described as follows

$$\begin{cases} \min\limits_{S_{jA}, S_{jH}} \ J \\ s.t. \quad 2S_{jA} - S_{jH} = S_j + i \\ \qquad i \in [0,1,...,6 - S_a] \end{cases} \tag{41}$$

TABLE III
SWITCHING FUNCTION RELATIONSHIPS IN VARIOUS SECTORS

Sector	Phase A	Phase B	Phase C
1	S_{a1}	S_{b1}	S_{c1}
2	S_{a1}-S_{b1}	S_{a1}	0
3	0	S_{a1}	S_{b1}
4	0	S_{a1}-S_{b1}	S_{a1}
5	S_{b1}	0	S_{a1}
6	S_{a1}	0	S_{a1}-S_{b1}

where i serves as an indicator for all the redundant switching states of the optimal voltage vector. For the first layer of the space voltage vector, which has the maximum redundant switching functions of 6, there are totally 14 switching states that needs to be evaluated in Stage II. For the other layers, the evaluation amount should be less than 14. Therefore, the calculation burden is dramatically decreased compared with the classical MPC, which has an evaluation amount of 9^3 = 729. Apparently, this proposed ST-MPC strategy can also be easily applied for the 9-level operation, in which there are maximum 8 switching states that need to be evaluated in Stage II.

IV. SIMULATION RESULTS

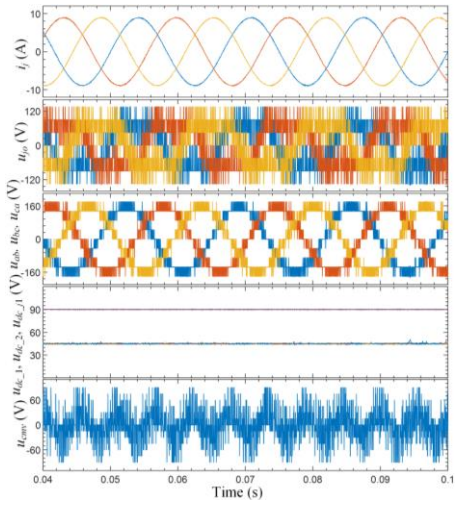
To evaluate the performance of the proposed ST-MPC for the hybrid ANPC-H converter, a simulation model is built up in MATLAB/Simulink. The schematic of the converter is identical to that in Fig. 1, and the system parameters for the ST-MPC are given in Table IV. Figs. 7-9 are the simulation results of 7-level operation of the hybrid ANPC-H converter. Since the C-MPC is computationally impractical, a modified conventional MPC (MC-MPC) is presented to compare with the proposed ST-MPC, which evaluates all the switching states of the three voltage vectors that encompass the reference voltage vector (as depicted in Fig. 5). Note that the 7-level operation is similar to the 9-level one, therefore, only the comparisons for the 7-level scenario are demonstrated below. In addition, since the only difference between this MC-MPC and the proposed ST-MPC is the current tracking approach in the first stage, which results in different execution times but the same performance in terms of CMV and dynamic response, the comparisons only focus on the steady-state performance.

TABLE IV
SYSTEM PARAMETERS FOR ST-MPC

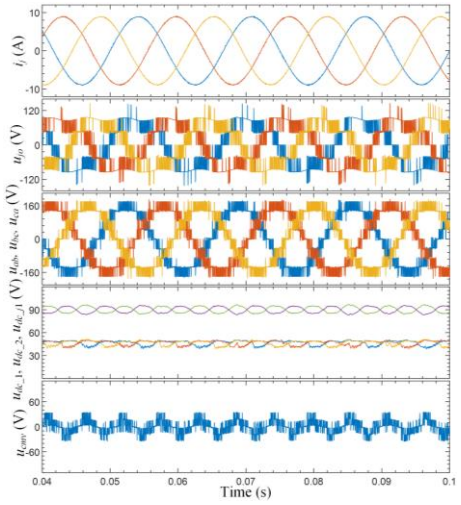
Description	Variable	Simulation	Experiment
Load inductance	L	4 mH	4 mH
Load resistance	R	10 Ω	10 Ω
DC-link capacitance	C	240 μF	240 μF
H-bridge capacitance	C_1	200 μF	200 μF
DC-link voltage	U_{dc}	180 V	180 V
H-bridge dc voltage (7-level)	u_{dc_j1}	45 V	45 V
H-bridge dc voltage (9-level)	u_{dc_j1}	30 V	30 V
Sampling frequency	f_s	40 kHz	40 kHz
Dead time	T_d	-	1 μs
Fundamental frequency	f	60 Hz	60 Hz

Fig. 7(a) and (b) are the steady-state performance of the ST-MPC with and without CMV reduction, respectively. As it can be seen, the phase voltage has 7 levels and the line voltage has 9 levels, the phase voltages with CMV reduction have fewer

switching actions compared with phase voltages without CMV reduction. In addition, the reduction of CMV can lead to an obvious increase on the dc capacitor voltage fluctuation, which indicates the trade-off between CMV reduction and the dc capacitor voltage balancing. This can also be interpreted as: part of the CMV can be utilized for dc capacitor voltage regulating, the dc voltage regulation and the CMV reduction will finally reach a compromise.



(a)



(b)

Fig. 7. Steady-state performance (7-level). (a) ST-MPC without CMV reduction (λ=0, ε=0.03%). (b) ST-MPC with CMV reduction (λ=0.023, ε=5%)

Fig. 8 shows the transient-state performance of the ST-MPC, where the reference current drops to half at 0.221 s and restores at 0.254 s. As it can be seen, the dc capacitor voltages are well maintained and the dynamic response is very fast. It can also be noticed that the fast-dynamic is secured by the rapid movement of the reference vector in complex plane, which is manifested by the line voltage surge at the changing time instant. It is noteworthy that since the transition time is intentionally set to the peak value point, this voltage surge reaches the maximum point that it can be, which is the extreme scenario. In addition, this voltage spike can be mitigated by selecting the adjacent vector of the reference vector, but the dynamic response will be compromised.

Figs. 9 and 10 illustrate the comparison of the current THD performance and average switching frequency versus current amplitude under different power factors (PFs): 0.99 and 0.55, the average switching frequency is calculated by averaging the real switching frequency of each power switch. When applying the parameters in Table IV, PF=0.99, when load resistance R=1 Ω, then PF=0.55. As exhibited, the MC-MPC and ST-MPC under 20 kHz sampling frequency are almost the same, the current THD of the ST-MPC under 40 kHz sampling frequency is superior to that of the MC-MPC under 20 kHz sampling frequency, but the average switching frequency is higher. It is also noteworthy that although the switching frequency of silicon IGBTs is usually kept at 1 kHz to 2 kHz for high power multilevel converters [37], the switching frequency of SiC MOSFETs can be as high as 4 kHz to 40 kHz with proper busbar and cooling system design [38]-[41].

The power loss analysis is performed using the method described in [41]. Figs. 11 and 12 show the power loss breakdown and efficiency comparison between ST-MPC and MC-MPC by using the loss data of a SiC MOSFET device (C2M0160120D, 1.2 kV, 19 A, 160 mΩ from CREE/Wolfspeed) [42], which is also used in the experimental prototype. As it can be seen from Fig. 11, the conduction loss contributes to the vast majority of the loss while the switching loss is very low, this is also the reason that the efficiency curves in Fig. 12 are almost the same under both 40 kHz and 20 kHz sampling frequency, although the average switching frequency doubles. Since the adopted MOSFET has a comparatively high on-state resistance (approximately 160 mΩ), the conduction loss is relatively high and the efficiency is not very high. In addition, because of the smaller resistance under PF=0.55 scenario, the converter output voltage is smaller and thus the output voltage level is less, which leads to a different efficiency curve.

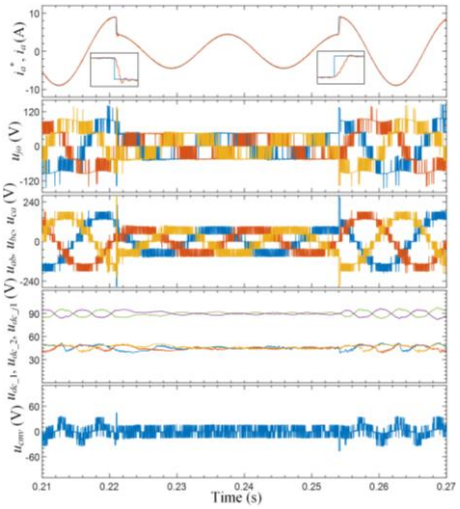
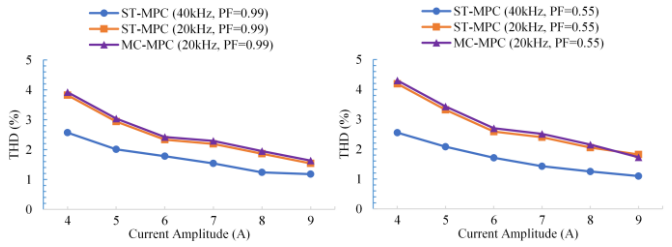
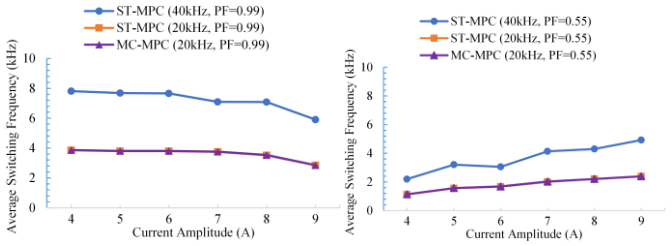


Fig. 8. Transient-state performance of the ST-MPC (7-level).



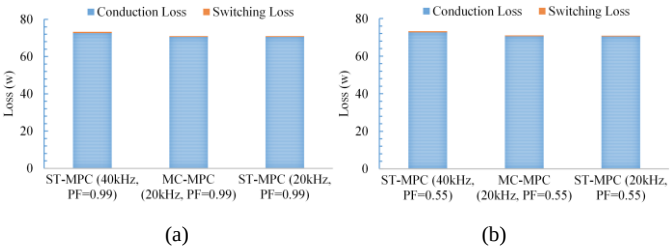
(a) (b)

Fig. 9. Current THD of the ST-MPC and MC-MPC (7-level). (a) PF=0.99. (b) PF=0.55.



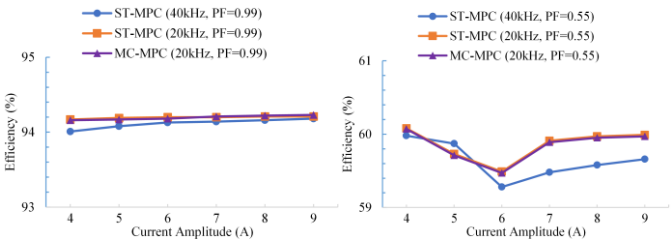
(a) (b)

Fig. 10. Average switching frequency of the ST-MPC and MC-MPC (7-level). (a) PF=0.99. (b) PF=0.55.



(a) (b)

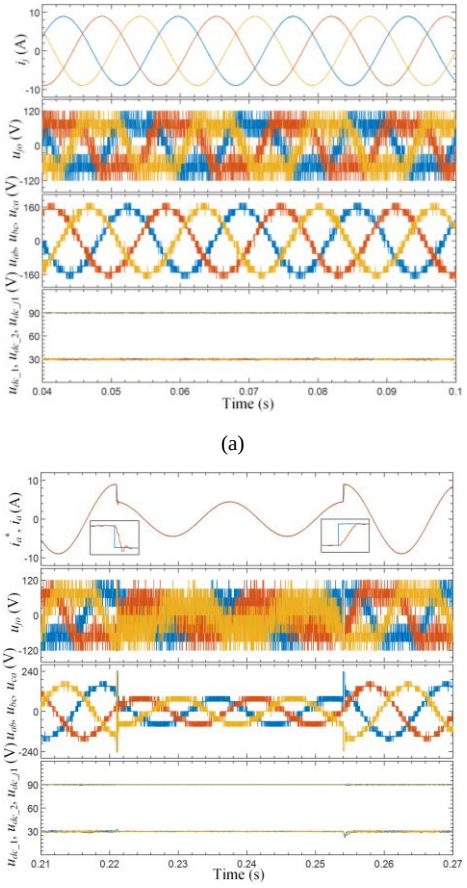
Fig. 11. Power loss comparison (7-level). (a) PF=0.99. (b) PF=0.55.



(a) (b)

Fig. 12. Efficiency comparison (7-level). (a) PF=0.99. (b) PF=0.55.

Fig. 13(a) and (b) are the 9-level operation of the hybrid ANPC-H converter under the proposed ST-MPC strategy at the steady- and transient-state, respectively. As it can be seen, similar to the 7-level operation in Figs. 7 and 8, the dc capacitor voltages are also well regulated and the dynamic response is very fast too. This indicates that the proposed ST-MPC strategy is applicable for both 7- and 9-level operation of the hybrid ANPC-H converter. Fig. 14 shows the current THD and average switching frequency of the ST-MPC under 9-level operation. It is obvious that the THD is lower compared with 7-level scenario. In Fig. 15, the operation limitation of the hybrid ANPC-H converter with the proposed ST-MPC method is obtained using simulation study. The modulation index, which is defined as the ratio of the output voltage amplitude to the virtual dc-link voltage $3U_{dc}/4$, is used as the horizontal axis, while the vertical axis is the power factor. For all the operation circumstances enclosed by the solid line, the voltages across the dc capacitors can be well regulated to their reference values. While for the conditions beyond the solid line, the voltages of the dc capacitors drift away from their reference values. This result is in accordance with the analysis presented in [10] and [12]. As the operation limitation is the inherent characteristic of this kind of three-level converter with cascaded floating H-bridge topology, the 9-level scenario is expected to have the same limitation as the 7-level scenario.



(a)

(b)

Fig. 13. Steady- and transient-state performance of the ST-MPC (9-level). (a) Steady-state performance. (b) Transient-state performance.

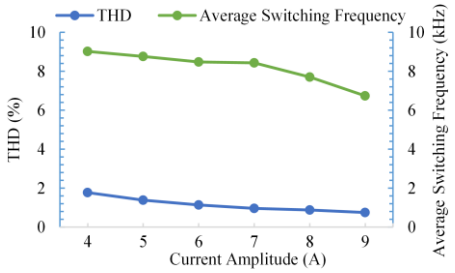


Fig. 14. Current THD performance and average switching frequency of the ST-MPC (9-level).

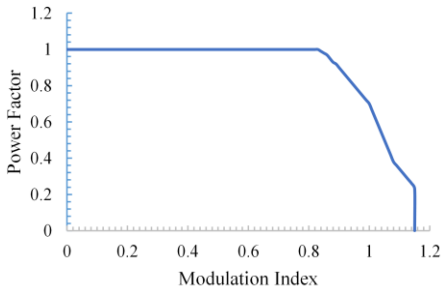


Fig. 15. Operation limitation of the hybrid ANPC-H converter at 7-level operation using the proposed ST-MPC.

V. Experimental Results

To further verify the proposed ST-MPC strategy by real-world experiment, an all-SiC hybrid ANPC-H converter prototype is constructed in the laboratory by using SiC MOSFET (C2M0160120D) from CREE/Wolfspeed. The parameters of the system are also given in Table IV. Fig. 16 demonstrates the experimental setup of the hybrid ANPC-H converter. The dSpace MicroLabBox is used for control and Intel Max-10 FPGA is adopted for gating signal generation. The gating signals are transferred through optic fibers form FPGA to gate driver in to enhance the immunity to the electromagnetic interference (EMI). The RL load and the dc source that feeding the dc-link are not exhibited in the picture.

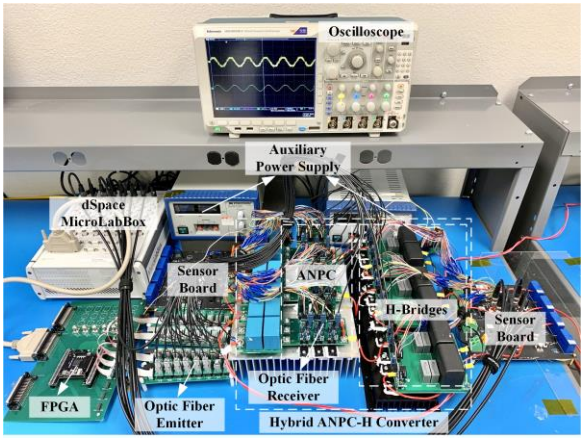


Fig. 16. Experimental setup of the hybrid ANPC-H converter prototype.

Fig. 17 demonstrates the comparison of the turnaround time among the three methods, where the turnaround time is measured in dSpace using the real-time mode. Apparently, the C-MPC consumes significantly longer time than the other two approaches, which is impossible to implement in practical conditions. As it can be seen, the MC-MPC consumes 32 μs to complete one control iteration, while the ST-MPC only takes 16 μs to finish the control algorithm. Therefore, the MC-MPC can theoretically be implemented at sampling frequency no higher than 30 kHz, while the proposed ST-MPC can theoretically be performed at maximum sampling frequency of 60 kHz. Fig. 18 (a) exhibits the experimental waveforms of the MC-MPC with a sampling frequency of 20 kHz. As it can be seen, the switching frequency is much lower compared with the ST-MPC waveforms in Fig. 18(b). Fig. 19 shows the steady-state performance with and without CMV reduction, while Fig. 20 demonstrates the transient-state performance, both under 7-level operation. As it can be seen from Fig. 19, the dc voltages are well regulated and there is an obvious dc voltage fluctuation increase when CMV reduction is applied, which is in accordance with the simulation. As it can be seen from Fig. 20, the dynamic response is fast. These results are in consistence with the simulation results. Fig. 21 exhibits the 9-level operation of the hybrid ANPC-H converter. As it can be seen, the dc capacitor voltages are also well regulated and the dynamic response is very fast.

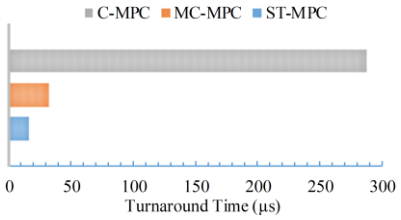
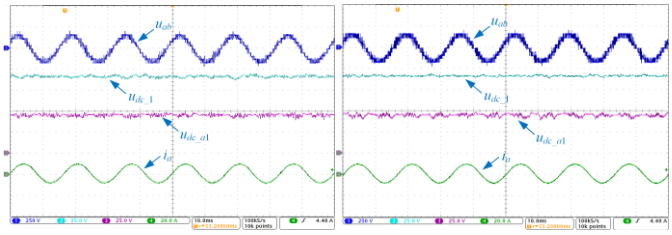
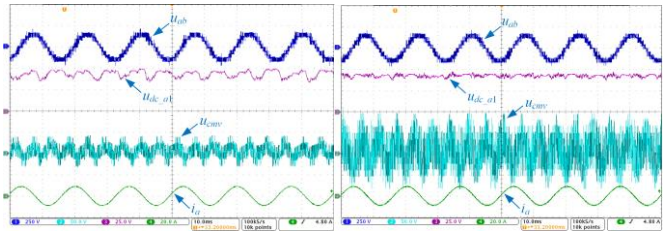


Fig. 17. Turnaround time comparison (7-level).



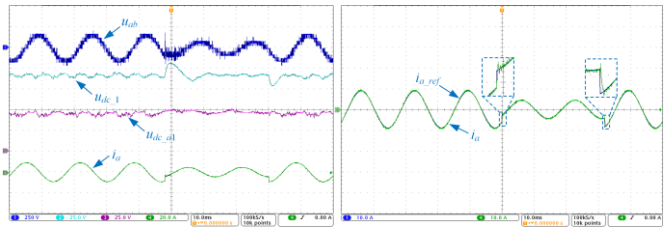
(a) (b)

Fig. 18. Steady-state performance of MC-MPC and ST-MPC (7-level, without CMV reduction). (a) MC-MPC. (b) ST-MPC.



(a) (b)

Fig. 19. Steady-state performance of the ST-MPC (7-level). (a) With CMV reduction. (b) Without CMV reduction.

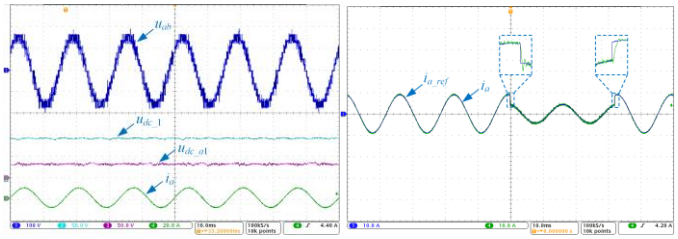


(a) (b)

Fig. 20. Transient-state performance of the ST-MPC (7-level). (a) Transient-state performance. (b) Reference and actual current.

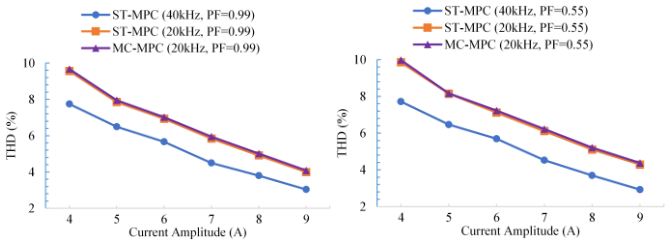
Fig. 22 shows the comparison of the current THD under different PFs. As it can be seen, the current THD of the ST-

MPC under 40 kHz sampling frequency is much better that of the ST-MPC and MC-MPC under 20 kHz sampling frequency, while the THD of the ST-MPC and MC-MPC are almost the same. This THD reduction is mainly resulted by the doubled sampling frequency used by ST-MPC, which is enabled by the high computational efficiency of the proposed ST-MPC.



(a) (b)

Fig. 21. Steady- and transient-state performance of the ST-MPC (9-level). (a) Steady-state performance. (b) Transient-state performance.



(a) (b)

Fig. 22. Current THD performance of the ST-MPC and MC-MPC (7-level). (a) PF=0.99. (b) PF=0.55.

VI. Conclusion

This paper proposes an ST-MPC strategy for a hybrid ANPC-H converter. The first stage of the proposed ST-MPC is to accomplish the optimal voltage vector selection by geometrical positioning in the complex plane, which is realized by simple coordinate transformation and rotation, while the second stage selects the best switching state that can balance the dc capacitor voltages and reduce the CMV. The computational efficiency is significantly improved compared with the C-MPC and the best current tracking is secured by neglecting weighting factor for dc capacitor voltage balancing. In addition, the geometrical positioning approach in the first stage is generic for an arbitrary multilevel converter with *N*-level output, thus, this proposed ST-MPC can be applied for both 7- and 9-level operation of the hybrid ANPC-H converter under different dc voltage ratios. Finally, both simulation and experimental results performed on an all-SiC hybrid ANPC-H converter prototype validate the feasibility and effectiveness of the proposed control strategy.

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