

# Epitaxial Dirac Semimetal Vertical Heterostructures for Advanced Device Architectures

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Exploiting the extraordinary transport and optical properties of three-dimensional topological semimetals for device applications requires epitaxial integration with semiconductors to carefully control carrier transport, yet no studies have established heteroepitaxy on top of any topological semimetals to date. Here, we demonstrate a novel approach toward fabricating heterostructures by epitaxially incorporating the Dirac semimetal  $\text{Cd}_3\text{As}_2$  between  $\text{Zn}_x\text{Cd}_{1-x}\text{Te}$  and  $\text{CdTe}$  layers via molecular beam epitaxy on  $\text{GaAs}$  (001) substrates. Our approach utilizes the higher energy (001) surface of  $\text{Cd}_3\text{As}_2$  to stabilize two-dimensional epitaxy of zinc blende semiconductors. To demonstrate the impact heterostructure formation offers to device performance, we fabricate an all-epitaxial, barrier-type vertical photodetector that accesses a different carrier separation mechanism than previously reported non-epitaxial junctions and consequently exhibits significantly reduced dark currents. Our results highlight the important role that epitaxial integration can play in accessing advanced architectures for topological semimetal-based devices.

## 1. Introduction

The entanglement and topological properties found in quantum materials have the potential to revolutionize optoelectronic and spintronic technologies.<sup>[1]</sup> Three dimensional (3D) topological semimetals are intriguing quantum materials for controlling the interplay between electrical potential, current, carrier concentrations and spin, but device development has lagged behind fundamental studies of quantum phenomena in these materials. Decades ago, when semiconductors faced a similar juncture, epitaxial growth of heterostructures proved critical for making the leap to high performance devices. The conceptualization and initial demonstration of semiconductor heterostructures eventually earned the 2000 Nobel Prize in Physics. Intentionally designed heterostructures will likely also play a dominant role in future quantum materials-based applications if they can be properly synthesized. To this end, epitaxial integration with semiconductors is a necessary next step, but it has largely not been demonstrated or developed to date.

Dirac and Weyl topological semimetals are characterized by the existence of bulk and surface states with linear band dispersions that touch near the Fermi level. Such electronic structures support high electron mobilities, ultra-fast carrier recombination times and strong broadband absorption that are advantageous for a number of applications, such as high-speed transistors, photodetectors and thermoelectrics.<sup>[2,3]</sup> The opposite chirality of Weyl nodes that exist in cases where inversion or time reversal symmetry is broken can also benefit spintronic applications that control the spin degrees of freedom.<sup>[4]</sup> Simple devices, ranging from metal contacts deposited on bulk crystals or nanostructures to oxide, polymer or two dimensional (2D) layers deposited on a single epitaxial semimetal layer, have already been demonstrated for a small subset of topological semimetals, including Cd<sub>3</sub>As<sub>2</sub> and TaAs.<sup>[5-12]</sup> However, these basic device geometries do not impart the functionality and charge control achieved in even the most simple semiconductor devices. For example, the dark currents remain high in semimetal photodetectors, making them difficult to operate in the desired reverse bias direction.<sup>[13]</sup> Suppression of dark current and realization of high reverse-bias responsivity requires advanced designs inspired by conventional photodetectors that utilize *vertical* architectures in which monolithic growth does not end at the semimetal. To date, heteroepitaxy has not been demonstrated on top Dirac or Weyl semimetals.

Here, we demonstrate epitaxial growth of CdTe/Cd<sub>3</sub>As<sub>2</sub>/Zn<sub>x</sub>Cd<sub>1-x</sub>Te double heterostructures on GaAs (001) substrates by molecular beam epitaxy (MBE). We show that selection of the

Cd<sub>3</sub>As<sub>2</sub> crystallographic orientation is essential for controlling the quality of the top CdTe layer. As proof that such heteroepitaxial structures can provide access to a wider range of device architectures, we present a Cd<sub>3</sub>As<sub>2</sub>-based vertical p-B-n (p-type contact/Barrier/n-type light absorber) barrier photodiode. This epitaxial heterostructure design enables additional control over majority and minority carrier transport that is not available in the simple metal-insulator-semimetal or Schottky junctions demonstrated to date. Our results provide a blueprint for fabricating vertical functional structures with high quality epitaxial materials and interfaces that will advance the state of the art in topological semimetal devices.

## 2. Results

### 2.1. Heteroepitaxy on Cd<sub>3</sub>As<sub>2</sub>

Cd<sub>3</sub>As<sub>2</sub> is one of the most studied 3D topological semimetal material systems. Early investigations of its properties were performed on bulk crystals and nanostructures, but recent success in epitaxial growth on a variety of substrates, including GaSb, GaAs, CdTe and mica, has opened the door for scalably fabricating devices.<sup>[14-19]</sup> Cd<sub>3</sub>As<sub>2</sub> has a tetragonal crystal structure, and the best epitaxy has been achieved by aligning its lowest energy (112) surface to the (111) surface of zinc blende semiconductor substrates and buffer layers.<sup>[14,15,17,20]</sup> The next major synthesis challenge for realizing practical, high-performance devices is epitaxially integrating it into heterostructures by growing semiconductors on top of Cd<sub>3</sub>As<sub>2</sub>.

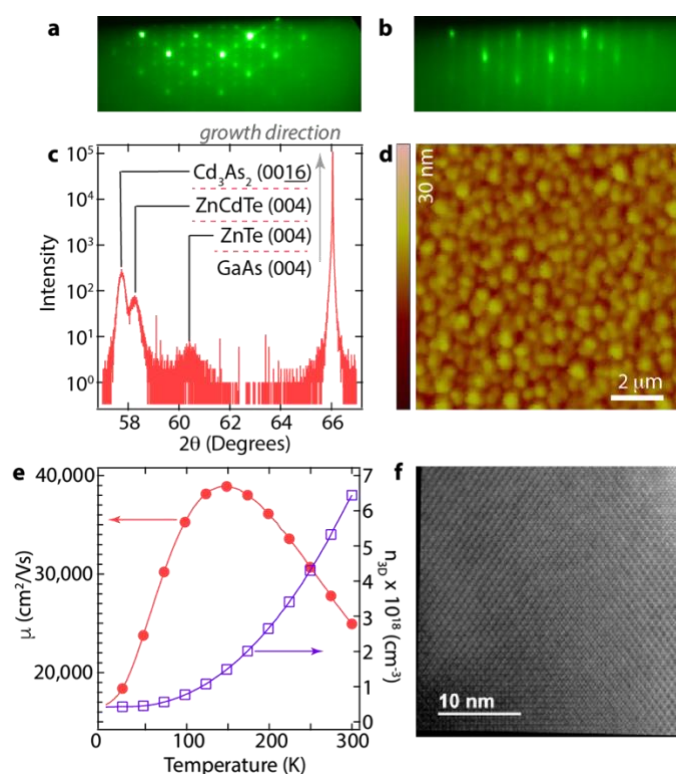
It is well known that material A can grow via a 2D mode on material B if the surface energy of A is lower than that of B. By the same argument, material B then will not readily grow on material A in a 2D mode, resulting in 3D growth modes that can introduce defects and even inhibit conformal double heterostructure formation. This complication is typically addressed in semiconductors by reducing the growth temperature to kinetically limit adatom mobility and suppress 3D islanding or by using surfactants to alter the surface energy. However, several factors restrict the use of these approaches for growth on Cd<sub>3</sub>As<sub>2</sub>. First, the multitude of mismatches in crystal structure, surface energy, lattice constant and bonding environments between Cd<sub>3</sub>As<sub>2</sub> and most conventional semiconductors promotes a 3D growth mode.<sup>[21]</sup> Second, the high vapor pressure of Cd<sub>3</sub>As<sub>2</sub> already requires growth temperatures below 200 °C, limiting the use of temperature and surfactants to achieve the desired 2D mode.

Here, we take a different approach to promoting 2D growth of semiconductors on Cd<sub>3</sub>As<sub>2</sub>: selecting the crystallographic orientation to reduce the surface energy mismatch. By accessing the higher energy Cd<sub>3</sub>As<sub>2</sub> (001) surface, rather than the (112) surface, we aim to reduce the surface energy mismatch with many zinc blende semiconductors and stabilize conformal growth on top of Cd<sub>3</sub>As<sub>2</sub>, without having to modify the growth temperature.

(001) oriented Cd<sub>3</sub>As<sub>2</sub> growth was previously reported on GaSb (001) substrates, although its higher surface energy required an InAs wetting layer for improved nucleation.<sup>[22]</sup> The high temperatures required for III-V materials are also prohibitive for growth on Cd<sub>3</sub>As<sub>2</sub>. Instead, we form the heterostructure with Zn<sub>x</sub>Cd<sub>1-x</sub>Te alloys. It is lattice-matched to Cd<sub>3</sub>As<sub>2</sub> at  $x = 0.42$  and can be grown directly on GaAs (111) and GaAs (001) as a buffer to mediate strain relaxation prior to Cd<sub>3</sub>As<sub>2</sub> growth.<sup>[17]</sup> Thus, Zn<sub>x</sub>Cd<sub>1-x</sub>Te provides a bridge to integrating Cd<sub>3</sub>As<sub>2</sub> into devices fabricated on large area GaAs substrates, and it has a bandgap that is large enough to effectively isolate electrical transport within the Cd<sub>3</sub>As<sub>2</sub> epilayer. CdTe (i.e.  $x = 0$ ) can additionally be grown at very low temperatures ( $< 200$  °C), making it a good candidate for heteroepitaxy on Cd<sub>3</sub>As<sub>2</sub>.

A paramount requirement for implementing this integration approach is that Cd<sub>3</sub>As<sub>2</sub> must be epitaxially grown in the higher energy (001) orientation without loss of performance compared to (112) oriented layers. The spotty reflection high energy electron diffraction (RHEED) patterns measured during Cd<sub>3</sub>As<sub>2</sub> growth initiation on nearly lattice-matched Zn<sub>x</sub>Cd<sub>1-x</sub>Te/GaAs (001) structures indicate that nucleation occurs via 3D islanding (Figure 1a). The RHEED patterns then turn streaky after several tens of nanometers, suggesting the epilayer smooths out to some degree as the growth proceeds (Figure 1b). X-ray diffraction (XRD) measurements (Figure 1c) confirm that the Cd<sub>3</sub>As<sub>2</sub> epilayers are also oriented in the (001) direction. The resulting morphology (Figure 1d) resembles coalesced spheres and is similar to the previous report of Cd<sub>3</sub>As<sub>2</sub> (001) growth on GaSb substrates.<sup>[22]</sup> However, the room temperature electron mobilities of our Cd<sub>3</sub>As<sub>2</sub> bulk epilayers (~300 nm thick) are nearly 25,000 cm<sup>2</sup>/Vs and are comparable to the highest reported values of (112) oriented as-grown Cd<sub>3</sub>As<sub>2</sub> epilayers (Figure 1e).<sup>[14,17]</sup> Variable temperature measurements show that the electron mobility increases to above 38,000 cm<sup>2</sup>/Vs around 150 K before decreasing at lower temperatures. This temperature dependence is similar to unpassivated bulk Cd<sub>3</sub>As<sub>2</sub> (112) epilayers grown on GaAs substrates reported in the literature, where the subsequent drop in mobility at low temperatures was attributed to an increased contribution from low mobility

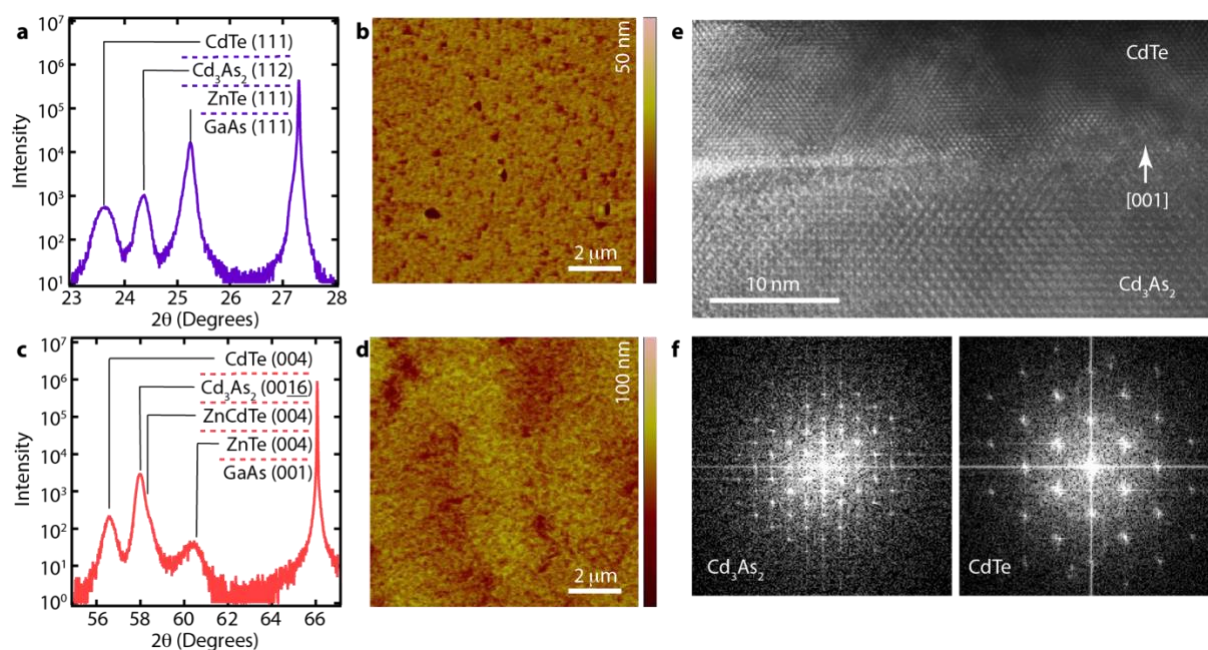
carriers that are also present.<sup>[23]</sup> The correspondence of carrier and mobility trends in our (001)-oriented epilayers with previously reported (112)-oriented films indicates that growing Cd<sub>3</sub>As<sub>2</sub> in the (001) orientation does not produce a trade-off in its transport properties. As many devices operate near room temperature, the low temperature mobility behavior is unlikely to be a detriment to device applications. Cross-sectional transmission electron microscopy (TEM) images (Figure 1f) otherwise confirm that the epilayers are single crystalline with an (001) orientation.



**Figure 1.** Cd<sub>3</sub>As<sub>2</sub> epitaxy in the (001) orientation. a) The spotty RHEED pattern of Cd<sub>3</sub>As<sub>2</sub> after 5 nm of growth on a Zn<sub>x</sub>Cd<sub>1-x</sub>Te/ZnTe/GaAs substrate structure reveals that Cd<sub>3</sub>As<sub>2</sub> growth nucleates in a 3D mode. The measurement was taken along the GaAs (110) direction. b) The RHEED pattern of the same Cd<sub>3</sub>As<sub>2</sub> epilayer after 100 nm of growth shows that the epilayer becomes smoother as the growth proceeds. c) XRD measurements of the Cd<sub>3</sub>As<sub>2</sub>/Zn<sub>x</sub>Cd<sub>1-x</sub>Te/ZnTe/GaAs substrate structure confirm that all layers are in the (001) orientation. d) AFM shows that the Cd<sub>3</sub>As<sub>2</sub> epilayer resembles coalesced islands and remains structured after 300 nm of growth. e) variable temperature electron concentration and mobility measurements of the Cd<sub>3</sub>As<sub>2</sub> layer indicate the rough growth does not compromise the transport properties, as the room temperature mobility is amongst the highest reported for as-

grown  $\text{Cd}_3\text{As}_2$  epilayers. f) The high-resolution TEM image of the  $\text{Cd}_3\text{As}_2$  epilayer confirms it is single crystalline.

To demonstrate semiconductor epitaxy on  $\text{Cd}_3\text{As}_2$ , we selected CdTe instead of a  $\text{Zn}_x\text{Cd}_{1-x}\text{Te}$  alloy to distinguish this layer in XRD and maintain a low growth temperature. Despite having a rougher surface,  $\text{Cd}_3\text{As}_2$  (001) is much better at promoting subsequent conformal CdTe heteroepitaxy than  $\text{Cd}_3\text{As}_2$  (112). XRD measurements (Figure 2a) indicate that CdTe (111) grows on  $\text{Cd}_3\text{As}_2$  (112), but atomic force microscopy (AFM) images of 20 nm thick CdTe films (Figure 2b) reveal a high density of pinholes. In stark contrast, XRD measurements (Figure 2c) confirm that CdTe epilayers can be grown in the (001) orientation on  $\text{Cd}_3\text{As}_2$  (001), but AFM images (Figure 2d) reveal that CdTe films as thin as 10 nm thick do not have the sharply defined pinholes observed in the (111) epilayers. High resolution (HR) TEM images of the CdTe/ $\text{Cd}_3\text{As}_2$  (001) heterostructure and their fast Fourier transforms (FFTs) reveal single crystalline layers on either side of an abrupt interface (Figures 2e,f), with the CdTe layer epitaxially aligned to the underlying  $\text{Cd}_3\text{As}_2$  layer. These results can be explained in the context of surface energy differences between  $\text{Cd}_3\text{As}_2$  and CdTe in these two orientations, where the higher energy  $\text{Cd}_3\text{As}_2$  (001) surfaces stabilize 2D growth of pinhole-free CdTe at thicknesses below 10 nm. An added benefit is that the (001) orientation is more compatible with existing manufacturing.



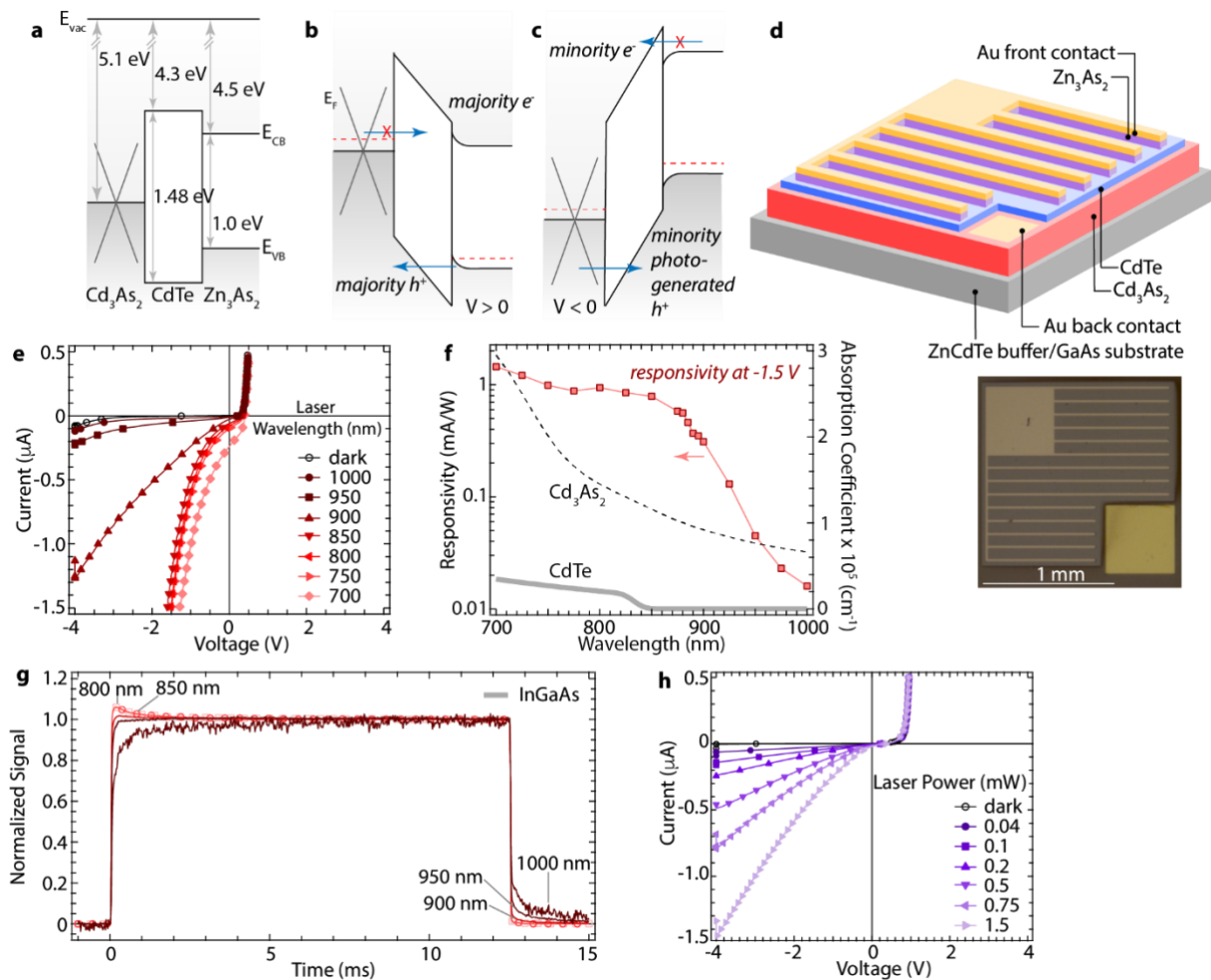
**Figure 2.** CdTe heteroepitaxy on Cd<sub>3</sub>As<sub>2</sub>. a) The XRD spectrum of a CdTe/Cd<sub>3</sub>As<sub>2</sub>/ZnTe/GaAs (111) structure show that CdTe (111) grows on Cd<sub>3</sub>As<sub>2</sub> (112). b) AFM image of a 20 nm CdTe (111) film grown in this manner reveals that it contains a high density of pinholes. c) The XRD spectrum of a corresponding CdTe/Cd<sub>3</sub>As<sub>2</sub>/Zn<sub>x</sub>Cd<sub>1-x</sub>Te/ZnTe/GaAs (001) sample confirms that CdTe (001) grows on Cd<sub>3</sub>As<sub>2</sub> (001). d) AFM image shows that 10 nm thin epilayers of CdTe (001) conformally cover Cd<sub>3</sub>As<sub>2</sub> (001) without pinholes. The e) HRTEM image and (F) FFTs of the CdTe/Cd<sub>3</sub>As<sub>2</sub> interface grown in the (001) orientation reveal that it is abrupt and the material on either side is single crystalline.

## 2.2. Vertical Photodetector

The ability to integrate Cd<sub>3</sub>As<sub>2</sub> into vertical heterostructures on large area substrates opens the door to realizing a wide range of device designs. To illustrate how our heteroepitaxial growth approach might be used in such ways, we demonstrate an epitaxial vertical photodetector. The appeal of using Cd<sub>3</sub>As<sub>2</sub> is that the Dirac band touching nodes allow for broadband light absorption, while its 3D structure enhances light absorption efficiency well beyond single layer graphene.<sup>[5,24]</sup> The ultra-short carrier recombination times (ps) and high electron mobilities within Cd<sub>3</sub>As<sub>2</sub> also hold promise for fast photodetector response.<sup>[6,25]</sup> The main challenge has been to implement a device design that can take full advantage of these properties. Initial photodetectors were demonstrated in simple metal-Cd<sub>3</sub>As<sub>2</sub> nanostructure-metal structures that principally operate through the photothermoelectric effect.<sup>[6,7]</sup> More recently, detectors fabricated from Cd<sub>3</sub>As<sub>2</sub>-organic, 2D and oxide junctions have been reported but exhibit weak rectification.<sup>[8,11]</sup> Notably, none of these designs allow the photodetector to be operated in reverse bias with low dark currents, as is possible in state-of-the-art p-i-n and barrier semiconductor devices.<sup>[13,26]</sup> Combining dark current control with the elegance of vertical carrier separation requires asymmetric heterojunctions designed to prevent majority carrier flow. As found in the case of graphene, creating a p-n junction directly from a semimetal is difficult, and Schottky junctions are often used.<sup>[27]</sup> Alternative approaches are needed to further improve semimetal-based photodetector performance.  
[13,26,27]

Building on our heteroepitaxial growth capabilities described above, we demonstrate a vertical photodetector design that enables carrier separation via a barrier type p-B-n operating principle.<sup>[28]</sup> Barrier device structures, used in HgCdTe photodetectors today, manage dark

current by introducing a high energy barrier to majority carrier flow from the light absorbing layer. The barrier layer simultaneously presents little obstacle to photogenerated minority carrier flow in reverse bias. Unlike a p-i-n junction, barrier type devices generally do not intentionally include a depletion region, which helps to suppress the dark current at zero and reverse biases. Such an approach is only possible with the ability to integrate materials selected for their band alignments across high-quality interfaces.



**Figure 3.** Vertical p-B-n barrier photodiode operational principles and performance. The band alignment of a p-B-n p-Zn<sub>3</sub>As<sub>2</sub>/CdTe/n-Cd<sub>3</sub>As<sub>2</sub> barrier diode under a) flat band, b) forward bias and c) reverse bias schematically show how the photodiode operates. d) top-down optical micrograph and 3D schematic of experimental photodiode. e) Dark and light IV curves, f) the photoreponse at -2V reverse bias, and g) temporal photoresponse of the photodiode measured at different wavelengths (constant power at 1 mW). The absorption coefficient of CdTe is displayed in panel f, while the temporal response of an InGaAs reference diode measured under 950 nm is also shown in panel g for comparison. h) Dark and light IV curves measured

under different laser powers (constant 900 nm wavelength) reveal the photodiode has a very low dark current and produces a strong photoresponse.

Our p-B-n device consists of p-Zn<sub>3</sub>As<sub>2</sub>/CdTe/n-Cd<sub>3</sub>As<sub>2</sub>, with n-Cd<sub>3</sub>As<sub>2</sub> acting as the light absorber and CdTe acting as an electron barrier. Like Cd<sub>3</sub>As<sub>2</sub>, Zn<sub>3</sub>As<sub>2</sub> has a tetragonal crystal structure but is a semiconductor with a 1.0 eV bandgap.<sup>[29,30]</sup> Our as-grown Zn<sub>3</sub>As<sub>2</sub> epilayers have hole concentrations  $\sim 5 \times 10^{18} \text{ cm}^{-3}$ , determined through Hall measurements.

Capacitance-voltage (C-V) measurements, detailed in the supplementary information, indicate this heterostructure has the flat-band alignment presented in Figure 3a. Ideally, a p-B-n structure would have zero valence band offsets between all three layers to freely pass minority holes photogenerated in the n-Cd<sub>3</sub>As<sub>2</sub> layer. However, undoped CdTe introduces a non-ideal valence band offset (Figure 3a). Schematics of the basic behavior of this junction are presented in Figures 3b,c. Given the higher carrier concentration and dielectric constant of Cd<sub>3</sub>As<sub>2</sub> ( $6 \times 10^{18} \text{ cm}^{-3}$  and 36) compared to Zn<sub>3</sub>As<sub>2</sub> ( $5 \times 10^{18} \text{ cm}^{-3}$  and 11), we expect the applied voltage to drop mainly over the CdTe and p-Zn<sub>3</sub>As<sub>2</sub> semiconductor layers so that much less band bending occurs in the Cd<sub>3</sub>As<sub>2</sub>.<sup>[31,32]</sup> Under relatively small forward bias, a current arises from majority hole flow from the p-Zn<sub>3</sub>As<sub>2</sub> layer to the n-Cd<sub>3</sub>As<sub>2</sub>, while majority electrons in the Cd<sub>3</sub>As<sub>2</sub> are blocked by the larger conduction band discontinuity at the n-Cd<sub>3</sub>As<sub>2</sub>/CdTe interface. In reverse bias, the majority hole current from the p-Zn<sub>3</sub>As<sub>2</sub> is now suppressed by the electric field, while the very low minority carrier concentrations in both layers limit minority carrier flow, leading to low dark currents in the device, even up to high applied reverse bias voltages. Minority holes photogenerated in the n-Cd<sub>3</sub>As<sub>2</sub> layer, on the other hand, are driven by the electric field under reverse bias from the n-Cd<sub>3</sub>As<sub>2</sub> to the p-Zn<sub>3</sub>As<sub>2</sub> provided they can traverse the CdTe valence band barrier via thermionic emission or tunneling. Thus, a photocurrent can be generated over a wide reverse bias range (-1 to -4 V).

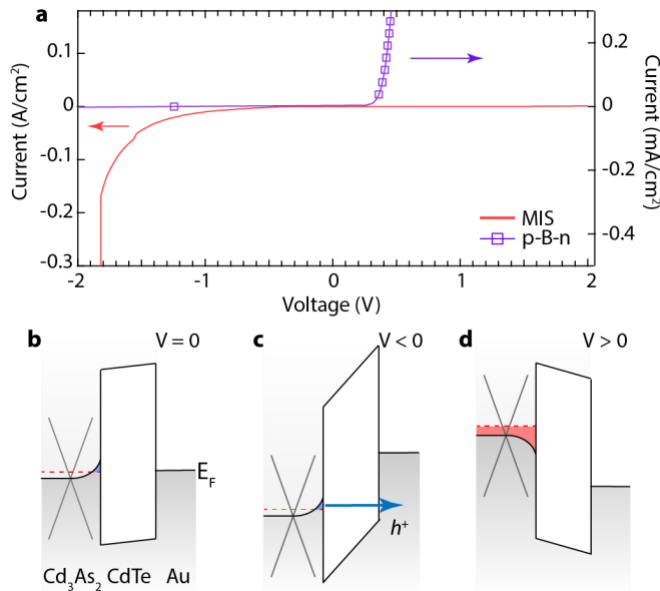
The photodetector, schematically represented in Figure 3d, was grown on a (001)-oriented Zn<sub>x</sub>Cd<sub>1-x</sub>Te/GaAs substrate platform. The p-Zn<sub>3</sub>As<sub>2</sub> has further been etched away from the regions between the front Au metal contacts such that light is incident directly on the CdTe layer. The room temperature dark current-voltage (I-V) curve of this device, shown in Figure 3e, exhibits rectifying behavior, where the forward current increases sharply above 0.5 V, but the dark current in reverse bias remains below 0.005  $\mu\text{A}$  out to -2 V and below 0.1  $\mu\text{A}$  out to -4 V. Light I-V curves measured under 1 mW photoexcitation over a range of near infrared

wavelengths, also displayed in Figure 3e, exhibit a sizeable photoresponse in reverse bias. Figure 3f shows the photoresponse measured at -1.5V reverse bias as a function of wavelength. At longer wavelengths, the responsivity strongly decreases with increasing wavelength, as photons are absorbed farther away from the CdTe/Cd<sub>3</sub>As<sub>2</sub> interface and the minority photogenerated holes are not as efficiently extracted (see supplementary information for complete absorption coefficient data). We note that the photoresponse measured at 1550 nm (not shown in Fig. 3) is approximately  $6 \times 10^{-5}$  mA/W because photogenerated hole collection is severely limited at this point. For photon wavelengths shorter than 850 nm, the rate of change in the responsivity with wavelength decreases. We attribute the behavior in this region to a competition between photocarrier generation in the Cd<sub>3</sub>As<sub>2</sub> layer and parasitic absorption and carrier recombination losses in the CdTe layer (see Figure 3f).

The photoresponse times, shown in Figure 3g, further confirm this picture of device operation. When minority holes are photogenerated close to the CdTe/Cd<sub>3</sub>As<sub>2</sub> junction with shorter wavelength photons, the photoresponse rise and fall times are on the order of 200-300  $\mu$ s. The small overshoot in the rise time in the photoresponse measured under 800 nm and 850 nm excitation has previously been attributed to space-charge effects in mid-IR quantum-well detectors.<sup>[33]</sup> A similar effect could occur in our p-B-n photodiode, where the fast photoinjection of carriers may cause a nonlinear response of the built-in field at the CdTe/Cd<sub>3</sub>As<sub>2</sub> interface. The response times are similar to that of a commercial InGaAs detector, shown in Figure 3g for comparison. Longer wavelength excitation results in slightly longer rise and fall tails, indicating holes are generated further away from the junction and require longer times to be extracted. Finally, power-dependent I-V curves measured with 900 nm excitation, displayed in Figure 3h, show that the photocurrent increases roughly linearly with increasing laser power, indicating that trap state filling does not substantially change device performance in this power range.

Overall, the performance of this p-B-n device exceeds that in Cd<sub>3</sub>As<sub>2</sub> photodiodes previously published in the literature, which are of smaller size but exhibit much larger dark currents of  $\mu$ A to mA at modest reverse biases of -2 V.<sup>[8,11]</sup> We note that the strong rectification of the p-B-n structure indicates that the main photocurrent generation mechanism is through field-assisted extraction of carriers across the barrier layer rather than through the photothermoelectric effect. The latter mechanism is present in photodetectors fabricated from freestanding Cd<sub>3</sub>As<sub>2</sub> nanostructures in which thermal gradients were generated.<sup>[6,7]</sup> Our p-B-n

photodetectors were more uniformly illuminated and are epitaxially grown on thermally conducting substrates, which would inhibit a significant thermal gradient from forming in the vertical carrier extraction direction.



**Figure 4.** Vertical MIS photodiode operational principles and performance. a) A comparison of the dark IV curves of the MIS and p-B-n diode structures. The p-B-n photodiode exhibits low dark current in reverse bias, while the MIS diode exhibits high dark current and breakdown near -2 V. Schematic band alignments of the MIS Cd<sub>3</sub>As<sub>2</sub>/CdTe/Au heterostructure under b)  $V = 0$ , c)  $V < 0$  and d)  $V > 0$  applied bias show how the increasing dark current is produced by band bending in the Cd<sub>3</sub>As<sub>2</sub> layer and accumulation of holes at the Cd<sub>3</sub>As<sub>2</sub>/CdTe interface.

Interestingly, the p-Zn<sub>3</sub>As<sub>2</sub> layer plays an important role in regulating the Fermi level in the Cd<sub>3</sub>As<sub>2</sub> layer. One well known effect in graphene/semiconductor Schottky diodes is that a voltage drop in the graphene layer substantially shifts the Fermi level through the small density of states near the Dirac node, leading to strong bias-dependent diode behavior.<sup>[27,34]</sup> A similar effect is expected in a Cd<sub>3</sub>As<sub>2</sub>/semiconductor/metal junction in which the semiconductor layer is not thick enough to accommodate all of the voltage drop.<sup>[5,35,36]</sup> To experimentally test this hypothesis, we fabricated a photodiode with a similar structure to that in Figure 3d but without the p-Zn<sub>3</sub>As<sub>2</sub> layer, creating a Cd<sub>3</sub>As<sub>2</sub>/CdTe/Au metal-insulator-

semiconductor (MIS) device. The dark I-V curve, shown in Figure 4a, is different than that of the p-B-n photodiode. Strikingly, the dark current increases substantially in reverse bias. This behavior can be explained by band bending that is now present in the Cd<sub>3</sub>As<sub>2</sub> layer (see supplementary information for details on its determination). Figure 4b shows the band bending at zero bias, where holes accumulate at the Cd<sub>3</sub>As<sub>2</sub>/CdTe interface. The band bending persists in reverse bias, leading to transport of accumulated holes through the CdTe layer and increasing dark current with increasing applied negative voltage (Figure 4c). Finally, breakdown in the MIS structure occurs at low reverse biases below -2 V (Figure 4a). From this result, we extract a breakdown field within the CdTe layer of  $\sim 6 \times 10^5$  V/cm, which is comparable to the reported values in the literature and further confirms the high quality of this thin heteroepitaxially-grown CdTe layer.<sup>[37]</sup> We note that no large increase is observed in the current under forward bias until breakdown (see Supplementary Information) because majority electrons are blocked from flowing from the Cd<sub>3</sub>As<sub>2</sub> through the CdTe layer (Figure 4d).

The comparatively low dark current in the p-B-n structure (also shown in Figure 4a) suggests that much less voltage drops across the Cd<sub>3</sub>As<sub>2</sub> in reverse bias when the p-Zn<sub>3</sub>As<sub>2</sub> layer is present. Instead, that voltage drops across the p-Zn<sub>3</sub>As<sub>2</sub> layer, preventing band bending and hole accumulation in the Cd<sub>3</sub>As<sub>2</sub>. Under reverse bias, where most photodiodes are operated, the p-Zn<sub>3</sub>As<sub>2</sub> therefore performs the important additional task of stabilizing the Fermi level in the Cd<sub>3</sub>As<sub>2</sub> conduction band and reducing the dark current.

### 3. Discussion

The heterostructure we have demonstrated here is novel among those used for Cd<sub>3</sub>As<sub>2</sub>-based photodetectors for three reasons. Primarily, it is the first all-epitaxial Cd<sub>3</sub>As<sub>2</sub>-based vertical heterojunction that is fundamentally capable of low dark currents when operated in reverse bias. This heterojunction is made possible by the ability to epitaxially grow thin (< 10 nm), high-quality semiconductor layers on Cd<sub>3</sub>As<sub>2</sub>. Implementation of a p-B-n structure over other diode designs, like a MIS structure or simple Schottky junction, also introduces a mechanism to pin the Fermi level within the Cd<sub>3</sub>As<sub>2</sub> conduction band under reverse bias and maintain low dark currents. Third, our use of the (001) crystallographic orientation, which enables heteroepitaxy on Cd<sub>3</sub>As<sub>2</sub>, also permits these heterostructures to be grown on large area GaAs (001) substrates, and therefore opens the door to integrating Cd<sub>3</sub>As<sub>2</sub> into more sophisticated devices fabricated using conventional manufacturing methods.

Several immediate opportunities exist for improving the performance of the heterojunction photodetectors demonstrated here. Notably, the photoresponsivity decreases for longer wavelengths, leading to poor mid-IR response. The primary cause is the lower absorption coefficient at lower photon energies (see Figure S4 in the supplementary information), which causes long wavelength photons to be absorbed further from the junction, on average. Reducing the electron concentration in the  $\text{Cd}_3\text{As}_2$  epilayer could extend the lifetime of the photogenerated minority holes and allow more to reach the  $\text{CdTe}/\text{Cd}_3\text{As}_2$  interface, where they will be swept across the barrier layer. As-grown  $\text{Cd}_3\text{As}_2$  is well-known to be highly n-type due to the formation of native point defects and identifying ways to lower the electron concentration will be an important step in this direction.

Additional strategies can be employed to increase the responsivity for all wavelengths. A transparent front contact could be added for better collection of photogenerated carriers, while an anti-reflective coating could be used in cases where detection of specific wavelengths is targeted. A barrier material with lower valence band offset with  $\text{Cd}_3\text{As}_2$  will also improve the flow of minority photogenerated holes to the p- $\text{Zn}_3\text{As}_2$  layer. Quaternary  $(\text{Hg,Cd,Zn})\text{Te}$  is one option for raising the valence band maximum without lowering the conduction band minimum substantially.<sup>[38]</sup> Finally, improving the  $\text{Zn}_x\text{Cd}_{1-x}\text{Te}$  buffer to utilize a metamorphic graded layer structure could help to control threading dislocation densities in the  $\text{Cd}_3\text{As}_2$  and  $\text{CdTe}$  epilayers and reduce recombination at defects.<sup>[39,40]</sup> However, this proof-of-concept demonstration shows that a range of high-performance devices are now possible with the ability to epitaxially grow thin semiconductors on  $\text{Cd}_3\text{As}_2$ .

While we have specifically focused on showing how heteroepitaxy of semiconductors on top of  $\text{Cd}_3\text{As}_2$  can enable photodetector device designs with improved performance, it should also serve as a vision for how such integration capabilities can advance topological semimetal-based devices more generally. The ability to epitaxially grow semiconductors on a variety of topological semimetal materials will expand the range of accessible device architectures to overcome limitations imposed by the semimetal. This will be particularly true of devices where the flow of majority and minority carriers must be carefully controlled. The specifics of the semiconductor and growth conditions will vary in each case, but the results presented here demonstrate the impact vertical epitaxial heterostructures can bring to topological semimetals.

#### 4. Conclusion

In summary, we have demonstrated the epitaxy of high-quality semiconductor layers on top of Cd<sub>3</sub>As<sub>2</sub> as a pathway to realizing advanced vertical device architectures with improved control over carrier transport. Two-dimensional CdTe epitaxy was stabilized on the (001) surface of Cd<sub>3</sub>As<sub>2</sub> epilayers grown on GaAs substrates. The utility of embedding topological semimetals in semiconductor structures to improve device performance was validated for a photodetector. Barrier-type structures formed with semiconductor barrier and p-layers regulate the flow of minority photogenerated holes out of the n-Cd<sub>3</sub>As<sub>2</sub> absorbing layer, resulting in low dark current and a strong photoresponse.

#### 5. Experimental Section/Methods

*Epitaxy and device fabrication.* Samples were grown in an interconnected MBE system with dedicated III-V and II-VI chambers. Cd<sub>3</sub>As<sub>2</sub> layers were grown from elemental Cd and As<sub>4</sub> sources with the same methods described in Reference 17. CdTe layers were grown from Cd and Te effusion cells with a 2:1 Te/Cd ratio. They were initially nucleated at a substrate temperature of 115°C before slowly increasing the temperature to 175-240 °C. Samples were annealed under an As overpressure at 250°C following growth. For device structures, Zn<sub>3</sub>As<sub>2</sub> was then grown at 250°C with a 2:1 As/Zn ratio. Photodetectors and devices for C-V measurements were fabricated with standard photolithography. Argon ion and wet chemical etching techniques were used to remove the telluride and arsenide layers, respectively. Au contacts were electroplated. The device structure and nominal layer thicknesses of the p-B-n photodetector are (in order from top to bottom): Au (1 micron)/Zn<sub>3</sub>As<sub>2</sub> (100 nm)/CdTe (10 nm)/Cd<sub>3</sub>As<sub>2</sub> (300 nm)/ZnCdTe (200 nm) /ZnTe (20 nm)/GaAs substrate. The Zn<sub>3</sub>As<sub>2</sub> was further chemically etched from in between the front Au contacts.

*Characterization.* Variable temperature Hall measurements were performed between 2-300 K in a Quantum Design Dynacool Physical properties measurement system. A current of 0.1 mA and a magnetic field of +/-0.1 T were used. Current-voltage and capacitance-voltage measurements were carried out by the Keithley 4200A-SCS parameter analyzer, and the frequency of the C-V measurement was fixed at 500 kHz. Cross-section samples for transmission electron microscopy (TEM) and scanning transmission electron microscopy (STEM) were prepared using a standard lift out technique, including in-situ deposition of a Pt

protective layer, in a FEI Nova NanoLab 200 dual beam focused ion beam (FIB) workstation. 30 kV Ga<sup>+</sup> ions were used for most of the preparation and the samples were finished off using < 5kV Ga<sup>+</sup> ions. The FIB damage was subsequently removed in a Fischione NanoMill using < 1 kV Ar<sup>+</sup> ions with the sample cooled using a liquid nitrogen cold stage. The samples were then examined in a FEI Tecnai F20 UltraTwin field emitting gun (FEG) STEM operated at 200 kV.

*Photodetector measurement.* The photo-I-V response was measured using a continuous wave laser focused to a 100- $\mu$ m diameter spot over the front contact grid. Curves were acquired in current-source, voltage-sense mode. Temporal waveforms used 0.1-mW or 2-mW peak laser power that was square-wave modulated using an acousto-optic modulator. The detector bias was held at -3.0 V and the output current was sunk in a 500 k $\Omega$  transimpedance amplifier and then digitized. A commercial InGaAs photodetector was measured in the same circuit at 950 nm excitation and 5  $\mu$ W of peak power.

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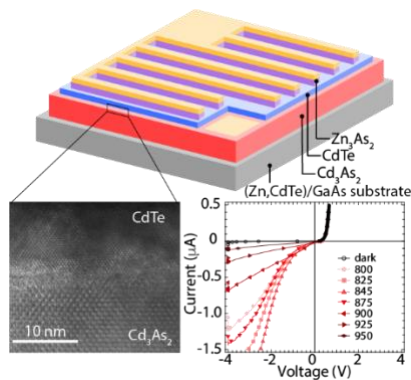
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Heteroepitaxy of semiconductors is demonstrated on top of the three-dimensional topological Dirac semimetal  $\text{Cd}_3\text{As}_2$ . The ability to incorporate topological semimetals within complex semiconductor device structures offers new pathways for advanced architectures with superior control of majority and minority carrier transport, as demonstrated for a barrier-type photodetector.

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### Epitaxial Dirac Semimetal Vertical Heterostructures for Advanced Device Architectures



## Supporting Information

### Epitaxial Dirac Semimetal Vertical Heterostructures for Advanced Device Architectures

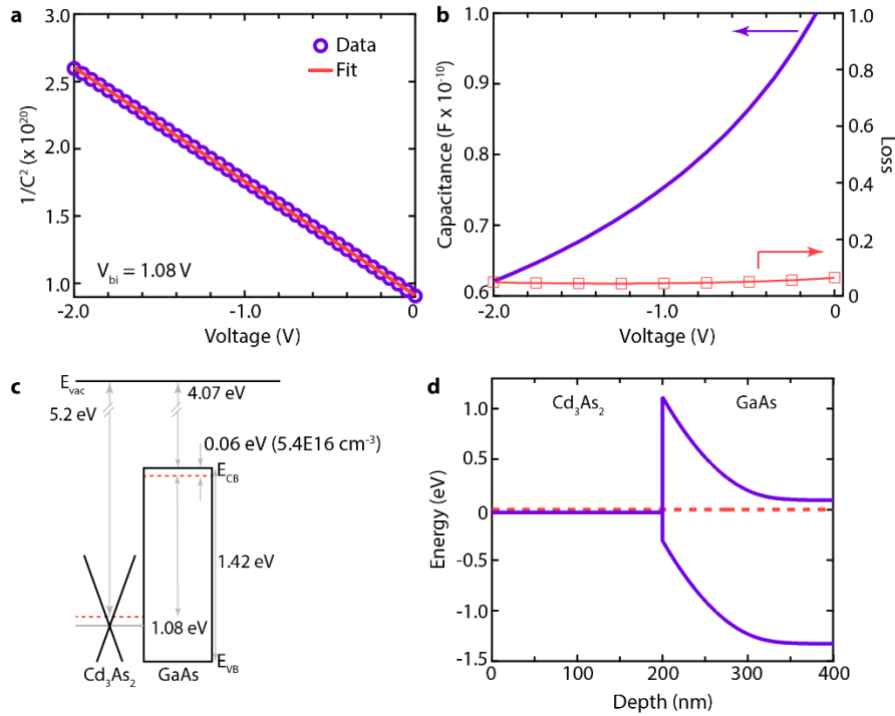
Anthony D. Rice, Choong Hee Lee, Brian Fluegel, Andrew G. Norman, Jocienne Nelson, Chun Sheng Jiang, Mark Steger, Deborah L. McGott, Patrick Walker and Kirstin Alberi\*

#### **Band Alignment in the p-B-n Structure**

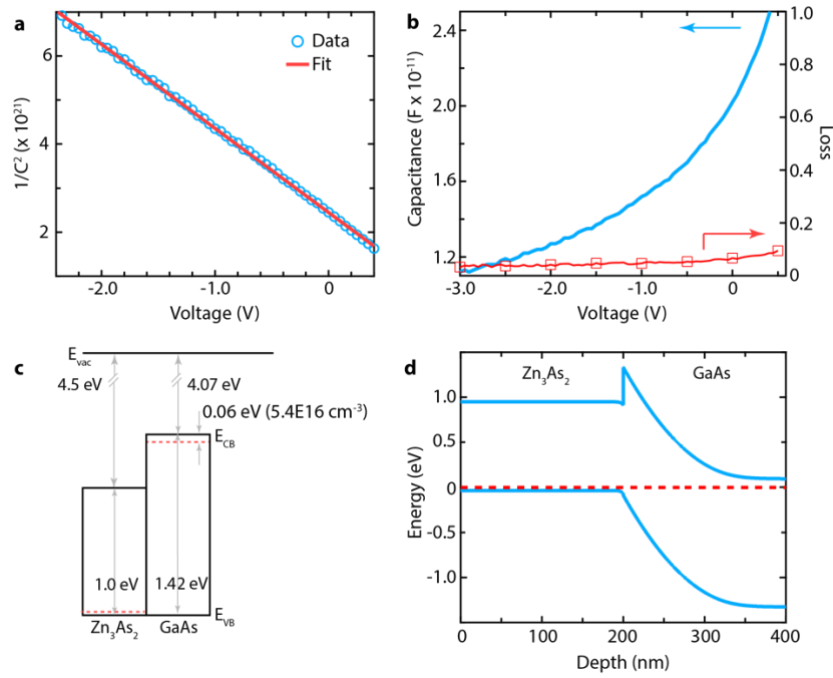
Capacitance-voltage (CV) measurements were used to determine the band alignment in the photodetector. Measurements were carried out on simpler isotype heterojunctions. For Cd<sub>3</sub>As<sub>2</sub>, they consisted of 200 nm of Cd<sub>3</sub>As<sub>2</sub> grown on n-GaAs ( $5.4 \times 10^{16} \text{ cm}^{-3}$ , 500 nm thick)/n<sup>+</sup> GaAs. Due to the larger dielectric constant of 36 and higher background doping of Cd<sub>3</sub>As<sub>2</sub> ( $\sim 1 \times 10^{18} \text{ cm}^{-3}$ ), most of the built-in voltage drops across n-GaAs layer and forms a Schottky barrier. A  $1/C^2$  plot (Figure S1a) was obtained from the C-V curve (Figure S1b) measured at 500 KHz. From these measurements, a built-in voltage,  $V_{bi}$ , of 1.08 eV was extracted. The corresponding band alignment is shown schematically in Figure S1c. The one-dimensional Schrodinger–Poisson solver software BandEng was used to further simulate the band bending at the heterointerface (Figure S1d).<sup>[1]</sup> We note that the Fermi level in the Cd<sub>3</sub>As<sub>2</sub> was assumed to be 100 meV above the Dirac point based on the doping.<sup>[2]</sup>

For Zn<sub>3</sub>As<sub>2</sub>, they consisted of 200 nm of Zn<sub>3</sub>As<sub>2</sub> grown on n-GaAs ( $5.4 \times 10^{16} \text{ cm}^{-3}$ , 500 nm thick)/n<sup>+</sup> GaAs. The Zn<sub>3</sub>As<sub>2</sub> layer was also heavily doped ( $5 \times 10^{18} \text{ cm}^{-3}$ ), resulting in a Schottky junction. The  $1/C^2$  plot in Figure S2a was obtained from the C-V curve in Figure S2b, and a  $V_{bi}$  value of 1.4 eV was extracted. The corresponding flat band energy diagram and simulated band bending in GaAs are shown in Figures S2c and S2d, respectively.

Finally, we used the known band alignments between GaAs and CdTe to determine the photodetector band alignments in Fig. 3 of the main text.<sup>[3,4]</sup>



**Figure S1.** CV measurements of  $\text{Cd}_3\text{As}_2$  band alignment. a),  $1/C^2$  plot obtained from b) CV measurements of a  $\text{Cd}_3\text{As}_2/\text{n- GaAs}/\text{n+ GaAs}$  substrate structure. c)  $\text{Cd}_3\text{As}_2/\text{n- GaAs}$  band alignment determined from the built-in voltage extracted from the CV measurements. The dashed horizontal lines represent the Fermi level in each material. d) band bending simulated in the n-GaAs layer.

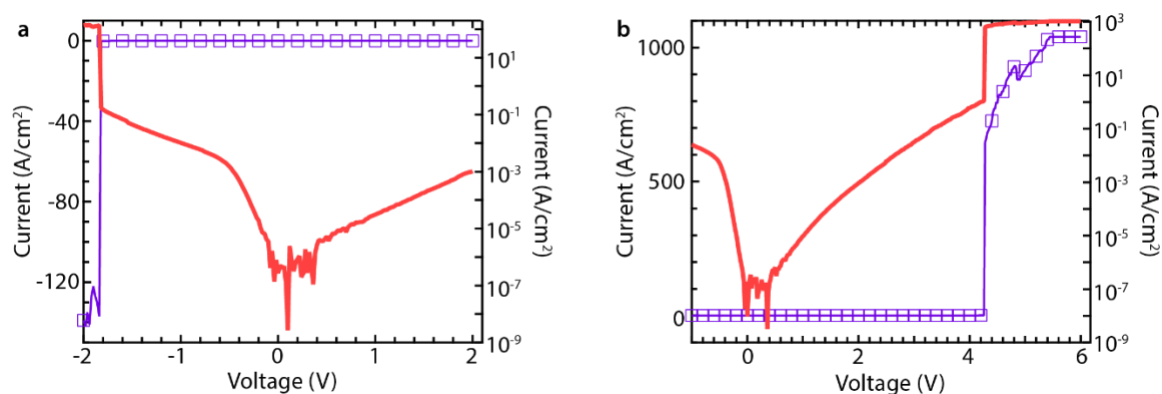


**Figure S2.** CV measurements of  $\text{Zn}_3\text{As}_2$  band alignment. a)  $1/C^2$  plot obtained from b) CV measurements of a  $\text{Zn}_3\text{As}_2/\text{n- GaAs}/\text{n+ GaAs}$  substrate structure. c)  $\text{Zn}_3\text{As}_2/\text{n- GaAs}$  band alignment determined from the built-in voltage extracted from the CV measurements. The dashed horizontal lines represent the Fermi level in each material. d) band bending simulated in the n-GaAs layer.

### Band Alignment in the MIS Structure

The energy band diagram of the MIS structure under thermal equilibrium conditions, shown in Figure 4b in the main text, was derived from the CdTe and Au energy band parameters published in the literature.<sup>[3-5]</sup> To better understand the band bending that is generated in the Cd<sub>3</sub>As<sub>2</sub>, additional breakdown measurements were performed.

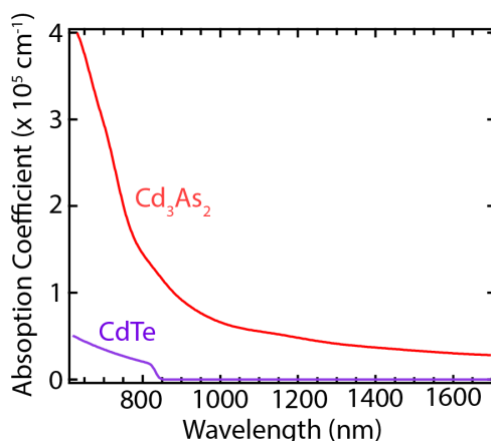
Figures S3a and S3b show the reverse and forward breakdown, respectively. Reverse breakdown occurs at a lower magnitude of applied voltage than forward breakdown. Furthermore, breakdown occurs when it is difficult to shift the Fermi level in the Cd<sub>3</sub>As<sub>2</sub> layer, forcing more voltage to drop across the CdTe layer. These two pieces of information suggest that the Fermi level initially resides in the Cd<sub>3</sub>As<sub>2</sub> valence band at thermal equilibrium. It is more difficult to shift the Fermi level into the higher density of states in the valence band by applying a reverse bias, leading to breakdown at low voltage (-1.8 eV). Conversely, the application of a forward voltage first shifts the Fermi level through the Dirac point and then into the higher density of states in the conduction band, leading to breakdown at a much higher voltage > 4 V. These measurements therefore confirm the qualitative band bending in the Cd<sub>3</sub>As<sub>2</sub> layer shown schematically in Figure 4 in the main text.



**Figure S3.** Breakdown measurements in the MIS structure. a) Breakdown of the Cd<sub>3</sub>As<sub>2</sub>/CdTe/Au MIS structure operated in reverse bias at -1.8 V occurs at a lower applied voltage than b) breakdown when operated in forward bias (> 4 V). These results indicate that the Fermi level initially resides in the valence band of the Cd<sub>3</sub>As<sub>2</sub> layer at thermal equilibrium.

## Absorption Coefficients

The absorption coefficient of our Cd<sub>3</sub>As<sub>2</sub> and CdTe epilayers were determined from ellipsometry measurements and are shown in Figure S4. This information is useful for understanding the wavelength dependence of the p-B-n photodetector presented in Figure 3 of the main text.



**Figure S4.** Absorption coefficients of Cd<sub>3</sub>As<sub>2</sub> and CdTe. The absorption coefficient of Cd<sub>3</sub>As<sub>2</sub> is much higher than CdTe over the entire wavelength range used for the p-B-n photodetector measurements. CdTe does not appreciably absorb light below 1.47 eV (above 840 nm).

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