

## **Technology: Power electronics**

### **HED: Targeting medium-voltage power electronics with vertical GaN devices**

**DEK:** Vertical GaN *p-n* diodes combine excellent efficiencies with incredibly fast protection from unwanted electromagnetic pulses

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We are living in an age of increased awareness of energy efficiency. This is partly caused by concerns over global warming, rammed home by alarming images of this year's floods and heat waves. However, it also comes from increasing use of battery power, particularly in transportation, and the need to make the most out of this stored energy.

For the electric grid and various microgrids, demand is on the rise for high-efficiency solid-state power conversion in the medium-voltage range, which roughly spans 1.2 kV to 20 kV. Power converters operating in this domain could serve in solid-state transformers operating at the grid distribution-level, such as those at 13.8 kV, as well as DC microgrids, including those proposed for all-electric aircraft at 10 kV.

Thanks primarily to a breakdown electric field that is far higher than that of silicon, wide-bandgap semiconductors, such as SiC and GaN, offer outstanding opportunities for improving medium-voltage power electronics. As well as reducing on-resistance, they can increase conversion efficiency and slash system size, due to higher switching frequencies. Of the two successors, GaN may ultimately have the upper hand at voltages of 10 kV and more, due to its higher electron mobility (see Figure 1).

The results shown in Figure 1 compare the performance of a type of GaN vertical power transistor known as a CAVET – its full name is a Current-Aperture Vertical-Electron Transistor – with a SiC MOSFET. Note, however, that the trend is applicable to other types of vertical power device. The term 'vertical' is used for device architectures that contain a thick, low-doped drift region. This layer provides the blocking voltage and governs the on-resistance of the device.

As the operating voltage increases, the efficiency of the GaN converter improves relative to that of SiC (this can be seen by comparing the performance of 1.2 kV and 8 kV devices). At first glance,

the increase is trivial, but this overlooks the need to consider the difference from 100 percent efficiency. Evaluated in this manner, which hones in on the loss, shows that the difference is substantial.

One major downside of vertical GaN devices is that they are not as mature as their SiC cousins, and in this regard, in a different league from those made from silicon. To fully evaluate the feasibility of vertical GaN there needs to be ongoing improvements in the epitaxial growth of GaN on its native substrate, as well as advances in device processing, such as those that enable effective edge termination structures.

To this end, our US collaboration, led by researchers at Sandia National Labs and involving engineers at the Naval Research Laboratory, Stanford University, Edynx, and Sonrisa Research, has established a vertical GaN foundry that is targeting 1.2 kV, 3.3 kV, and 6.5 kV devices. This holistic effort combines epitaxial growth with wafer metrology, device design, processing and characterization – the latter includes investigation of yield, reliability testing, and failure analysis. We are also undertaking a parallel effort that is focusing on higher-voltage structures, eventually up to 20 kV, and targeting specialized devices with a very fast breakdown that are capable of protecting the electric grid from electromagnetic pulses.

We have undertaken extensive mapping of bare GaN substrates and epiwafers with GaN p-n diode structures grown by MOCVD. Tools for this mapping include an optical profiling system, Raman spectroscopy, and typical mercury probe. The profiling system's capabilities are illustrated in Figure 2, which has maps of three 2-inch wafers featuring 8  $\mu\text{m}$ , 10  $\mu\text{m}$  and 12  $\mu\text{m}$ -thick drift layers with a net doping density of  $1.3 \times 10^{16} \text{ cm}^{-3}$ . For our foundry effort, we tend to use such structures for fabricating 1.2 kV devices.

Fabrication of our devices occurs at the 2-inch wafer scale, using a foundry environment at the US Naval Research Laboratory. Here, standard processing techniques for III-N devices realize contacts, isolation, and so on.

#### <Crosshead> **Evaluating edge termination**

When producing these GaN diodes, the most critical process step is edge termination, which is realized by ion implantation. Although etch-based processes have been shown to achieve high performance, we employ implantation, because this enables a planar process that is compatible with true foundry manufacturing. Using ion implantation, we have processed epitaxial wafers into devices with various combinations of junction termination extensions and guard rings (see Figure 3 for photos of typical GaN foundry wafers and associated forward current-voltage characteristics).

Measurements on our diodes reveal excellent turn-on behaviour and an electroluminescence typical of a GaN *p-n* junction. For diodes with areas ranging from 0.1 mm<sup>2</sup> to 1.0 mm<sup>2</sup>, forward

current capability is more than 5 A, corresponding to current densities spanning 500 A/cm<sup>2</sup> to 5000 A/cm<sup>2</sup>. The related specific on-resistance is 0.3 mΩ-cm<sup>2</sup> to 1.2 mΩ-cm<sup>2</sup>.

We have also assessed the breakdown voltage of our devices. Sampling twelve of them from a single wafer shows that the breakdown voltages exceed 1.3 kV in all cases – this is approximately 90 percent of the theoretical parallel-plane limit. Note that the precise nature of the breakdown depends on the details of edge termination. Devices receiving a shallower termination implant profile exhibit a breakdown indicative of avalanche behaviour and characterized by an abrupt increase in current.

We are also exploring other approaches to edge termination. They include a bevel design, which we have evaluated with extensive numerical simulations (one example is shown in Figure 4, with results for a 5° bevel). One key finding of this work is the need for very small bevel angles, employed to ensure that the electric field at the edge of the structure is maintained below the ideal parallel-plane maximum electric field (it is around 3.1 MV/cm for the case shown). We have drawn on the results of simulations to guide our fabrication of bevel-terminated diodes, using either a flowed photoresist for bevel angles of 5°, 15°, and 50°, or greyscale lithography for a bevel angle of 1°.

With vertical GaN power devices at an early stage of development, it is not surprising that reliability studies are relatively rare. Our team is adding to them, using high-temperature operating life tests to assess the forward diode current stability, and evaluating reverse current stability with high-temperature reverse-bias testing. In both cases, test conditions are carefully monitored to ensure that the device's temperature and its bias stay constant throughout this test.

One key finding of these investigations is that there is a significant increase in the forward current during high-temperature operating life testing. Another important observation is that when the diode is biased in the avalanche region, there is a change in the avalanche current during high-temperature reverse-bias testing. Thermal considerations limit the DC avalanche current, which exhibits a thermal transient during the first minute at elevated temperatures.

Our team has also conducted failure analysis on selected failed devices. This includes inspecting a diode that failed high-temperature reverse bias testing with emission microscopy (see Figure 5). Using this technique, we observed that the emission is near the edge termination of the device, indicating that this portion of the diode is responsible for its failure.

#### <Crosshead> **Protecting the grid**

Electromagnetic pulses pose a significant threat to the electric grid, as they could potentially cause blackouts over an extremely large geographical area. For electromagnetic pulses with transients shorter than a microsecond, over-voltage conditions that ensue could cause damage

to today's grids. One solution is to introduce fast breakdown GaN *p-n* diodes – they are capable of clamping the voltage across equipment on the grid when it is subjected to such pulses.

A target voltage for this specialized but critical application is 20 kV. This blocking voltage provides an adequate margin for protecting, with a single device, distribution-level equipment, when typically operating at up to 13 kV; and it provides a building-block for protecting sub-transmission equipment, as only a small number of stacked devices are needed to reach 69 kV, a typical requirement for this application.

We have started on the path to producing 20 kV devices, with efforts to date focusing on '5 kV class' GaN *p-n* diodes. These devices have an epitaxial structure that consists of a 45  $\mu\text{m}$ -thick drift region with a net *n*-type doping in the  $2\text{-}5 \times 10^{15} \text{ cm}^{-3}$  range. Like the foundry diodes, the heterostructure has been grown by MOCVD. The anode design contains a two-layer *p*-region with a *p*-minus layer (magnesium level of around  $1 \times 10^{18} \text{ cm}^{-3}$ ) near the junction and a higher *p*-doped layer (magnesium level of around  $3 \times 10^{19} \text{ cm}^{-3}$ ) on top. After epitaxial growth, wafers are processed using a multi-step junction-termination flow, using sequential  $\text{BCl}_3/\text{Cl}_2$  inductively coupled plasma etches.

Electrical measurements of a representative 150  $\mu\text{m}$ -diameter diode reveal that it is extremely well-behaved under reverse bias, exhibiting a low leakage current until the onset of abrupt breakdown at around 4.2 kV (see Figure 6). When operated under forward bias at 3.75 V, the diode shows good turn-on and a differential specific on-resistance of  $3.8 \text{ m}\Omega\text{-cm}^2$ , calculated when defining the area as that of the *p*-contact.

To assess the capability of these diodes for electromagnetic pulse protection, we measured response times with a transmission-line system. This approach, drawing on a setup previously used to measure the reverse-recovery time of GaN *p-n* diodes, provides an upper bound of 1.3 ns for the time to breakdown. This incredibly short time demonstrates that this diode can arrest the fast component of an electromagnetic pulse.

While vertical GaN power devices hold promise for medium-voltage power electronics, challenges must still be overcome related to substrates, epitaxial materials growth, and device processing. Additionally, there is a need to characterize and understand yield and reliability, to enable the fabrication process to become commercially viable. Our team is examining these issues as we establish a foundry for fabricating vertical GaN *p-n* diodes. Additionally, we are pursuing specialized applications, such as electromagnetic pulse protection, that utilize the diodes' fast breakdown response. Further research will determine the full extent of the capabilities of vertical GaN power devices.

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<Figure captions>

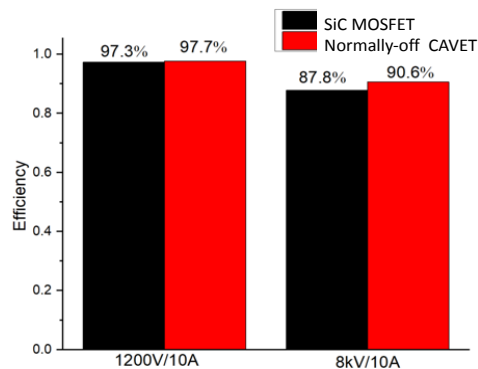


Figure 1. Simulated switching efficiency improvement for vertical GaN CAVETs (a type of vertical transistor) compared with SiC MOSFETs at 1.2 kV and 8 kV. Mobilities of 950 and 1200 cm<sup>2</sup>/Vs

are used for SiC and GaN, respectively (taken from D. Ji et al. *Int. J. High-Speed Elec. Sys.* **28(01n02)**, 1940010 (2019)).

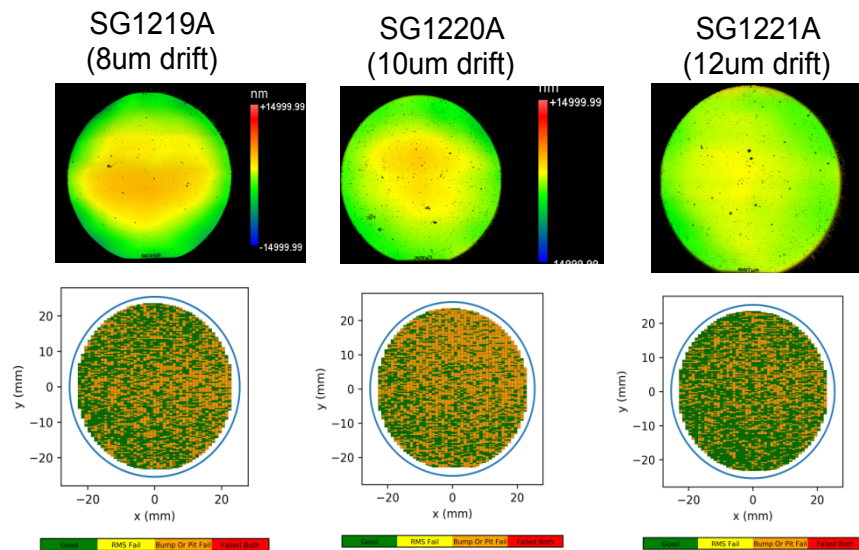


Figure 2. Optical profiles of 2-inch diameter GaN substrates with 8  $\mu\text{m}$ , 10  $\mu\text{m}$ , and 12  $\mu\text{m}$  drift regions grown by MOCVD. The top portion of the figure shows the raw data, while the bottom portion shows yield maps: green indicates a good device; yellow a failure, due to root-mean-square (RMS) roughness; orange a failure due to a bump or pit; and red a failure due to both modes.

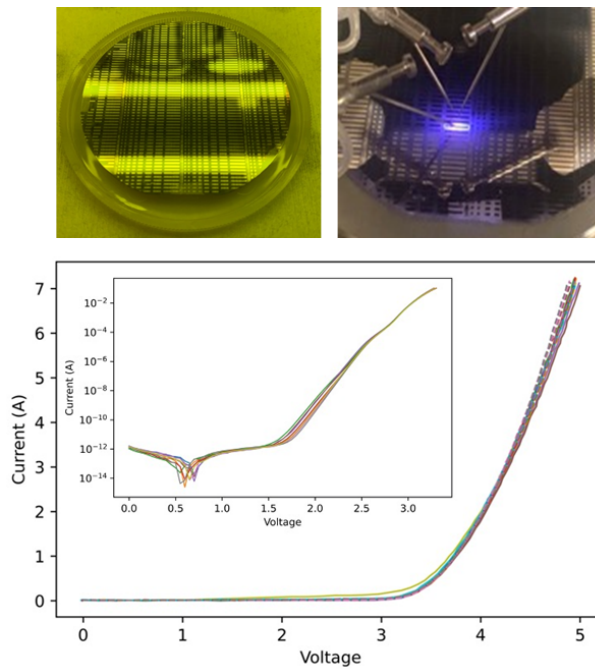


Figure 3. A photo of a typical GaN  $p$ - $n$  diode foundry wafer (top left), and such a wafer under test (top right), with the visible sub-bandgap light emission. The bottom portion of the figure shows representative forward current-voltage curves, where devices labelled A through F have areas varying from approximately 0.1 to 1.0 mm<sup>2</sup>.

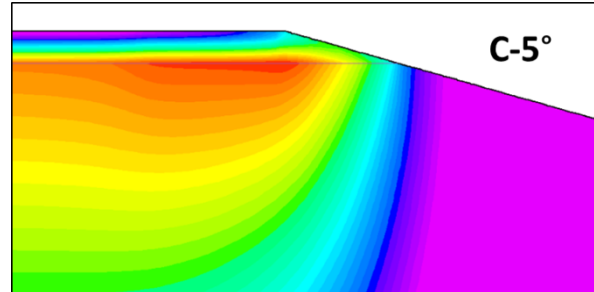


Figure 4. Electric field magnitude for a 5° bevel termination with an 8 μm-thick drift region with a net  $n$ -type doping of  $1.3 \times 10^{16}$  cm<sup>-3</sup> and a 500 nm-thick anode layer with a magnesium concentration of  $3 \times 10^{17}$  cm<sup>-3</sup> to achieve  $p$ -type doping.

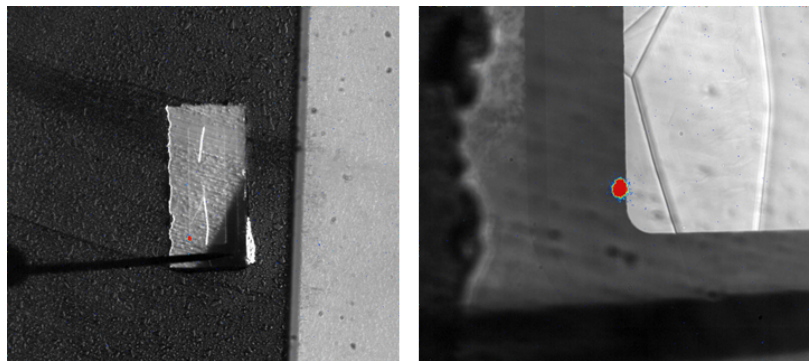


Figure 5. Left image shows an emission microscopy image of a GaN  $p$ - $n$  diode at 1 kV and 0.5 μA under 2.5x magnification. A single emission spot is visible at the corner of the device at the termination of the junction-termination extension. Right image shows expanded view of the emission spot.

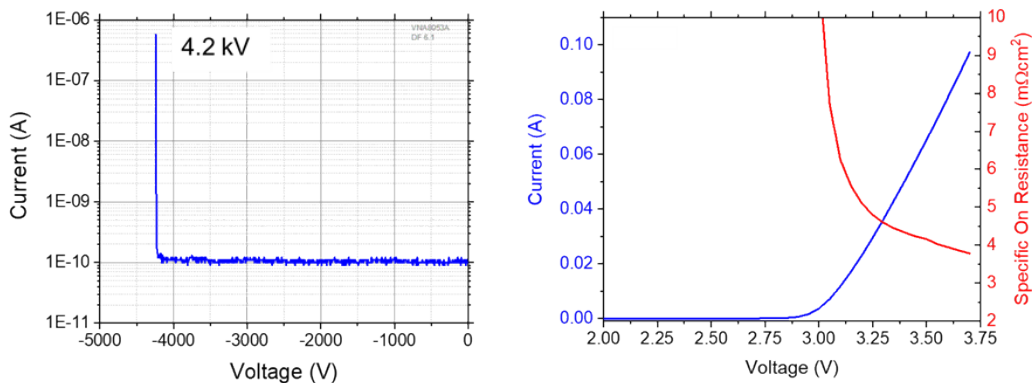


Figure 6. Current-voltage characteristics of GaN  $p$ - $n$  diodes with 45  $\mu\text{m}$ -thick drift regions intended for an electromagnetic pulse arrestor. Left panel shows low reverse-bias leakage current and breakdown around 4.2 kV; and right panel shows forward-bias current and differential specific on-resistance, which is approximately  $3.8 \text{ m}\Omega \text{ cm}^2$  at 3.75 V.