A Perspective on the Electro-Thermal Co-Design of Ultra-Wide Bandgap Lateral Devices

Sukwon Choi[1,a)], Samuel Graham[2], Srabanti Chowdhury[3], Eric R. Heller[4], Marko J. Tadjer[5], Gilberto Moreno[6], Sreekant Narumanchi[6]

[1]*Department of Mechanical Engineering, The Pennsylvania State University, University Park, Pennsylvania 16802, USA*
[2] *George W. Woodruff School of Mechanical Engineering, Georgia Institute of Technology, Atlanta, Georgia 30332, USA*
[3]*Department of Electrical Engineering, Stanford University, Stanford, California 94305, USA*
[4]*Air Force Research Laboratory, Wright-Patterson Air Force Base, Ohio 45433, USA*
[5] *Naval Research Laboratory, Washington, DC 20375, USA*
[6] *Center for Integrated Mobility Sciences, National Renewable Energy Laboratory, Golden, Colorado 80401, USA*

[a)] Author to whom correspondence should be addressed: sukwon.choi@psu.edu

Abstract

Fundamental research and development of ultra-wide bandgap (UWBG) semiconductor devices are underway to realize next-generation power conversion and wireless communication systems. Devices based on aluminum gallium nitride ($Al_xGa_{1-x}N$, *x* is the Al composition), β-phase gallium oxide (β-Ga_2O_3), and diamond give promise to the development of power switching devices and radio frequency (RF) power amplifiers with higher performance and efficiency than commercial wide bandgap semiconductor devices based on gallium nitride (GaN) and silicon carbide (SiC). However, one of the most critical challenges for the successful deployment of UWBG device technologies is to overcome adverse thermal effects that impact the device performance and reliability. Overheating of UWBG devices originates from the projected high power density operation and the poor intrinsic thermal properties of $Al_xGa_{1-x}N$ and β-Ga_2O_3. This article delineates the need and process for the "electro-thermal co-design" of laterally-configured UWBG electronic devices and provides a comprehensive review of current state-of-the-art thermal characterization methods, device thermal modeling practices, and both device- and package-level thermal management solutions.

Keywords: Electro-thermal co-design, thermal characterization, thermal management of electronics, thermal properties, ultra-wide bandgap (UWBG) semiconductors.

I. Introduction to the UWBG Semiconductors

Until the late 1980s, the mainstream semiconductor materials for power and radio frequency (RF) applications were Si, Ge, and conventional group III-V compound semiconductors such as GaAs and InP. Currently, wide bandgap (WBG) semiconductors GaN and SiC have become the second most important group of semiconductor materials after Si. These WBG materials form the basis of light emitting diode (LED)-based solid-state lighting[1,2] as well as advanced power and RF electronics[3–5]. As GaN and SiC technologies move closer to maturity, these devices are approaching the theoretical limit of the achievable performance, which is dictated by their fundamental material properties. To meet the demanding requirements for higher power/frequency

commercial and military applications, device engineers are pursuing the development of next-frontier devices based on ultra-wide bandgap (UWBG) semiconductors $Al_xGa_{1-x}N$, β-Ga_2O_3, and diamond.[6–8]

A number of figures of merit (FOMs) are often used to show the relative merits of a particular semiconductor material for use in electronics, and UWBG materials generally show an increased FOM over lower bandgap semiconductors. The Johnson figure of merit (JFOM)[9] is often used to compare the potential of materials for building high-frequency transistors. The JFOM is defined as $JFOM = V_{BR}f_T$, where V_{BR} is the breakdown voltage and f_T is the unity gain cutoff frequency. The JFOM can also be expressed as $v_{sat}E_C$, where v_{sat} and E_C are the saturated carrier velocity and critical electric field, respectively. Table I shows that the JFOMs of $Al_xGa_{1-x}N$ and β-Ga_2O_3 surpass those for WBG materials, and diamond exhibits a JFOM comparable to GaN. Therefore, these UWBG materials offer the potential for the development of next-generation RF power amplifiers.

On the other hand, the lateral figure of merit (LFOM)[10] is a metric that compares the theoretically achievable switching performance of laterally-configured transistor devices. It is defined as $LFOM = V_{BR}^2/R_{ON,SP}$, where $R_{ON,SP}$ is the specific ON-resistance. Accounting for the lateral device geometry, the LFOM can also be expressed as $q\mu n_s E_C^2$, where q is the electron charge, μ is the channel mobility, and n_s is the sheet charge density. The LFOM is analogous to the conventional Baliga figure of merit (BFOM[11]; a modified version has recently been reported[12]) applicable to unipolar vertical power switches. It should be noted that LFOMs in **Table I** for UWBG devices are calculated based on mobility values currently reported in literature for early-stage devices. Even in premature stages, UWBG devices have LFOMs approaching or greater than established GaN devices. The high LFOMs offered by the UWBG materials give promise to the development of lateral power switches with kV-range breakdown voltages and minimized device footprints.

Table I. Material properties and figures of merit for conventional, WBG, and UWBG semiconductors. Data were adopted from references [8,13–20]. The LFOM calculation (normalized with respect to Si) assumes $n_s=10^{13}$ cm^{-2} and uses reported device channel mobilities. For diamond, the mobility and saturation velocity for holes are listed.

Property	Conventional		WBG		**UWBG**		
	Si	GaAs	SiC	GaN	**$Al_{0.85}Ga_{0.15}N$**	**β-Ga_2O_3**	**Diamond**
Bandgap, E_G (eV)	1.12	1.43	3.26	3.42	5.61	4.8	5.47
Relative dielectric constant, ε	11.9	13.1	10.1	9.7	8.68	10	5.7
Breakdown field, E_C (MV/cm)	0.3	0.4	3	3.3	10.7	8	10
Carrier (channel) mobility μ (cm^2/Vs)	1400	8500	1020	1350(2000)	45(250)	200(180)	3800(69)
Carrier saturation velocity, v_{sat} (cm/s)	1×10^7	2×10^7	2×10^7	2.7×10^7	2.28×10^7	1.5×10^7	0.8×10^7
Thermal conductivity, k (W/mK)	150	46	490	130	**8.5**	**11-27**	**2400**
Normalized JFOM ($v_{sat}E_C$)	1	2.7	20	30	**81**	**40**	**27**
Normalized LFOM ($q\mu n_s E_C^2$)	1	11	73	170	**230**	**100**	**55**

The enhancement in device-level performance according to the superior JFOM and LFOM translates into commensurate improvement in system-level size, weight, and power (SWaP) and efficiency. In particular, β-Ga_2O_3 offers the potential to address the cost performance trade-off for established WBG semiconductors by providing lower-cost melt-grown wafers and the higher performance suggested by the FOMs.[21] These advantages can be leveraged to improve power

efficiency gains of 5G network base stations and to build lighter and more efficient power conversion systems for electric vehicles, aircraft, spacecraft, and sustainable energy sources.

II. Representative Laterally-Configured UWBG Semiconductor Devices

The bandgap energy, E_G, of $Al_xGa_{1-x}N$ peaks at 6.2 eV (x=1)[22], which results in the largest breakdown field (15.4 MV/cm)[12] among all the UWBG semiconductors listed in **Table I**. Moreover, the piezoelectric nature of the material allows for the fabrication of a high electron mobility transistor (HEMT) structure[23], which offers high electron sheet density (>10^{13} cm^{-2}) and mobility without impurity doping. A typical $Al_xGa_{1-x}N$-channel HEMT structure[24] is shown in **Figure 1 (a)**. Briefly, a 1-4 μm thick $Al_xGa_{1-x}N$ channel/buffer layer is heteroepitaxially grown on a non-native substrate such as AlN/sapphire[14,25,26] templates, GaN/SiC[27] templates, and AlN[28,29]. Subsequently, a thin (~20 nm) higher Al-content $Al_yGa_{1-y}N$ (y~x+0.15) barrier layer is grown over the $Al_xGa_{1-x}N$ channel. The $Al_yGa_{1-y}N/Al_xGa_{1-x}N$ heterointerface physically governs the device behavior through the formation of a polarization-doped two-dimensional electron gas (2DEG)[23]. It should be noted that the $Al_xGa_{1-x}N$ system can readily take advantage of the global manufacturing infrastructure associated with commercial InGaN LEDs, $Al_xGa_{1-x}N$-based ultra-violet LEDs[30], and GaN electronics.

The primary advantage of β-Ga_2O_3 (E_G~4.8 eV)[18] over the other UWBG materials is that high crystalline quality substrates can be synthesized at low cost using melt growth techniques such as Czochralski and edge-defined film-fed growth, similar to the case of the melt-grown substrates that support ubiquitous Si devices.[31] While the intrinsic β-Ga_2O_3 material suffers from a relatively low bulk electron mobility[32,33], innovative device architectures such as the β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ modulation-doped field effect transistor (MODFET)[20,34,35] shown in **Figure 1 (b)** are being developed to overcome the room temperature mobility limitations arising from the strong Frölich interaction in β-Ga_2O_3.[36,37] A 2DEG channel is formed near the heterointerface via modulation doping, where electrons are transferred from a Si delta-doped region in the β-$(Al_xGa_{1-x})_2O_3$ barrier. Since the carriers are physically separated from the donor ions, scattering from the ionized impurities is greatly suppressed as well, enabling an overall higher electron mobility than earlier β-Ga_2O_3 lateral transistor structures ($\mu < 100$ cm^2/Vs)[31].

The favorable properties of diamond such as the large bandgap energy (E_G=5.47 eV), high critical electric field (8-10 MV/cm), high hole saturation velocity (0.8×10^7 cm/s), and the highest known thermal conductivity are listed in **Table I**.[8] The hydrogen (H)-terminated diamond field effect transistor (FET) structure[15] shown in **Figure 1 (c)**, along with the recent advances in diamond substrate synthesis by high-pressure-high-temperature (HPHT) and chemical vapor deposition (CVD) processes, gives promise to the establishment of diamond electronics technologies. To circumvent difficulties in substitutional doping[8,38], the H-terminated diamond FET utilizes surface transfer doping[39]. Microwave hydrogen plasma treatment is used to achieve hydrogen termination of the diamond surface. The interaction between the H-terminated surface and adsorbed ions present in the atmosphere or an electron acceptor layer (e.g., MoO_3[40], V_2O_5[41]) results in energy band bending that creates a two-dimensional hole gas (2DHG) with a carrier density in excess of 10^{13} cm^{-2}. To improve the stability of the 2DHG channel, the device is passivated with a protective layer (e.g., hydrogen silsesquioxane (HSQ)[42], Al_2O_3[43], and SiO_2[44]).

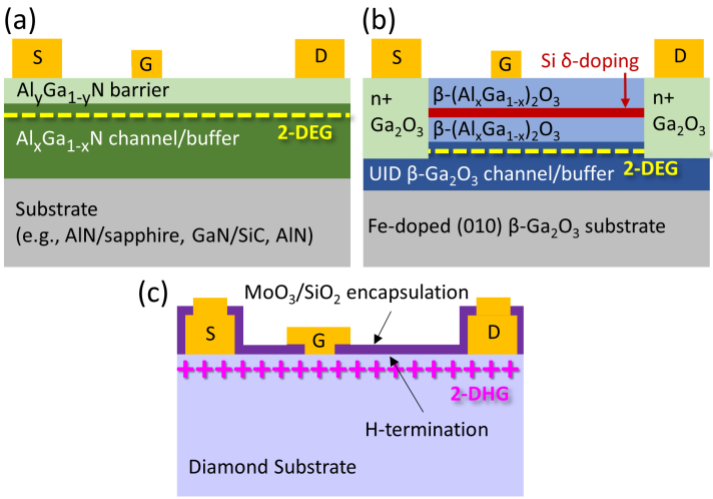

Figure 1. Schematic epitaxial structures of (a) an $Al_xGa_{1-x}N$-channel HEMT, (b) a β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ MODFET, and (c) an H-terminated diamond FET.

While the main focus of this work is laterally-configured UWBG devices, active research on the development of vertically oriented power transistors[45] and diodes[46–48] for applications that demand extreme voltage (>1 kV) and current levels (>100 A) are underway. Because the device technologies for UWBG lateral devices are relatively more mature than vertical devices, we will delineate the need and process for the "electro-thermal co-design" of UWBG electronics using case studies based on laterally-configured devices.

III. Thermal Challenges

The high voltage/power operation and aggressive device scaling (i.e., reducing the device gate and channel lengths) enabled by the superior LFOMs of UWBG materials (**Table I**) will translate into extremely high-power densities within the active region (~1 MW/cm^2) as shown in **Figure 2**. However, the room temperature thermal conductivity of $Al_xGa_{1-x}N$ (<10 W/mK)[17] and β-Ga_2O_3 (anisotropic; 11-27 W/mK)[13] are the lowest among the technologically relevant semiconductor materials listed in Table I. The intended harsh operating conditions and poor thermal properties will result in excessive device self-heating unless proper thermal management solutions are implemented. Although the large bandgap energy may mitigate uncontrolled carrier conduction in the semiconductor caused by the increased thermal energy, the ohmic and gate contacts are not likely to withstand the extremely high channel temperatures. Due to the excellent thermal conductivity of diamond, a misconception can arise that diamond electronics should be free of thermal issues. However, one of the largest challenges associated with H-terminated diamond FETs is the stability of the 2DHG channel at high temperatures or under harsh environmental conditions.[42,49] For instance, at temperatures beyond 200°C, the C-H bonds and/or the surface adsorbates were shown to be detrimentally impacted, resulting in an irreversible loss of the surface p-type conduction.[42] Accordingly, device developers are recognizing that overheating is a major bottleneck to the success of the UWBG device technologies. In fact, no UWBG device reported to this day has achieved the performance expected by the superior JFOM/LFOM partly because a thermally limited technological plateau has been reached. As shown in **Figure 2**, it is necessary to engineer and reduce the junction-to-package thermal resistance of UWBG devices to a level

comparable to or lower than today's WBG GaN and SiC counterparts to realize the targeted high power density operation. To accomplish this goal, the first step is to understand both thermal transport within UWBG materials and the physical mechanisms (i.e., electro-thermal interactions) that lead to device self-heating. The next step will be to design thermal management solutions based on the fundamental knowledge gained from experiments and computational studies.

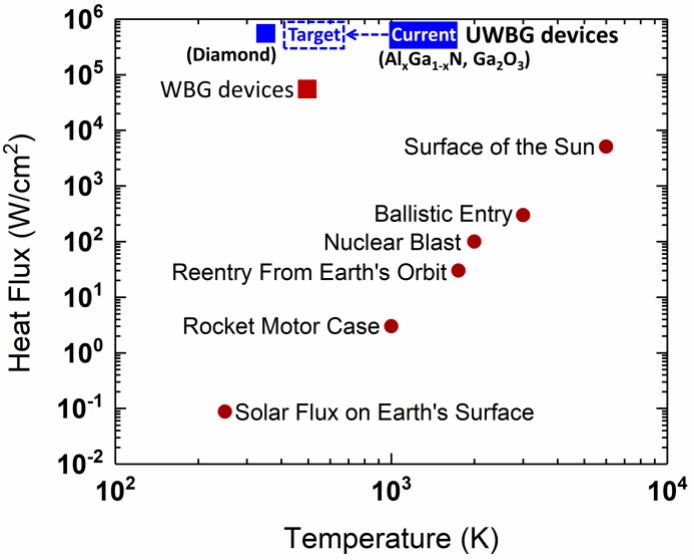

Figure 2. The heat flux challenge of UWBG power electronic devices (presuming operation at ~10 W/mm) and the role of electro-thermal co-design to reduce the device thermal resistance. For WBG and UWBG devices, the dissipated power was normalized with respect to the active area, i.e., the total area of the device channel.

IV. Electro-Thermal Co-Design

Traditionally, the design of power switching devices and RF power amplifiers has solely focused on maximizing the electrical performance by optimizing the epitaxial growth (e.g., AlGaN/GaN heterostructures) and improving device processing techniques (e.g., Ohmic contacts, field plate structures). Self-heating issues were indirectly recognized by the degradation of electrical performance[50] and their mitigation was considered to be an engineering problem that would result in de-rating of the device power output or improving the package-level design. However, as discussed above, UWBG devices are highly prone to overheating and thermal failure, with a minimal thermal margin to engineer. Current design practices, however, are often unable to accurately predict the thermal feedback caused by the power dissipation, leaving an incomplete model of the device performance and reliability. Such design practices may result in the development of less reliable components with degraded performance, both from an electrical and thermal/mechanical[51] standpoint. The need for electro-thermal co-design, which essentially means thermal considerations are incorporated into the device design from the initial stage of the device development process, has already proven to be essential to exploit the full potential of GaN RF power amplifiers.[52]

The design of thermal management solutions for UWBG devices requires a physics-based model that accurately predicts the channel peak temperature rise under specified operating conditions. Creating such device thermal model requires the following electro-thermal co-design

process. First, the physical properties that dictate the electronic and thermal transport within/across UWBG materials and interfaces must be accurately measured. Electrical characterization methods to determine electronic properties (e.g., carrier density, mobility, and saturation velocity) and device-specific electrical parameters (e.g., Ohmic contact resistance) are well established. However, thermal characterization methods suitable for measuring the thermo-physical properties of UWBG semiconductors are less accessible to device engineers and must be carefully chosen in real practices. Second, the device self-heating behavior in response to a specified voltage bias condition must be precisely estimated. This requires a 3D coupled electro-thermal modeling scheme that begins with solving for the charge transport and electrostatic potential within the semiconductor device. The Joule heat distribution derived from the electrical part of the coupled modeling scheme (2D simulation may be sufficient for many devices)[53] is then imported into a 3D finite element thermal model that adopts the measured thermo-physical properties. The modeling output will be the device surface and internal temperature fields. Third, optical thermography techniques with sufficiently high spatial/temporal resolutions and measurement sensitivity are necessary to capture the physical processes associated with the unconventional characteristic length scales and operational environments (i.e., extreme heat flux, electric field, frequency) and to validate the multi-physics device model. Care must be exercised; respected techniques can easily have a factor of two disagreement in temperature rise at the micro/nanoscale.[54–57] Finally, the validated device thermal model can be used for the design of device- and system-level passive and active thermal management solutions. **Figure 3** illustrates the electro-thermal co-design process for UWBG semiconductor devices.

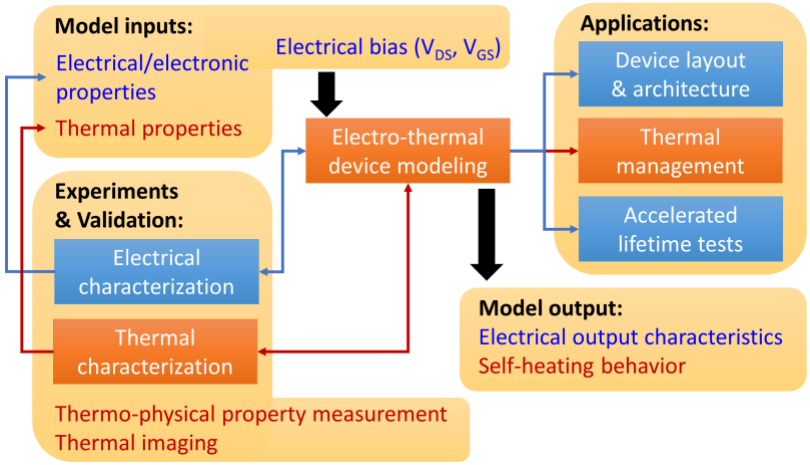

Figure 3. Flow diagram of the device-level electro-thermal co-design process.

1. Thermo-Physical Property Measurement

The $Al_xGa_{1-x}N$ structure can be viewed as a wurtzite phase GaN crystal with Al atoms randomly substituting the Ga cations within the group III sub-lattice. Early reports show inconsistent results possibly due to the low quality of the tested materials and/or the low measurement sensitivity of the metrology techniques.[58–60] Laser-based optical pump-probe techniques such as time-domain thermoreflectance (TDTR)[61] and frequency domain thermoreflectance (FDTR)[62] are ideal for the thermal conductivity measurement of $Al_xGa_{1-x}N$ and other UWBG thin films. Recent TDTR and FDTR measurement results for ~1 μm thick metal organic chemical vapor deposition (MOCVD)-grown $Al_xGa_{1-x}N$ films are illustrated in **Figure 4**

(a).[17] A remarkable reduction in the room temperature thermal conductivity with respect to the base GaN (x=0; the bulk value can reach beyond 200 W/mK[63–65]) and AlN (x=1; the bulk value can reach up to ~320 W/mK[66–68]) crystals is observed. The observed U-shaped trend is universal for ternary alloy semiconductors, which is a manifestation of phonon-alloy disorder scattering[69–71]. Above room temperature (or from ~100 K), the thermal conductivity of crystalline solids including GaN and AlN are well known to monotonically decrease with temperature.[64,66–68,72,73] However, we report data in **Figure 4 (b)** that shows the thermal conductivity of $Al_xGa_{1-x}N$ (x=0.3) remains relatively constant from 78 K up to 450 K, similar to the behavior of amorphous materials[71,74]. Data in **Figure 4 (a)** and **(b)** show that phonon-alloy disorder scattering dominates the thermal conductivity of the solid solution. **Figure 4 (c)** shows the thermal conductivity (at room temperature) of $Al_{0.9}Ga_{0.1}N$ films with different thickness (100 – 1300 nm).[75] These results reveal the relatively large contribution of propagating vibrational modes with relatively long mean free paths (~1 μm) to the thermal conductivity of $Al_{0.9}Ga_{0.1}N$. While $Al_xGa_{1-x}N$-channel HEMTs have been suggested to be suitable for extreme-temperature applications,[17,76–78] thermal property data at high temperatures are lacking. Also, as top-side cooling methods are thought to be most suitable for the thermal management of $Al_xGa_{1-x}N$-channel HEMTs (to be discussed in **Figure 8 (b)**),[79] studies on the thermal transport across the $Al_xGa_{1-x}N$/metal contact interfaces are demanded. We report in **Figure 4 (d)** the temperature dependence of the interfacial boundary conductance between a Ti/Au metal contact and $Al_{0.3}Ga_{0.7}N$ measured by the TDTR method. The increasing trend of the thermal boundary conductance with temperature due to phonon coupling enhancement[80] should be considered when optimizing the thermal design of flip-chip configurations[81] that will extract heat from the 2DEG region through the metal contacts towards the thermal bumps and carrier wafer.

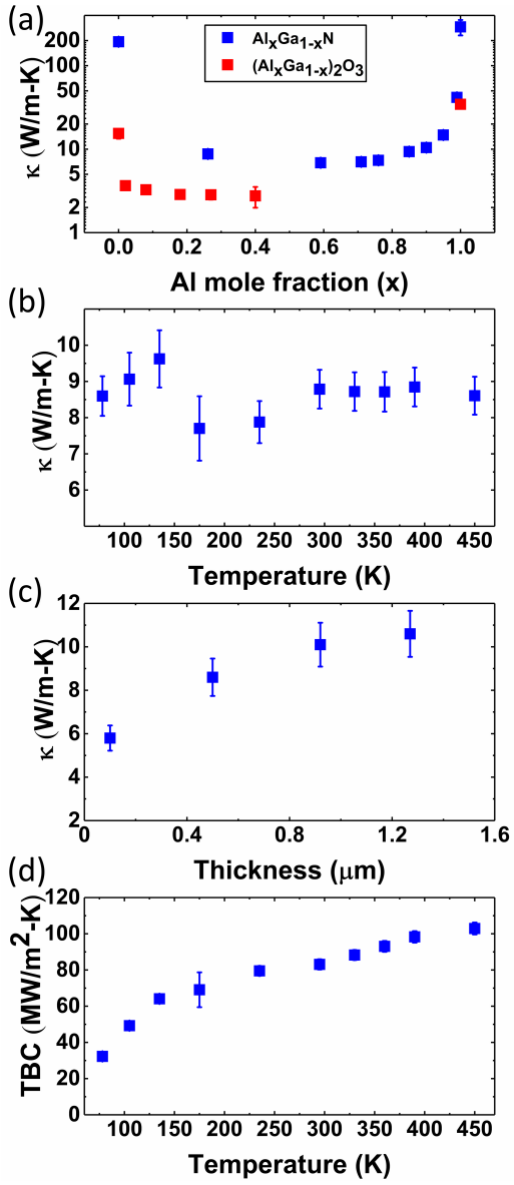

Figure 4. (a) The cross-plane thermal conductivity of c-plane $Al_xGa_{1-x}N$ and ($\bar{2}01$)-oriented β-$(Al_xGa_{1-x})_2O_3$ obtained from our TDTR and FDTR measurements. Data were adopted from references [17,82]. (b) The temperature dependence of the thermal conductivity of an $Al_{0.3}Ga_{0.7}N$ thin film. (c) The film thickness dependence of the thermal conductivity of an $Al_{0.9}Ga_{0.1}N$ film. Data were adopted from reference [75]. (d) The temperature dependence of the thermal boundary conductance between a Ti/Au metal contact and $Al_{0.3}Ga_{0.7}N$.

β-Ga_2O_3 exhibits a relatively low and anisotropic thermal conductivity.[13,83,84] The room temperature cross-plane thermal conductivity of (010), (001), ($\bar{2}01$), and (100)-oriented substrates were reported to be 27.0 W/mK, 14.7 W/mK, 13.3 W/mK, and 10.9 W/mK, respectively.[13] With regards to phonon-point defect scattering mechanisms in β-Ga_2O_3, the reduction in the thermal conductivity caused by Ga and O vacancies has been studied using first-principles calculation.[85] Also, a weak doping dependence of the thermal conductivity of β-Ga_2O_3 has been experimentally demonstrated.[86] Phonon-boundary scattering effects associated with β-Ga_2O_3 thin films have been

studied by characterizing mechanically exfoliated (100)-oriented thin films. The thermal conductivity in the [100] direction was shown to increase from 4.7 to 11.5 W/mK when the film thickness increased from 206 to 768 nm.[87,88] A similar trend was observed in ~250 nm thick ($\bar{2}01$)-oriented β-Ga_2O_3 thin films grown via pulsed laser deposition (PLD).[89] The thermal conductivity of β-$(Al_xGa_{1-x})_2O_3$ (which is necessary to create a MODFET structure in **Figure 2 (b)**) was reported for x=0.18 and was determined to be 3.6 W/mK in the [010] direction and 3.1 W/mK in the direction perpendicular to the ($\bar{2}01$) plane.[90] **Figure 4 (a)** shows the thermal conductivity of ($\bar{2}01$)-oriented β-$(Al_xGa_{1-x})_2O_3$ thin films grown via metalorganic vapor phase epitaxy (MOVPE)[91] on sapphire substrates measured by FDTR and TDTR.[82] Similar to the case of $Al_xGa_{1-x}N$, phonon-alloy disorder scattering dominates the thermal transport within β-$(Al_xGa_{1-x})_2O_3$. Both solid solutions possess a periodic lattice structure; however, the basis/lattice points lack compositional homogeneity due to the chemical disorder associated with the group-III cationic sublattice, occupied by Al and Ga atoms.[92] The thermal conductivities of β-Ga_2O_3 and β-$(Al_xGa_{1-x})_2O_3$ heteroepitaxial thin films grown on c-plane and 6° offcut sapphire substrates and the interfacial thermal transport has been studied in reference [82]. The low effective thermal conductivity of β-$(Al_{0.1}Ga_{0.9})_2O_3/Ga_2O_3$ superlattices due to phonon scattering from multiple interfaces has been reported.[93] Also, chemical reactions that impede thermal transport across various metal/β-Ga_2O_3 interfaces have been reported.[94,95] To this end, the understanding of thermal transport within β-Ga_2O_3 has matured. However, the thermal properties of other interesting polytypes including α-Ga_2O_3 (with a larger E_G=5.3 eV, albeit with concerns associated with its thermal instability[96]) and ε-Ga_2O_3 (which offers potential to form a polarization-induced 2DEG[97]) are yet to be reported.

While diamond can be used as an active host material to construct UWBG semiconductor devices, it will also play a crucial role to mitigate overheating of $Al_xGa_{1-x}N$ and β-Ga_2O_3 electronics through integration efforts. The diamond integration approach has been proven to be effective in the development of GaN-on-diamond RF electronics.[52] The two methods for diamond integration will be (i) direct growth of diamond using microwave chemical vapor deposition (CVD)[98,99] and (ii) bonding of polycrystalline diamond with devices[100,101]. The thermal conductivity of bulk polycrystalline diamond films is generally isotropic and can be as high as 2200 W/mK, which is similar to that of bulk single crystal diamond.[98] However, the thermal conductivity within the first micron of synthesis is much lower than the bulk value and is highly anisotropic due to phonon scattering with nucleation region defects and boundaries of the columnar grains.[102,103] Reports on diamond growth on GaN have shown that the in-plane thermal conductivity of nanocrystalline diamond is less than 100 W/mK while the cross-plane thermal conductivity is less than 200 W/mK within the first micron of film growth.[104,105] As the film grows thicker, the average grain size increases and transitions to a more bulk film behavior with isotropic properties, usually within the first 15 μm of film growth.[106] The lateral grain size within the first micron is often found to be smaller than 200 nm in diameter[104] (**Figure 5 (a)**) while bulk values are seen with diamond grains above a micron in diameter. Therefore, growth methods that can control the rapid expansion of grain size from the diamond seed layer while also controlling texture within the first few microns of growth[107–109] (**Figure 5 (b)**) will create higher thermal conductivity polycrystalline diamond films. Another crucial aspect of diamond integration with UWBG semiconductors is the interfacial thermal boundary resistance (TBR). The lowest TBR for polycrystalline diamond grown on GaN (using a 3 nm SiN_x interlayer) was reported to be ~9.5 m^2K/GW.[110] For both direct growth and bonding methods, the low thermal conductivity of the SiN_x seeding/bonding layer (**Figure 5 (c)**) was shown to dominate the effective TBR at the GaN/diamond interface.[111,112] Recently, the first study on the direct growth of polycrystalline

diamond on β-Ga_2O_3 has been reported (**Figure 5 (a)**).[113] A diamond thermal conductivity and effective diamond/β-Ga_2O_3 TBR of ~110 W/mK and ~30.2 m^2K/GW, respectively, were measured. Experimental studies that demonstrate the enhancement of the $Al_xGa_{1-x}N$ and β-Ga_2O_3 device performance through diamond integration, however, are still in their infancy. For example, the electrical and thermal performance of mechanically exfoliated nano-membrane β-Ga_2O_3 FETs transferred over diamond and sapphire substrates was reported. [114] In general, such Van der Walls bonded structures result in a poor thermal conductance (~17 MW/m^2K)[88], which was shown to improve by 10× for atomic layer deposition (ALD)-grown nanocrystalline β-Ga_2O_3 films on diamond.[115] Perhaps the largest thermal improvement in β-Ga_2O_3 devices is expected from structures bonded with low damage to a diamond substrate.

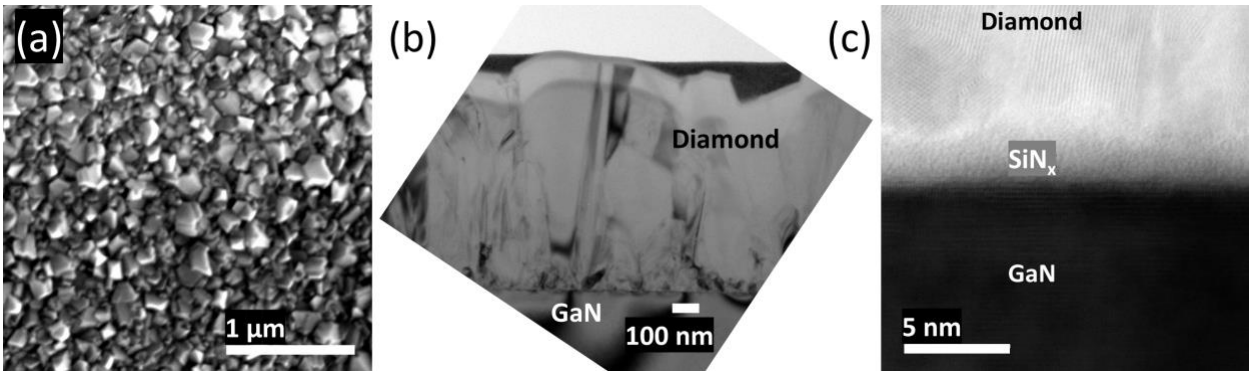

Figure 5. (a) A plan-view scanning electron microscopy (SEM) image of a 267 nm-thick polycrystalline diamond film grown on a $(\bar{2}01)$ β-Ga_2O_3 substrate.[113] Cross-sectional transmission electron microscopy (TEM) images that show (b) the columnar grain growth of polycrystalline diamond and (c) SiN_x seeding/interlayer between the polycrystalline diamond film and the GaN layer underneath.

2. Electro-Thermal Modeling

While mature devices might be represented electro-thermally by analytical models or parameterized circuit models, early and research-level devices commonly are best understood by a method that allows realistic geometry, layouts and (sometimes novel) physics to be inputted. Finite element simulation is a versatile approach suitable for these purposes. Here, the 3D (or 2D-3D hybrid as appropriate) material layout and geometry are discretized and meshed. Appropriate material properties such as the low- and high-field carrier mobility, thermal conductivity, thermal boundary resistances, doping and trap profiles, Ohmic contact resistance (which may have substantial diode-like nonlinearities in early devices), and other relevant factors that may impact electrical and/or thermal transport must be considered to obtain quantitatively meaningful predictive results. Further, as UWBG materials can operate over a wide temperature range, it is easily overlooked that the temperature-dependent material properties over the full temperature range pertinent to the purpose of the simulation must be in place.[116]

The electro-thermal model must self-consistently solve the Poisson, current continuity, drift-diffusion or better (e.g., electro-hydrodynamic), heat generation, and the heat diffusion equations to derive the electrostatic potential, electron concentration, lattice temperature (and sometimes also electron energy/temperature distributions), and trap occupancy statistics as appropriate for the physics in the simulation. Finally, the resulting set of differential equations are discretized and coupled and finally the solution is obtained by a nonlinear iteration method for each condition and bias point of interest. As a side note, the aforementioned process is for steady-state modeling. At

this point, most of the tools needed for transient simulations (e.g., for realistic power switching) are already in place. In particular, the heat capacities, kinetics of trap occupancy (e.g., capture cross-section), and the size of the simulation domain may need to be adjusted to turn a steady-state model into a transient one.

It is important to project the 2D Joule heat distribution obtained from the 2D electrical model along the channel width so that a 3D volumetric heat generation profile is obtained, which is imported into a 3D finite element thermal model. This 2D-3D coupling process is necessary to prevent over-estimation of the channel temperature obtained from the 2D electrical model, which ignores the heat spreading through the absent third dimension. A significant downside of the finite element method can be computational complexity and long simulation times. Some devices allow simplifications without sacrificing accuracy. Oftentimes reflection symmetry can be used to halve or quarter a device such as a field effect transistor (FET) with an even number of fingers or 2D cylindrical symmetry can be used to represent a circular "ring FET" sometimes employed in early device testing. Some details of the electro-thermal modeling of UWBG devices can be found in references [90,116].

Numerous commercial software packages and open-source efforts exist. These can automate the finite element process (e.g., discretization, convergence) well, but at the time of this writing, care must be taken when simulating UWBG materials and physics as these software packages have predominantly a silicon semiconductor heritage. Therefore, one should create material property/parameter files that are accurate over the relevant/wide temperature ranges and make sure physics important to UWBG simulation (e.g., under high electric fields) are properly set up. Examples for various UWBG device simulations include a β-Ga_2O_3 Schottky barrier diode (SBD)[117], metal-oxide-semiconductor field-effect transistor (MOSFET)[118,119], metal-semiconductor field-effect transistor (MESFET)[120,121], MODFET[90], vertical fin field-effect transistor (FinFET)[122], and $Al_xGa_{1-x}N$-channel HEMT[17,79]. Exemplary steady-state simulation results for the heat generation profile and internal temperature distribution of a homoepitaxial β-Ga_2O_3 MOSFET are shown in **Figure 6**. Here, a top-side cooling approach was modeled to draw heat out of the ohmic contacts and the gate, which drove a sharp temperature gradient estimated to peak at 1.2 K/nm due to the low thermal conductivity of β-Ga_2O_3.

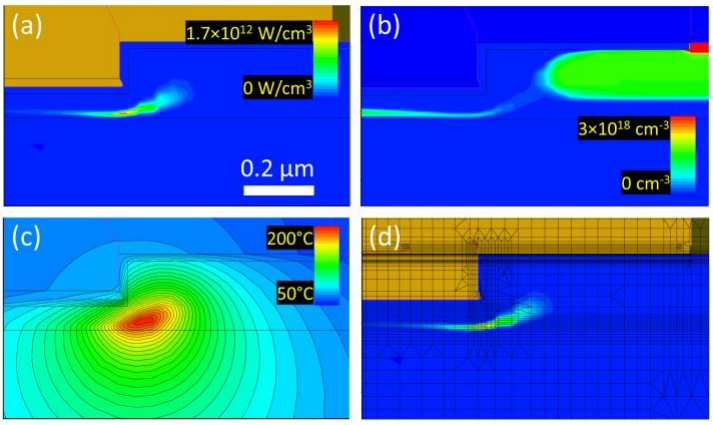

Figure 6. Exemplary simulation results neat the drain side corner of the gate for a homoepitaxial β-Ga_2O_3 MOSFET operating at 5.7 W/mm. (a) The volumetric heat generation profile. (b) The electron density. (c) The cross-sectional temperature field near the drain side corner of the gate where 5°C per division is used for the isothermal contours. (d) The mesh created to perform the simulation.

Transient mixed-mode electro-thermal TCAD simulation was performed on a β-Ga_2O_3 diode in a surge current circuit.[123] An analytical electro-thermal device model was incorporated into a simulation program with integrated circuit emphasis (SPICE) electro-thermal network model to simulate the device temperature rise during the surge transient, considering various packaging configurations.[124] These studies have not accounted for heat spreading in all three dimensions; however, the simplified device modeling schemes allow an understanding of the circuit-level electro-thermal dynamics of the device while employing various die-level cooling packages.

Under the demanding high voltage/power service conditions, extreme heat fluxes and the low thermal conductivity of β-Ga_2O_3 and $Al_xGa_{1-x}N$-based electronics result in the formation of extremely large local electric field spikes and temperature gradients within the device structure. Notably, as macro-scale thermal management improves, the local thermal gradients are expected to get worse. For example, refer to Fig 31.4 and 31.11 of reference [125] for (respectively) a comparative picture of electrical and thermal responses in β-Ga_2O_3. The methods described above and illustrated in **Figure 6** will paint an increasingly incomplete picture for applications such as component lifetime prediction and reliability physics studies that demand accurate estimation of the device peak temperature. Sub-continuum scale quasi-ballistic thermal transport effects that occur under such extreme heat flux and electric field conditions may need to be accounted for by solving the Boltzmann transport equation in the 3D thermal model, instead of the Fourier's law of heat conduction.[57] For the β-Ga_2O_3 materials system, sufficient information[83,126,127] has been gathered to implement such multi-scale multi-physics modeling in practice.

3. Device Thermography

Under high voltage and power operating conditions that lead to nonlinear heat generation within dimensionally scaled UWBG devices, sharp temperature gradients form across the channel region (especially for the low thermal conductivity $Al_xGa_{1-x}N$ and β-Ga_2O_3 systems). Electrical-temperature sensitive parameter (E-TSP) methods[119] are commonly used in industry to estimate the channel/junction temperature and thereby assess the device thermal resistance. However, electrical methods are limited to the measurement of the average temperature across the entire device channel, which results in a significant under estimation of the device peak temperature.[128] Therefore, to validate the electro-thermal device models to be used for the design of thermal management solutions, high-resolution temperature mapping capabilities are necessary. Since the current channel for lateral UWBG devices are located several tens of nanometers below the device surface (**Figure 1**), *in situ* thermography techniques that can probe the surface temperature of the UWBG semiconductor are demanded.

At present, optical thermography techniques such as infrared thermal microscopy, thermoreflectance imaging, and micro-Raman thermometry are commonly used for the temperature mapping of wide bandgap counterparts such as GaN HEMTs.[54,55] However, these techniques are incapable of probing the channel temperature of UWBG devices. Infrared thermography is incapable of probing the semiconductor channel due to its transparency to infrared thermal radiation.[56] It also lacks the spatial resolution (~3 μm)[129], which is necessary to probe the channel peak temperature. This technique has been used to measure the temperature of rough metal electrodes (with relatively large area) of a β-Ga_2O_3 SBD[117] and MOSFET[118] at elevated base temperatures. Thermoreflectance thermal imaging has been used to probe the metal electrode temperature of β-Ga_2O_3 SBDs[117], MOSFET[118], MODFET[90], and $Al_xGa_{1-x}N$-channel HEMTs[17,54,79]. We report in **Figure 7 (a)** the self-heating pattern of a two-finger H-terminated

diamond MESFET under a power dissipation level of 4.2 W/mm. The gate length and width of this device are 1 μm and 120 μm, respectively. However, visible to near-ultraviolet wavelength illumination sources, commonly used for thermoreflectance imaging, cannot probe the channel region because UWBG semiconductors are transparent at these optical wavelength regimes.[57] Micro-Raman thermometry also lacks the sensitivity to measure the UWBG channel surface because optical probing is typically carried out by using a sub-bandgap laser excitation source (e.g., a 532 nm laser). Micro-Raman thermometry for GaN devices[130–132] (e.g., GaN HEMTs) also typically employs a sub-bandgap laser. In this case, the common practice of growing GaN on a dissimilar material (i.e., non-native substrate) gives Raman selectivity to the GaN thickness (commonly ~ 1 μm). For GaN HEMTs, this is arguably sufficient[133], but for UWBG devices, this will typically result in severe depth averaging and underestimation of the channel surface temperature. The standard Raman thermography technique has been used to characterize the cross-sectional temperature field of a β-Ga_2O_3 SBD diced perpendicular to the $(\bar{2}01)$ plane.[117] The optical transparency of the UWBG material and the confocality of the Raman microscope have been leveraged to characterize the temperature rise of the constituent layers (i.e., $Al_xGa_{1-x}N$, AlN, sapphire) of an as-grown $Al_xGa_{1-x}N$-channel HEMT.[79]

At the time being, Raman thermography techniques that take advantage of low-dimensional materials as discrete (i.e., TiO_2 nanoparticles) or continuous (i.e., 2D layered materials) surface temperature transducers are most suitable for measuring the channel surface temperature of UWBG devices. Nanoparticle-assisted Raman thermometry has been used to measure the steady-state temperature rise of discrete points on the channel of β-Ga_2O_3 MOSFETs[119,134], a MODFET[90], and $Al_xGa_{1-x}N$-channel HEMTs[17,79]. This method was also used to study the transient thermal dynamics of $Al_xGa_{1-x}N$-channel HEMTs.[54,79] Reference [135] used nano-particle assisted Raman thermometry to compare the thermal performance of an H-terminated diamond FET with those for devices based on GaN, β-Ga_2O_3, and $Al_xGa_{1-x}N$. 2D material-assisted Raman thermography was developed based on the characterization of a β-Ga_2O_3 MODFET.[136] In **Figure 7 (b)**, we demonstrate continuous surface temperature mapping of an $Al_{0.45}Ga_{0.55}N/Al_{0.3}Ga_{0.7}N$ HEMT using this technique. CVD-grown monolayer MoS_2 was utilized as the surface temperature transducer. The next step will be to develop a high-resolution non-invasive, non-contact method that can directly probe the surface temperature of UWBG devices without such intermediate sensing material. It should be noted that optical methods are most suitable for the characterization of bare-die devices. For packaged devices, de-lidding is necessary to obtain optical access to the device surface.

As a final note, when validating electro-thermal simulation results using local temperature values acquired from the aforementioned optical thermography techniques, it is important to create a temperature probe in the model with dimensions that correspond to the spatial resolution of the experimental method. As shown in **Figure 6 (c)**, very large temperature gradients form in β-Ga_2O_3 and $Al_xGa_{1-x}N$ devices due to the low thermal conductivity of the base materials. Therefore, the simulated device peak temperatures are, in general, much higher than that probed by the optical methods with a spatial resolution on the order of 0.5 – 1 μm.

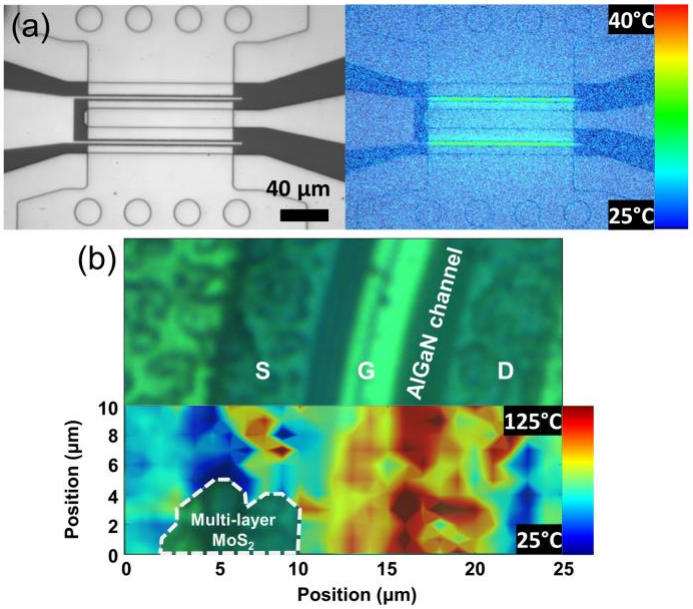

Figure 7. (a) An optical (left) and thermoreflectance image (right) of an H-terminated diamond MESFET operating under V_{GS}=0 V, V_{DS}=-8.9 V, and P=4.2 W/mm. (b) A continuous 2D temperature map of a circular $Al_{0.45}Ga_{0.55}N/Al_{0.3}Ga_{0.7}N$ HEMT under V_{GS}=1.6 V, V_{DS}=29 V, and P=1 W/mm, which was generated by a 2D material-assisted Raman thermography technique. A multi-layer region of the MoS_2 surface temperature transducer was excluded from the resulting thermal image.

4. Device-Level Thermal Management

Both $Al_xGa_{1-x}N$ and β-Ga_2O_3 devices require device-level cooling solutions that locate the thermal heat sink in proximity to (ideally, <1 µm[52]) the heat source (i.e., the 2DEG channel). Here we discuss thermal management scenarios for a β-Ga_2O_3 lateral FET, where the aim is to extract heat from the bottom-side, top-side, or both sides of the device (i.e., double-sided cooling). Most conclusions derived from the foregoing discussion on a β-Ga_2O_3 lateral FET will equally apply to an $Al_xGa_{1-x}N$-channel HEMT.

A recent study[118] on the device-level thermal management of a single-channel β-Ga_2O_3 MOSFET revealed that the channel temperature rise of a homoepitaxial device could (hypothetically) exceed 1500 K under a targeted power dissipation level of 10 W/mm (3D electro-thermal simulation was performed in this work, where the device base temperature was kept at 25°C and the device surface was exposed to natural convection). This corresponds to a junction-to-package thermal resistance (R_{Th}) of 150 mm·K/W, which is unacceptably high. Results in this work highlight that a composite wafer, which consists of a thin β-Ga_2O_3 layer integrated with a high thermal conductivity substrate (e.g., SiC, diamond), can mitigate device overheating. For the β-Ga_2O_3 materials system, composite wafers formed by wafer bonding can serve as platforms for subsequent device fabrication that allow growth of homoepitaxial layers with the highest crystalline quality without threading dislocations. However, to maintain the structural integrity of the composite wafer without causing interface damage, low-temperature film deposition techniques such as low-temperature MOVPE[137] should be used during the device processing steps. The fabrication of a β-Ga_2O_3/SiC composite substrate and subsequent homoepitaxial growth of a high-quality epitaxial

layer via low-temperature MOVPE has been demonstrated.[138] Additional studies on the fabrication of β-Ga_2O_3 composite wafers can be found in references [139–142]. For $Al_xGa_{1-x}N$-based lateral transistors, devices can be directly constructed on high-thermal conductivity single crystal AlN substrates instead of fabricating a composite substrate via wafer bonding.[28,29] Simulation results for bottom-side cooling of an $Al_xGa_{1-x}N$-channel HEMT can be found in reference [79]. To further reduce the R_{Th}, bottom-side cooling methods would need to be augmented by a high-thermal conductivity surface heat spreader (e.g., polycrystalline diamond [113,143]) combined with an active top-side heat extraction mechanism (e.g., air-jet impingement cooling[144]) to form a double-sided cooling platform[90,121,122].

Top-side cooling via flip-chip integration[81] is an alternative approach for the device-level thermal management. The key to accomplishing maximized top-side heat extraction using this configuration is to passivate the device surface with a high-thermal conductivity material (e.g., polycrystalline diamond[113]), locate large-area gold thermal bumps between the device metal electrodes, and use a high-thermal conductivity carrier wafer (e.g., SiC, diamond). While top-side heat extraction alone via flip-chip integration was shown to be sufficient to reduce the device thermal resistance to manageable levels,[79,90,118] one may flip-chip a device fabricated on a composite wafer to maximize the heat transfer performance (i.e., double-sided cooling[90,121,122]).

It should be noted that the experimental evaluation of the improvement in the thermal performance of UWBG devices augmented by such device-level thermal management solutions is still in its infancy. Recently, the effectiveness of bottom-side and double-sided cooling configurations for high-current, packaged β-Ga_2O_3 SBDs has been reported through experiments.[123,145] The thermal management of multi-finger β-Ga_2O_3 and $Al_xGa_{1-x}N$ transistors will be much more challenging than the case of a single-channel device (at identical power density operation), as shown in reference [138], because of the significantly increased device thermal resistance (3-4× higher R_{Th} for a 6-finger β-Ga_2O_3 device as compared to a single finger transistor)[138] due to the thermal cross-talk[146,147]. Similarly, aggravated self-heating of vertically-configured multi-fin β-Ga_2O_3 FinFETs as compared to single-fin β-Ga_2O_3 devices has been reported.[148]

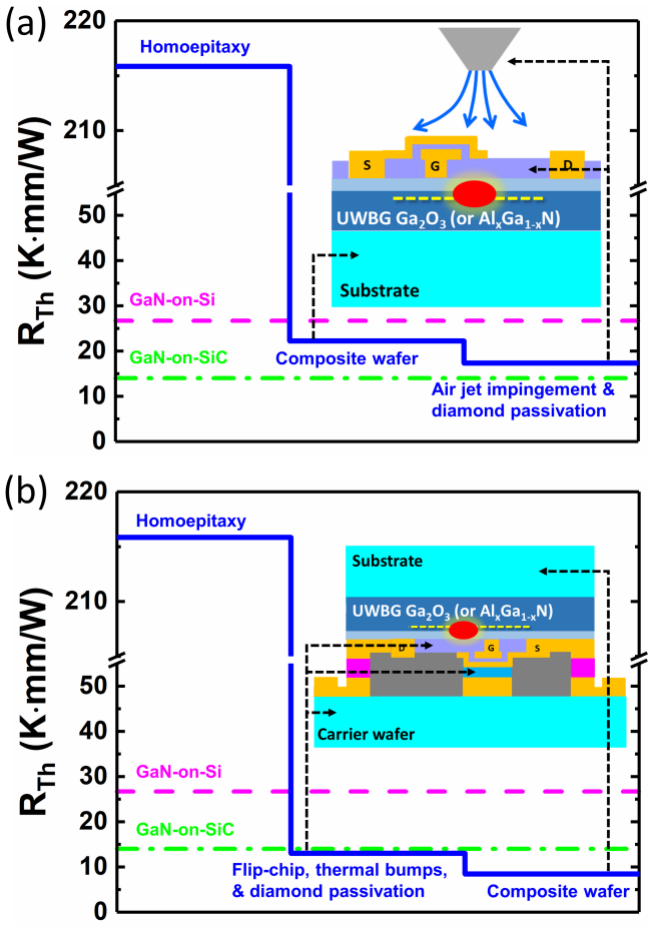

Figure 8. Improvement of the β-Ga_2O_3 device thermal resistance by augmenting the device architecture based on (a) bottom-side (substrate engineering) and (b) top-side (flip-chip integration) cooling solutions.

Exemplary simulation results in **Figure 8 (a)** show that the thermal resistance of a six-finger β-Ga_2O_3 lateral FET with a source-connected field plate (the gate length, gate-to-source distance, gate-to-drain distance, and gate-to-gate pitch are 0.5 μm, 1.3 μm, 4.3 μm, and 45 μm, respectively) can be reduced to a level similar to today's commercial GaN HEMTs fabricated on Si and SiC[130,149] substrates by optimizing the electro-thermal device-design. In this simulation, the homoepitaxial device was augmented by replacing the native substrate with a polycrystalline diamond substrate[150] (the thicknesses of the substrate and the remaining β-Ga_2O_3 layer are 500 μm and 2 μm, respectively), incorporating a 2 μm thick polycrystalline diamond passivation layer[104,105,151], and integrating air-jet impingement cooling with a convective heat transfer coefficient of 17 kW/m^{2}K[144]. Further analysis of the modeling results (not shown) indicate that it is critical to minimize the thickness of the β-Ga_2O_3 layer of the composite substrate[118] and maximize the thermal conductance of the passivation layer by using a high-thermal conductivity material and/or growing it as thick as possible. Simulation results in **Figure 8 (b)** show the flip-chip hetero-integration approach[81] applied to the multi-finger β-Ga_2O_3 device fabricated on a (010)-oriented β-Ga_2O_3 substrate. This device is flip-chipped on a polycrystalline diamond carrier wafer while the device surface is passivated with polycrystalline diamond, and a 2 μm thick gold thermal

bump[152–154] is inserted between the source-connected field plate and the polycrystalline diamond carrier wafer. The device architecture is further augmented by replacing the native substrate with synthetic polycrystalline diamond. The simulation results suggest that the flip-chip integration approach is indeed a viable solution to minimize the device junction-to-package thermal resistance, which can be even lower than that for today's GaN-on-Si power HEMTs and GaN-on-SiC RF power amplifiers. However, it should be noted that the interfacial thermal boundary resistances across various material interfaces between the device surface and the carrier wafer are neglected in this simulation. Also, for this configuration, caution should be taken since any added capacitance may negatively impact the device high-frequency performance. For example, while the source-connected field plate is usually grounded for most RF power amplifiers, the drain electrode experiences a large RF voltage swing. For this reason, a thermal bump was only inserted between the carrier wafer and the source-connected field plate (but not the drain electrode) in the flip-chip configuration shown in **Figure 8 (b)**. For such cases, electrical simulation[155] should accompany the thermal design to estimate the effect of a thermal bump on the device switching performance. More details of this diamond-incorporated flip-chip integration scheme for UWBG lateral devices can be found in reference [156].

Thermal management of H-terminated diamond FETs should be approached from a different angle. As shown in **Figure 7 (a)**, diamond devices exhibit extraordinary thermal performance. Therefore, the need to enhance heat extraction from the device channel is minimal. However, one of the biggest challenges for H-terminated diamond FETs is to preserve the long-term environmental and thermal stability of the transfer-doped 2DHG channel.[42,49] For instance, the C-H bonds and/or the surface adsorbates of an air-exposed H-terminated diamond FET were shown to be detrimentally impacted beyond an ambient temperature of 200°C, resulting in an irreversible loss of the surface p-type conduction.[42] In general, diamond surface properties show a strong dependency on its chemical termination. Although H-terminated surfaces are found to be less reactive than oxygen desorbed surfaces, the instability of the 2DHG can be linked to the vulnerability of the C-H bond when left exposed to air for a significant duration of time. Also, operating conditions can further degrade the hydrogen saturation of the surface. When capped with Al_2O_3, the surface is protected from the atmosphere, in particular, from the hydroxide (OH^-) ions. Although the exact mechanism of the supply of 2DHG under passivation of the surface can be debated, it is possible that the acceptor-like states at the Al_2O_3/diamond interface sources the supply of the 2DHG. The presence of fixed negative charge in the Al_2O_3 can lead to charge enhancement. Stable operation of an H-terminated diamond FET as well as a complementary FET up to 350°C was reported, enabled by an Al_2O_3-based dielectric technology.[157] The stability of the process was attributed to the high-temperature Al_2O_3 deposition which allowed a less susceptible H-termination. A mobility enhancement was also observed as a result of the treatment.

V. Packaging and Industrial Perspective

The potential low cost of β-Ga_2O_3 devices and packages make them very appealing for power electronics for automotive and renewable energy applications.[21] Components based on β-Ga_2O_3 and other UWBG materials could potentially meet the stringent cost and performance targets for automotive power electronics and electric traction drive applications.[158,159] The significant amount of research on SiC-based and to some extent β-Ga_2O_3-based power electronics has focused on reaching the overall converter system-level cost parity with respect to Si-based power electronics, while achieving significant performance and power density gains. This acknowledges the fact that

currently the cost of SiC devices, as an example, is at least a factor of three higher (or more) than that of Si devices. However, starting with a low-cost, high-performance, and reliable power semiconductor device would be very helpful for automotive original equipment manufacturers to make the value proposition of (U)WBG power electronics as compared to Si power electronics. This is because, ultimately the power devices are the starting point and the heart of power conversion systems. This aspect, along with the fact that much higher figures of merit can be obtained from β-Ga_2O_3 and other UWBG materials - as compared to Si, SiC and GaN - makes UWBG power electronics an attractive research direction with potentially high-return.

While substantial research is being conducted on the design and development of novel device configurations,[160] significant questions and challenges related to packaging need to be addressed. Packaging of devices enables electrical connections and functionality, and also device heat dissipation. In most Si- and SiC-based power electronics modules, devices are attached to metalized ceramic substrates which are then soldered to copper or aluminum baseplates to form the module. This is typical for automotive power electronics modules.[161] Module heat is dissipated by directly cooling the bottom of the baseplate or by mounting the module to a cold plate with thermal grease applied at the baseplate-to-cold plate interface. Double-side-cooled packaging doubles the heat rejection area resulting in lower thermal resistance and improves electrical performance by eliminating the restrictive top-side wire bonds.[162]

The low thermal conductivity of β-Ga_2O_3 devices requires packaging solutions that place the heat exchanger near the device heat source. References [123,145] experimentally demonstrated passive thermal management of high-current, packaged β-Ga_2O_3 SBDs via bottom-side and double-sided cooling configurations. In terms of active cooling, finite element modeling has been used to compare the thermal performance of Si, SiC, and β-Ga_2O_3-based power modules under different packaging configurations.[163] The thermal modeling results in this work[163] indicate that top-side cooling of the device with dielectric fluids is an effective thermal management strategy for β-Ga_2O_3 modules, because the cooling solution is in direct contact with the devices. Top-side cooling with dielectric fluids is a potential thermal management solution for both lateral and vertical β-Ga_2O_3 devices and is an improvement over air cooling solutions due to the inferior thermal properties of air. The results show that under steady-state, a β-Ga_2O_3-based package will likely have only about 4% (device-cooled configuration) to 11% (baseplate-cooled configuration) higher thermal resistance than the SiC-based package for a fluid heat transfer coefficient (HTC) of 10,000 W/m^2K; this is a typical HTC obtained from the water-ethylene glycol coolant for numerous vehicular/mobility applications. This work also shows that the short circuit requirements for β-Ga_2O_3 are as stringent as those for SiC and GaN, i.e., the devices and components will have to be designed around these short circuit requirements. Overall, this work[163] points towards the feasibility of UWBG (β-Ga_2O_3)-based packaging for automotive and other applications provided that appropriate UWBG power devices that can operate under adequate voltage and current levels can be fabricated in the future.

Reliability concerns associated with direct fluid contact with devices (e.g., material compatibility, fluid contaminants) can be alleviated by placing copper plates on the top side (or both sides) of the devices and cooling the exposed surfaces of the copper via dielectric fluids. This approach eliminates direct fluid contact with the devices, increases surface area (i.e., fins) for improved thermal performance, and adds thermal mass to mitigate transient heat loads. A similar packaging concept (copper plate bonded to both sides of device, eliminate metalized ceramic substrate) is used by the 2016 Toyota Prius power module, but Si devices cooled with a water-

ethylene glycol solution are utilized.[164] A study[124] modeled the thermal performance of different β-Ga_2O_3 Schottky diode packaging configurations and evaluated a top-side cooling approach. They report that attaching the heat dissipating side of the β-Ga_2O_3 diode (e.g., junction side) to a copper baseplate improves transient thermal performance by eliminating heat conduction through the low-thermally-conductive β-Ga_2O_3 substrate side.

Cooling with dielectric fluids can be improved using jet impingement cooling strategies to provide localized high heat transfer coefficients near the heat sources. The authors have recently investigated a cooling approach using AmpCool-100 dielectric fluid jets impinging on finned copper plates. **Figure 9** below demonstrates recent experimentally validated computational fluid dynamics (CFD) modeling results depicting the AmpCool-100 slot jets cooling a SiC device via single-phase heat transfer to achieve a low junction-to-fluid thermal resistance of 19 mm^2K/W. A similar strategy could be used for UWBG devices. The dielectric fluid approach may be a viable automotive power electronics cooling solution if new driveline fluids (e.g., similar to the automatic transmission fluid) are developed specifically for these applications. Further thermal performance improvements can be made using two-phase (boiling) heat transfer where HTC$\geq$100 kW/m^2K can be achieved.

Thermomechanical stresses are another factor that needs to be considered for reliable packaging of UWBG devices. Diamond devices benefit from their high thermal conductivity but are brittle and have a relatively low coefficient of thermal expansion which presents thermomechanical packaging challenges. Finite element thermomechanical modeling of diamond, Si, and SiC devices mounted on metalized ceramic substrates revealed that diamond results in significantly higher stresses at the die and die attach compared with Si and SiC.[165]

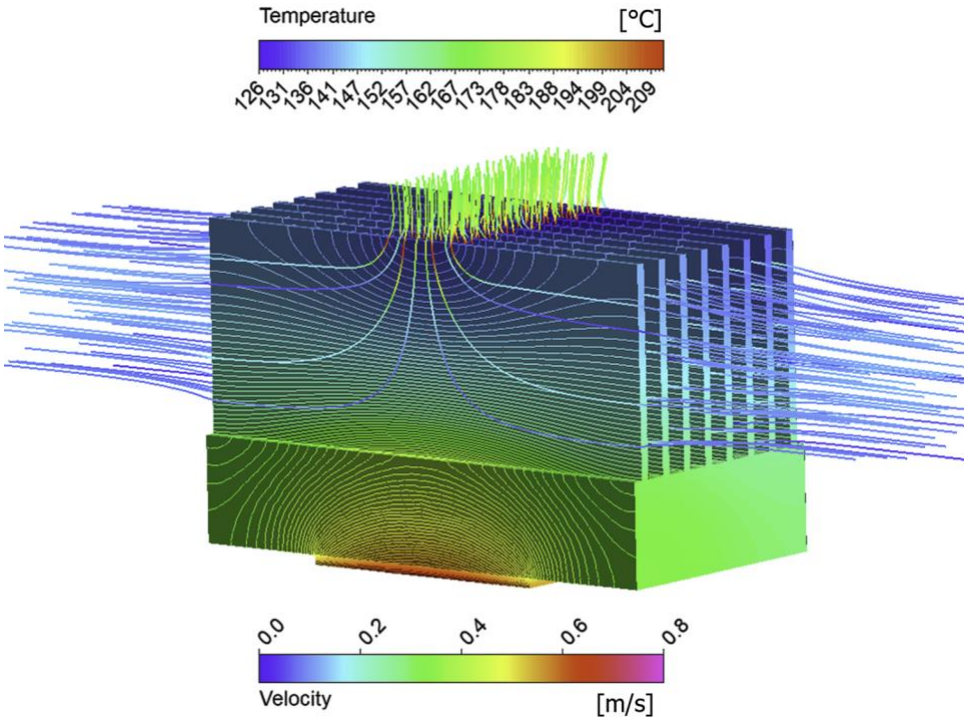

Figure 9. CFD-predicted temperatures and velocity streamlines for a cooling solution using dielectric fluid jets impinging on densely-finned copper plate attached to the top-side of a device. AmpCool-100 fluid enters at 70°C and the 25 mm^2 device dissipates 7,160 kW/m^2.

VI. Conclusion

For legacy semiconductor materials, it was sufficient to consider the thermal aspects after the design and fabrication of an operational device. Doping profiles, channel geometry, and the layer stack were optimized electrically, and the thermal aspects were considered after these were finalized. For UWBG semiconductors, we see evidence that electro-thermal co-design techniques are essential even at this early stage to commercialize high-power, high-voltage, and fast-switching UWBG devices for next-generation power electronics and wireless communication applications. On the materials side, more theoretical and experimental work needs to be done to understand the physics of thermal transport within UWBG materials and solid solutions under extreme electric field and temperature conditions where the effect of structural deformation and electron-phonon interactions will become prominent. On the device side, multi-scale multi-physics models and thermal characterization methods need to be developed that can capture subcontinuum-scale thermal transport mechanisms that may lead to amplified heating within the nanoscopic extreme electric field region of UWBG devices. The newly-developed modeling and characterization methods will become essential tools supporting near-future device reliability studies and temperature-accelerated direct current (DC) operational life tests[149,166,167]. UWBG device architectures must employ device-level thermal management solutions that minimize the device junction-to-package thermal resistance. This device-level electro-thermal co-design process will eventually lead to higher device performance, prolonged component lifetime, and improved system-level size, weight, and power (SWaP) and efficiency.

Acknowledgment

This work was supported by the AFOSR Young Investigator Program (Grant No. FA9550-17-1-0141, Program Officer: Dr. Michael Kendra, Dr. Brett Pokines, also monitored by Dr. Kenneth Goretta) and NSF (CBET-1934482, Program Director: Dr. Ying Sun). Sukwon Choi acknowledges his current/former group members James Spencer Lundh, Bikramjit Chatterjee, Yiwen Song, and Daniel Shoemaker for assisting him with preparing this article. He also acknowledges Joan M. Redwing (Pennsylvania State University), Sriram Krishnamoorthy (University of Utah), Albert G. Baca, Robert J. Kaplar, Thomas E. Beechem (Sandia National Laboratories), and Tony G. Ivanov (Army Research Laboratory) for providing materials and devices used to generate data shown in this work. He also thanks Donald L. Dorsey (Air Force Research Laboratory), Christopher D. Nordquist (Sandia National Laboratories), Brian M. Foley, and Susan E. Trolier-McKinstry (Pennsylvania State University) for fruitful discussions while preparing this prospective article. Research at the Naval Research Laboratory was supported by the Office of Naval Research. This work was authored in part by the National Renewable Energy Laboratory (NREL), operated by Alliance for Sustainable Energy, LLC, for the U.S. Department of Energy (DOE) under Contract No. DE-AC36-08GO28308. Funding was provided by the U.S. DOE and NREL. The views expressed in the article do not necessarily represent the views of the DOE or the U.S. Government. The U.S. Government retains and the publisher, by accepting the article for publication, acknowledges that the U.S. Government retains a nonexclusive, paid-up,

irrevocable, worldwide license to publish or reproduce the published form of this work, or allow others to do so, for U.S. Government purposes.

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

References

[1] H. Amano, M. Kito, K. Hiramatsu, and I. Akasaki, Jpn. J. Appl. Phys. **28**, L2112 (1989).
[2] S. Nakamura, T. Mukai, and M. Senoh, Jpn. J. Appl. Phys. **30**, L1998 (1991).
[3] R.. Trew, G.L. Bilbro, W. Kuang, Y. Liu, and H. Yin, IEEE Microw. Mag. 56 (2005).
[4] I.C. Kizilyalli, Y.A. Xu, E. Carlson, J. Manser, and D.W. Cunningham, in *2017 IEEE 5th Work. Wide Bandgap Power Devices Appl.* (2017), p. 417.
[5] U. Mishra, S. Likun, and T. Kazior, Proc. IEEE **96**, 287 (2008).
[6] J.Y. Tsao, S. Chowdhury, M.A. Hollis, D. Jena, N.M. Johnson, K.A. Jones, R.J. Kaplar, S. Rajan, C.G. Van de Walle, E. Bellotti, C.L. Chua, R. Collazo, M.E. Coltrin, J.A. Cooper, K.R. Evans, S. Graham, T.A. Grotjohn, E.R. Heller, M. Higashiwaki, M.S. Islam, P.W. Juodawlkis, M.A. Khan, A.D. Koehler, J.H. Leach, U.K. Mishra, R.J. Nemanich, R.C.N. Pilawa-Podgurski, J.B. Shealy, Z. Sitar, M.J. Tadjer, A.F. Witulski, M. Wraback, and J.A. Simmons, Adv. Electron. Mater. **4**, 1600501 (2017).
[7] S.J. Pearton, F. Ren, M. Tadjer, and J. Kim, J. Appl. Phys. **124**, 220901 (2018).
[8] C.J.H. Wort and R.S. Balmer, Mater. Today **11**, 22 (2008).
[9] E. Johnson, in *1958 IRE Int. Conv. Rec.* (1965), pp. 27–34.
[10] M.E. Coltrin, A.G. Baca, and R.J. Kaplar, ECS J. Solid State Sci. Technol. **6**, S3114 (2017).
[11] B.J. Baliga, J. Appl. Phys. **53**, 1759 (1982).
[12] Y. Zhang and J.S. Speck, Semicond. Sci. Technol. **35**, 125018 (2020).
[13] Z. Guo, A. Verma, X. Wu, F. Sun, A. Hickman, T. Masui, A. Kuramata, M. Higashiwaki, D. Jena, and T. Luo, Appl. Phys. Lett. **106**, 111909 (2015).
[14] A.G. Baca, A.M. Armstrong, A.A. Allerman, E.A. Douglas, C.A. Sanchez, M.P. King, M.E. Coltrin, T.R. Fortune, and R.J. Kaplar, Appl. Phys. Lett. **109**, 033509 (2016).
[15] S. Russell, S. Sharabi, A. Tallaire, and D.A.J. Moran, IEEE Trans. Electron Devices **62**, 751 (2015).
[16] A.F.M. Anwar, S. Shangli Wu, and R.T. Webster, IEEE Trans. Electron Devices **48**, 567 (2001).
[17] B. Chatterjee, J.S. Lundh, Y. Song, D. Shoemaker, A.G. Baca, R.J. Kaplar, T.E. Beechem, C. Saltonstall, A.A. Allerman, A.M. Armstrong, B.A. Klein, A. Bansal, H.R. Seyf, D. Talreja, A. Pogrebnyakov, E. Heller, V. Gopalan, A.S. Henry, J.M. Redwing, B. Foley, and S. Choi, IEEE Electron Device Lett. **43**, 461 (2020).
[18] S.J. Pearton, J. Yang, P.H. Cary, F. Ren, J. Kim, M.J. Tadjer, and M.A. Mastro, Appl. Phys. Rev. **5**, 11301 (2018).
[19] K. Ghosh and U. Singisetti, J. Appl. Phys. **124**, 85707 (2018).
[20] Y. Zhang, C. Joishi, Z. Xia, M. Brenner, S. Lodha, and S. Rajan, Appl. Phys. Lett. **112**, 233503 (2018).
[21] S.B. Reese, T. Remo, J. Green, and A. Zakutayev, Joule **3**, 903 (2019).

[22] R.R. Pelá, C. Caetano, M. Marques, L.G. Ferreira, J. Furthmüller, and L.K. Teles, Appl. Phys. Lett. **98**, 151907 (2011).
[23] O. Ambacher, J. Smart, J.R. Shealy, N.G. Weimann, K. Chu, M. Murphy, W.J. Schaff, L.F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, J. Appl. Phys. **85**, 3222 (1999).
[24] A.G. Baca, A.M. Armstrong, B.A. Klein, A.A. Allerman, E.A. Douglas, and R.J. Kaplar, J. Vac. Sci. Technol. A **38**, 20803 (2020).
[25] A.G. Baca, A.M. Armstrong, A.A. Allerman, B.A. Klein, E.A. Douglas, C.A. Sanchez, and T.R. Fortune, ECS J. Solid State Sci. Technol. **6**, S3010 (2017).
[26] A.G. Baca, B.A. Klein, A.A. Allerman, A.M. Armstrong, E.A. Douglas, C.A. Stephenson, T.R. Fortune, and R.J. Kaplar, ECS J. Solid State Sci. Technol. **6**, Q161 (2017).
[27] S.H. Sohel, A. Xie, E. Beam, H. Xue, T. Razzak, S. Bajaj, S. Campbell, D. White, K. Wills, Y. Cao, W. Lu, and S. Rajan, Appl. Phys. Express **13**, 36502 (2020).
[28] H. Tokuda, M. Hatano, N. Yafune, S. Hashimoto, K. Akita, Y. Yamamoto, and M. Kuzuhara, Appl. Phys. Express **3**, 121003 (2010).
[29] N. Yafune, K. Akita, S. Hashimoto, M. Kuzuhara, Y. Yamamoto, and H. Tokuda, Electron. Lett. **50**, 211 (2014).
[30] M. Shatalov, W. Sun, R. Jain, A. Lunev, X. Hu, A. Dobrinsky, Y. Bilenko, J. Yang, G.A. Garrett, L.E. Rodak, M. Wraback, M. Shur, and R. Gaska, Semicond. Sci. Technol. **29**, 84007 (2014).
[31] M. Higashiwaki and G.H. Jessen, Appl. Phys. Lett. **112**, 60401 (2018).
[32] M. Higashiwaki, K. Sasaki, H. Murakami, Y. Kumagai, A. Koukitu, A. Kuramata, T. Masui, and S. Yamakoshi, Semicond. Sci. Technol. **31**, 34001 (2016).
[33] G. Seryogin, F. Alema, N. Valente, H. Fu, E. Steinbrunner, A.T. Neal, S. Mou, A. Fine, and A. Osinsky, Appl. Phys. Lett. **117**, 262101 (2020).
[34] Y. Zhang, Z. Xia, J. Mcglone, W. Sun, C. Joishi, A.R. Arehart, S.A. Ringel, and S. Rajan, IEEE Trans. Electron Devices **66**, 1574 (2019).
[35] M.J. Tadjer, F. Alema, A. Osinsky, M.A. Mastro, N. Nepal, J.M. Woodward, R.L. Myers-Ward, E.R. Glaser, J.A. Freitas, A.G. Jacobs, J.C. Gallagher, A.L. Mock, D.J. Pennachio, J. Hajzus, M. Ebrish, T.J. Anderson, K.D. Hobart, J.K. Hite, and C.R. Eddy Jr., J. Phys. D. Appl. Phys. **54**, 34005 (2020).
[36] N. Ma, N. Tanen, A. Verma, Z. Guo, T. Luo, H. (Grace) Xing, and D. Jena, Appl. Phys. Lett. **109**, 212101 (2016).
[37] K. Ghosh and U. Singisetti, J. Mater. Res. **32**, 4142 (2017).
[38] R. Kalish, J. Phys. D. Appl. Phys. **40**, 6467 (2007).
[39] K. Hirama, H. Takayanagi, S. Yamauchi, Y. Jingu, H. Umezawa, and H. Kawarada, in *2007 IEEE Int. Electron Devices Meet.* (2007), pp. 873–876.
[40] S.A.O. Russell, L. Cao, D. Qi, A. Tallaire, K.G. Crawford, A.T.S. Wee, and D.A.J. Moran, Appl. Phys. Lett. **103**, 202112 (2013).
[41] K.G. Crawford, L. Cao, D. Qi, A. Tallaire, E. Limiti, C. Verona, A.T.S. Wee, and D.A.J. Moran, Appl. Phys. Lett. **108**, 42103 (2016).
[42] K.G. Crawford, D. Qi, J. McGlynn, T.G. Ivanov, P.B. Shah, J. Weil, A. Tallaire, A.Y. Ganin, and D.A.J. Moran, Sci. Rep. **8**, 3342 (2018).
[43] M. Kasu and T. Oishi, in *2016 IEEE Compd. Semicond. Integr. Circuit Symp.* (2016), pp. 1–4.
[44] T.G. Ivanov, J. Weil, P.B. Shah, A.G. Birdwell, K. Kingkeo, and E.A. Viveiros, in *2018 IEEE/MTT-S Int. Microw. Symp. - IMS* (2018), pp. 1461–1463.

[45] M.H. Wong and M. Higashiwaki, IEEE Trans. Electron Devices **67**, 3925 (2020).
[46] W. Li, K. Nomoto, Z. Hu, D. Jena, and H.G. Xing, IEEE Trans. Electron Devices **67**, 3938 (2020).
[47] M. Dutta, F.A.M. Koeck, W. Li, R.J. Nemanich, and S. Chowdhury, IEEE Electron Device Lett. **38**, 600 (2017).
[48] M. Malakoutian, M. Benipal, F.A. Koeck, R.J. Nemanich, and S. Chowdhury, IEEE J. Electron Devices Soc. **8**, 614 (2020).
[49] H. Kawarada, H. Tsuboi, T. Naruo, T. Yamada, D. Xu, A. Daicho, T. Saito, and A. Hiraiwa, Appl. Phys. Lett. **105**, 13510 (2014).
[50] R. Gaska, A. Osinsky, J.W. Yang, and M.S. Shur, IEEE Electron Device Lett. **19**, 89 (1998).
[51] S. Choi, E. Heller, D. Dorsey, R. Vetury, and S. Graham, J. Appl. Phys. **114**, 164501 (2013).
[52] A. Bar-Cohen, J.J. Maurer, and D.H. Altman, J. Electron. Packag. **141**, 040803 (2019).
[53] E.R. Heller and A. Crespo, Microelectron. Reliab. **48**, 45 (2008).
[54] J.S. Lundh, Y. Song, B. Chatterjee, A.G. Baca, R.J. Kaplar, A.M. Armstrong, A.A. Allerman, B.A. Klein, D. Kendig, H. Kim, and S. Choi, J. Electron. Packag. **142**, 031113 (2020).
[55] S.K. Oh, J.S. Lundh, S. Shervin, B. Chatterjee, D.K. Lee, S. Choi, J.S. Kwak, and J.-H. Ryou, J. Electron. Packag. **141**, 20801 (2019).
[56] A. Sarua, H. Hangfeng Ji, M. Kuball, M.J. Uren, T. Martin, K.P. Hilton, and R.S. Balmer, IEEE Trans. Electron Devices **53**, 2438 (2006).
[57] B. Chatterjee, C. Dundar, T.E. Beechem, E. Heller, D. Kendig, H. Kim, N. Donmezer, and S. Choi, J. Appl. Phys. **127**, 44502 (2020).
[58] W. Liu and A.A. Balandin, J. Appl. Phys. **97**, 073710 (2005).
[59] W. Liu and A.A. Balandin, Appl. Phys. Lett. **85**, 5230 (2004).
[60] B.C. Daly, H.J. Maris, W.K. Ford, G.A. Antonelli, L. Wong, and E. Andideh, J. Appl. Phys. **92**, 6005 (2002).
[61] D.G. Cahill, Rev. Sci. Instrum. **75**, 5119 (2004).
[62] A.J. Schmidt, R. Cheaito, and M. Chiesa, Rev. Sci. Instrum. **80**, 094901 (2009).
[63] T.E. Beechem, A.E. McDonald, E.J. Fuller, A.A. Talin, C.M. Rost, J.-P. Maria, J.T. Gaskins, P.E. Hopkins, and A.A. Allerman, J. Appl. Phys. **120**, 95104 (2016).
[64] Q. Zheng, C. Li, A. Rai, J.H. Leach, D.A. Broido, and D.G. Cahill, Phys. Rev. Mater. **3**, 14601 (2019).
[65] Y. Song, J. Lundh, W. Wang, J. Leach, D. Eichfeld, A. Krishnan, C. Perez, D. Ji, T. Borman, K. Ferri, J.-P. Maria, S. Chowdhury, J.-H. Ryou, B. Foley, and S. Choi, J. Electron. Packag. **142**, 041112 (2020).
[66] Y.R. Koh, Z. Cheng, A. Mamun, M.S. Bin Hoque, Z. Liu, T. Bai, K. Hussain, M.E. Liao, R. Li, J.T. Gaskins, A. Giri, J. Tomko, J.L. Braun, M. Gaevski, E. Lee, L. Yates, M.S. Goorsky, T. Luo, A. Khan, S. Graham, and P.E. Hopkins, ACS Appl. Mater. Interfaces **12**, 29443 (2020).
[67] G.A. Slack, R.A. Tanzilli, R.O. Pohl, and J.W. Vandersande, J. Phys. Chem. Solids **48**, 641 (1987).
[68] R.L. Xu, M. Munõz Rojo, S.M. Islam, A. Sood, B. Vareskic, A. Katre, N. Mingo, K.E. Goodson, H.G. Xing, D. Jena, and E. Pop, J. Appl. Phys. **126**, (2019).
[69] B. Abeles, Phys. Rev. **131**, 1906 (1963).
[70] S. Adachi, J. Appl. Phys. **102**, 63502 (2007).
[71] H.R. Seyf, L. Yates, T.L. Bougher, S. Graham, B.A. Cola, T. Detchprohm, M.-H. Ji, J. Kim, R. Dupuis, W. Lv, and A. Henry, Npj Comput. Mater. **3**, 49 (2017).
[72] E. Ziade, J. Yang, G. Brummer, D. Nothern, T. Moustakas, and A.J. Schmidt, Appl. Phys.

Lett. **107**, 91605 (2015).
[73] E. Ziade, J. Yang, G. Brummer, D. Nothern, T. Moustakas, and A.J. Schmidt, Appl. Phys. Lett. **110**, 31903 (2017).
[74] D.Q. Tran, N. Blumenschein, A. Mock, P. Sukkaew, H. Zhang, J.F. Muth, T. Paskova, P.P. Paskov, and V. Darackchieva, Phys. B Condens. Matter 411810 (2019).
[75] T.E. Beechem, C.B. Saltonstall, and A.A. Allerman, *Size Dictated Thermal Conductivity of GaN and AlGaN* (2018).
[76] A.G. Baca, A.M. Armstrong, A.A. Allerman, B.A. Klein, E.A. Douglas, C.A. Sanchez, and T.R. Fortune, ECS J. Solid State Sci. Technol. **6**, S3010 (2017).
[77] S. Mollah, K. Hussain, R. Floyd, A. Mamun, M. Gaevski, M.V.S. Chandrashekhar, I. Ahmad, G. Simin, V. Wheeler, C. Eddy, and A. Khan, Phys. Status Solidi **217**, 1900802 (2020).
[78] P.H. Carey, F. Ren, A.G. Baca, B.A. Klein, A.A. Allerman, A.M. Armstrong, E.A. Douglas, R.J. Kaplar, P.G. Kotula, and S.J. Pearton, IEEE J. Electron Devices Soc. **7**, 444 (2019).
[79] J.S. Lundh, B. Chatterjee, Y. Song, A.G. Baca, R.J. Kaplar, T.E. Beechem, A.A. Allerman, A.M. Armstrong, B.A. Klein, A. Bansal, D. Talreja, A. Pogrebnyakov, E. Heller, V. Gopalan, J.M. Redwing, B.M. Foley, and S. Choi, Appl. Phys. Lett. **115**, 153503 (2019).
[80] B.F. Donovan, C.J. Szwejkowski, J.C. Duda, R. Cheaito, J.T. Gaskins, C.-Y. Peter Yang, C. Constantin, R.E. Jones, and P.E. Hopkins, Appl. Phys. Lett. **105**, 203502 (2014).
[81] S. Choi, G.M. Peake, G.A. Keeler, K.M. Geib, R.D. Briggs, T.E. Beechem, R.A. Shaffer, J. Clevenger, G.A. Patrizi, J.F. Klem, A. Tauke-Pedretti, and C.D. Nordquist, IEEE Trans. Components, Packag. Manuf. Technol. **6**, 740 (2016).
[82] Y. Song, P. Ranga, Y. Zhang, Z. Feng, H.-L. Huang, M.D. Santia, S.C. Badescu, C.U. Gonzalez-Valle, C. Perez, K. Ferri, R.M. Lavelle, D.W. Snyder, B.A. Klein, J. Deitz, A.G. Baca, J.-P. Maria, B. Ramos-Alvarado, J. Hwang, H. Zhao, X. Wang, S. Krishnamoorthy, B.M. Foley, and S. Choi, ACS Appl. Mater. Interfaces **13**, 38477 (2021).
[83] M.D. Santia, N. Tandon, and J.D. Albrecht, Appl. Phys. Lett. **107**, 41907 (2015).
[84] P. Jiang, X. Qian, X. Li, and R. Yang, Appl. Phys. Lett. **113**, 232105 (2018).
[85] Z. Yan and S. Kumar, Phys. Chem. Chem. Phys. **20**, 29236 (2018).
[86] M. Slomski, N. Blumenschein, P.P. Paskov, J.F. Muth, and T. Paskova, J. Appl. Phys. **121**, 235104 (2017).
[87] Y. Zhang, Q. Su, J. Zhu, S. Koirala, S.J. Koester, and X. Wang, Appl. Phys. Lett. **116**, 202101 (2020).
[88] Z. Cheng, L. Yates, J. Shi, M.J. Tadjer, K.D. Hobart, and S. Graham, APL Mater. **7**, 31118 (2019).
[89] N. Blumenschein, M. Slomski, P.P. Paskov, F. Kaess, M.H. Breckenridge, J.F. Muth, and T. Paskova, in *Proc.SPIE* (2018).
[90] B. Chatterjee, Y. Song, J.S. Lundh, Y. Zhang, Z. Xia, Z. Islam, J. Leach, C. McGray, P. Ranga, S. Krishnamoorthy, A. Haque, S. Rajan, and S. Choi, Appl. Phys. Lett. **117**, 153501 (2020).
[91] P. Ranga, A. Bhattacharyya, A. Chmielewski, S. Roy, R. Sun, M.A. Scarpulla, N. Alem, and S. Krishnamoorthy, Appl. Phys. Express **14**, 25501 (2021).
[92] H. Peelaers, J.B. Varley, J.S. Speck, and C.G. Van de Walle, Appl. Phys. Lett. **112**, 242101 (2018).
[93] Z. Cheng, N. Tanen, C. Chang, J. Shi, J. McCandless, D. Muller, D. Jena, H.G. Xing, and S. Graham, Appl. Phys. Lett. **115**, 92105 (2019).
[94] J. Shi, C. Yuan, H.-L. Huang, J. Johnson, C. Chae, S. Wang, R. Hanus, S. Kim, Z. Cheng, J.

Hwang, and S. Graham, ACS Appl. Mater. Interfaces **13**, 29083 (2021).
[95] H.T. Aller, X. Yu, A. Wise, R.S. Howell, A.J. Gellman, A.J.H. McGaughey, and J.A. Malen, Nano Lett. **19**, 8533 (2019).
[96] E. Ahmadi and Y. Oshima, J. Appl. Phys. **126**, 160901 (2019).
[97] S.B. Cho and R. Mishra, Appl. Phys. Lett. **112**, 162101 (2018).
[98] T. Bai, Y. Wang, T.I. Feygelson, M.J. Tadjer, K.D. Hobart, N.J. Hines, L. Yates, S. Graham, J. Anaya, M. Kuball, and M.S. Goorsky, ECS J. Solid State Sci. Technol. **9**, 53002 (2020).
[99] D.E. Field, J.A. Cuenca, M. Smith, S.M. Fairclough, F.C.-P. Massabuau, J.W. Pomeroy, O. Williams, R.A. Oliver, I. Thayne, and M. Kuball, ACS Appl. Mater. Interfaces **12**, 54138 (2020).
[100] Z. Cheng, F. Mu, L. Yates, T. Suga, and S. Graham, ACS Appl. Mater. Interfaces **12**, 8376 (2020).
[101] P. Chao, K. Chu, C. Creamer, J. Diaz, T. Yurovchak, M. Shur, R. Kallaher, C. McGray, G.D. Via, and J.D. Blevins, IEEE Trans. Electron Devices **62**, 3658 (2015).
[102] A. Sood, R. Cheaito, T. Bai, H. Kwon, Y. Wang, C. Li, L. Yates, T. Bougher, S. Graham, M. Asheghi, M. Goorsky, and K.E. Goodson, Nano Lett. **18**, 3466 (2018).
[103] E. Bozorg-Grayeli, A. Sood, M. Asheghi, V. Gambin, R. Sandhu, T.I. Feygelson, B.B. Pate, K. Hobart, and K.E. Goodson, Appl. Phys. Lett. **102**, 111907 (2013).
[104] J. Anaya, S. Rossi, M. Alomari, E. Kohn, L. Tóth, B. Pécz, K.D. Hobart, T.J. Anderson, T.I. Feygelson, B.B. Pate, and M. Kuball, Acta Mater. **103**, 141 (2016).
[105] Y. Zhou, R. Ramaneti, J. Anaya, S. Korneychuk, J. Derluyn, H. Sun, J. Pomeroy, J. Verbeeck, K. Haenen, and M. Kuball, Appl. Phys. Lett. **111**, 041901 (2017).
[106] L. Yates, A. Sood, Z. Cheng, T. Bougher, K. Malcolm, J. Cho, M. Asheghi, K. Goodson, M. Goorsky, F. Faili, D.J. Twitchen, and S. Graham, in *2016 IEEE Compd. Semicond. Integr. Circuit Symp.* (2016), pp. 1–4.
[107] M. Malakoutian, M.A. Laurent, and S. Chowdhury, Crystals **9**, 498 (2019).
[108] M.A. Laurent, M. Malakoutian, and S. Chowdhury, Semicond. Sci. Technol. **35**, 15003 (2019).
[109] M. Malakoutian, C. Ren, K. Woo, H. Li, and S. Chowdhury, Cryst. Growth Des. **21**, 2624 (2021).
[110] L. Yates, J. Anderson, X. Gu, C. Lee, T. Bai, M. Mecklenburg, T. Aoki, M.S. Goorsky, M. Kuball, E.L. Piner, and S. Graham, ACS Appl. Mater. Interfaces **10**, 24302 (2018).
[111] H. Sun, R.B. Simon, J.W. Pomeroy, D. Francis, F. Faili, D.J. Twitchen, and M. Kuball, Appl. Phys. Lett. **106**, 111906 (2015).
[112] J. Cho, D. Francis, D.H. Altman, M. Asheghi, and K.E. Goodson, J. Appl. Phys. **121**, 055105 (2017).
[113] M. Malakoutian, Y. Song, C. Yuan, C. Ren, J.S. Lundh, R.M. Lavelle, J.E. Brown, D.W. Snyder, S. Graham, S. Choi, and S. Chowdhury, Appl. Phys. Express **14**, 055502 (2021).
[114] J. Noh, S. Alajlouni, M.J. Tadjer, J.C. Culbertson, H. Bae, M. Si, H. Zhou, P.A. Bermel, A. Shakouri, and P.D. Ye, IEEE J. Electron Devices Soc. **7**, 914 (2019).
[115] Z. Cheng, V.D. Wheeler, T. Bai, J. Shi, M.J. Tadjer, T. Feygelson, K.D. Hobart, M.S. Goorsky, and S. Graham, Appl. Phys. Lett. **116**, 62105 (2020).
[116] B. Chatterjee, Electro-Thermal Investigation of Next Generation Wide Bandgap Electronics, The Pennsylvania State University, 2020.
[117] B. Chatterjee, A. Jayawardena, E. Heller, D.W. Snyder, S. Dhar, and S. Choi, Rev. Sci. Instrum. **89**, 114903 (2018).
[118] B. Chatterjee, K. Zeng, C.D. Nordquist, U. Singisetti, and S. Choi, IEEE Trans. Components,

Packag. Manuf. Technol. **9**, 2352 (2019).
[119] N.A. Blumenschein, N.A. Moser, E.R. Heller, N.C. Miller, A.J. Green, A. Popp, A. Crespo, K. Leedy, M. Lindquist, T. Moule, S. Dalcanale, E. Mercado, M. Singh, J.W. Pomeroy, M. Kuball, G. Wagner, T. Paskova, J.F. Muth, K.D. Chabak, and G.H. Jessen, IEEE Trans. Electron Devices **67**, 204 (2020).
[120] N. Kumar, D. Vaca, C. Joishi, Z. Xia, S. Rajan, and S. Kumar, IEEE Electron Device Lett. **41**, 641 (2020).
[121] C. Yuan, Y. Zhang, R. Montgomery, S. Kim, J. Shi, A. Mauze, T. Itoh, J.S. Speck, and S. Graham, J. Appl. Phys. **127**, 154502 (2020).
[122] R.H. Montgomery, Y. Zhang, C. Yuan, S. Kim, J. Shi, T. Itoh, A. Mauze, S. Kumar, J. Speck, and S. Graham, J. Appl. Phys. **129**, 85301 (2021).
[123] M. Xiao, B. Wang, J. Liu, R. Zhang, Z. Zhang, C. Ding, S. Lu, K. Sasaki, G.-Q. Lu, C. Buttay, and Y. Zhang, IEEE Trans. Power Electron. **36**, 8565 (2021).
[124] C. Buttay, H.-Y. Wong, B. Wang, M. Xiao, C. Dimarino, and Y. Zhang, Microelectron. Reliab. **114**, 113743 (2020).
[125] M. Higashiwaki and S. Fujita, *Gallium Oxide: Materials Properties, Crystal Growth, and Devices* (Springer Nature, 2020).
[126] M. Schubert, R. Korlacki, S. Knight, T. Hofmann, S. Schöche, V. Darakchieva, E. Janzén, B. Monemar, D. Gogova, Q.-T. Thieu, R. Togashi, H. Murakami, Y. Kumagai, K. Goto, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, Phys. Rev. B **93**, 125209 (2016).
[127] K. Ghosh and U. Singisetti, Appl. Phys. Lett. **109**, 72102 (2016).
[128] N. Killat, M. Kuball, T.-M. Chou, U. Chowdhury, and J. Jimenez, in *2010 IEEE Int. Reliab. Phys. Symp.* (IEEE, 2010), pp. 528–531.
[129] J. Dallas, G. Pavlidis, B. Chatterjee, J.S. Lundh, M. Ji, J. Kim, T. Kao, T. Detchprohm, R.D. Dupuis, S. Shen, S. Graham, and S. Choi, Appl. Phys. Lett. **112**, 73503 (2018).
[130] S. Choi, E.R. Heller, D. Dorsey, R. Vetury, and S. Graham, IEEE Trans. Electron Devices **60**, 1898 (2013).
[131] T. Beechem, A. Christensen, S. Graham, and D. Green, J. Appl. Phys. **103**, 124501 (2008).
[132] M. Kuball and J.W. Pomeroy, IEEE Trans. Device Mater. Reliab. **16**, 667 (2016).
[133] R. Pearson, B. Chatterjee, S. Kim, S. Graham, A. Rattner, and S. Choi, J. Electron. Packag. **142**, 021012 (2020).
[134] J.W. Pomeroy, C. Middleton, M. Singh, S. Dalcanale, M.J. Uren, M.H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, M. Higashiwaki, and M. Kuball, IEEE Electron Device Lett. **40**, 189 (2019).
[135] J.S. Lundh, D. Shoemaker, A.G. Birdwell, J.D. Weil, L.M. De La Cruz, P.B. Shah, K.G. Crawford, T.G. Ivanov, H.Y. Wong, and S. Choi, Appl. Phys. Lett. **119**, 143502 (2021).
[136] J.S. Lundh, T. Zhang, Y. Zhang, Z. Xia, M. Wetherington, Y. Lei, E. Kahn, S. Rajan, M. Terrones, and S. Choi, ACS Appl. Electron. Mater. **2**, 2945 (2020).
[137] A. Bhattacharyya, P. Ranga, S. Roy, J. Ogle, L. Whittaker-Brooks, and S. Krishnamoorthy, Appl. Phys. Lett. **117**, 142102 (2020).
[138] Y. Song, D. Shoemaker, J.H. Leach, C. McGray, H.-L. Huang, A. Bhattacharyya, Y. Zhang, C.U. Gonzalez-Valle, T. Hess, S. Zhukovsky, K. Ferri, R.M. Lavelle, C. Perez, D.W. Snyder, J.-P. Maria, B. Ramos-Alvarado, X. Wang, S. Krishnamoorthy, J. Hwang, B.M. Foley, and S. Choi, ACS Appl. Mater. Interfaces (2021).
[139] C.-H. Lin, N. Hatta, K. Konishi, S. Watanabe, A. Kuramata, K. Yagi, and M. Higashiwaki, Appl. Phys. Lett. **114**, 32103 (2019).

[140] Z. Cheng, F. Mu, T. You, W. Xu, J. Shi, M.E. Liao, Y. Wang, K. Huynh, T. Suga, M.S. Goorsky, X. Ou, and S. Graham, ACS Appl. Mater. Interfaces **12**, 44943 (2020).
[141] W. Xu, Y. Wang, T. You, X. Ou, G. Han, H. Hu, S. Zhang, F. Mu, T. Suga, Y. Zhang, Y. Hao, and X. Wang, in *2019 IEEE Int. Electron Devices Meet.* (2019), pp. 12.5.1-12.5.4.
[142] Y. Wang, W. Xu, G. Han, T. You, F. Mu, H. Hu, Y. Liu, X. Zhang, H. Huang, T. Suga, X. Ou, X. Ma, and Y. Hao, IEEE Trans. Electron Devices **68**, 1185 (2021).
[143] M.J. Tadjer, T.J. Anderson, M.G. Ancona, P.E. Raad, P. Komarov, T. Bai, J.C. Gallagher, A.D. Koehler, M.S. Goorsky, D.A. Francis, K.D. Hobart, and F.J. Kub, IEEE Electron Device Lett. **40**, 881 (2019).
[144] B. Kwon, T. Foulkes, T. Yang, N. Miljkovic, and W.P. King, IEEE Trans. Components, Packag. Manuf. Technol. **10**, 220 (2020).
[145] B. Wang, M. Xiao, J. Knoll, C. Buttay, K. Sasaki, G.-Q. Lu, C. Dimarino, and Y. Zhang, IEEE Electron Device Lett. **42**, 1132 (2021).
[146] A. Manoi, J.W. Pomeroy, R. Lossy, R. Pazirandeh, J. Würfl, M.J. Uren, T. Martin, and M. Kuball, Solid. State. Electron. **57**, 14 (2011).
[147] B. Chatterjee, D. Ji, A. Agarwal, S.H. Chan, S. Chowdhury, and S. Choi, IEEE Electron Device Lett. **42**, 723 (2021).
[148] B. Chatterjee, W. Li, K. Nomoto, H.G. Xing, and S. Choi, Appl. Phys. Lett. **119**, 103502 (2021).
[149] S. Choi, E.R. Heller, D. Dorsey, R. Vetury, and S. Graham, IEEE Trans. Electron Devices **60**, 159 (2013).
[150] D. Altman, M. Tyhach, J. McClymonds, S. Kim, S. Graham, J. Cho, K. Goodson, D. Francis, F. Faili, F. Ejeckam, and S. Bernstein, Fourteenth Intersoc. Conf. Therm. Thermomechanical Phenom. Electron. Syst. 1199 (2014).
[151] E.O. Ziade, Thermal Transport in Thin Films and across Interfaces, Boston University, 2017.
[152] S. Jangam and S.S. Iyer, IEEE Trans. Components, Packag. Manuf. Technol. **10**, 1758 (2020).
[153] R. Mahajan, Z. Qian, R.S. Viswanath, S. Srinivasan, K. Aygün, W. Jen, S. Sharan, and A. Dhall, IEEE Trans. Components, Packag. Manuf. Technol. **9**, 1952 (2019).
[154] S.S. Iyer, S. Jangam, and B. Vaisband, IBM J. Res. Dev. **63**, 5:1 (2019).
[155] B.D. Tierney, S. Choi, S. DasGupta, J.R. Dickerson, S. Reza, R.J. Kaplar, A.G. Baca, and M.J. Marinella, IEEE Trans. Electron Devices **64**, 3740 (2017).
[156] D. Shoemaker, M. Malakoutian, B. Chatterjee, Y. Song, S. Kim, B.M. Foley, S. Graham, C.D. Nordquist, S. Chowdhury, and S. Choi, IEEE Trans. Components, Packag. Manuf. Technol. **11**, 1177 (2021).
[157] C. Ren, M. Malakoutian, S. Li, and S. Chowdhury, in *2020 Device Res. Conf.* (2020), pp. 1–2.
[158] S. Chowdhury, E. Gurpinar, G.-J. Su, T. Raminosoa, T.A. Burress, and B. Ozpineci, in *2019 IEEE Transp. Electrif. Conf. Expo* (2019), pp. 1–8.
[159] M. Muratori, M. Alexander, D. Arent, M. Bazilian, P. Cazzola, E.M. Dede, J. Farrell, C. Gearhart, D. Greene, A. Jenn, M. Keyser, T. Lipman, S. Narumanchi, A. Pesaran, R. Sioshansi, E. Suomalainen, G. Tal, K. Walkowicz, and J. Ward, Prog. Energy **3**, 22002 (2021).
[160] R. Kotecha, W. Metzger, B. Mather, S. Narumanchi, and A. Zakutayev, ECS J. Solid State Sci. Technol. **8**, Q3202 (2019).
[161] G. Moreno, S. Narumanchi, X. Feng, P. Anschel, S. Myers, and P. Keller, J. Electron. Packag. **144**, 011004 (2021).
[162] M. Hayes, M. Anwar, A. Tata, M. Teimorzadeh, and T. Achatz, SAE Int. J. Altern.

Powertrains **4**, 145 (2015).
[163] P. Paret, G. Moreno, B. Kekelia, R. Kotecha, X. Feng, K. Bennion, B. Mather, A. Zakutayev, S. Narumanchi, S. Graham, and S. Kim, in *2018 IEEE 6th Work. Wide Bandgap Power Devices Appl.* (2018), pp. 287–294.
[164] T. Burress, Present. US Dept. Veh. Technol. Off. Annu. Merit Rev., US Dept. Energy (2017).
[165] N. Fusté, O. Aviñó, M. Vellvehi, X. Perpiñà, P. Godignon, R. Seddon, I. Obieta, J. Maudes, and X. Jordà, in *2020 21st Int. Conf. Therm. Mech. Multi-Physics Simul. Exp. Microelectron. Microsystems* (2020), pp. 1–8.
[166] S. Lee, R. Vetury, J.D. Brown, S.R. Gibb, W.Z. Cai, J. Sun, D.S. Green, and J. Shealy, in *IEEE Int. Reliab. Phys. Symp. Proc.* (IEEE, 2008), pp. 446–449.
[167] A.R. Coutu, A.R. Lake, D.B. Christiansen, R.E. Heller, A.C. Bozada, S.B. Poling, D.G. Via, P.J. Theimer, E.S. Tetlak, R. Vetury, and B.J. Shealy, Electronics **5**, 32 (2016).