

# Development of High-Efficiency GaAs Solar Cells Grown on Nanopatterned GaAs Substrates

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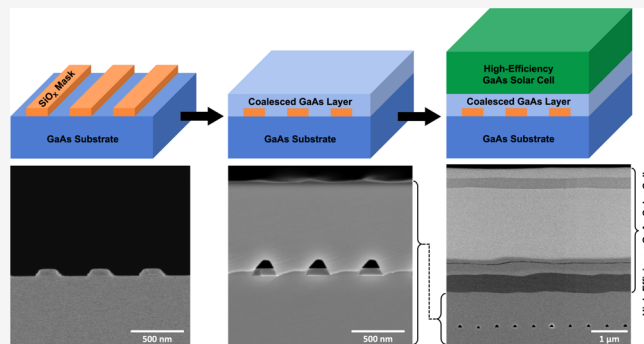
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**ABSTRACT:** One approach to reducing the cost of high-efficiency III–V devices involves adding patterned layers to heteroepitaxial or homoepitaxial substrates to facilitate substrate removal and reuse. However, few studies have focused explicitly on high-quality devices grown over patterned substrates, which is required for any cost saving to be beneficial. In this work, we demonstrate the growth of high-efficiency GaAs solar cells on GaAs substrates patterned with an array of nanoscale SiO<sub>x</sub> mask stripes. We show that reducing the pattern dimensions to submicron length scales with nanoimprint lithography enables defect-free coalescence. By varying the growth conditions, faceting of the epilayer material during overgrowth of the patterned mask was also controlled. A V/III ratio of 200 during MOVPE overgrowth produced smooth coalesced epilayers, which is desirable for the growth of subsequent device layers. Inverted GaAs front homojunction devices grown on patterned GaAs(001) substrates achieved threading dislocation densities below  $5 \times 10^5 \text{ cm}^{-2}$  and maintained >23% solar cell efficiencies at one sun illumination, equivalent to control devices grown on unpatterned epi-ready substrates.



## INTRODUCTION

Lowering the fabrication costs remains a major barrier for large-scale terrestrial adoption of high-efficiency III–V-based photovoltaics. High-quality single-crystalline III–V substrates make up a significant portion of device manufacturing costs, alongside epitaxial growth and cell processing.<sup>1,2</sup> Methods for reducing the substrate costs by reusing expensive III–V substrates have been proposed and studied over the past few decades.<sup>3–5</sup> However, epitaxial lift-off is the only commercially successful substrate cost reduction technique that has been demonstrated to date largely due to its ability to produce full wafer areas of flawless epitaxial materials, but it can suffer from lengthy processing times and substrate reparation steps.<sup>6,7</sup>

Some reuse techniques rely on patterning the substrate with an inert dielectric mask material (SiO<sub>x</sub>, SiN<sub>x</sub>, etc.) prior to epitaxial growth. This mask can be used as a mechanically weak layer for subsequent spalling or other release processes.<sup>8,9</sup> The most well-known implementation of this method is the CLEFT (cleavage of lateral epitaxial films for transfer) process, which uses the overgrowth of GaAs over micron-scale lateral mask stripes patterned onto GaAs(110) substrates to create weak layers for substrate release and reuse.<sup>3</sup> After many years of development, the highest reported efficiency for GaAs solar cells grown by CLEFT was 21.5%.<sup>10</sup> A recent study by Ironside et al. demonstrated the planar growth of GaAs on micron-scale stripe-patterned GaAs substrates by MBE, but defect formation

was still observed in the coalesced material.<sup>11</sup> Lateral epitaxial overgrowth of the III–V material on patterned substrates has been studied extensively in the past, primarily for GaN, but the studies have rarely focused on large area devices such as solar cells.<sup>12</sup> Because the electrical properties and performance of these large area devices are much more sensitive to crystalline defects, a key aspect of homoepitaxial growth of solar cell devices on patterned substrates is to ensure that no defects are introduced during coalescence.

The work presented here uses a pattern of linear stripes similar to those in previous studies but with the lateral dimensions reduced to submicron distances via the use of nanoimprint lithography (NIL). Critically, this reduction in scale significantly reduces the density of coalescence-related threading dislocations for a stripe-pattern geometry by decreasing the magnitude of crystallographic alignment errors between the neighboring regions of epitaxial overgrowth. If the relative alignment errors due to distortions in the laterally

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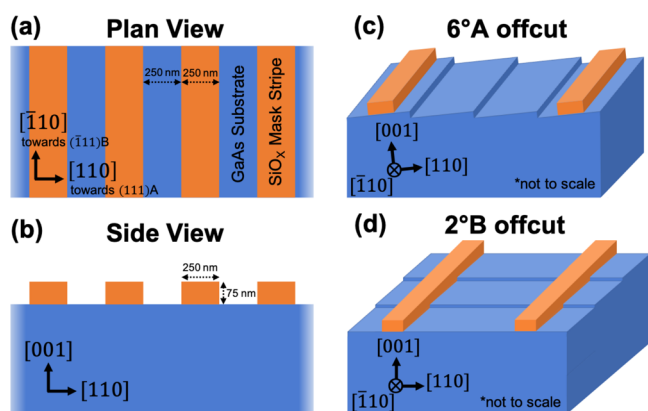
overgrown material are reduced to less than half of its lattice constant, the coalescing material can align to avoid the formation of coalescence-related dislocations.<sup>13</sup> Successful implementation of these methods for large area devices, such as solar cells, requires precise control over three crucial steps—nucleation, lateral overgrowth, and coalescence. Unoptimized conditions for any of these processes introduce undesired surface morphologies and crystallographic defects that are detrimental to the overall device performance.

In this study, we report key factors for growing high-efficiency GaAs solar cells on GaAs substrates patterned with an array of nanoscale SiO<sub>x</sub> mask stripes. The influence of pattern orientation (with respect to the substrate offcut direction) and the metalorganic vapor-phase epitaxy (MOVPE) V/III ratio on crystallographic defect formation and epilayer surface morphology evolution is discussed. The impact of these factors on material quality after coalescence is assessed by measuring threading dislocation densities (TDDs) and solar cell performance metrics of GaAs homojunction devices grown on patterned GaAs substrates.

This work is aimed at demonstrating the growth of high-quality III–V devices over patterned substrates with the intention of strengthening the prospects of substrate reuse by incorporating a mechanically weak layer for spalling or another release method. However, our findings may also be extended to other homo- or heteroepitaxial systems to help guide the growth of high-quality coalesced epilayers for use in low-cost, high-efficiency III–V semiconductor devices.

## EXPERIMENTAL DETAILS

Figure 1 shows a representative schematic of a nanopatterned substrate used in this work. Silica (SiO<sub>x</sub>) mask stripes were patterned



**Figure 1.** (a) Plan view and (b) side view of a substrate patterned with NIL. Blue represents the GaAs substrate and orange represents the SiO<sub>x</sub> mask. Mask stripes were oriented along [110], which were (c) parallel to the substrate step edges for 6°A offcuts and (d) orthogonal to the step edges for 2°B offcuts.

on 2 in. diameter GaAs(001) substrates offcut 6° toward (111)A or 2° toward (111)B using NIL; hereafter, these substrates will be called “6°A” and “2°B”, respectively. Silica was used in this work because it is a common inert mask material for lithographic patterning, but the use of other mask materials, such as SiN<sub>x</sub>, could also be envisioned. Mask openings between SiO<sub>x</sub> stripes were 250 nm wide, and SiO<sub>x</sub> stripe dimensions measured 250 nm wide and 75 nm tall and span the entire length of the masked area. The SiO<sub>x</sub> stripes were oriented such that the (111)A planes were orthogonal to the [110] stripe direction in all samples. Thus, the sides of the SiO<sub>x</sub> stripes were aligned parallel to

the substrate step edges for 6°A substrates and perpendicular to the substrate step edges for 2°B substrates.

Reactive ion etching with a CHF<sub>3</sub>/CF<sub>4</sub>/N<sub>2</sub> chemistry was used to break through the SiO<sub>x</sub> mask and expose the GaAs surface between the mask stripes. The patterned substrates were cleaned immediately before MOVPE growth by etching in 1 NH<sub>4</sub>OH/1 H<sub>2</sub>O<sub>2</sub>/50 DI H<sub>2</sub>O solution for 10 s followed by rinsing in DI H<sub>2</sub>O and IPA. All MOVPE growth was carried out in a custom-built atmospheric pressure reactor. The reactor temperature was ramped up to 700 °C from ambient temperature in 10 min under an AsH<sub>3</sub> and purified hydrogen atmosphere and held for 3 min at 700 °C before GaAs growth was initiated. For the coalesced GaAs buffers, the ratio of AsH<sub>3</sub> to trimethylgallium (V/III) was set to 60 or 200 and the growth rate was fixed at a nominal rate of 3 μm/h. For solar cell devices, inverted GaAs front homojunction cells were grown on top of the coalesced buffer layers. Following epilayer growth, the reactor was cooled to ambient temperature under an AsH<sub>3</sub> atmosphere.

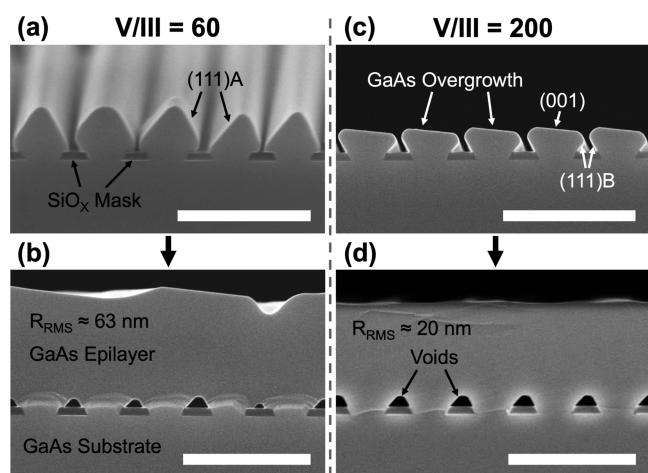
Inverted solar cell devices were processed as described in ref 14 with two additional steps due to the use of patterned substrates. After substrate etching, the samples were etched in 5% HF for 60 s to remove the SiO<sub>x</sub> mask, followed by etching with 2 NH<sub>4</sub>OH/1 H<sub>2</sub>O<sub>2</sub>/10 DI H<sub>2</sub>O for 150 s to remove the GaAs buffer layer before continuing with the standard inverted cell processing. For the final implementation of the intended application, the substrates would be separated from the epilayer for reuse and the process would be adapted accordingly. The device area was 0.116 cm<sup>2</sup>, with an illuminated area of 0.101 cm<sup>2</sup>. Bilayer MgF<sub>2</sub>/ZnS antireflection coatings were deposited by thermal evaporation.

External quantum efficiency (EQE) and reflectance were measured on a custom-built system using a tungsten–halogen lamp and a 270 m monochromator, with a built-in reflectance diode. Current–voltage (*J–V*) curves were measured under a simulated AM1.5G spectrum using an XT-10 solar simulator with a Xe arc lamp. Using a calibrated GaAs reference cell and spectral mismatch correction factor, the light intensity was accurately adjusted to simulate 1 sun conditions.<sup>15</sup>

Cross-sectional and plan-view scanning electron micrographs were acquired on a Hitachi S-4800 scanning electron microscope or an FEI Nova NanoSEM 630 operating at 5 kV. Electron channeling contrast imaging (ECCI) was performed using a vCD backscatter detector inserted underneath the pole piece on the FEI Nova NanoSEM 630 operating at 25 kV accelerating voltage and 3.2 nA beam current. Cross sections were prepared by simply cleaving along <110> directions. Surface roughness was measured using a Keyence confocal laser scanning microscope at 50× (286 × 215 μm area) and 150× (95 × 71 μm area).

## RESULTS AND DISCUSSION

**Growth Conditions and Surface Morphology.** Attaining a smooth top surface morphology for the growth of subsequent device layers is nearly as important as achieving low defect densities for the coalesced epilayers. This is especially true for III–V devices, where cell architectures often contain very thin layers (<10 nm) that can be easily disrupted by adverse surface roughness. Controlling the morphology of the overgrown material prior to coalescence can significantly influence the final top surface roughness of the coalesced buffer layer on which subsequent device layers are grown. Inspired by the work of Lee et al.<sup>16</sup> and Moll et al.,<sup>17</sup> we studied the influence of the V/III ratio on the preferential growth directions and faceting of precoalesced GaAs grown on patterned 6°A substrates. Figure 2 shows the difference in the overgrowth morphology of GaAs prior to coalescence when grown under a V/III ratio of 60 versus 200. Changing the V/III ratio changes the As chemical potential within the reactor environment, which alters the surface energies of low-index GaAs surfaces, which in turn can influence any preferential faceting.



**Figure 2.** Cross-sectional SEM viewing down [110] showing the overgrowth morphology and surface roughness as a function of the V/III ratio on 6°A substrates. (a) Lower V/III ratio of 60 favors (111)A facet formation and overgrowth in a spade-like morphology, resulting in a (b) rougher coalesced epilayer. (c) Higher V/III ratio of 200 favors (001) and (111)B facet formation, resulting in a (d) smoother coalesced epilayer. Scale bars are 1  $\mu\text{m}$ .

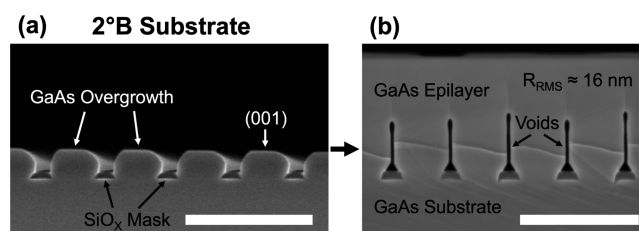
At a lower V/III ratio of 60, GaAs overgrew in a spade-like morphology (see Figure 2a), which creates a rough, undulating film at the point of initial coalescence. After 1  $\mu\text{m}$  of growth, significant surface pitting was still observed (Figure 2b) and the root mean square (RMS) surface roughness ( $R_{\text{RMS}}$ ) was approximately 63 nm. Such a morphology requires growing thicker epilayers to flatten out the coalesced film and is therefore less ideal for the growth of subsequent device epilayers.

Increasing the V/III ratio to 200 (thereby increasing the As chemical potential) results in preferential faceting of the (001) and (111)B surfaces as seen in Figure 2c. Note that the morphology is also more consistent between the neighboring overgrowths. The very flat, tilted top of each overgrowth is consistent with a (001) facet, which can be completely step-free because of the offcut direction. Such a lack of steps may enhance Ga adatom diffusion to the overgrowth edges, contributing to the lateral growth of the overhanging (111)B facets. It is difficult to determine whether these morphology changes as a function of As chemical potential are influenced more by surface kinetics or by surface energy and thermodynamics. However, based on the prior literature and this work, there is reason to hypothesize that both play a role in the resulting overgrowth morphology. Further growth of this morphology leads to a more uniform film at the point of initial coalescence, resulting in a RMS surface roughness of around 20 nm after 1  $\mu\text{m}$  of growth (Figure 2d). These results clearly show the impact of the overgrowth morphology on the surface roughness of the coalesced epilayers.

Another aspect of the overgrowth morphology that warrants attention is the formation of voids above the  $\text{SiO}_x$  mask stripes due to preferential faceting in the early stages of overgrowth. The shape and consistency of these voids could impact fracture mechanics for spalling, so further investigation of factors affecting void formation is merited. The voids formed above the mask stripes were larger using a V/III ratio of 200 compared to 60 (see Figure 2).

**Pattern Orientation and Substrate Offcut.** Epilayers were also grown on 2°B substrates with mask stripes oriented

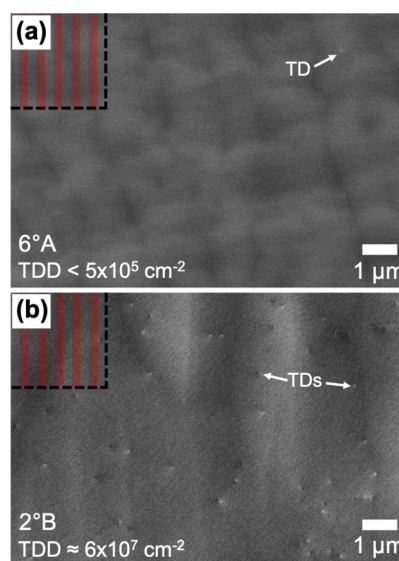
perpendicular to the substrate step edges, as shown in Figure 1d. Figure 3 shows the overgrowth behavior and coalesced



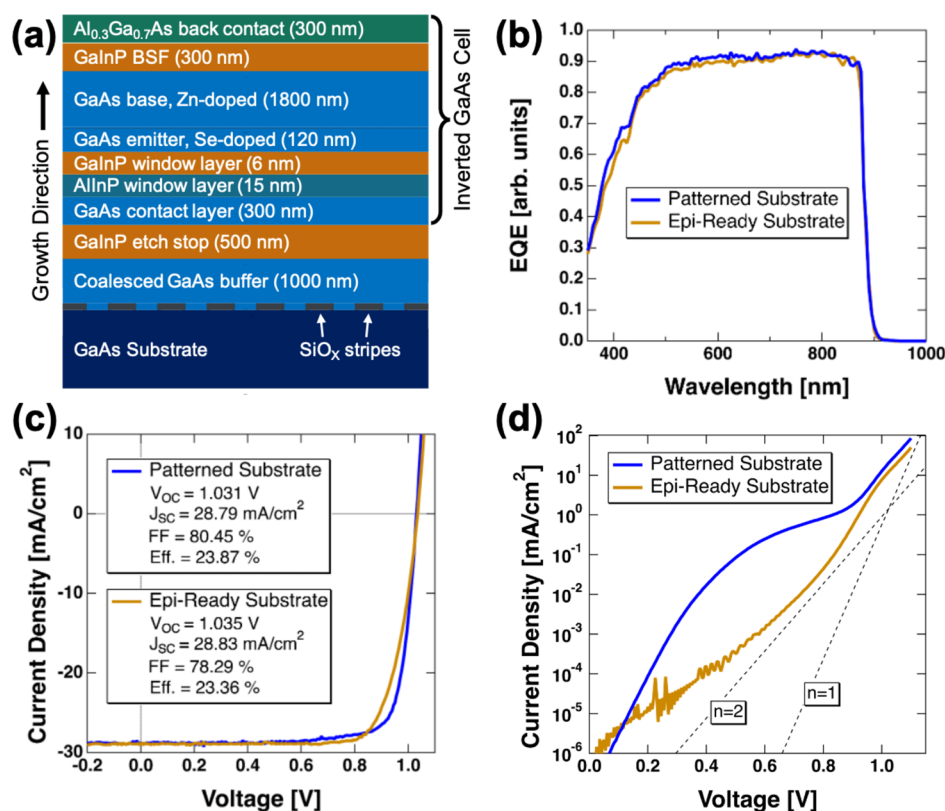
**Figure 3.** Cross-sectional SEM viewing down [110] showing the (a) overgrowth morphology and (b) surface roughness of a 1  $\mu\text{m}$  thick coalesced GaAs buffer grown on a 2°B substrate with a V/III ratio of 200. Preferential (001), (110), and (110) faceting is observed, leading to a more vertical overgrowth and taller void structures. Scale bars are 1  $\mu\text{m}$ .

buffer surface morphology for the resulting samples. The overgrowth morphology is consistent across large areas and favors (001) faceting. However, the resulting void structures are much taller. This could be due to the energetics of (110) and (110) faceting or the kinetics of the mass transport supplying material for lateral growth. In contrast to the nearly step-free top (001) surfaces for the 6°A sample shown in Figure 2c, the step density on the top (001) surfaces for the 2°B sample in Figure 3a is similar to that of the substrate. This likely reduces the lateral mobility of group III atoms across the top (001) surface to the sidewalls, hindering lateral overgrowth.

Although the overgrowth behavior and top surface morphology of the growth on 2°B substrates ( $R_{\text{RMS}} \approx 16$  nm) are comparable to those on the 6°A substrates, ECCI shows a difference of two orders of magnitude in the TDD between the two orientations. Figure 4a,b displays the ECCI micrographs of representative areas from the top surfaces of the inverted front homojunction GaAs solar cells grown on patterned 6°A and 2°B substrates, respectively. The GaAs cell



**Figure 4.** TDDs measured by ECCI indicate over two orders of magnitude lower TDD in GaAs cells grown on patterned (a) 6°A substrates compared to (b) 2°B substrates. Insets in the top-left corners schematically show the underlying pattern to scale.



**Figure 5.** (a) Schematic of the GaAs front homojunction cell architecture as grown on a patterned GaAs substrate. Cells were inverted and coated with an ARC before solar cell measurement. Representative (b) EQE, (c) light  $J-V$  characteristics, and (d) dark  $J-V$  characteristics for devices grown on patterned substrates and control devices grown on unpatterned epi-ready substrates. Guides for  $n = 1$  and  $n = 2$  diode behavior are shown in the dark  $J-V$  plot.

grown on a patterned  $6^\circ\text{A}$  substrate was found to be nominally defect-free, aside from a few areas of defects clustered around widely scattered extrinsic patterning imperfections from NIL, which are discussed later. For this sample, an upper TDD limit of  $\approx 5 \times 10^5 \text{ cm}^{-2}$  was measured over a total area of  $2380 \mu\text{m}^2$ , which included defect-free areas as well as areas containing defect clusters. The GaAs cell grown on a patterned  $2^\circ\text{B}$  substrate had an average TDD of  $\approx 6 \times 10^7 \text{ cm}^{-2}$  measured over a total area of  $565 \mu\text{m}^2$ . Note that the total imaging area needed for statistical accuracy decreases as the defect density increases. The reason for the significant increase in the TDD on the  $2^\circ\text{B}$  substrate is not fully understood at this time, but we hypothesize that it could be due to taller overgrowth prior to coalescence, which increases the chance for crystallographic alignment errors between neighboring overgrowths.<sup>13</sup>

While this work only focused on linear stripe patterns, we envision that many other combinations of pattern orientation and substrate offset could produce defect-free and smooth coalesced epilayers if the optimal growth conditions are identified.<sup>13</sup> Some of the variables that merit further investigation include different pattern geometries and dimensions, patterns oriented away from the major crystallographic substrate axes, composition of the overgrowth layer, and growth temperature to change the surface energies and preferential faceting. From this study, the main factors for producing smooth, defect-free coalesced epilayers appear to be managing the overgrowth morphology such that the (001) facets are dominant and the mask dimensions are small enough to ensure that the overgrown material maintains rigidity and crystallographic registry with the neighboring overgrowths

during coalescence. If a pattern with larger dimensions is needed, then, other pattern topologies should be considered. In particular, a contiguous-epilayer mask topology (e.g. disjoint mask pads) could be used instead as it should enable defect-free coalescence to arbitrarily large dimensions.<sup>13</sup>

**Solar Cell Measurements.** To assess macroscale material quality, GaAs front homojunction devices, shown in Figure 5a, were grown on  $1 \mu\text{m}$  thick coalesced buffer layers (V/III ratio = 200) on patterned  $6^\circ\text{A}$  substrates. EQE (Figure 5b) was measured over a wavelength range of 350–1000 nm. High quantum efficiency was observed across the entire above-band gap range and is equivalent to that of control devices grown on unpatterned epi-ready substrates. This indicates that the carrier collection efficiency and carrier diffusion length did not suffer due to growth on these patterned substrates.

Figure 5c shows the  $J-V$  characteristics of the devices grown on patterned substrates as well as control devices. As expected from the QE, the  $J_{\text{SC}}$  of the devices grown on patterned substrates is also comparable to that of the control devices. The  $V_{\text{OC}}$  of the devices grown on patterned substrates is comparable to the  $V_{\text{OC}}$  of the control devices, indicating that crystalline material quality was maintained. Although the control devices grown in this work are not state-of-the-art for GaAs, they provide a comparison showing that growth of high-efficiency GaAs cells on patterned substrates is achievable. However, it is worth noting that the current state-of-the-art device architectures may need to be redesigned to accommodate some of the challenges in using patterned substrates, such as rougher surface morphologies. While it is not fully understood at this time, an unoptimized device architecture

may contribute to below average fill factors exhibited by the devices demonstrated in this work. Solar cell design and performance can be further optimized from the devices shown here, but the focus of this work is on demonstrating growth on patterned substrates with no detriment to material quality and device efficiency. Furthermore, based on the low TDD measured by ECCL, we find that the higher efficiency cell designs would not be significantly degraded by nonradiative recombination due to crystal defects.<sup>18</sup>

Dark  $J$ - $V$  data are plotted on a semilog scale in Figure 5d to show the shunting behavior indicated by the hump in the dark  $J$ - $V$  curve that was observed in the devices on patterned substrates. We suspect that this shunting behavior was due to extrinsic imperfections introduced during the NIL patterning process, and this should be remedied by more careful sample handling and processing. These results provide clear evidence that III-V photovoltaic devices can be grown on patterned substrates while maintaining the high conversion efficiencies expected from standard devices grown on unpatterned epi-ready substrates.

We have demonstrated that high-efficiency III-V devices can be grown on patterned substrates, which is promising for multiple substrate reuse techniques. Future attempts at releasing inverted GaAs devices to enable reuse of the patterned GaAs substrates can be done by mechanical and/or electroacoustic spalling.<sup>19,20</sup> As demonstrated by prior CLEFT studies, the interface between the III-V material and patterned SiO<sub>x</sub> stripes should act as a mechanically weak layer and facilitate crack propagation. This should be even more pronounced in structures with voids above the mask because the empty space might further accentuate crack propagation as well as create stress concentrations near void edges. Studies have shown that device efficiencies are maintained throughout the spalling and transfer processes, and this is expected to be the case for devices grown on patterned substrates as well.<sup>21,22</sup> Ideally, the patterned mask will remain adhered to the substrate after spalling to eliminate the need for repatterning, thereby further lowering the processing costs.

## CONCLUSIONS

Growth of high-efficiency GaAs solar cells was demonstrated on GaAs substrates patterned with an array of nanoscale SiO<sub>x</sub> mask stripes. Controlling the morphology of the epilayer material as it overgrows the mask was found to be important for maintaining defect-free and smooth epilayers during coalescence and subsequent growth of device layers. Using a high V/III ratio of 200 during GaAs overgrowth and coalescence on 6°A substrates with SiO<sub>x</sub> stripes oriented parallel to the step edges promoted (001) faceting and a consistent overgrowth morphology, leading to defect-free and smooth coalesced buffer layers. Inverted GaAs front homojunction devices grown on these buffers maintained solar cell efficiencies equivalent to those of control devices grown on unpatterned epi-ready substrates. Future work will focus on using the region containing the patterned mask array as a mechanically weak layer to enable controlled spalling for substrate reuse.

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## Notes

The authors declare no competing financial interest.

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## REFERENCES

- (1) Horowitz, K. A.; Remo, T. W.; Smith, B.; Ptak, A. J. *A Techno-Economic Analysis and Cost Reduction Roadmap for III-V Solar Cells*. NREL/TP-6A20-72103; National Renewable Energy Laboratory: Golden, CO, 2018.
- (2) Wilson, G. M.; et al. The 2020 photovoltaic technologies roadmap. *J. Phys. D: Appl. Phys.* **2020**, *53*, 493001.
- (3) McClelland, R. W.; Bozler, C. O.; Fan, J. C. C. A technique for producing epitaxial films on reuseable substrates. *Appl. Phys. Lett.* **1980**, *37*, 560–562.
- (4) Bauhuis, G. J.; Mulder, P.; Haverkamp, E. J.; Schermer, J. J.; Bongers, E.; Oomen, G.; Köstler, W.; Strobl, G. Wafer reuse for repeated growth of III-V solar cells. *Prog. Photovoltaics* **2010**, *18*, 155–159.
- (5) Sweet, C. A.; Schulte, K. L.; Simon, J. D.; Steiner, M. A.; Jain, N.; Young, D. L.; Ptak, A. J.; Packard, C. E. Controlled exfoliation of (100) GaAs-based devices by spalling fracture. *Appl. Phys. Lett.* **2016**, *108*, 011906.
- (6) Cardwell, D.; Kirk, A.; Stender, C.; Wibowo, A.; Tuminello, F.; Drees, M.; Chan, R.; Osowski, M.; Pan, N. Very High Specific Power ELO Solar Cells (>3 kW/kg) for UAV, Space, and Portable Power Applications. *2017 IEEE 44th Photovoltaic Specialist Conference*, 2017; pp 3511–3513.
- (7) Cheng, C.-W.; Shiu, K.-T.; Li, N.; Han, S.-J.; Shi, L.; Sadana, D. K. Epitaxial lift-off process for gallium arsenide substrate reuse and flexible electronics. *Nat. Commun.* **2013**, *4*, 1577.
- (8) Bozler, C.; McClelland, R. W.; Fan, J. C. C. Ultrathin, high-efficiency solar cells made from GaAs films prepared by the CLEFT Process. *IEEE Electron Device Lett.* **1981**, *2*, 203–205.
- (9) Bayram, C.; Bedell, S. W.; Sadana, D. K. Engineered base substrates for releasing III-V epitaxy through spalling. U.S. Patent 9,245,747 B2, January 26, 2016.

(10) Gale, R. P.; McClelland, R. W.; King, B. D.; Fan, J. C. C. Thin-film solar cells with over 21% conversion efficiency. *Sol. Cells* **1989**, *27*, 99–106.

(11) Ironside, D. J.; Skipper, A. M.; Leonard, T. A.; Radulaski, M.; Sarmiento, T.; Dhingra, P.; Lee, M. L.; Vuckovic, J.; Bank, S. R. High-Quality GaAs Planar Coalescence over Embedded Dielectric Microstructures Using an All-MBE Approach. *Cryst. Growth Des.* **2019**, *19*, 3085–3091.

(12) Ironside, D. J.; Skipper, A. M.; García, A. M.; Bank, S. R. Review of lateral epitaxial overgrowth of buried dielectric structures for electronics and photonics. *Prog. Quant. Electron.* **2021**, *77*, 100316.

(13) McMahon, W. E.; Vaisman, M.; Zimmerman, J. D.; Tamboli, A. C.; Warren, E. L. Perspective: Fundamentals of coalescence-related dislocations, applied to selective-area growth and other epitaxial films. *APL Mater.* **2018**, *6*, 120903.

(14) Duda, A.; Ward, S.; Young, M. *Inverted Metamorphic Multijunction (IMM) Cell Processing Instructions*. NREL/TP-5200-54049; National Renewable Energy Laboratory: Golden, CO, 2012.

(15) Osterwald, C. R. Translation of Device Performance Measurements to Reference Conditions. *Sol. Cells* **1986**, *18*, 269.

(16) Lee, S. C.; Huffaker, D. L.; Brueck, S. R. J. Faceting of a quasi-two-dimensional GaAs crystal in nanoscale patterned growth. *Appl. Phys. Lett.* **2008**, *92*, 023103.

(17) Moll, N.; Kley, A.; Pehlke, E.; Scheffler, M. GaAs equilibrium crystal shape from first principles. *Phys. Rev. B* **1996**, *54*, 8844–8855.

(18) Jain, N.; Hudait, M. K. Impact of Threading Dislocations on the Design of GaAs and InGaP/GaAs Solar Cells on Si Using Finite Element Analysis. *IEEE J. Photovolt.* **2013**, *3*, 528–534.

(19) Chen, J.; Packard, C. E. Controlled spalling-based mechanical substrate exfoliation for III-V solar cells: A review. *Sol. Energy Mater. Sol. Cells* **2021**, *225*, 111018.

(20) Bertoni, M.; Coll, P. G. Sound-assisted crack propagation for semiconductor wafering. U.S. Patent US 201,906,198 A1, February 28, 2019.

(21) Shahrjerdi, D.; Bedell, S. W.; Ebert, C.; Bayram, C.; Hekmatshoar, B.; Fogel, K.; Lauro, P.; Gaynes, M.; Gokmen, T.; Ott, J. A.; Sadana, D. K. High-efficiency thin-film InGaP/InGaAs/Ge tandem solar cells enabled by controlled spalling technology. *Appl. Phys. Lett.* **2012**, *100*, 053901.

(22) Shahrjerdi, D.; Bedell, S. W.; Bayram, C.; Lubguban, C. C.; Fogel, K.; Lauro, P.; Ott, J. A.; Hopstaken, M.; Gayness, M.; Sadana, D. Ultralight High-Efficiency Flexible InGaP/(In)GaAs Tandem Solar Cells on Plastic. *Adv. Energy Mater.* **2013**, *3*, 566–571.