**Journal of Low Temperature Physics manuscript No.**
(will be inserted by the editor)

# Fabrication of OMT-coupled Kinetic Inductance Detector for CMB Detection

**Q. Y. Tang**[1] · **P. S. Barry**[2] · **T. W. Cecil**[2] · **E. Shirokoff**[1]

the date of receipt and acceptance should be inserted later

**Abstract** Future cosmic microwave background (CMB) experiments, including the large scale ground based Stage Four CMB Experiment (CMB-S4), satellites, and balloons, aim to map the CMB to an unprecedented precision in order to answer several key questions in cosmology. However, to reach the target noise sensitivity, more than 100,000 detectors will be needed. Arrays of kinetic inductance detectors (KIDs) are a promising alternative for experiments that require large number of detectors due to the intrinsic multiplexing capabilities. We present the fabrication procedure for a prototype planar orthomode transducer (OMT)-coupled multi-colour KID array optimized for 220/270 GHz frequency bands. These devices are made from silicon-on-insulator (SOI) wafers to provide a low-loss substrate for the KIDs. The OMT couples the two polarizations of light from a wide-band feed-horn to separate Nb/SiN/Nb microstrip lines, which are then coupled to Al/Nb lumped-element KIDs (LEKIDs). The silicon on the backside of the OMT is etched away using deep reactive ion etch (DRIE) to release the OMT membrane to enable operation over a wide-bandwidth. Finally, the buried oxide is removed underneath the KID capacitors in order to minimize two-level system (TLS) noise and loss mitigation. We achieved a good yield (>80%) on our prototype devices.

**Keywords** fabrication, kinetic inductance detector, cosmic microwave background

## 1 Introduction

The next generation cosmic microwave background experiment (CMB-S4) is a collaboration with several telescopes in the Atacama desert of Chile and the South Pole. The main science goals include testing the theory of inflation, solving the neutrino mass hierarchy problem, hunting for light relics from the early universe, and measuring the evolution of massive galaxy clusters [1]. However, the target sensitivity needed to do this requires $\approx 5 \times 10^5$ detectors. The traditional detectors used for CMB experiments, the transition edge sensor (TES) bolometers, are well-understood and characterized. Nonetheless, scaling up to $10^5$

[1]Kavli Institute of Cosmological Physics, University of Chicago, Chicago, IL 60637, USA
[2]Division of High Energy Physics, Argonne National Laboratory, Lemont, IL 60439
E-mail: tangq@uchicago.edu

detectors for TES bolometers remains a challenge in terms of fabrication and readout multiplexing.

Kinetic inductance detectors (KIDs) are a type of athermal pair-breaking detectors that offer high multiplexing ratios without the need for ancillary wired connections. Several non-CMB millimeter and sub-millimeter wavelength experiments have deployed - or are currently developing - KIDs, such as SuperSpec, NIKA2, TolTEC, BLAST-TNG, and OLIMPO [2-6]. Feedhorn-OMT coupled detectors are now commonly used in CMB experiments due to the low polarization error and control over beam shape that can be achieved with feedhorns.

There are multiple on-going developments toward feedhorn coupled multi-colour KID polarimeters for CMB experiments. To date, most designs have been based on OMT-coupled $\lambda/4$ CPW resonators using a novel optical coupling scheme, such as the devices proposed by Johnson et al [7]. Resonators based on distributed resonators present a unique challenge, and are constrained by the competing requirements to both absorb the power along the length of the region of high-current density and not sacrifice noise and stability.

In the LEKID-based design we present here, the inductor and capacitor elements of the KID are physically separated, allowing independent optimization of the inductor that forms the mm-wave absorber, and the capacitor geometry, critical to the stability of the resonator. In this paper, we present the fabrication process of a prototype 8-pixel array of two-colour, dual-polarization, OMT-coupled LEKIDs.

## 2 Design

The current design of the detectors is optimized for the 220 GHz and 270 GHz band observation (each with observing band of 20%). These frequencies are needed in CMB experiments to constrain the foreground contamination of the CMB signal by measuring the thermal emission from galactic dust. Incoming light travels down an array of feed horns, feeding a single-mode circular waveguide to the OMT structure on our detector wafer. To maxmize the optical coupling efficiency across the observing band, the OMT probes are placed on a 4 µm thin Si device layer of a silicon-on-insulator (SOI) wafer, which has been released from the bulk Si wafer. A quarter wavelength backshort and RF choke are located behind the OMT probes and are required to maximize coupling of the signal to the OMT and minimize stray signal leakage into the Si carrier wafer. The signal travels from the Nb OMT probes to the microstrip via a CPW-to-microstrip transition section. We employ a Nb/$SiN_x$/Nb inverted microstrip, based off [8]. We use a cross-under structure to gather the signal from the orthogonal OMT probes for a single polarization to a hybrid tee. We also use a set of bandpass microstrip filters to define our observing band. The combined mm-wave signal from the hybrid goes into the Al inductor part of the LEKID. The interdigitated capacitor (IDC) is formed from Nb to both maximize responsivity by confining quasiparticles to the inductor, while reducing direct stimulation in the capacitor. Lastly, the KID is capacitively coupled to the Nb readout transmission line. A subsequent paper with a more detailed discussion of the design and the optimization procedure of the detectors is currently in preparation.

## 3 Fabrication

Fabrication begins with a 4-inch high resistivity ($> 1\,\mathrm{k}\Omega \cdot \mathrm{cm}$) silicon-on-insulator (SOI) wafer, with a handle thickness of 450 µm, a 0.5 µm silicon oxide layer, and 4 µm device

layer. Fig. 2 shows the process flow in detail and contains the step numbers referred by the text below in parentheses. The specific parameters used in each lithography and plasma etch/deposition are shown in Tables 1 and 2, respectively. Microscope images of the final devices are shown in Fig. 1.

Prior to each lithography step, the wafer is cleaned using a sonicated acetone, isopropyl alcohol (IPA), and deionized (DI) water baths, followed by a vacuum dehydration step. After spinning resist (cf. Tab. 1), we expose the pattern using a maskless direct write lithography writer from Heidelberg Instruments[1]. We remove the resist after each etching step first by using an $O_2$ plasma asher[2] at 70°C to remove the crust layer of resist. We then clean the wafer using a heated sonicated NMP (1-Methyl-2-pyrrolidon) bath, followed by an IPA and DI water bath.

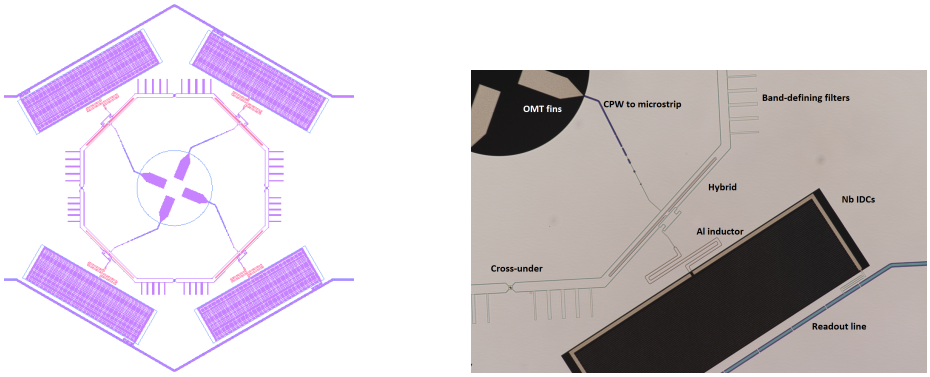


**Fig. 1** *Left*. Layout design of an pixel on the chip. *Right*. Labelled close-up of the OMT structure coupled to a KID through a microstrip.

The SOI wafer (step 0) is first cleaned with a buffered hydrofluoric (HF) acid bath dip to remove the native oxide followed by a dehydration step. We then deposit 100 nm of sputtered Al (step 1) [3]. The Al layer forms the inductor and the sum-port termination of the hybrid, and is etched using a standard phosphoric acid-based Al etchant (step 2). Prior to depositing the Nb layer, we perform a short ion-mill step to remove the native oxide to ensure a clean galvanic contact between the Al and the Nb layers. Then we sputter 250 nm of Nb layer (step 3). We pattern the OMT probes, interdigitated capacitor (IDC) fingers, microstrip wiring, and readout lines on the Nb layer. The Nb layer is then dry etched using an inductively coupled plasma (ICP) fluorine etcher[4] (step 4, cf. Tab. 2). We then grow the dielectric layer of our microstrip, 500 nm of $SiN_x$, over our wafer (step 5) using High Density Plasma Chemical Vapor Deposition (HDPCVD) [5]. We also deposit 2 µm of silicon oxide ($SiO_x$) on the backside of the wafer (step 6) to counteract the stress of the oxide layer on the device side of our wafer and to serve as extra protection for the deep silicon etch.

[1] Heidelberg MLA150: https://himt.de/index.php/maskless-write-lasers.html

[2] YES CV200 RFS Plasma Strip/Descum System: http://www.yieldengineering.com/products/plasma-strip-descum-systems/cv200rf-series

[3] AJA ATC 2200 UHV Sputtering System: http://www.ajaint.com/atc-series-sputtering-systems.html

[4] PlasmaTherm ICP Fluorine Etcher: http://www.plasma-therm.com/apex_SLR.html

[5] Plasma-Therm Apex SLR: http://www.plasma-therm.com/versaline.html

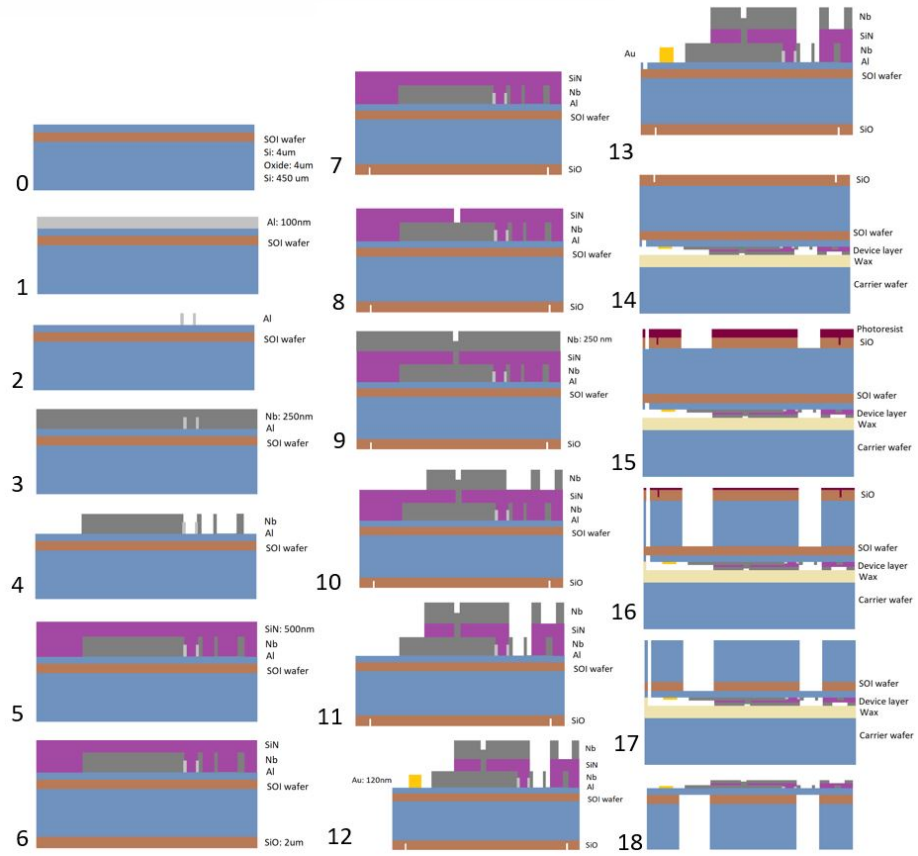


**Fig. 2** Cartoon of cross section view of the wafer during all the processing steps. The bottom right figure shows the OMT and mm-wave transmission line, the IDC, and the microwave readout region from left to right. See text for details of process steps.

| Step | Layer | Photoresist | Laser (nm) | Dosage ($mJ/cm^2$) |
|---|---|---|---|---|
| 2 | Al KIDs | AZ 1512 | 375 | 120 |
| 4,10 | Nb CPW/ground plane | AZ 703 | 375 | 185 |
| 7 | Backside SiO2 alignment cross | AZ 703 | 375 | 220 |
| 8 | $SiN_x$ vias | AZ 703 | 375 | 185 |
| 11 | $SiN_x$ over KIDs/OMT | AZ 1512 | 375 | 110 |
| 12,13 | Gold liftoff, Frontside Si | AZ 1518 | 375 | 200 |
| 15 | OMT and KID membranes DRIE | AZ 4620 | 405 | 600 |

**Table 1** Lithography details for fabrication of detector wafer. Step number matches the process step shown in Figure 2.

After depositing the dielectric layers, we pattern alignment features on the backside of our wafer and etch into the $SiO_x$ layer on the backside of the wafer with the ICP fluorine etcher (step 7). We then remove the resist and pattern the $SiN_x$ layer on the frontside of the wafer and fluorine etch to open up the nitride for the vias for the crossover structure for our microstrip (step 8). After removing resist, we use an ion gun again to remove any oxide on

| Step | Recipe | ICP Power (W) | Bias Power (W) | Pres. (mTorr) | He Pres. (Torr) | Gas 1 flow (sccm) | Gas 2 flow (sccm) | Gas 3 flow (sccm) |
|---|---|---|---|---|---|---|---|---|
| 4,10 | Nb etch | 600 | 50 | 50 | 5 | $CF_4$, 40 | $CHF_3$, 10 | Ar, 10 |
| 5 | $SiN_x$ dep | 1200 | 1 | 10 | 5 | $SiH_4$, 25 | $N_2$, 30 | Ar, 10 |
| 6 | $SiO_x$ dep | 800 | 200 | 10 | 5 | $SiH_4$, 20 | $O_2$, 50 | Ar, 30 |
| 7 | $SiO_x$ etch | 800 | 200 | 5 | 4 | $O_2$, 45 | - | - |
| 8,11 | $SiN_x$ etch | 100 | 20 | 30 | 5 | $SF_6$, 20 | - | - |

**Table 2** Recipes used for chemical vapor deposition and plasma etch. Step number matches the processes shown in Figure 2.

the exposed bottom layer of Nb structures (to ensure galvanic contact for our cross-under wiring) before sputtering 250 nm of Nb (step 9) as our ground plane. We pattern and etch the Nb layer to form the OMT membranes and open up the KIDs (step 10) and subsequently pattern and etch the $SiN_x$ layer to open the capacitor part of our detectors (step 11). We then do a liftoff to deposit 120 nm of Au pads along the edges of our chips for heat sinking (step 12). We also pattern and etch the 4 µm of device Si layer down to the oxide layer to form the dicing lines of our detector (step 13). Fig. 1 shows images from an optical microscope of the detector after the front-side processing.

The most delicate part of our detector fabrication is releasing the OMT and KID membranes. We do so by first bonding our detector wafer *detector side down* onto a carrier Si wafer by wax bonding (step 14). The carrier wafer is necessary to physically support the membrane during the DRIE process. We pattern the backside of our detector wafer to form holes for the OMT and KIDs membranes as well as the outlines of the device chip for release from the wax wafer. To etch the backside of the wafer, we first use a buffered hydrofluoric (HF) bath to remove the 2 µm of $SiO_x$ (step 15). Then we use a deep reactive ion etcher (DRIE)[6] to deep etch the bottom layer of 450 µm of Si down to the 0.5 µm of oxide of the SOI wafer (step 16). We then remove any remaining resist with a nanostrip bath and then all the exposed oxide by another buffered HF bath (step 17) and release the individual chips from the carrier wafer using an acetone bath to dissolve the wax (step 18). A photo of a finished device is shown in Fig. 3.

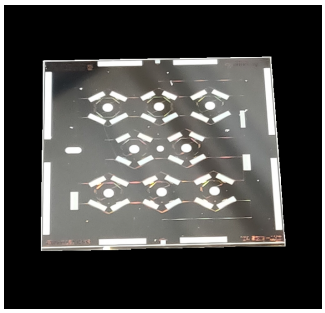

**Fig. 3** Photograph of a finished device.

During our initial fabrication run, we used a SOI wafer with 4 µm thick oxide layer. However, we observed that during the DRIE processing (step 15), the etch rate of the Si

[6] Plasma-Therm Versaline DSE: http://www.plasma-therm.com/etch-dse.html

handle wafer stayed consistent until the last $\sim$20 µm of Si before the oxide layer. After this point, the etch rate became negligible for the remaining Si. This is likely due to charge build-up caused by the thick oxide layer just beneath the $\sim$20 µm thick Si layer, which repelled the ions used in the reactive ion etch. We found that by decreasing the SOI oxide layer thickness to $\lesssim$1 µm, we were able to etch completely through the handle Si layer and expose the oxide layer.

## 4 Conclusions

We have described the development of a fabrication process for OMT-coupled KIDs. The process is compatible with dual-polarization, mutli-chroic pixels. We have fabricated a prototype 8-pixel OMT-coupled KID array intended for CMB applications, with a yield $>$80%. Results of the device performance will be described in a follow-up paper. We plan to fabricate a kilo-pixel array upon satisfactory demonstration.

**Acknowledgements** This work is partially supported by NSF award #1554565 and the Kavli NSF-PFC3 Detector Development grant. This work was supported in part by the Kavli Institute for Cosmological Physics at the University of Chicago through grant NSF PHY-1125897 and an endowment from the Kavli Foundation and its founder Fred Kavli. This work made use of the Pritzker Nanofabrication Facility of the Institute for Molecular Engineering at the University of Chicago, which receives support from SHyNE, a node of the National Science Foundations National Nanotechnology Coordinated Infrastructure (NSF NNCI-1542205).

## References


1. *CMB-S4* Collaboration, arXiv:1610.02743 [astro-ph.CO]
2. E. Shirokoff, et al. *Proc. SPIE*, **8452**, 84520R, (2012) DOI:10.1117/12.927070
3. A. Catalano, et al. *J. Low Temp. Phys.* (2018) **193**, 916, (2018) DOI: 10.1007/s10909-018-1884-5
4. J.E., Austermann, et al. *J. Low Temp. Phys.*, **193**, 120, (2018) DOI:10.1007/s10909-018-1949-5
5. N.P. Lourie, et al. *Proc. SPIE*, **10700**, 1070022, (2018) DOI:10.1117/12.2314380
6. A. Paeilla, et al. J. Low Temp. Phys. This Special Issue (2019)
7. B.R. Johnson, et al. *Proc. SPIE*, **9914**, 99140X (2016) DOI:10.1117/12.2233243
8. P. Barry, et al. *J. Low Temp. Phys.* **194**, 176, (2018), DOI:10.1007/s10909-018-1943-y.