Ultrathin silicon oxide prepared by in-line plasma-assisted N_2O oxidation (PANO) and the application for n-type polysilicon passivated contact

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Abstract

We develop a plasma-assisted nitrous-oxide (N_2O) gas oxidation (PANO) method to prepare the ultrathin silicon oxide (SiO_x) for polysilicon (poly-Si) passivated contact. The effects of preparation conditions, including the substrate temperature, processing time, and plasma power, are studied. Afterwards, we integrate the PANO SiO_x into the polysilicon passivated contact and optimize the passivation and contact performances. Excellent surface passivation with the n-type poly-Si and PANO SiO_x on the n-type c-Si wafer is achieved by 880°C annealing, which shows competitive passivation quality to the one with NASO SiO_x. Champion implied open-circuit voltage (iV_{oc}) and single-sided recombination saturated current (J_0)

reach 730 mV and 4.3 fA/cm^2 after crystallization; and they are further improved to 747 mV and 2.0 fA/cm^2 (3×10^{15}cm^{-3}) after subsequent AlO_x/SiN_x hydrogenation. Using transmission electron microscopy (TEM), we find that the thickness of PANO SiO_x ranges 1.1~2.4 nm and the controlled nitric acid oxidized SiO_x (NAOS) ranges 1.3~1.8 nm. The contact resistivity (ρ_c) is typically <10 m**Ω**.cm^2 with the annealing temperature of >820^{o}C. Also, the crystallinity, phosphorous in-diffusion profile, and current-leaking density of the passivated contacts are investigated. In general, the PANO SiO_x and in-situ doping amorphous silicon precursor can be fabricated in one PECVD system without additional equipment or transfer procedures, which is favorable for the high-efficiency, low-cost industrial manufacture.

Keywords: polysilicon passivated contact; plasma-assisted N_2O oxidation; ultrathin silicon oxide; TOPCon.

Introduction

Polysilicon (poly-Si) passivated contact, also named as TOPCon [1, 2] or POLO [3], has been proven as an excellent carrier selective structure with distinguished surface passivation and contact resistivity [4], leading to the 26.1% [5] record-efficiency p-type solar cell with interdigitated-back contact and the 25.8% [6] n-type solar cell with the front-and-rear contact. More importantly, the poly-Si passivated contact technology is compatible with the current crystalline-Si (c-Si) solar-cell manufacture lines including both the Al back-surface field (Al-BSF) and the passivated emitter and rear contact (PERC) technologies. It is proved that people can upgrade the existing manufacture line to the one produces high-efficiency passivated–contacted c-Si solar cells with the average efficiency of >23% [7]. The concept of high-efficiency poly-Si passivated-contact solar cell has been accepted gradually by the photovoltaic community and considered as the next-generation technology.

The quality of ultra-thin SiO_x is critical for surface passivation; thus, to develop a proper method to grow SiO_x is essential. Wet-chemical oxidation (nitric acid [8], ozone water [9], mixed acid [10]), thermal oxidation [3, 11], the ozone oxidation [12], and nitrous oxide (N_2O) plasma-assisted oxidation [13, 14] have been proven as the effective methods to achieve the high-quality SiO_x with the saturated recombination current density (J_0) of <10 fA/cm^2 for the electron-selected contact [4]. However, most of the methods mentioned above are not an in-situ fabrication process and require additional equipment investment. From the view of simplifying the manufacture processes, an in-situ method without additional equipment is desirable for industrial production.

Plasma-enhanced chemical vapor deposition (PECVD) is the promising tool to deposit in-situ doping a-Si precursor for industry [15, 16]; thus, to develop an in-line SiO_x-growth process using the same PECVD system would be essential for mass production. In the solar cell industry, the PECVD-deposited SiO_x is widely used for suppressing potential-induced degradation (PID) [17]. However, the shortcoming of this process is challenging to limit the SiO_x thickness within 2 nm, because the deposition of SiO_x that is grown from the reaction of silane (SiH_4) and N_2O is too fast to be controlled precisely. In contrast, the oxidation process for growing ultra-thin SiO_x is more favorable because oxide thickness depends on the diffusing energy of oxygen atoms and becomes self-saturated in oxidation process [18, 19].

In this work, we used plasma-assisted N_2O oxidation (PANO) to fabricate the ultra-thin SiO_x layer for poly-Si passivated contact. This work is not the first report concerning PANO SiO_x. Jeon et al. have reported [13] the application of PANO SiO_x for poly-Si passivated contact; however, they focused on the impact of interface-states density (D_{it}) but did not reveal the details of how to achieve excellent surface passivation [13]. Also, we have published a paper [14] discussing the integration of PANO SiO_x to passivated contact that passivates p-type Si wafer; however, the paper did not show the details of preparation and characterization of PANO SiO_x.

Different from the two works mentioned above, herein, we report the detailed information about PANO SiO_x, including the effects of oxidation condition, the characterization of PANO SiO_x, and the optimization of passivation quality. We used the PANO SiO_x to fabricate the n-type poly-Si passivated-contact structure on n-type c-Si; and we achieved an excellent surface passivation of a single-sided J_0 of 4.3 fA/cm^2 and an implied open-circuit voltage (iV_{oc}) of 730 mV prior the hydrogenation, and 2.0 fA/cm^2 and 747 mV after the hydrogenation, which is competitive with the one with nitric acid oxidized SiO_x (NAOS) [20]. More essential, this work proves that PANO SiO_x and amorphous silicon can be realized in one PECVD chamber, which avoids the damage of ultra-thin SiO_x by automation when transferring wafers. The plasma oxidation technology is a competitive candidate for in-line industrial mass manufacture for high-efficiency c-Si solar cells.

Experimental details

One-sided mirror-polished 4-inch n-type Czochralski (CZ) c-Si wafer was used as the substrates for characterizing the thickness of SiO_x. The 6-inch, ~3 Ω-cm, 180-μm thick solar-grade n-type CZ c-Si wafer polished by KOH solution was used as the substrates of lifetime samples. The ultra-thin SiO_x on wafer surface was grown by plasma-assist N_2O oxidation with high-purity (99.999%) N_2O as the source of oxygen. The effects of the substrate temperature (150°C-400°C), the oxidation time (30 sec-1200 sec), and the radio-frequency (RF) power (5W-20W) on the growth of SiO_x were investigated. In comparison, the SiO_x grew from the 110^{o}C nitric acid (HNO_3) bath was used as the reference specimens. Following the growth of SiO_x, a 40-nm in-situ phosphorus-doped a-Si:H thin film was deposited on the SiO_x with silane (SiH_4), phosphine (PH_3), and hydrogen (H_2) as the reaction gases. After deposition, the samples were subjected to the high-temperature annealing at 820°C to 950°C for crystallizing the a-Si:H thin film.

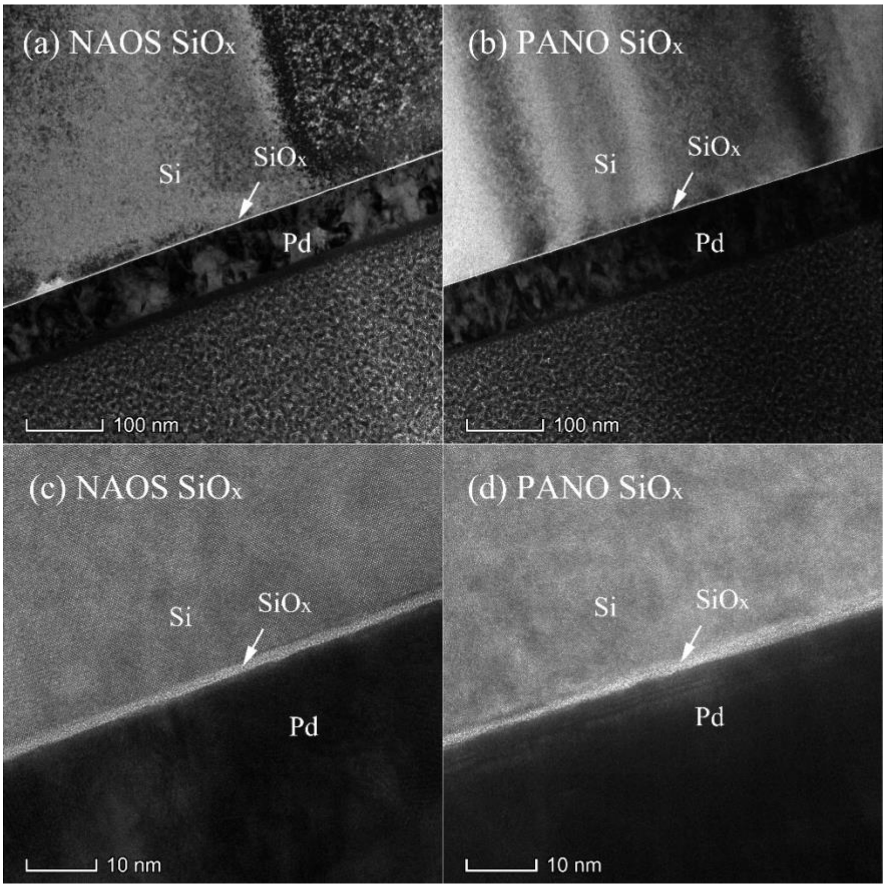
The n-type passivated-contact solar cell with the area of 2cm×2cm was fabricated, whose fabrication procedures were demonstrated as follows. The random pyramids on the front surface were formed by KOH etching. The p^+ emitter was formed by BBr_3 diffusion using a Tempress furnace. The rear poly-Si passivated structure was prepared by the above-mentioned processes, including the growth of PANO SiO_x (200 °C/600s), as well as the controlled NAOS SiO_x (110 °C/900s), the deposition of P-doped a-Si:H, and the crystallization annealing. The p^+ emitter was passivated by a stack of the atomic-layer-deposited (ALD) Al_2O_3 and the PECVD-deposited SiN_x. The front Ti/Pd/Ag electrode of 5 μm and the rear full-area Ag electrode of 800 nm were prepared. Finally, the solar cells were subjected to a forming gas anneal (FGA) at 300 °C for 10 min.

The thickness of ultra-thin SiO_x on polished CZ wafer was measured by spectral ellipsometry (SE) spectroscopy (J.A. Woollam, M-2000DI), and TEM. The structure for ellipsometry measurement was Si-substrate/SiO_x, and the measurement was carried out immediately after the growth of SiO_x. The structure for TEM measurement was Si-substrate/SiO_x/Pd(100nm), which the Pd capping layer was used to protect the SiO_x layer. The chemical-bonding configurations of SiO_x layer were analyzed by X-ray photoelectron spectroscopy (XPS). The minority carrier lifetime was characterized using quasi-steady-state photoconductance (QSSPC) (Sinton WCT-120) measurements. The active phosphorus profile of the poly-Si passivated contact was measured using an electrochemical capacitance-voltage (ECV) system (Buchanan, CVP21). The crystalline structure of the poly-Si layer was characterized by Raman measurement with a 325-nm excitation laser (Renishaw, inVia-reflex). The contact resistivity was measured using the Cox-Strack method [21]. Conductive Atomic Force Microscopy (c-AFM) imaging [22-24] was based on the contact mode of AFM (Veeco D5000 and NSV controller). The solar cells were characterized by one-sun light current density versus voltage (*J-V*) measurements under a solar simulator (Oriel, Sol3A) with the AM 1.5 illumination (100 mW/cm^2) at 25°C.

Results and Discussion

The cross-sectional images of as-grown NAOS and PANO SiO_x layers were taken using the TEM, as shown in Figs 1(a) and (b). The SiO_x layers are grown by the HNO_3 oxidation at 110°C for 900 sec and by the plasma-assisted oxidation at 200°C substrate temperature for 600 sec. We observe that both the as-grown NAOS and PANO SiO_x layers are uniform across the interface without pinholes or other defects. From the high-resolution TEM images, we find that the thickness of NAOS SiO_x ranges 1.3~1.8 nm and the one of PANO SiO_x ranges 1.1~2.4 nm; furthermore, the typical thicknesses of NAOS SiO_x and PANO SiO_x are 1.3~1.6 nm and 1.4~1.7 nm, as shown in Figs 1(c) and (d). PANO SiO_x layer has a broader thickness distribution and a larger overall thickness in comparison with the NAOS SiO_x.

Also, we find that the Si/SiO_x interfaces of the two kinds of SiO_x display different features. The interfaces on both sides of the NAOS SiO_x are evident, from which one can distinguish the Si-substrate lattice and the amorphous SiO_x layer. However, the interface of the PANO SiO_x is dispersive in some zone, which makes it difficult to distinguish the Si-substrate lattice and the SiO_x layer. Thus, it is difficult to determine accurate SiO_x thickness. The dispersive interface was perhaps caused by the enhanced in-diffusion of the oxygen atom and the enhanced oxidation, which results in the unclear SiO_x/Si interface.



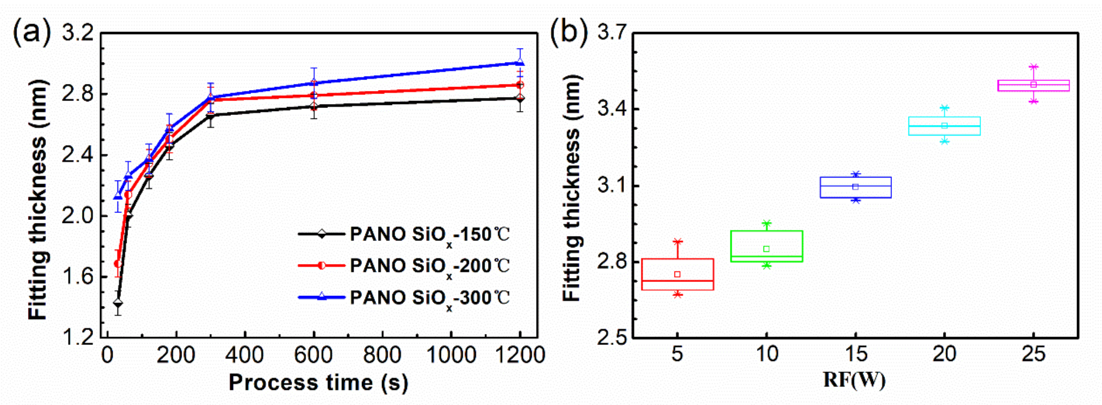
Figures 1. (a, b) TEM images and (c, d) high-resolution TEM images of the as-grown (a, c) NAOS and (b, d) PANO SiO_x. The NAOS and PANO SiO_x are grown by the 110$_o$C HNO_3 oxidation for 900 sec and by the 200$_o$C plasma-assisted oxidation for 600 sec, respectively.

The above-mentioned 110$_o$C NAOS SiO_x and 200$_o$C PANO SiO_x are also measured using ellipsometer with Cauchy model. The numerically fitting thicknesses of the NAOS and PANO SiO_x are typically 2.62 nm and 2.74 nm, respectively, which deviate from the TEM-determined SiO_x thicknesses significantly. The TEM-estimated SiO_x thickness is accurate; in contrast, the ellipsometer fitting SiO_x thickness is not accurate but overestimated.

We would like to discuss the reliability of ellipsometer and why use it before the presentation of the ellipsometer measured results. 1) Cauchy model is used to fitting SiO_x thickness in ellipsometer since it works best when the material has no optical absorption in the visible spectral range. 2) However, to fit an accurate SiO_x thickness is perhaps difficult by using ellipsometer no matter with the fitting models. Typically, one can achieve nm-level accuracy, only if he/she determines one quantity (e.g. thickness) and are absolutely sure what is measured. Otherwise, one may find the fitting results containing random and systematic uncertainty. Furthermore, it is challenging to determine the thickness and refractive index of a film accurately if the thickness < 10 nm at the same.

Therefore, we are not desired to obtain the accurate SiO_x thickness using ellipsometer measurement in this work, since the thickness of SiO_x is < 5 nm with the unknown n and k. We only use ellipsometer measurement to estimate the relative (not absolute) SiO_x thickness, which aims to study the effects of deposition time, substrate temperature, and RF power on the change tendency of SiO_x thickness.

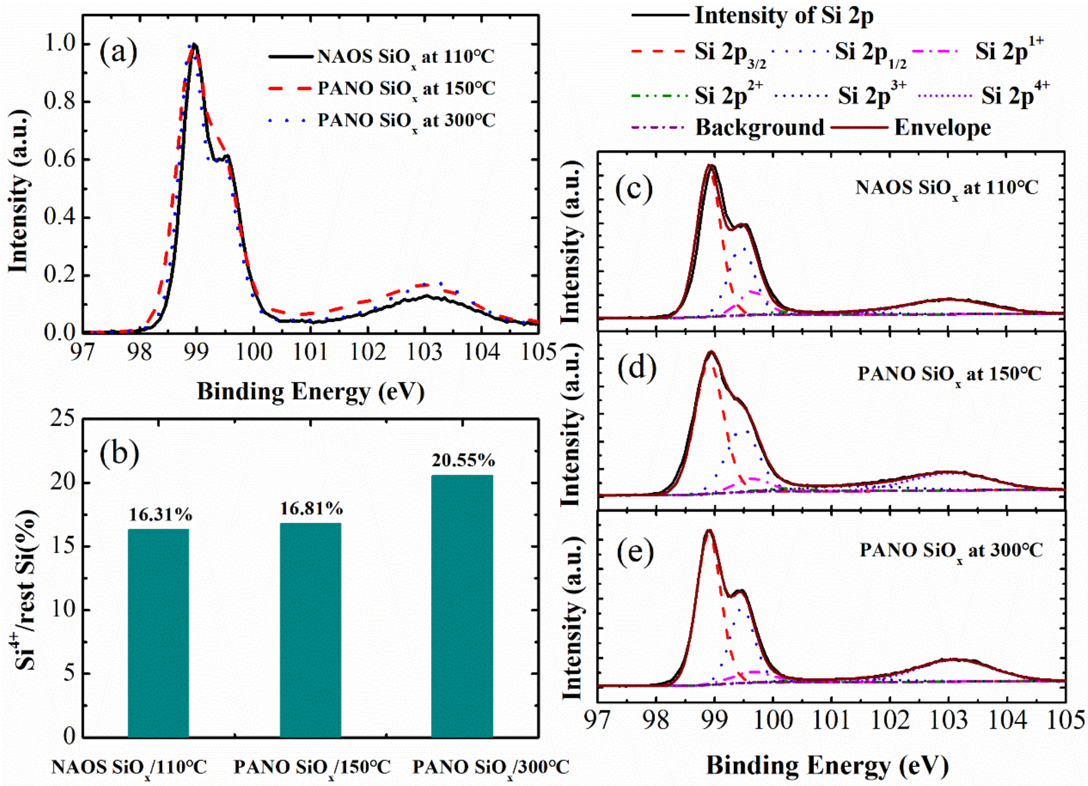
From Figs. 2, we find the following observation. 1) The thickness of PANO SiO_x proliferates at the first tens of seconds but tends to be saturated with the extending processing time; 2) the overall PANO SiO_x layers become thicker with the increment of substrate temperature; 3) the saturated thickness of PANO SiO_x grows with the increase of the power from 5W to 25W. The above results reveal that the PANO SiO_x has a self-saturated thickness, which depends on the substrate temperature and RF power. It is known that the oxide layer grows when oxygen atoms pass through the existing SiO_x layer and reach the Si/SiO_x interface. Thus, the saturated SiO_x thickness is determined by the penetration depth of oxygen with given diffusion energy [18, 19]. Increasing the substrate temperature enhances the diffusion coefficient of atomic oxygen in the SiO_x and increasing the RF power provides high energy for ionized oxygen atoms to penetrate deeper in the SiO_x, both of which helps to increase the SiO_x saturated thickness.



Figures 2. Effects of (a) the processing time, substrate temperature (5W), and (b) RF power (200$_o$C) on the thickness of the PANO SiO_x layer.

The chemical bond configurations of SiO_x plays a key role in determining the passivation quality [10, 25]. The Si 2p bonding energy is analyzed for identifying the stoichiometry of the SiO_x. The 2p binding energy of Si is scrutinized in the range from 97 eV to 105 eV. The peaks of Si $2p_{3/2}$ and Si $2p_{1/2}$ locate at 98.9eV and 99.48eV, respectively. The peak at 98.9eV corresponds to the silicon (Si_{0+}), while the peak at approximately 103eV corresponds to the SiO_2 (Si_{4+}). In details, the peaks of SiO_2 and its sub-stoichiometric species of Si_2O (Si^+), SiO (Si^{2+}), Si_2O_3 (Si^{3+}) are each shifted by 3.3-4.8, 0.95, 1.75 and 2.48 eV from the Si $2p_{3/2}$ peak, respectively [12].

The overall XPS spectra, the enlarged local spectra, and the decompositions of XPS spectra of the as-grown NAOS and PANO SiO_x are showed in Figs. 3(a-e) respectively; and the proportion of various Si sub-stoichiometric species are summarized in Table 1. The Si^{4+} peak of the PANO SiO_x is higher than the one of the NAOS SiO_x, indicating that PANO SiO_x exhibits a higher proportion of Si^{4+}. Furthermore, when the substrate temperature increases from 150°C to 300°C, the oxidization degree of PANO SiO_x is enhanced. The detailed calculation shows that Si^{4+} are 16.3%, 16.8%, and 20.6% in the HNO_3 oxidized, 150^oC N_2O plasma-oxidized, and 300^oC N_2O plasma-oxidized SiO_x, respectively. A higher proportion of high valence-state oxidized Si, such as Si^{4+}, is an indicator of high-quality SiO_x, which would be favorite for achieving high-quality surface passivation [10, 12]. The above results tell us that the N_2O plasma oxidization with a higher substrate temperature is helping to prepare high-quality SiO_x. The enhanced oxidation effects by plasma-assisted oxidation and the substrate temperature are attributed to two main reasons. First, plasma provides high-energy oxygen atoms which can penetrate deeper into the SiO_x layer. Second, raising substrate temperature provides additional energy for oxygen atoms which enhances the capability of oxidation.



Figures 3. (a) XPS spectra, (d) the proportions of Si^{4+}, and (c, d, e) the decompositions of the XPS spectra of the 110$_o$C NAOS, 150$_o$C PANO, and 300$_o$C PANO SiO_x films.

Table 1. The percentage of the sub-stoichiometric Si species of the 110$_o$C NAOS, 150$_o$C PANO, and 300$_o$C PANO SiO_x films.

	Si $2p_{3/2}$	Si $2p_{1/2}$	Si^{1+}	Si^{2+}	Si^{3+}	Si^{4+}
NAOS SiO_x	47.5	23.7	8.7	1.4	2.3	16.3
PANO 150$_o$C	46.6	23.3	5.5	1.5	6.3	16.8
PANO 300$_o$C	46.7	23.3	5.4	0.4	3.6	20.6

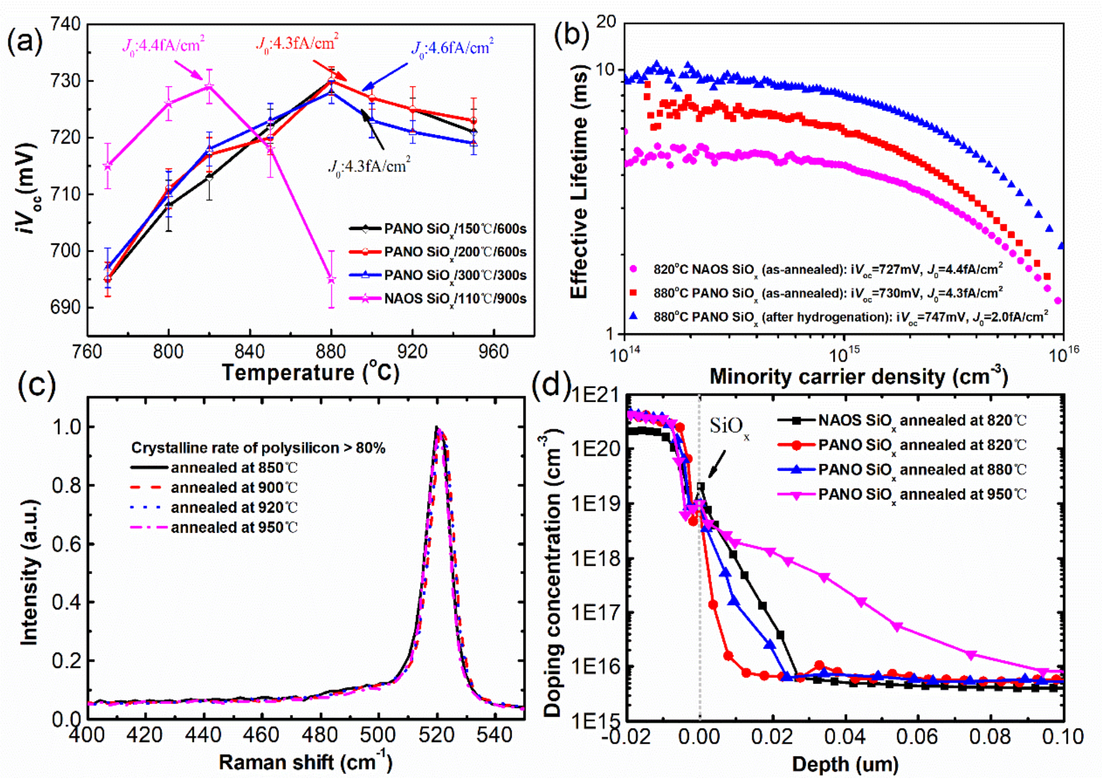


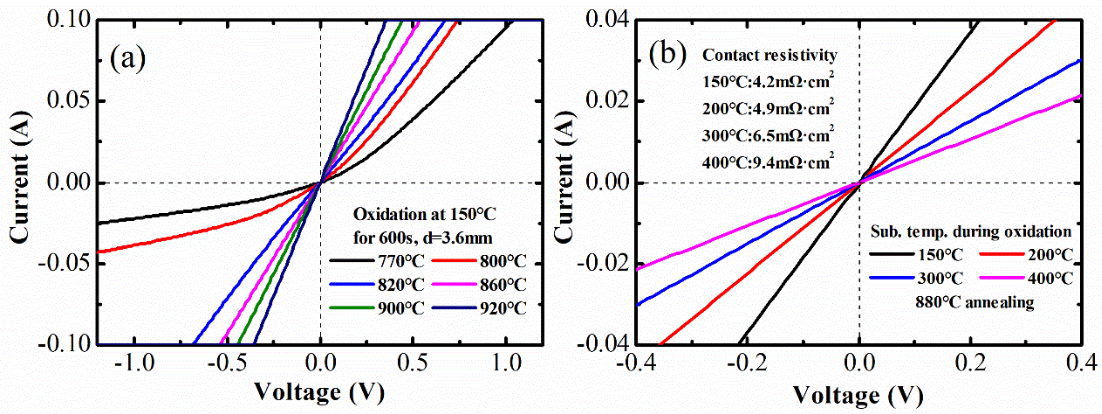
Figure 4. (a) iV_{oc} versus the annealing temperature of the bifacial passivated n-c-Si with the PANO-SiO_x/n+-poly and the reference NAOS-SiO_x/n+-poly-Si without hydrogenation process. (b) Effective lifetime of the best-passivated sample with the NAOS and the PANO SiO_x layer. (c) 325nm-laser Raman spectra and (d) the phosphorus in-diffusion profiles of the poly-Si layers subjected to the annealing at various temperatures. The PANO SiO_x used in Figs. 4(b-d) is grown at 200°C substrate for 600 sec.

The effects of the crystallization temperature on surface passivation are given in Fig. 4(a). The best surface passivation of the as-annealed poly-Si passivated contact with the NAOS SiO_x appears at 820°C, whose champion iV_{oc} and single-sided J_0 are 727 mV and 4.4 fA/cm^2 (Δn=1×10^{15}cm^{-3}) respectively. In contrast, the optimal crystallization temperature of the as-annealed poly-Si passivated contact with PANO SiO_x appears at around 880°C. The passivated contacts with the 150°C/600s,

$200^{o}C/600s$, and $300^{o}C/300s$ PANO SiO_x exhibit similar passivation quality. Surface passivation of the as-annealed passivated contacts with PANO SiO_x is competitive to the one with NAOS SiO_x, i.e., champion iV_{oc}, single-sided J_0, and effective lifetime (τ_{eff}) are 727 mV and 4.3 fA/cm^2 (Δn=3×10^{15}cm^{-3}), respectively. It is noted that the effective lifetime (τ_{eff}) of PANO SiO_x lifetime sample is higher than the one with NAOS SiO_x, which may result from the improved chemical passivation of interfacial SiO_x and the enhanced impurity gettering by the rising annealing temperature [26-28], as shown in Fig. 4(b). We also did hydrogenation using the AlO_x/SiN_x capping and annealing. Champion passivation quality is improved further to iV_{oc}=747 mV, J_0=2.0 fA/cm^2 (Δn=3×10^{15}cm^{-3}), and τ_{eff}=9.0 ms (Δn=1×10^{15}cm^{-3}), which passivation quality is competitive among the existing results [4].

Raman measurement with 325-nm excitation laser is used to detect the crystallinity of the P-doped poly-Si [29], as shown in Fig. 4(c). The Raman spectra of the poly-Si thin films annealed at $850^{o}C$-$950^{o}C$ are overlapped generally, indicating the full crystallization of poly-Si as the temperature of >$850^{o}C$. Thus, the differences in surface passivation caused by annealing temperature cannot be attributed to the crystallinity but other reasons.

ECV measurement is carried out to investigate the effect of annealing temperature on phosphorous in-diffusion profile, as shown in Fig. 4(d). We observe the following phenomena: 1) a remarkable pile-up of phosphorus is found at the interfacial SiO_x; 2) the PANO SiO_x leads to a shallower in-diffusion profile than the NAOS one with the $820^{o}C$ annealing; 3) the in-diffusion of phosphorous is enhanced with the increment of temperature. From the above ECV curves, we can derive two conclusions. First, the PANO SiO_x displays enhanced suppression for phosphorus in-diffusion, which should be attributed to the increase of SiO_x thickness. Second, the surface passivation is highly related with the phosphorus in-diffusion profile with the facts that 1) an un-sufficient (820°C annealing) or an over (950°C annealing) in-diffusion profile leads to the inferior surface passivation; and 2) both the proper in-diffusion profiles (880°C-annealed PANO SiO_x and 820°C-annealed NAOS SiO_x) lead to excellent surface passivation. Thus, a higher crystallization temperature is required for the poly-Si passivated contact with PANO SiO_x, which helps to achieve a proper in-diffusion profile for excellent passivation.



Figures 5. (a) Typically J-V curves of the poly-Si passivated contact subjected to the annealing at the temperature ranging from 770°C and 920°C. The corresponding diameter of the Al electrode is 3.6 mm. (b) Typically *J-V* curves and contact resistivity values of the poly-Si passivated contact whose SiO_x was grown at the various substrate temperatures ranging between 150°C and 400°C.

Cox-Strack measurement is carried out to estimate the contact resistivity (ρ_c) [21]. The test results for the structure of GaIn/n-c-Si/SiO_x/n^+ poly-Si/Al is given in Fig. 5(a) for the PANO SiO_x grown at 150 ^{o}C for 600 sec and annealed at different temperatures. The *J-V* curve shows a Schottky rectifying feature as the annealing temperature below 800 ^{o}C but becomes the Ohmic feature as the annealing temperature above 820 ^{o}C. The contact resistance decreases with the increase of the annealing temperature, and the ρ_c becomes less than 10 mΩ.cm ^{2} as the annealing temperature is higher than 820 ^{o}C.

Furthermore, the effect of PANO SiO_x thickness (controlled by substrate temperature) on contact performance is investigated, as shown in Fig. 5(b). The poly-Si contacts with the PANO SiO_x formed at 150-400 ^{o}C substrate temperature keep as Ohmic contact when annealed at 880 ^{o}C with the ρ_c of <10 mΩ.cm ^{2}, and the lowest ρ_c of 4.2 mΩ.cm ^{2} is achieved with 150 ^{o}C substrate temperature. Herein, raising substrate temperature and SiO_x thickness has small effects on contact resistivity. The reason can be attributed that 880 ^{o}C high-temperature annealing ensures the crystallization of amorphous silicon and the in-diffusion of phosphorus impurity, which leads to the similar interface band structure and carrier transportation possibility. Generally, the contact resistivity of the poly-Si contact with the PASO SiO_x satisfies the requirement of contact for the high-efficiency full rear-contact solar cells.

As shown in Figs. 6, the c-AFM measurement was carried out to examine the 820 ^{o}C- and 920 ^{o}C-annealed poly-Si passivated contacts with the PANO SiO_x grown at 200 ^{o}C substrate. We can find the following observation. 1) The density of the leaking-current spots is in the range of 1×10^{10} cm $^{-2}$ ~ 1×10^{11} cm $^{-2}$; 2) the typical sizes of the leaking spots range 10-40 nm; 3) the density and size of the leaking-current spots increase with annealing temperature.

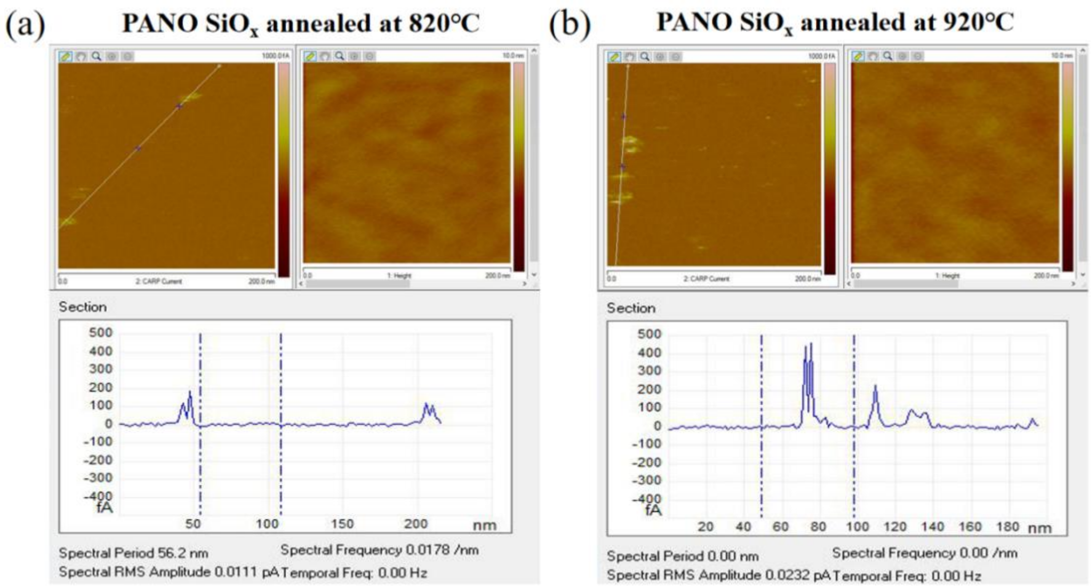


Figure 6. c-AFM image (top left), AFM image (top right), and leaking current along the line (bottom) in c-AFM image of the robust poly-Si passivated contact with the PANO SiO$_x$ subjected to the (a) 820^{o}C and (b) 920^{o}C annealing, whose single-sided J_{0}s are 7.1 and 6.1 fA/cm^2 respectively.

The tip radius of the c-AFM is about 40 nm. However, the probe/Si contact area depends on the contact force setting and material hardness; it is unknown and should be smaller than the tip radius in most measurement conditions. Another factor that may affect the measured spot size is current spreading from the Si/SiO$_x$ interface to the surface where the current is collected. Considering the probe/Si contact area (or resolution) and the current route spreading, it is expected that the leaking spot size would be smaller than the tip radius of 40 nm.

The density and size of the leaking spots are coincident with the previous work reported by K Lancaster et al. [30] and our group [31]. To interpret the nature of these conductive paths is very complicated, and these are no substantial evidence to prove the nature of leaking-current spots as the pinhole only. The leaking-current spot may be originated from the pinholes, the interfacial oxide with reduced thickness but still intact, or the grain boundary at the neighboring area. Thus, further study is required to understand the micro conductance mechanism of c-Si/SiO_x/poly-Si and to reveal the nature of the leaking-current spots. In general, our experiment indicates that the robust poly-Si passivated contact (excellent J_0 of <5 fA/cm^2) with PANO SiO_x possesses a high density (>1×10^{10} cm^{-2} but <1×10^{11} cm^{-2}) of leaking-current spots with the size of 10-40 nm.

Herein, we would like to explain two issues. First, the density of the leaking-current spot detected by c-AFM deviates significantly from the density of the etching pit that is interpreted as pinholes reported by Tetzlaff [32] and Wietler [33]. Two reasons might cause the difference. 1) The c-AFM measurement is non-destructive and sensitive, which detects the tiny leaking current originated from not only pinhole but also thin oxide or grain boundary. 2) The etching method perhaps only reveals one part of the pinholes, such as pinhole clusters or super pinholes, since some of the small-sized pinholes may be peeled off by over-etching. Second, the poly-Si passivated contact with the leaking-current spots of >10^{10}cm^{-2} seems too high to achieve excellent surface passivation, which deviates the theoretical prediction given by Peibst [34, 35]. The reason for the deviation is still unknown because the relationship between c-AFM results and the theoretical model is not established yet.

Finally, the poly-Si passivated contact with the 200^{o}C PANO SiO_x was integrated into the n-type solar cells. The device structure and the best light *J-V* curves are given in Fig. 7. The average efficiency of the poly-Si passivated-contact n-type solar cells with PANO SiO_x is 20.5%, and the champion efficiency reaches 21.01%. The efficiency and the results presented above indicate that PANO SiO_x integrated into solar cells exhibits competitive performances in comparison with the NAOS SiO_x reported previously [10].

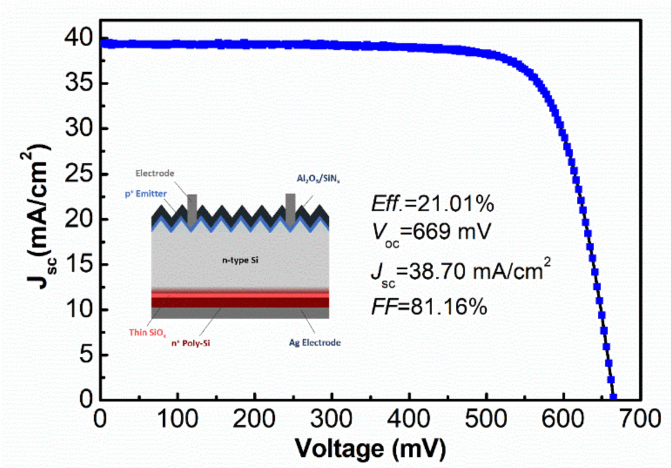


Figure 7. Light *J-V* curves of the typical n-type poly-Si passivated-contact solar cells with PANO SiO_x grown at 200^{o}C for 600 sec (5 W). The area of the solar cells is 2cm×2cm.

Summary

In summary, we developed the PANO method to grown ultra-thin interface SiO_x and used this SiO_x to fabricate the high-quality poly-Si passivated contact. In comparison with the NAOS SiO_x, the PANO SiO_x possessed higher average thickness. The optimized crystallization temperature happened at around 880^{o}C for the best passivation quality with PANO SiO_x. For the poly-Si passivated contact with the PANO SiO_x, champion iV_{oc} of 730mV and single-sided J_0 of 4.3 fA/cm^2 (Δn=3×10^{15}cm^{-3}) after crystallization, and was improved to 747 mV, 2.0 fA/cm^2 (Δn=3×10^{15}cm^{-3}), and τ_{eff}=9.0

ms (Δn=1×10^{15}cm^{-3}) after subsequent AlO_x/SiN_x hydrogenation, which passivation quality is competitive among the existing results. The ρ_c became <10 mΩ.cm^2 when the annealing temperature was >820^{o}C. Noted that, according to the c-AFM measurement, robust poly-Si passivated contact with the PANO SiO_x possessed a high density (1×10^{10} ~1×10^{11} cm^{-2}) of current-leaking spots with the sizes of 10~40 nm. Using PANO SiO_x, we developed the n-type poly-Si passivated-contact solar cell with an efficiency of 21.01%, indicating that the PANO SiO_x is a robust material for passivated-contact solar cell. Overall, the essential advantage of PANO method was able to fabricate PANO SiO_x and amorphous silicon in one PECVD chamber, which avoids the damage of ultra-thin SiO_x by automation when transferring wafers. This work suggested that the PANO SiO_x is promising for industrial manufacture using the in-line PECVD processes.

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