CDP1 – A Data Concentrator Prototype for the Deep Underground Neutrino Experiment

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***Abstract*— The design, power analysis and tests of a first COLDATA Prototype (CDP1) design in 65nm process for the Long Baseline Neutrino Facility (LBNF) and the Deep Underground Neutrino Experiment (DUNE) are presented. CDP1 is a prototype ASIC, for the COLDATA chip, a data concentrator operated in liquid argon. CDP1 is a test vehicle to qualify most of the analog and digital blocks such as LVDS transmitters and receivers, a 1.28 Gbps serializer, a phase locked loop, I^2C for slow control, fast command receiver and calibration logic at cryogenic temperature. The test measurements of these blocks are carried out at room temperature (300K) and at cryogenic temperature (77K). The test measurements presented in this article are in good agreement with the simulation results.**

***Index Terms*—Cryogenic Electronics, DUNE Electronics, Data Concentrator, PLL, Serializer**

I. Introduction

THE Deep Underground Neutrino Experiment (DUNE) is a dual site experiment consisting of two sets of detectors: one in Illinois (Near Detectors) and the other in South Dakota (Far Detectors) [1]. These detectors will enable scientists to search for new subatomic phenomena and potentially transform our understanding of neutrinos and their role in the Universe. Two of the four far detectors will be single-phase time projection chamber, each with 10K tons of liquid argon operating at cryogenic temperature (89K).

Designing Integrated Circuits (IC) for cryogenic temperature is a major challenge for DUNE. Most of the failure mechanisms in CMOS devices are highly temperature dependent. Fortunately, most of these failure mechanisms improve at lower temperature. However, hot carrier degradation gets considerably worse and this is the primary concern for DUNE [2] electronics. Hot carriers degrade the device performance both in NMOS and PMOS transistors, there-by affecting the lifetime of the read-out electronics in the cryostat. It is the fundamental requirement of LBNF/DUNE that the readout electronics must survive over the entire lifetime of the experiment, approximately 20 years. The collaboration has carried out lifetime studies on selected 180nm, 130nm and 65nm CMOS processes [3][4]. It was reported in [4] that, to achieve a life time in excess of 20 years, 130nm process require minimal design changes, whereas 65nm process does not specifically require any design changes. Also, 65nm process has a nominal voltage of 1.2V, which is already lower than the maximum allowable cryogenic temperature of 1.3V. Thus, 65nm devices are more resistant to cryogenic hot carrier degradation. Therefore, the DUNE collaboration has chosen 65nm low-power CMOS process for the data concentrator ASIC.

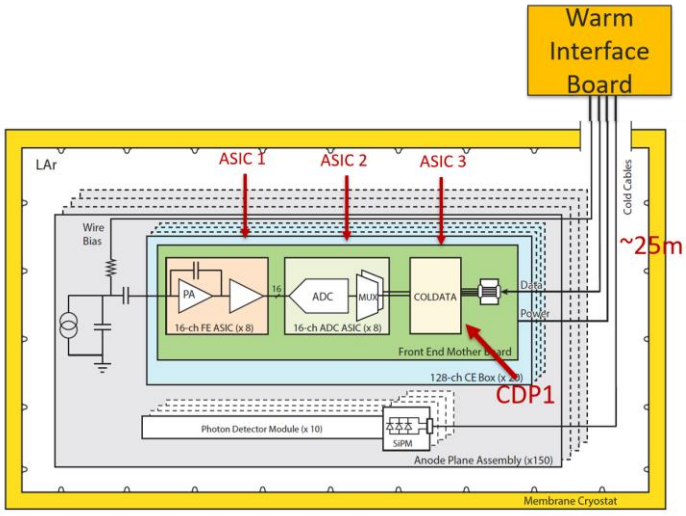

Fig. 1. DUNE Front End Electronics mother board showing different ASICs [5]

The front-end mother boards of DUNE are completely immersed in a liquid argon [5]. Fig.1, shows the assembly of ASICS on the front-end mother boards associated with DUNE cold electronics. Each mother board has three ASICs, each serving a different purpose. The first (ASIC 1) amplifies the signals arising from the interaction of the neutrino particle with the liquid argon, the second (ASIC 2) is an Analog to Digital Converter (ADC) chip that digitizes the incoming analog signals and the third (ASIC 3) is a data concentrator that captures the incoming digital data from several ADCs and sends it over high speed output link. The high-speed output data is sent to the back-end data acquisition system over a ~25m twinax cable. The back-end electronics reside outside of the cryostat. CDP1 being a prototype chip, does not implement line drivers to drive such long cables. The performance measurements reported in this article are carried out on a short coaxial cable (~1m).

The front-end amplifier ASIC, recording the events, was previously developed in [6]. CDP1 is not the final concentrator chip, it is the first prototype design of the DUNE data concentrator that was designed and extensively tested to measure the performance of the major analog and digital building blocks. In this paper, any circuitry inside the cryostat is referred as cold electronics and any circuitry outside the

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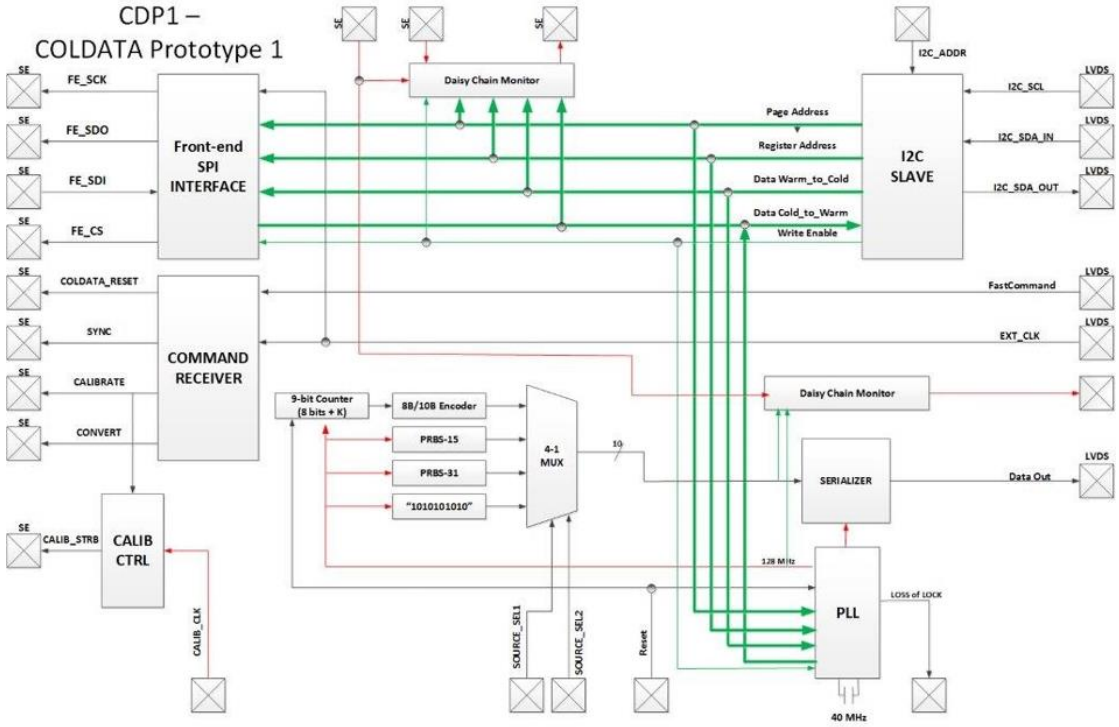

Fig. 2. CDP1 Architecture showing all the analog and digital blocks

cryostat is referred as warm side or warm electronics.

For CDP1, several tests were performed at both room (300K) and cryogenic temperature (77K) to verify the functionality of the digital design and to measure the performance of the main mixed signal circuits which will be used in the final design. The performance results along with the power dissipation measurements of each of these circuitries are summarized at the end this article.

II. CDP1 Building Blocks

CDP1 implemented in a 65nm CMOS process hosts all the building blocks that will be used in the final version of the data concentrator chip, except for those blocks related to the framing of incoming data from the ADC, since the format of these frames had not been set before the CDP1 development was complete. The final specifications of the DUNE data concentrator were formalized recently [6]. Fig. 2, shows the block diagram of the CDP1 architecture, and the purpose of each of these blocks is briefly described in this section.

I²C Slave: The purpose of the I²C slave is to download control information to configure the data concentrator chip. The I²C master controlling the I²C slaves is kept outside of the cryostat. Their communication protocol is a slightly modified version of the standard I²C protocol [7]. As the communication from warm to cold is along, approximately 25m of cable, the single-ended CMOS signaling of the I²C standard has been abandoned in favor of LVDS signaling.
Because of these changes, the bi-directional SDA line of the I²C standard is no longer practical and has been replaced with two SDA lines, I2C_SDA_IN and I2C_SDA_OUT. The LVDS SCL lines remains functionally unchanged from their I²C standard counterpart except the clock stretching is not implemented. The master and slave communication follow a 3-word format. The first word contains the page address (7 bit) and the Read/!Write bit. The second word contains the register address (8 bit). The third word contains the data. The first four bits of the page address are the chip ID. If the transmitted chip ID does not correspond to the chip's actual ID, then no data will be read or written.

Front-end Amplifier SPI Interface: Each front-end amplifier chip [6] has a 3-pad interface that enables certain controls of the chip (e.g. global reset) and permits programming of the chip via a pseudo-SPI protocol. The three pads are CS (Chip Select), SDI (Serial Data Input) and CK_STRB (Clock Strobe). A fourth pad SDO (Serial Data Output) is not involved in the various controls of the interface. Care has been taken with the interface to avoid any unwanted transitions on the CS, SDI or CK_STRB lines that could result in unwanted functions being executed on the LARASIC chip.

Command Receiver: The command receiver is synchronous to the system clock and each command is four-bit wide. Whenever a valid four-bit command is issued from the warm side, the corresponding signal will be generated on the chip. These commands are responsible for time-sensitive signals like synchronization, initiation of calibration or conversion for the ADCs etc.

Serializer: A custom 10:1 1.28 Gbps serializer was designed to send the data collected from eight ADC ICs on the motherboard

out of the cryostat. As mentioned earlier, since CDP1 is a prototype chip, the data used to verify the functionality of the serializer is from a pattern generator on the chip rather than from ADC itself. The various pattern generators implemented on the chip generate different types of data including pseudo-random bit streams (PRBS-15 and PRBS-31), alternating 1 and 0 and a simple 9-bit counter.

The serializer is based on an architecture that is depicted in Fig. 3. As can be seen, the incoming 10-bit parallel data at 128 Mbps is split into two 5-bit words, as the two 5:1 MUXs serialize the 128 Mbps data rate to 640 Mbps data rate. Following the 5:1 MUXs, a 2:1 MUX is used to generate the 1.28 Gbps data by serializing two 640 Mbps data streams using a 640 MHz clock. The 1.28 Gbps data are sampled and synchronized using a flip-flop before being converted to a differential signal. The Current-Mode Logic (CML) driver shown here is a provisional driver that can drive a short coaxial cable. However, for the final data concentrator chip, a dedicated line-driver with pre-emphasis and equalization circuits will be included, which can drive long twinax cables at both room and cryogenic temperature.

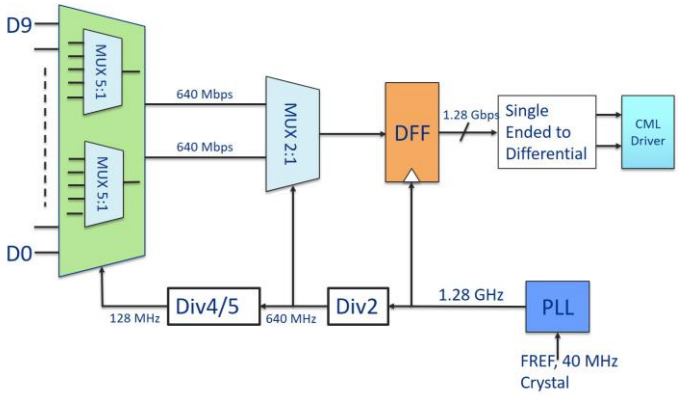

Fig. 3. 1.28Gbps serializer architecture, along with the needed intermediate clock frequencies

Phase Locked Loop (PLL): There are many publications on PLL and data links in the High Energy Physics (HEP) community [8]-[11]. In DUNE project, prior to this submission, several PLL architectures have been designed and their performance were measured at both room and cryogenic temperature. A temperature-compensated PLL design using a triple path PLL design was published in [12], which has a very stable performance over wide temperature range. Considering the design reliability and simplicity, we chose a single-path PLL architecture in CDP1, which has a good performance at both room and cryogenic temperature, meeting the requirements of DUNE data concentrator.

Fig. 4 shows the block diagram of the single-path PLL, which consists of a phase and frequency detector (PFD), a charge pump (CHP), a low pass filter (LPF), a Voltage-Controlled Oscillator (VCO) and a divider. The schematic of the charge pump is shown in Fig. 5. The phase and frequency error between the reference clock CK_{REF} and the feedback clock CK_{FB} detected by the PFD would generate *UP* and *DN* signals that drive the charge pump to charge or discharge the LPF. The control voltage VCTL would go up or down to tune the varactors of the VCO, and thus align the phase and frequency with the reference clock CK_{REF}. The LC based VCO has a capacitance bank controlled by a 6-bit digital word from the I^2C, which acts as the frequency coarse-timing function to make sure the PLL can operate at its optimal working point at different temperature. The PLL uses a 40 MHz reference signal generated from a MEMS oscillator and the output frequency of the PLL is centered around 2.56 GHz. The bandwidth of the PLL is designed to be 1.5MHz, the inductor in the VCO has an inductance of 1.4 nH with the quality factor of 14, and the Kvco is set to be about 100MHz/V. The main parameters are selected based on a linear model of the PLL [13][14]. All the intermediate frequencies (128MHz, 640MHz and 1.28GHz) for the various serializer stages are obtained through dividers in the PLL and serializer. The PLL performance is measured and analyzed in both open and closed loop. In the open loop operation, the VCO control voltage is supplied through an external control voltage (VCEXT), where as in the closed loop operation, the internal control voltage is monitored through an Analog Testing Output (ATO) pin.

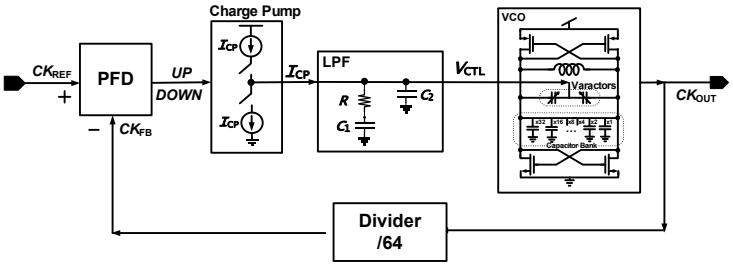

Fig. 4: The block diagram of a single path Phase Locked Loop (PLL)

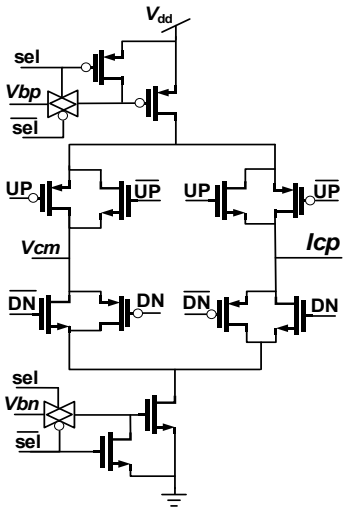

Fig. 5. The circuit schematic of charge pump (CHP)

8b/10b encoder: To achieve DC balance at the back-end data acquisition receivers, the incoming 8-bit data is encoded to a 10bit word on the chip before transmission. The implementation is based on 8b/10b encoder standard as in [14]. This also guarantees enough state transitions to allow reasonable clock recovery in the back-end data receiver.

LVDS Transmitter (Tx) and Receiver (Rx): Custom LVDS Rx and Tx were designed to interface to the warm electronics. These Rx/Tx were designed to operate at multiple supply voltages from 2.5V down to 1.8V and over a wide temperature range from 300K to 77K with a load termination of 100 Ohms. The LVDS Rx can receive a differential voltage signal ranging from 100mV to rail-to-rail. The LVDS Tx has programmable output current varying from 2mA to 8mA.

Through CDP1, we have tested the functionality of LVDS drivers & receivers, 1.28 Gbps serializer, PLL, slow control I^2C, calibration logic for the front ends, fast command receiver and 8b/10b encoder at room temperature and, more importantly at the cryogenic temperature. Their performance results are discussed in Section V.

III. Digital Standard Cell Library and Characterization

The digital logic in CDP1 is realized through semi-custom design flow using industry-standard CAD tools. For the digital designs, a custom digital standard cell library was developed based on the standard cell library provided by the foundry. In foundry provided library, all transistor lengths are of minimum size (60nm). However, previous studies clearly indicated that longer device lengths are an effective way to improve circuit lifetimes through the consequent reduction in hot-carrier degradation effects [4]. Therefore, in the custom standard cell library, the lengths of transistors have been increased from 60nm to 90nm. As a design guide, minimum gate length of 90nm has been used for analog and mixed-signal designs too. The width of transistors, together with the height (9-track) and routing grid of the cells, were left unchanged, so the custom library is inherently slower than the original. This is slightly compensated by the increased mobility in cryogenic operation, and because of the moderate speed requirements of the design, does not constitute an issue. The modified digital standard cell library contains 230 cells, covering the standard types of logic gates and drive strengths and is enough to synthesize all the digital logic. The foundry provided device simulation model are valid for the temperature range of -40ºC to 125ºC, which is not the operating temperature for the DUNE ASICs. Hence, to verify the circuit behavior at cryogenic temperatures (77K), the collaboration had worked with a third-party company to develop cryogenic SPICE device models.

Furthermore, with the new cryogenic device models, a new set of standard cell timing libraries was characterized at various corners using a commercial timing library characterization tool. The overall corners based on Process, Voltage and Temperature (PVT) are summarized in Table II. These corner-based timing libraries were used for timing optimization during static timing analysis in the automatic place and route design flow. This ensured that the data path timing was met at each of these corners.

As it is understood from the device SPICE modelling studies [2], both mobility and threshold voltage (Vth) of the MOS device increase at cryogenic temperature. Depending on the dominant factor, the performance of a logic gate can increase or decrease at cryogenic temperature. Fig. 5. shows a plot of the comparison of timing libraries characterized at cryogenic temperature corner (TT, 1.2V, -189^{0}C) with respect to their room temperature equivalent (TT, 1.2V, 25^{0}C). In a timing library, the gate delays are arranged in a Look Up Tables (LUTs) format, characterized for a set of load capacitance and input transition time. The plot shows the delay data for the full set of digital cells (230 cells). Different colors in the plot represents different standard cells. In the plot, the ratio of the difference between the delays in the two libraries is plotted against the absolute difference between them on the x-axis. The positive ratio of difference in the plot means that the total drive current is dominated by the increase of Vth at cryogenic temperature translating to performance decrease. On the other hand, the negative ratio of difference means that the drive current is dominated by the increase of mobility so the performance increases. Hence, the timing libraries are characterized at several corners to capture all these variations.

As can be seen, in the threshold dominated region the performance of the logic gate is decreased at cryogenic temperature and the maximum ratio of difference is around ~90%, where as in the mobility dominated region the performance of the logic gate increases at cryogenic temperature and the maximum ratio of difference is around ~40%.

TABLE I
PVT CORNERS CONSIDERED FOR TIMING OPTIMIZATION

Process	Voltage	Temperature (^{0}C)
FF	1.08	0
SS	1.32	125
TT	1.20	25
FF	1.08	-189
SS	1.32	-189
TT	1.20	-189

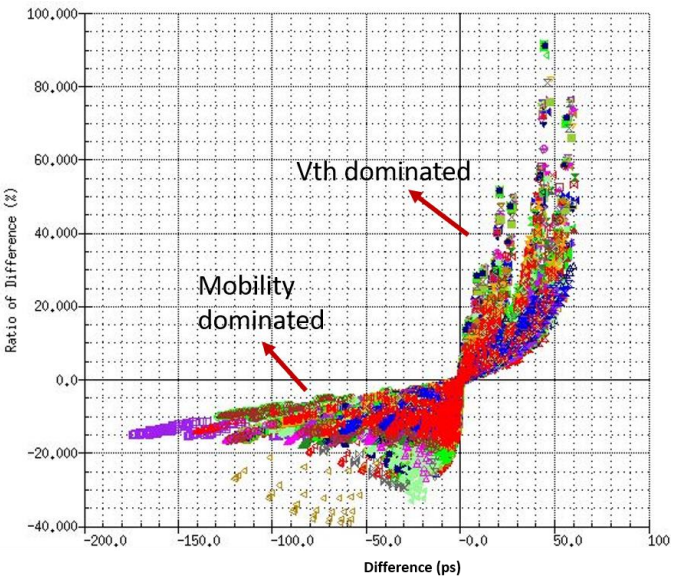

Fig.6. Comparison of timing libraries characterized at room temperature and cryogenic temperature. The difference of the delay is plotted against its % change. Figure also shows which of the parameter Vth or mobility, that is dominated in the device currents at cryogenic temperature .

IV. Power Domains and Measurements

CDP1 has four power domains namely, VDD IO, VDD CORE, VDDA and VDDD. VDD IO is a 2.5V power supply mainly used for the LVDS Tx and Rx, VDD_CORE is a 1.2V power supply for the digital logic on the chip. The PLL-Serializer is an independent block having two dedicated power domains namely analog power supply (VDDA) and digital power supply (VDDD). Both these supplies are operating at 1.2V.

We have measured the power dissipation in each domain by varying the cryostat temperature in either direction from 55K to 300K and from 300K to 55K. The measurements were carried out on two different boards, each having a different CDP1 chip. The current measured in each of these power domains for both the boards were almost the same. Fig. 7, shows the current consumption in each of the power domain for one of the boards. As can be seen in the figure, the current consumption is not the same while ramping the cryostat temperature up or down. However, this variation is less than <=5%, hence was not found to be problematic. The power dissipation in each of the power domain at the room temperature and at the cold is summarized in Table III. It is the LVDS Tx/Rx, that consume significant portion of the total dissipated power on the chip.

Table II
Power Dissipation in Each of the Power Domain

Supply Domain	Power (300K)	Power (77K)
VDD IO	352.5 mW	144 mW
VDD CORE	0.346 mW	0.351 mW
VDDA	13.8 mW	14.8 mW
VDDD	0.194 mW	0.190 mW

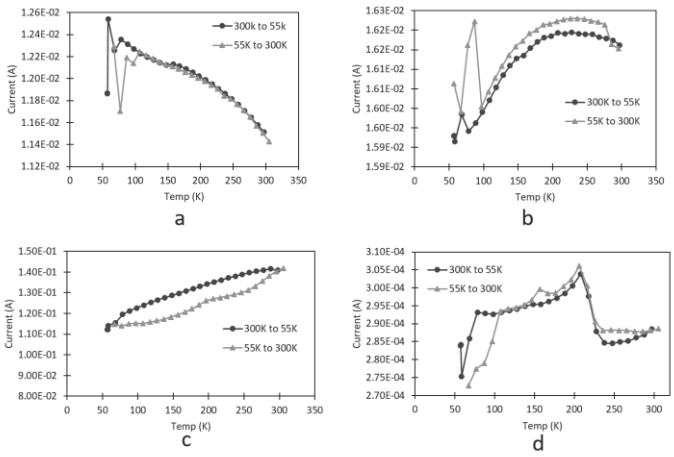

Fig. 7. Current consumption in various power domains over a temperature range from 55K to 300K and vice-versa. a) VDDA domain b) VDDD domain c) VDD IO domain d) VDD CORE domain

V. CDP1 Verification and Testing

The overall verification of the digital logic was based on Assertions and Universal Verification Methodology (UVM); whereas, the functionality of the analog blocks was verified through SPICE simulations. The fully integrated chip (analog and digital blocks) was verified through mixed-signal simulations. CDP1 is a 2mm x 2mm ASIC and Fig. 7. shows the wire-bonding connections from the bare die to the traces on the chip board.

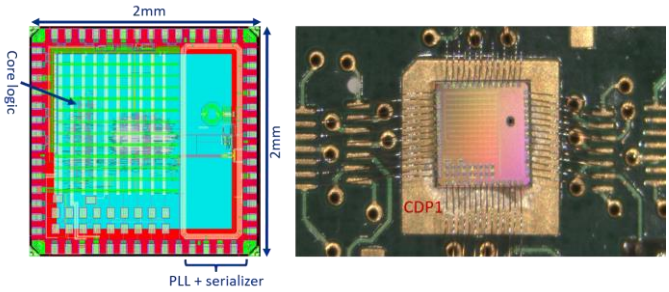

Fig. 8. CDP1 layout and its wire bonding on the daughter board

The test system is based on a PXIe Crate, FPGA modules and Lab View software from National Instruments (Fig. 9). The cryostat used for the testing is a PT-60 cryocooler which can cool a large copper plate. With reference to Fig. 10, which shows the magnified board setup placed inside the cryostat, the CDP1 chip which is on the back of the PCB, is directly and closely in contact with the chilled copper plate. There are two different boards in our test setup called Warm Board and Cold Board. The cryostat, as explained, cools the copper plate and the Cold Board that is in contact with this plate down to the cryogenic temperature. An RTD device on the Cold Board monitors the temperature of the CDP1 chip. The auxiliary commercial-of -the-shelf (COTS) circuits for signal interface and transmission are mounted on the Warm Board. The eye diagrams and bit error rate measurements of the LVDS Tx/Rx, PLL and serializer outputs was obtained with a Tektronix DSA 72004C.

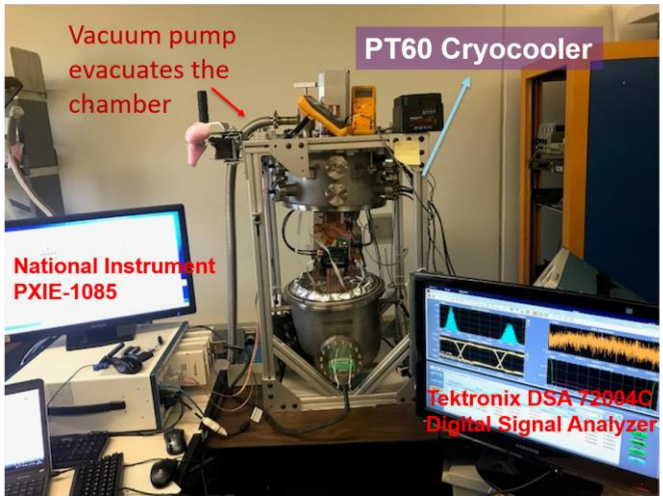

Fig. 9. CDP1 overall test setup

The first test that was carried out is the read and write operations on all the configuration registers through I^2C slave. These operations were repeatedly performed at both room and cryogenic temperature. The I^2C slave had no functionality issues at both the room and cryogenic temperature. After that, the fast command and SPI protocol was thoroughly verified at both room and cryogenic temperature. Verifying digital blocks had inherently verified digital design methodology and more importantly the in-house characterized timing libraries.

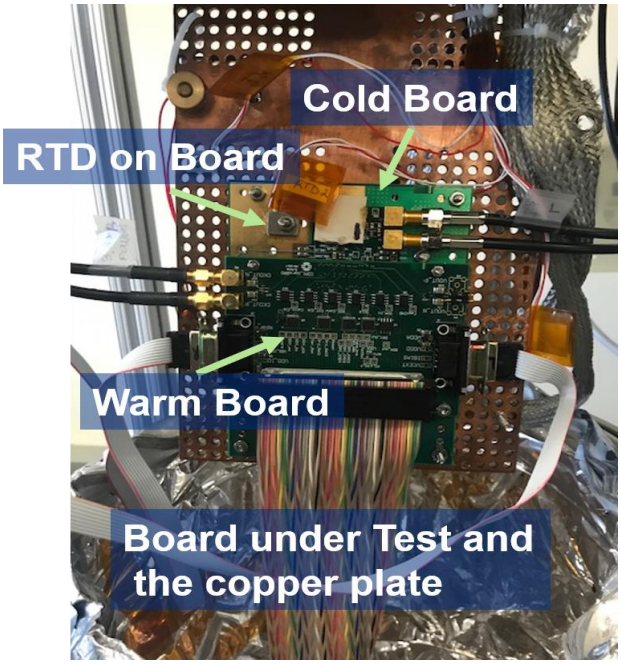

Fig. 10. Cooling plate showing cold and warm board

To measure the performance of LVDS Rx and Tx, a dedicated test structure was designed on another chip prior to CDP1. It is composed of an LVDS Rx and Tx and connected in such a way that the output of the LVDS Rx is an input to LVDS Tx. A 64MHz differential square wave is given as input to the Rx. An eye diagram of the transmitter output is shown in Fig. 11 and the jitter measurements are summarized in Table IV. The total jitter has increased in cryogenic temperature but is still tolerable. The eye is wide open at 77K having a width of ~96% of the unit interval.

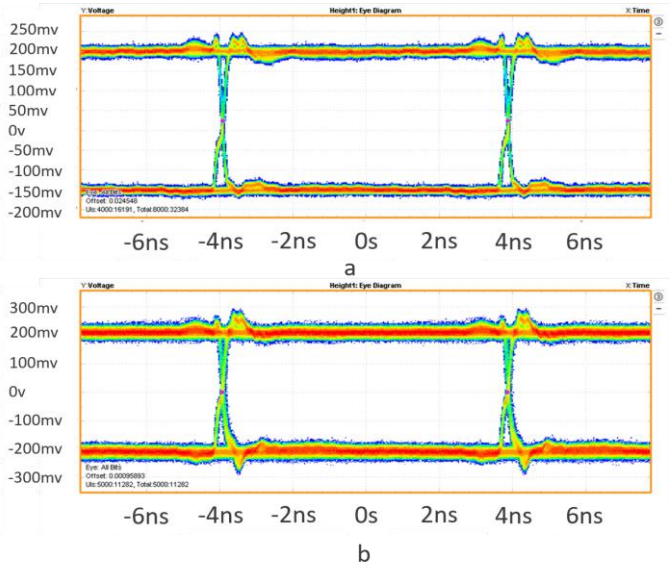

Fig. 11. Eye diagram of LVDS test structure a) at room temperature 300K b) at cryogenic temperature 77K

The test measurements of the PLL are carried out when is at open loop and as well as at closed loop. Fig. 12a shows the measured output frequency of VCO, giving an insight of the VCO tuning range for each of the capacitance band. The measurements are performed both at room temperature and cryogenic temperature i.e. 300K and 77K respectively. In both cases the expected VCO output frequency of 2.56GHz is within the tuning range.

TABLE III
JITTER MEASUREMENTS OF LVDS TEST STRUCTURE

		300K	77K
Total Jitter @ 1e-12 BER	Peak-to-Peak	200 ps	339 ps
Random Jitter (RJ-&&)	Standard deviation	8 ps	18 ps
Deterministic Jitter (DJ-&&)	Peak-to-Peak	87 ps	95 ps
Width @ 1e-12 BER	Unit Interval (fraction of period)	0.97	0.96

Fig. 12b plots the variation of control voltage as a function of temperature while the PLL is operated in a closed loop configuration. By fixing the capacitance through I^2C, the PLL control voltage is registered in the lock state for different cryostat temperature. We observed that there are several bands in which the PLL can always be locked over the entire range of the temperature variation.

Table IV, summarizes the performance of the PLL output clock in the lock state. We measured the various components of the jitter (Total Jitter (TJ), Random Jitter (RJ) and Deterministic Jitter (DJ)) at 300K and 77K. As can be seen there are several capacitance bands in which the PLL is locked. There are also several bands in which the PLL is locked at 300K but did not lock at 77K and vice-versa. For example, in Band 20, the PLL did not lock (NL is abbreviated as Not Locked in Table V) at 300K but it is locked at 77K. The lowest jitter at room temperature (300K) is obtained for the Band 26 configuration of 12.74ps, whereas at cryogenic temperature (77K), which is of interest for DUNE electronics, the lowest jitter was obtained for the Band 32 configuration of 8.8ps. Another observation is that for most of the capacitance bands, the PLL performance at cryogenic temperature is better the room temperature performance.

The serializer performance is measured against various on-chip pattern generators. Fig. 12, shows the eye diagram of a 1.28 Gbps serializer at room temperature (300K) and cryogenic temperature (77k) for the PRBS-15 data pattern as an input. The eye is wide open and the corresponding jitter measurement results for various input data streams are summarized in Table V. The total jitter for the PRBS-15 input data stream at 300K and 77K is 112.02ps and 120.44ps, respectively. The total jitter has slightly increased at the cryogenic temperature compared to room temperature for all the input data streams. However, the percent increase is quite small and within the tolerable limits of the system.

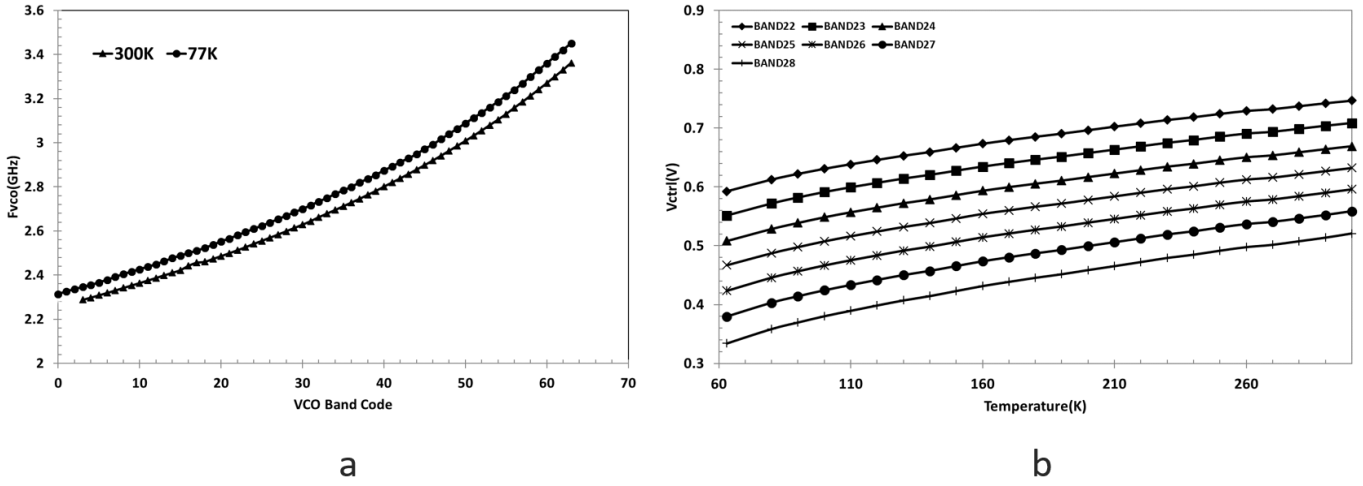

Fig. 12. PLL performance at room temperature and cryogenic temperature a) Voltage Controlled Oscillator (VCO) tuning range b) PLL control voltage variation for different capacitance bands where the PLL is locked.

TABLE IV
JITTER MEASUREMENT RESULTS OF A PLL AT 300K AND 77K

Cap. Band	TJ (ps)		RJ (fs)		DJ (ps)	
	300K	77K	300K	77K	300K	77K
Band 20	NL	9.38	NL	511.50	NL	2.42
Band 21	NL	9.73	NL	511.94	NL	2.56
Band 22	13.12	9.45	821.09	514.76	1.69	2.07
Band 23	13.16	9.67	830.77	512.00	1.45	2.75
Band 24	13.04	9.75	819.20	518.42	1.45	2.98
Band 25	12.84	10.89	808.29	514.05	1.43	3.92
Band 26	12.74	11.85	823.70	515.00	1.19	4.62
Band 27	13.44	12.86	829.30	516.57	1.46	5.09
Band 28	13.06	12.29	845.90	515.69	1.26	5.42
Band 29	14.51	12.64	925.26	517.53	1.07	5.26
Band 30	14.03	11.04	908.70	512.26	1.16	4.73
Band 31	13.52	14.28	895.68	560.41	1.12	6.53
Band 32	13.60	8.80	894.80	510.00	0.91	1.83
Band 33	13.14	NL	885.08	NL	0.80	NL
Band 34	12.96	NL	893.37	NL	0.54	NL

For conciseness, we have just included the eye diagram measurements from one of the input data patterns PRBS-15.

TABLE V
JITTER MEASUREMENT RESULTS OF A 1.28GBPS SERIALIZER AT 300K AND 77K

Data Pattern	TJ (ps)		RJ (fs)		DJ (ps)	
	300K	77K	300K	77K	300K	77K
PRBS-15	112.0	120.4	3.0	3.3	64.6	72.3
PRBS-31	113.0	117.2	3.1	3.0	67.6	72.1
8-bit counter	89.9	98.5	1.4	0.6	70.2	89.6
0101…	15.2	21.2	0.8	0.60	1.4	12.7

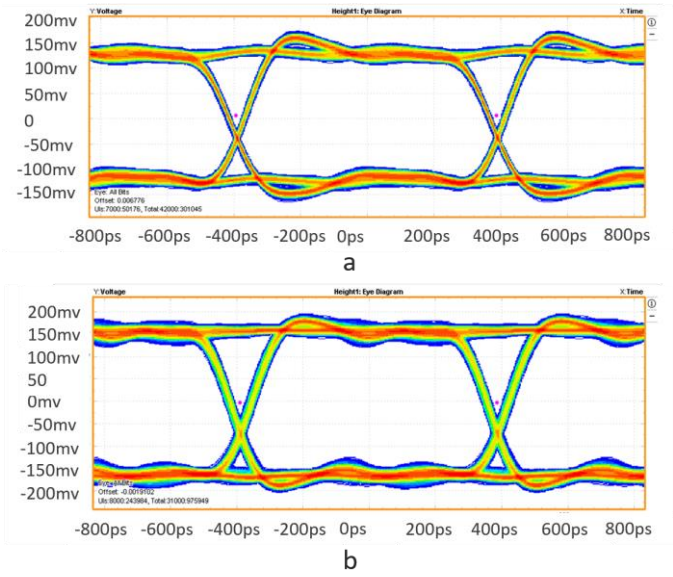

Fig. 13: Serializer eye diagram for a PRBS-15 input data stream a) at room temperature (300K) b) at cryogenic temperature (77K)

VI. CONCLUSION AND FUTURE WORK

The performance and power dissipation of all the major analog and digital circuits was measured at room temperature and cryogenic temperature. For the digital logic, we have considered additional corners covering cryogenic temperature, for which the timing libraries are characterized and included in the digital design flow. We could close the timing successfully at all these corners. This ensured that the digital logic is functional both at the room and cryogenic temperature. Through CDP1, we have also validated our in-house developed timing libraries at cryogenic temperature. Whereas for analog blocks, the designed PLL can compensate the VCO frequency drift over the large temperature variation. There are several bands of VCO that the PLL can lock over the entire temperature

range (77K-300K). The 10:1 serializer can serialize the 10-bit, 128Mbps parallel input data to 1.28Gbps serial data stream. The observed eye diagrams on the scope are wide open, with a jitter performance of ~112ps and ~120ps at room and cryogenic temperature respectively for an input PRBS pattern. The measurements reported in this paper were done over ~1m coaxial cable as CDP1 being a prototype chip. The measured results were in close agreement with the targeted design and within the allocated budget.

The design teams are now actively building the additional blocks such as the data frame formatter, transmitter equalization and pre-emphasis circuit in line driver needed for the final version of the DUNE data concentrator integrated circuit.

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