

1        **Understanding the charge transport mechanisms through ultrathin SiO<sub>x</sub>**  
2        **layers in passivated contacts for high-efficiency silicon solar cells**

3        Abhijit S. Kale,<sup>1</sup> William Nemeth,<sup>2</sup> Harvey Guthrey,<sup>2</sup> Ellis Kennedy,<sup>3</sup> Andrew G. Norman,<sup>2</sup>  
4        Matthew Page,<sup>2</sup> Mowafak Al-Jassim,<sup>2</sup> David L. Young,<sup>2</sup> Sumit Agarwal,<sup>1</sup> and Paul Stradins<sup>2</sup>

5        <sup>1</sup>Colorado School of Mines, Golden, CO, 80401, USA, <sup>2</sup>National Renewable Energy Laboratory,  
6        Golden, CO, 80401, USA, <sup>3</sup> University of California, Berkeley, CA, 94720, USA.

7        Abhijit S. Kale, Prof. Sumit Agarwal  
8        Chemical and Biological Engineering Department  
9        Colorado School of Mines  
10       1613 Illinois Street,  
11       Golden, CO 80401  
12       USA  
13       E-mail: akale@mymail.mines.edu, sagarwal@mines.edu

14  
15       William Nemeth, Dr. Harvey Guthrey, Dr. Andrew G. Norman, Matthew Page, Dr. Mowafak Al-  
16       Jassim, Dr. David L. Young, Dr. Paul Stradins  
17       National Renewable Energy Laboratory  
18       15013 Denver West Parkway  
19       Golden, CO 80401  
20       USA  
21       E-mail: William.Nemeth@nrel.gov, Harvey.Guthrey@nrel.gov, Andrew.Norman@nrel.gov,  
22       Matthew.Page@nrel.gov, mowafak.aljassim@nrel.gov, David.Young@nrel.gov,  
23       Pauls.Stradins@nrel.gov

24  
25       Ellis Kennedy  
26       Department of Materials Science and Engineering,  
27       University of California, Berkeley  
28       Berkeley, CA 94720  
29       USA  
30       E-mail: ellisrae@berkeley.edu

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## 1 **Abstract**

2           We report on the microscopic structure of the SiO<sub>x</sub> layer and the transport mechanism in  
3 polycrystalline Si (*poly*-Si) passivated contacts, which enable high-efficiency crystalline Si (*c*-Si)  
4 solar cells. Using electron beam induced current (EBIC) measurements, we accurately map  
5 nanoscale conduction enabling pinholes in 2.2 nm thick SiO<sub>x</sub> layers in a *poly*-Si/SiO<sub>x</sub>/*c*-Si stack.  
6 These conduction enabling pinholes appear as bright spots in EBIC maps due to carrier transport  
7 and collection limitations introduced by the insulating 2.2 nm SiO<sub>x</sub> layer. Performing high-  
8 resolution transmission electron microscopy at a bright spot identified with EBIC reveals that  
9 conduction pinholes in SiO<sub>x</sub> can be regions of thin tunneling SiO<sub>x</sub> rather than a geometric pinhole.  
10 Additionally, selectively etching the underlying *poly*-Si layer in contacts with 1.5 and 2.2 nm thick  
11 SiO<sub>x</sub> layers using tetramethylammonium hydroxide results in pinhole-like etch features in both  
12 contacts. However, EBIC measurements for a contact with a thinner, 1.5 nm SiO<sub>x</sub> layer do not  
13 reveal pinholes, which is consistent with uniform tunneling transport through the 1.5 nm SiO<sub>x</sub>  
14 layer. Finally, we theoretically show that reducing the metal to *c*-Si contact size from microns, like  
15 in *p*-PERC, to tens of nanometers, like in *poly*-Si contacts, allows lowering of the unpassivated  
16 contact area by several orders of magnitude thus resulting in the excellent passivation, as has been  
17 demonstrated for these contacts.

## 18 **Manuscript text**

19           Solar is a prime candidate for meeting future world energy demands, and Si photovoltaics  
20 (PV) is the leading technology dominating the solar market. Processing and manufacturing  
21 optimization have made Si PV economically comparable to fossil-fuel-based energy sources.  
22 However, to utilize its full potential, and lower the net \$/kWh cost of electricity, it is important to

1 increase the cell efficiency. Efficiency improvements in monocrystalline silicon (*c*-Si) based solar  
2 cells have been achieved by transitioning from the traditional Al-back surface field (20.3%),<sup>1</sup> to  
3 *p*-type passivated emitter rear contact (*p*-PERC) (25.0%),<sup>1-3</sup> to polycrystalline Si (*poly*-Si) contacts  
4 (26.1%),<sup>4</sup> to Si heterojunction cells (26.7%).<sup>5</sup> These improvements are enabled by lowering or  
5 almost completely eliminating the fraction of the silicon surface that is directly in contact with the  
6 metal used for charge collection. Amongst these high-efficiency architectures *poly*-Si contacts are  
7 prime candidates for next-generation Si PV because their high thermal stability makes them  
8 compatible with current mainstream cell manufacturing processes like Ag-paste firing.<sup>6-13</sup>  
9 However, the wide-scale industrial implementation of these structures has been limited due to high  
10 processing costs, and a lack of fundamental understanding from a manufacturing perspective.

11 The very low defect density at the SiO<sub>x</sub>/*c*-Si interface is crucial to enable the ultrahigh  
12 efficiencies reported for these cells. Passivation with SiO<sub>x</sub> has been previously utilized in both the  
13 Al-BSF and *p*-PERC cells.<sup>14-15</sup> The *poly*-Si/SiO<sub>x</sub>/*c*-Si structure has also been well studied in  
14 various Si based electronic devices such as bipolar junction transistors.<sup>16-17</sup> The *poly*-Si/SiO<sub>x</sub>  
15 contact structure was introduced to *c*-Si solar cells by Yablonovitch in the 1980's,<sup>6</sup> followed by  
16 Gan in the 1990's.<sup>7</sup> However, only recently significant improvements to this structure were  
17 reported, which resulted in a 25.1% cell efficiency, a record in 2015.<sup>18</sup> Since then, interest in this  
18 topic has piqued but one of the main factors still not well understood is the carrier transport through  
19 the SiO<sub>x</sub> layer.<sup>19-20</sup>

20 Based on the thickness of the SiO<sub>x</sub> layer, *poly*-Si/SiO<sub>x</sub> passivated contacts can be classified  
21 into two broad categories. The first category is described as tunneling contacts with SiO<sub>x</sub> thickness  
22 ≤1.5 nm, incorporated into a *poly*-Si/SiO<sub>x</sub>/*c*-Si stack, which is then annealed between 850–900 °C,  
23 and has resulted in 25.8% cell efficiency.<sup>21</sup> For these contacts, tunneling through the SiO<sub>x</sub> layer is

1 likely the dominant conduction mechanism.<sup>19, 22-24</sup> The second category, described as pinhole  
2 contacts, consist of an SiO<sub>x</sub> layer with thickness >2 nm within the *poly*-Si/SiO<sub>x</sub>/*c*-Si stack, which  
3 are annealed at significantly higher temperatures between 1000–1050 °C, and have resulted in  
4 26.1% cell efficiency.<sup>4</sup> For these contacts the dominant conduction mechanism is proposed to be  
5 direct conduction between the *poly*-Si layer and the *c*-Si absorber through geometric pinholes in  
6 the SiO<sub>x</sub> layer, formed due to high temperature annealing.<sup>7, 20</sup> Nanoscale pinhole formation via  
7 balling-up of SiO<sub>x</sub> is governed by thermodynamics, and occurs so as to reduce the surface energy  
8 of the SiO<sub>x</sub> layer.<sup>25-26</sup> The extent of balling-up depends on both SiO<sub>x</sub> thickness and annealing  
9 temperature and hence these parameters need to be taken into consideration while optimizing the  
10 *poly*-Si/SiO<sub>x</sub>/*c*-Si contact performance for passivation and conduction. While evidence of localized  
11 conducting regions in an otherwise insulating SiO<sub>x</sub> layer can be inferred by measuring conductivity  
12 through the SiO<sub>x</sub> layer,<sup>13, 27</sup> and via selective etching with a tetramethylammonium hydroxide  
13 (TMAH) solution,<sup>28</sup> the actual observation of the pinhole structure through imaging techniques is  
14 challenging due to their small size, likely 10s of nm, and low surface density,  $\sim 10^5\text{--}10^9\text{ cm}^{-2}$ .<sup>29</sup>

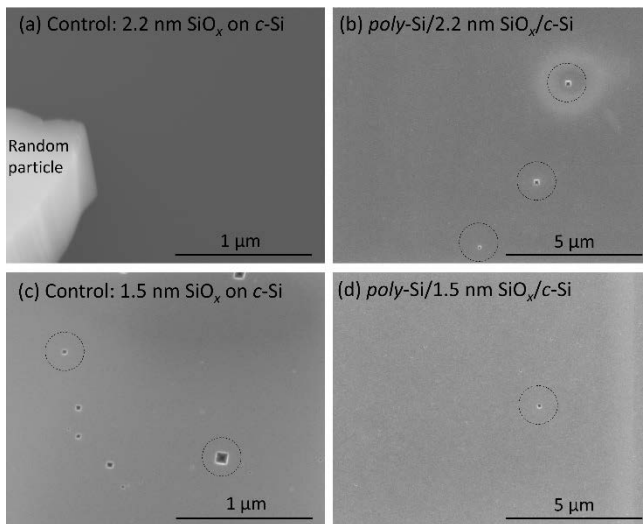
15 In this work, we aim to verify the existence of pinholes in both thick (>2 nm) and thin  
16 (<2 nm) SiO<sub>x</sub> passivating contacts using electron-beam-induced current (EBIC) measurements that  
17 allows for the detection of conductive regions non-destructively while revealing their microscopic  
18 origin through high-resolution transmission electron microscopy (TEM). Our EBIC measurements  
19 support the hypothesis that uniform tunneling transport and locally enhanced conduction through  
20 thinner SiO<sub>x</sub> regions are the dominant transport mechanisms in contacts with 1.5 and 2.2 nm SiO<sub>x</sub>,  
21 respectively. Performing TEM at a region identified as potential pinhole with EBIC reveals this  
22 location to be a thinner SiO<sub>x</sub> region facilitating tunneling transport instead of direct conduction  
23 between *poly*-Si and *c*-Si. To maintain consistency with current terminology,<sup>13</sup> we use the term

1 “pinholes” to refer to features that allow for locally enhanced conduction through an otherwise  
2 non-conducting SiO<sub>x</sub> layer: these features are not necessarily a geometric pinhole.

3 Double-side-polished, phosphorous-doped, float-zone Si(100), 1–5 Ω·cm resistivity, ~280  
4 μm thick wafers were cleaned using piranha, RCA-1 and RCA-2,<sup>30</sup> followed by treatment with  
5 1% aqueous HF. Subsequently, either a 1.5 or 2.2 (±0.05) nm thick dry thermal SiO<sub>x</sub> layer was  
6 grown on the cleaned wafers in a quartz tube furnace with 6:1 N<sub>2</sub>-to-O<sub>2</sub> gas flow ratio. The SiO<sub>x</sub>  
7 thickness was determined by spectroscopic ellipsometry. Doped or intrinsic (*i*) hydrogenated  
8 amorphous Si (*a*-Si:H) was then deposited on both sides of the oxidized wafers using plasma  
9 enhanced chemical vapor deposition (PECVD), as described previously.<sup>31</sup> For the contacts with  
10 1.5 nm SiO<sub>x</sub> layer, the *n*<sup>+</sup>-*a*-Si:H/SiO<sub>x</sub>/*c*-Si/SiO<sub>x</sub>/*p*<sup>+</sup>-*a*-Si:H structures were annealed at 850 °C for  
11 30 min in a quartz tube furnace under N<sub>2</sub>. For the pinhole contacts with 2.2 nm SiO<sub>x</sub> layer, first the  
12 *i*-*a*-Si:H/SiO<sub>x</sub>/*c*-Si/SiO<sub>x</sub>/*i*-*a*-Si:H structures were annealed at 1025 °C for 30 min. Following  
13 treatment with 1% aqueous HF, doped *a*-Si:H layers were deposited to form  
14 *n*<sup>+</sup>-*a*-Si:H/*i*-*poly*-Si/SiO<sub>x</sub>/*c*-Si/SiO<sub>x</sub>/*i*-*poly*-Si/*p*<sup>+</sup>-*a*-Si:H structures and the samples annealed at  
15 850 °C for 30 min resulting in *n*<sup>+</sup>-*poly*-Si/SiO<sub>x</sub>/*c*-Si/SiO<sub>x</sub>/*p*<sup>+</sup>-*poly*-Si structures. We performed a  
16 two-step annealing process for the 2.2 nm SiO<sub>x</sub> contacts to ensure that the extent of conduction  
17 pinhole formation in SiO<sub>x</sub> was not influenced by the different dopant types, i.e., phosphorous and  
18 boron,<sup>32-33</sup> thus, resulting in the best passivation. The structures were then coated with Al<sub>2</sub>O<sub>3</sub>  
19 grown by atomic layer deposition, followed by annealing in forming gas to drive in excess  
20 hydrogen for passivation.<sup>31, 34</sup> Few of these samples were metallized with Al via thermal  
21 evaporation through shadow masks to create 4 cm<sup>2</sup> bifacial test cells. No post-metallization  
22 annealing was performed. Cell performance was quantified using current-voltage (*J-V*)  
23 measurements. EBIC measurements were performed on the same cells, at un-metallized regions,

1 using a scanning electron microscope (SEM) (JEOL JSM-7600) with images acquired using an  
2 electron beam accelerating voltage of 5 kV and beam current of  $\sim 1$  nA. Unmetallized sister  
3 samples were used for TMAH-etching experiments.

4 The open-circuit voltage ( $V_{oc}$ ) for the test cells with the 1.5 and 2.2 nm  $\text{SiO}_x$  layer was  
5  $705 \pm 2$  and  $695 \pm 2$  mV, respectively, indicating good passivation in both contacts. The  
6 corresponding fill-factors were  $75.1 \pm 0.5\%$  (1.5 nm  $\text{SiO}_x$ ) and  $66.3 \pm 0.5\%$  (2.2 nm  $\text{SiO}_x$ ), which  
7 translates to a series resistance<sup>35</sup> of 0.86 and 1.46  $\Omega$ , respectively, indicating that there is sufficient  
8 conduction through the  $\text{SiO}_x$  layer in both the contacts. Thus, we can infer that both the cells have  
9 passivated contacts suitable for follow-up measurements. To ensure unambiguous interpretation  
10 of TMAH-etching and EBIC experiments, the bifacial test cells were fabricated with polished Si  
11 wafers without a transparent conducting oxide or anti-reflection layer. We have demonstrated  
12  $\sim 21.4\%$  front/back *poly*-Si cells using very similar processing conditions.<sup>36</sup>

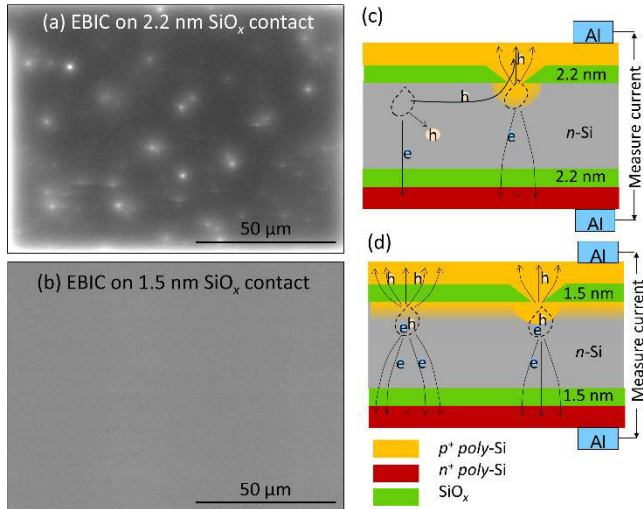


13  
14 FIG. 1. SEM images of polished *c*-Si surface after etching different test structures in 15% TMAH  
15 solution at 75 °C for 3 min. The images correspond to (a) *c*-Si wafer with 2.2 nm thick  $\text{SiO}_x$  layer;  
16 (b)  $n^+$ -*poly*-Si contact with 2.2 nm thick  $\text{SiO}_x$  layer that was annealed at 1025 °C, (c) *c*-Si wafer

1 with 1.5 nm thick SiO<sub>x</sub> layer; and (d) *n*<sup>+</sup>-*poly*-Si contact with 1.5 nm thick SiO<sub>x</sub> layer that was  
2 annealed at 850 °C.

3 TMAH is very selective in removing Si over SiO<sub>x</sub>.<sup>37</sup> For example, using a 15% TMAH  
4 solution at 75 °C the etch times for our 50 nm thick *n*<sup>+</sup>-*poly*-Si layer and 1.5 nm thermal SiO<sub>x</sub> layer  
5 are ~10 and ~300 s, respectively. Hence, by over-etching the *n*<sup>+</sup> *poly*-Si, in our case for 3 min, a  
6 sufficiently large etch pit can be created in the underlying *c*-Si wafer through pinholes that may be  
7 present in the SiO<sub>x</sub> layer: these etch pits can then be visualized by SEM. However, a similar  
8 experiment is difficult to perform for *p*<sup>+</sup>-*poly*-Si contacts due to comparable etch times for a 50 nm  
9 thick *p*<sup>+</sup>-*poly*-Si and a 1.5 nm thermal SiO<sub>x</sub> layer. Figure 1 shows the SEM images of the wafer  
10 surface with different initial film stacks after etching with TMAH solution. Our control sample  
11 (see Fig. 1a) is a wafer with 2.2 nm thermal SiO<sub>x</sub> layer, which after etching does not show any  
12 surface features. A particle on the surface was intentionally captured to ensure that we were indeed  
13 focused on the polished *c*-Si surface. However, when a *n*<sup>+</sup>-*poly*-Si layer with 2.2 nm SiO<sub>x</sub> is etched  
14 (see Fig. 1b), we observe numerous inverted pyramid-like features, highlighted by dotted circles.  
15 These are most likely formed due to TMAH-induced etching in the presence of local non-  
16 uniformities in the SiO<sub>x</sub> layer that originate due to annealing of the 2.2 nm SiO<sub>x</sub> contact at 1025  
17 °C. Figure 1c shows the SEM image of an etched wafer surface with a 1.5 nm thermal SiO<sub>x</sub> layer.  
18 Surprisingly, even though this sample was without a *poly*-Si layer, we still notice the presence of  
19 numerous inverted pyramid-like features. These are observed irrespective of the etching  
20 conditions, 3–15 min in TMAH at 60–75 °C. Since it is known that SiO<sub>x</sub> grows uniformly and  
21 almost stress-free on a flat *c*-Si surface,<sup>38</sup> we speculate that the etch pits observed in Fig. 1d  
22 (*n*<sup>+</sup>-*poly*-Si with 1.5 nm SiO<sub>x</sub> contact) are simply artifacts created by non-uniform TMAH-etching  
23 of the thin SiO<sub>x</sub> layer. Hence, the formation of etch pits after TMAH-etching in a 1.5 nm SiO<sub>x</sub>

1 contact is inconclusive. Therefore, we further studied these contacts using EBIC measurements,  
2 which is non-destructive, and sensitive to electronic effects.



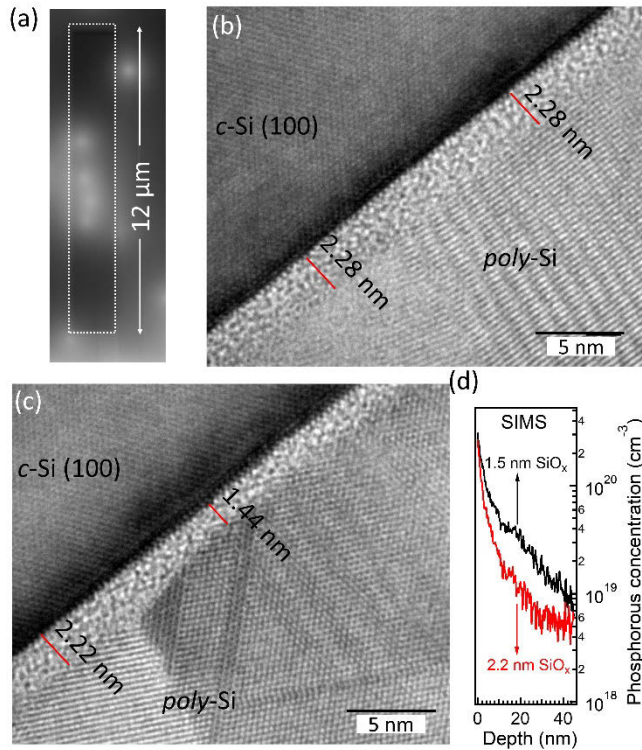
4 FIG. 2. EBIC maps of  $p^+$ -*poly*-Si passivated contacts with (a) 2.2 nm and (b) 1.5 nm thick  $\text{SiO}_x$   
5 layer. Schematic of proposed current transport pathways in passivated contact cell test structures  
6 with (c) 2.2 nm and (d) 1.5 nm thick  $\text{SiO}_x$  layer.

7 The intensity in EBIC images results from the separation of electron-hole pairs generated  
8 by the electron beam within a SEM and subsequent collection of these excited carriers, which  
9 results in a current.<sup>39-40</sup> The generated current depends on the interaction of charge carriers with  
10 defects or inhomogeneities in the device and the carrier collection probability. Thus, EBIC  
11 measurements can result in maps with either no features due to spatially uniform carrier collection,  
12 darker features due to carrier recombination in regions with defects, or brighter features due to  
13 enhanced local carrier collection. Figures 2a and 2b show the EBIC images of the metallized test  
14 cells measured on  $p^+$ -*poly*-Si side with the 2.2 and 1.5 nm  $\text{SiO}_x$  contact, respectively. Figures 2c  
15 and 2d show the schematic of the proposed carrier recombination and current pathways for the  
16 same. The density of bright spots in the EBIC images for  $n^+$ -*poly*-Si side of the same test cells was  
17 similar to  $p^+$ -*poly*-Si side, and therefore not discussed. We can see that while the EBIC map for

1 the 2.2 nm SiO<sub>x</sub> contact shows numerous bright spots, the 1.5 nm SiO<sub>x</sub> contact does not show any  
2 features. We attribute the bright spots in Fig. 2a to enhanced conduction through the 2.2 nm SiO<sub>x</sub>  
3 layer. If recombination at a pinhole in a conducting SiO<sub>x</sub> layer is significant then a pinhole region  
4 should appear darker in EBIC. However, for the case of a contact where the SiO<sub>x</sub> layer is non-  
5 conducting, carrier collection probability is much higher in proximity to a pinhole, thus resulting  
6 in a higher EBIC signal.<sup>39-40</sup> As shown schematically in Fig. 2c, there are two components to the  
7 locally enhanced EBIC signal in Fig. 2a: first, a depletion region forms underneath a pinhole due  
8 to higher dopant diffusion from *p*<sup>+</sup>-*poly*-Si into the wafer directly through the SiO<sub>x</sub> pinhole  
9 compared to the continuous SiO<sub>x</sub> layer, thus, improving carrier separation.<sup>41</sup> Second, there is  
10 reduced charge collection far from pinholes due to lateral diffusion requirements introduced by the  
11 insulating 2.2 nm thick continuous SiO<sub>x</sub> layer. Any holes excited away from the pinhole need to  
12 first diffuse to a pinhole location before being collected by the *p*<sup>+</sup>-*poly*-Si layer. The measured  
13 current will reduce due to hole recombination during this diffusion. While the quantification of  
14 these and/or other effects is difficult, nonetheless, we can infer from the bright spots in the EBIC  
15 image in Fig. 2a that local pinhole-like transport dominates for the contacts with ~2.2 nm thick  
16 SiO<sub>x</sub> layer. Further analysis shows that the intensity of the bright spots varies: this suggest that the  
17 size of the pinhole-like features varies or carrier collection probability varies due to differences in  
18 the structures of these pinhole-like defects.

19         The lack of contrast in the EBIC image for the 1.5 nm SiO<sub>x</sub> contact (Fig. 2b) means that  
20 the carrier collection efficiency is uniform over the sample surface. This is possible only when the  
21 resistance to carrier transport through a SiO<sub>x</sub> layer and pinholes (if they exist) is comparable during  
22 the EBIC measurement. Thus, we can conclude that tunneling through SiO<sub>x</sub> is the likely dominant  
23 carrier transport mechanism for the 1.5 nm SiO<sub>x</sub> contact. It must be noted that the absence of any

1 bright or dark spots compared to the background in the EBIC image for these contacts cannot be  
 2 interpreted as absence of pinholes. It is possible that the diffused junction underneath the  $\text{SiO}_x$   
 3 layer, formed due to dopant diffusion during the 850 °C anneal,<sup>41</sup> separates the carriers very  
 4 efficiently. Hence, recombination at pinholes, which would otherwise lead to dark spots, might not  
 5 influence EBIC intensity, i.e., field-effect passivation dominates over chemical passivation.<sup>42</sup>



6  
 7 FIG. 3. (a) EBIC image of region lifted out by FIB for TEM. Dotted rectangle shows the signal  
 8 generated under the protective Pt layer. Cross sectional TEM image of pinhole type passivated  
 9 contact at two different locations showing: (b) Uniform  $\text{SiO}_x$  thickness; and (c) Local thinning of  
 10  $\text{SiO}_x$  layer. (d) SIMS depth profile of phosphorous underneath the  $\text{SiO}_x$  layer of passivated contact  
 11 with 1.5 (black) and 2.2 (red) nm thick  $\text{SiO}_x$  layer after annealing at 850 °C. SIMS data reproduced  
 12 from reference.<sup>41</sup>

13 Since, the probability of detection of pinholes using techniques like TEM is very low due  
 14 to their small size and low surface density,<sup>29</sup> we perform site-specific TEM of a potential pinhole

1 via EBIC imaging in a dual-beam focused ion beam (FIB) workstation (FEI Nova NanoLab 200).  
2 After identifying a region with a few bright spots in EBIC (see dotted rectangle in Fig. 3a), a  
3 protective Pt layer was locally deposited on top of it. The TEM cross-section specimen was then  
4 prepared near the center of bright spots by standard FIB liftout methods, and the Ga<sup>+</sup> ion FIB  
5 damage removed by low energy (<1 kV) Ar<sup>+</sup> ion milling while cooling the sample using liquid N<sub>2</sub>  
6 in a Fischione NanoMill. Diffraction and phase contrast high-resolution TEM imaging were then  
7 performed on the prepared sample using a TEM (FEI Tecnai G<sup>2</sup>30 SuperTwin) operated at 200  
8 kV. Most of our ~260 high-resolution TEM images appear as shown in Fig. 3b, a uniform layer of  
9 ~2.3 nm thick SiO<sub>x</sub> separating the *c*-Si wafer and the *poly*-Si layer. However, in one image (see  
10 Fig. 3c) we observed significant localized thinning of the ~2.3 nm thick SiO<sub>x</sub> layer to ~1.4 nm. We  
11 refer to this thinned down SiO<sub>x</sub> region as a conduction pinhole. We consider this as a significant  
12 finding since previous TEM studies demonstrating SiO<sub>x</sub> balling-up were performed on samples  
13 intentionally annealed to very high temperatures or had a very thin SiO<sub>x</sub> layer causing significant  
14 SiO<sub>x</sub> balling-up, resulting in very poor passivation.<sup>19, 25-26</sup> Our sample still retained good  
15 passivation (695 mV  $V_{oc}$ ) and conduction. The ~1.4 nm thick SiO<sub>x</sub> layer is within the tunneling  
16 regime and should result in effects similar to a geometric pinhole in the SiO<sub>x</sub> layer, i.e., enable  
17 conduction, may create etch pits during TMAH-etching, and appear as a bright spot in EBIC.  
18 Additionally, the thinner SiO<sub>x</sub> layer will allow for more dopant diffusion than the thicker SiO<sub>x</sub>  
19 layer, as shown by the secondary ion mass spectrometry (SIMS) depth profile in Fig. 3d, which  
20 has been reproduced from our previous work.<sup>41</sup> This enhanced dopant diffusion will create a local  
21 depletion region under the thinner SiO<sub>x</sub> region allowing for more efficient carrier separation during  
22 the EBIC measurements, thus resulting in conduction pinholes to appear bright as witnessed in  
23 Fig. 2a. We would like to clarify that in our experiments we have separated out the conduction

1 pinhole formation step (1025 °C) and the dopant diffusion step (850 °C). Since SIMS does not  
2 have the lateral resolution to distinguish the locally thin ~1.4 nm SiO<sub>x</sub> regions from the surrounding  
3 2.2 nm thick SiO<sub>x</sub> regions (see Fig. 3c), we instead perform SIMS on two separate samples with  
4 1.5 and 2.2 nm thick SiO<sub>x</sub> layers within the *poly*-Si/SiO<sub>x</sub>/*c*-Si stack annealed to 850 °C.

5 The results in Figs. 2 and 3 show that tunneling through SiO<sub>x</sub> is the dominant transport  
6 mechanism in both 1.5 and 2.2 nm SiO<sub>x</sub> contacts. The visual identification of conduction pinhole  
7 as a locally thinned tunneling SiO<sub>x</sub> layer was possible due to in situ milling within the vicinity of  
8 a bright spot identified during the EBIC measurement. However, it is possible that we may have  
9 milled away the actual pinhole and are instead just imaging a section that is away from the center  
10 of a crater-shaped structure. We also cannot rule out the possibility that while some conduction  
11 pinholes may be true geometrical pinholes, others might correspond to regions with locally thin  
12 tunneling SiO<sub>x</sub> layer as suggested by Fig. 3c. This agrees with the fact that the brightness of the  
13 pinholes varies in the EBIC image for the pinhole type contact shown in Fig. 2a.

14 High performance of Si solar cells is enabled by passivated contacts with low contact  
15 resistivity while maintaining high degree of surface passivation. In *p*-PERC cells with an  
16 efficiency potential of ~24%,<sup>43</sup> good surface passivation is realized by localized back surface field  
17 contacts between Al and *c*-Si through 10s of microns wide openings made through a dielectric  
18 Al<sub>2</sub>O<sub>3</sub>/SiN<sub>x</sub> passivation layer stack. Below, we show that the contact performance is expected to  
19 improve remarkably by reducing the local contact (geometric pinhole) size to nanometers. Indeed,  
20 the metal to semiconductor contact area fraction  $f$  determines the surface recombination losses in  
21 the cell via the total diode current pre-factor  $J_{o,total}$ , which is given by Eq. 1, where  $J_{o,pinhole}$  and  
22  $J_{o,oxide}$  are the pre-factors for the unpassivated metallized region and the passivated oxide region,  
23 respectively.

$$J_{o,total} = f \times J_{o,pinhole} + (1 - f) \times J_{o,oxide} \quad (1)$$

On the other hand, the total contact resistivity, which determines the fill-factor, is a sum of area-independent specific contact resistivity,  $R_{pinhole}$  ( $\Omega \cdot \text{cm}^2$ ), in the pinhole and the spreading resistance within the wafer underneath the pinhole. The spreading resistance for effective pinhole radii,  $r$ , that are much less than the wafer thickness, can be approximated as  $\rho_w/4r$  for wafer bulk resistivity of  $\rho_w$ .<sup>44</sup> Thus the total resistance,  $R_{total}$ , is given by

$$R_{total} = \left( R_{pinhole} + \frac{\rho_w}{4r} \times \pi r^2 \right) / f \approx \pi \rho_w r / 4f. \quad (2)$$

The 2<sup>nd</sup> term in Eq. 2, which relates to spreading resistance, is 2-3 orders of magnitude greater than the  $R_{pinhole}$  term for pinhole sizes between 1 nm to 10  $\mu\text{m}$ . The interesting conclusion to draw from Eq. 2 is that for the same  $R_{total}$ , as the size of pinhole decreases from  $\sim 10 \mu\text{m}$  in  $p$ -PERC to  $\sim 10 \text{ nm}$  in pinhole containing *poly*-Si contact, the unpassivated area fraction  $f$  can be lowered by nearly three orders of magnitude. This feature of nanostructured  $>2 \text{ nm}$   $\text{SiO}_x$  contacts allows for sufficient conduction through the pinholes in  $\text{SiO}_x$  layer in passivated contacts while resulting in very low  $J_o$ . It must be noted that while the  $J_{o,pinhole}$  term in Eq. 1 has some inverse dependence on the pinhole size,<sup>45</sup> the 26.1% cell demonstrated by such contacts shows that there is a net improvement in device performance when using nanostructured contacts.<sup>4</sup> Hence, we can treat pinhole containing *poly*-Si contacts as a category of PERC,<sup>3</sup> i.e., “nano-PERC” contacts, exhibiting nanometer size instead of micron size holes in the passivating  $\text{SiO}_x$  layer. We also propose that instead of using high temperature annealing, other pinhole formation techniques such as nano-imprint lithography<sup>46</sup> could be explored. Therefore, local nano-pinhole contacts are excellent candidates for the next generation  $c$ -Si photovoltaics, and could have potential uses in other photovoltaic and electronics technologies.

1           In summary, we have demonstrated the use of EBIC to map conduction enabling pinholes  
2 in *poly*-Si/SiO<sub>x</sub> passivated contacts. Pinhole-like structures appear as bright spots in contacts with  
3 ~2.2 nm SiO<sub>x</sub> layer due to carrier transport and collection limitations. Site-specific TEM  
4 investigation revealed that a conduction pinhole can be a region of tunneling SiO<sub>x</sub> layer. The  
5 detection of similar pinholes in 1.5 nm SiO<sub>x</sub> contacts was challenging due to TMAH-etching  
6 artifacts and defect detection limitations in EBIC measurements: this is consistent with the  
7 tunneling nature of the 1.5 nm SiO<sub>x</sub> layer. Thus, the carrier transport mechanism in both 1.5 and  
8 2.2 nm thick SiO<sub>x</sub> contacts is through tunneling, the difference being uniform tunneling in the first  
9 case while tunneling through locally thin SiO<sub>x</sub> regions in the latter. Finally, we propose a nano-  
10 PERC concept which might allow for high efficiency *c*-Si cells.

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