Thermo-mechanical lift-off and re-contacting of CdTe solar cells

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ABSTRACT: Controlled delamination of thin-film photovoltaics (PV) post-growth can reveal interfaces that are critical to device performance, yet are poorly understood due to their inaccessibility within the device stack. In this work, we demonstrate a technique to lift off thin-film solar cells from their glass substrates in a clean, reproducible manner by first laminating a

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polymeric backsheet to the device, then thermally shocking the system at low temperatures ($T \leq -30^{\circ}C$). To enable clean delamination of diverse thin-film architectures, a theoretical framework is developed and key process control parameters are identified. Focusing on CdTe devices, we show that the lamination temperature and device architecture control the quality of lift-off, while the rate at which the film stack is removed is controlled by the delamination temperature. Crack-free CdTe devices are removed and successfully re-contacted, recovering up to 80% of the original device efficiency. The areal density of these devices is ~0.4 kg m^{-2}, a reduction of over an order of magnitude relative to their initial weight on glass. The framework developed here provides a pathway toward both the development of inexpensive, flexible PV with high specific power and the study of previously buried interfaces in thin-film architectures.

1. Introduction

In thin-film photovoltaics (PV), such as cadmium telluride (CdTe) and $CuIn_xGa_{1-x}Se_2$ (CIGS), delamination is typically considered to be a catastrophic failure and careful precautions are taken to ensure that it does not occur during device fabrication. However, if state-of-the-art devices could be robustly delaminated post-growth, the specific power (power-to-weight ratio) would be drastically improved while maintaining low-cost, high-throughput processes, and material quality associated with high-temperature growth. Additionally, controlled delamination, or 'lift-off,' enables access to critical interfaces that have been buried under microns of material during standard device growth. These interfaces can then be studied using standard surface analysis techniques, such as x-ray photoelectron spectroscopy,[1, 2] and/or modified to improve device performance.[3-5] In superstrate CdTe, this is particularly interesting because the newly exposed interface is directly adjacent to the p-n heterojunction, which will allow for techniques

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that have been used to characterize and passivate the back interface[6,7] now to be used at the previously inaccessible front interface.

The concept of lift-off was first demonstrated in 1978 by Konagai *et al.*[8] for epitaxially-grown monocrystalline GaAs films. In their work, a sacrificial layer (AlGaAs) was grown between the substrate and device and then preferentially etched post-growth to release the thin-film device. Bedell *et al.*[9] later developed a technique in which a stressor layer and flexible handle were adhered to a GaAs crystal and pulled in tension to propagate a carefully initiated crack along a preferred crystallographic plane. While this technique eliminated the need for a sacrificial layer, it was limited to single-crystal systems and could not, therefore, be applied to less expensive polycrystalline technologies like CdTe and CIGS.

Using the sacrificial layer approach, Tiwari *et al.* developed a process to make polycrystalline CdTe and CIGS solar cells on polyimide films by constructing a glass/NaCl/polyimide/solar cell stack, then dissolving the NaCl in water.[10,11] This technique was able to produce good device performance, but it required careful process optimization and reduced growth temperatures to accommodate the relatively low thermal tolerance of polyimide (450-500˚C). Alternatively, the Minemoto group followed the direction of Bedell *et al.* and lifted off CIGS films by bonding a lift-off handle (glass, polyimide) to the device using epoxy and pulling in tension.[12] While flexible, crack-free devices have been demonstrated using this method,[5] significant process and device optimization was required, making the translation of this method to other thin-film technologies difficult.

In this work, we demonstrate crack-free lift-off of CdTe and CIGS device stacks through a two-step process that consists of first laminating a polymeric backsheet to the standard devices, then thermally shocking the system at low temperatures ($T \leq -30$˚C). This causes the polymer to

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contract quickly and pull the polycrystalline film cleanly off of its glass substrate. The uniqueness of this work is in the theoretical framework that is developed and key process control parameters that are identified to enable clean delamination of diverse thin-film architectures. Focusing on CdTe, we demonstrate that lift-off quality and rate can be controlled by adjusting thermal strain through key temperature set points. After lift-off at the front contact interface in superstrate CdTe, device functionality is restored through re-application of a transparent front contact and 11% device efficiency (~80% of original device efficiency) is achieved.

2. Theoretical Framework

In this section, the mechanism of delamination is discussed in order to identify the critical parameters involved. Figure 1 displays a schematic illustration of delamination in a simplified system containing only four layers: (1) glass substrate/superstrate, (2) thin-film solar cell, (3) stressor, and (4) handle. Delamination in both CdTe and CIGS occurs preferentially between the glass (layer 1) and solar cell (layer 2) due to an accumulation of 2-D layered material ($CdCl_2$[1] and $MoSe_2$,[13] respectively), which creates a weak interface. While the theoretical framework developed here can be applied to thin-film delamination generally, we illustrate concepts using superstrate CdTe solar cells. Table 1 summarizes the composition and relevant material properties at ambient temperature for layers in this system. It should be noted that material property values for polyethylene-co-vinyl acetate (EVA) are approximate and greatly depend on the vinyl acetate content. In general, larger amounts of vinyl acetate reduce crystallinity and physical crosslinking, lowering the modulus (stiffness).[14] Because we work with particularly low vinyl acetate content here (< 10 wt%, compared to 28 to 33 wt% for typical encapsulation), we approximate the material properties [modulus, coefficient of thermal expansion (CTE)] of EVA in Table 1 as those for its

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low-density polyethylene (LDPE) resin precursor.[15] This gives a general view of EVA properties relative to the other layers at ambient temperature.

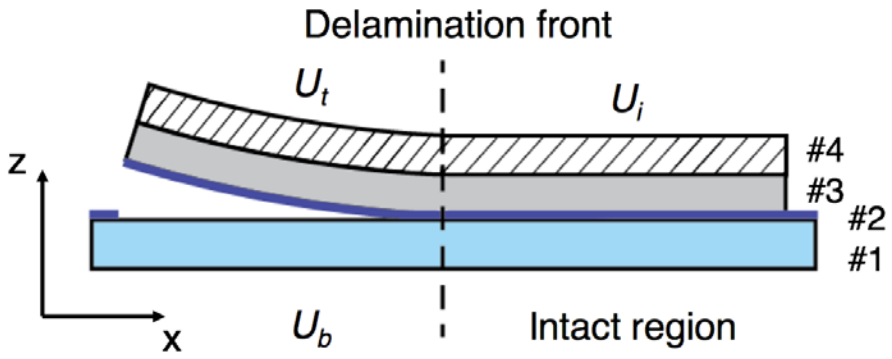

Figure 1. Illustration of delamination propagation using an energy-balance approach with four layers: 1) glass, 2) solar cell, 3) stressor, 4) handle. U_t, U_b, and U_i represent strain energy in the top sub-stack, bottom sub-stack, and intact region, respectively.

Layer Name [#]	Composition	Thickness (μm)	Modulus (GPa)	CTE (ppm C^{-1})
Glass [#1]	Glass (AF45, SLG)	700, 3000	66[16], 73[17]	4.5[16], 8.3[18]
	TCO	0.3	62.4 – 75.1[19]	3.76[20]
Solar Cell [#2]	CdS	0.1	70[21]	4.7[22]
	CdTe	4	52[21]	4.9[22]
	(Au)	0.1	78[23]	14.2[22]
Stressor [#3]	EVA	150	~0.15[15]	100 – 200[24]
Handle [#4]	PET	130	2.76 – 4.14[25]	65[22]
	Kynar® PVDF	30	1.7[26]	150[26]

Table 1. Summary of layers used in analysis: Layer 1, "Glass" is composed of the glass substrate (either Schott AF45 or soda-lime glass (SLG)) and a transparent conducting oxide (TCO), (SnO_2:F/SnO_2), layers. TCO is included in layer 1 rather than layer 2 because it is separated from the solar cell during delamination. Layer 2, "Solar Cell" is composed of the remaining layers in the superstrate CdTe device: CdS, CdTe, and in some cases Au, as discussed later. Layer 3, "Stressor" is polyethylene-co-vinyl acetate (EVA) with low vinyl acetate content (< 10 wt%) here. Material properties given are for its low-density polyethylene (LDPE) precursor. Layer 4, "Handle" is polyethylene terephthalate (PET) and a thin Kynar® polyvinylidene fluoride (PVDF) layer.

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Assuming that the lateral dimensions of the film are much greater than the thickness, the interior of the film (far away from the edges where there are no shear stresses or shear strains) is under equi-biaxial tension,[27] such that the stresses (σ) satisfy $\sigma_{xx} = \sigma_{yy},\ \sigma_{zz} = 0,$ and $\sigma_{ij} = 0$ for $i \neq j$, while the strains (ε) satisfy $\varepsilon_{ij} = 0$ for $i \neq j$, where σ_{ij} is the stress tensor and ε_{ij} is the strain tensor. Accordingly, we can describe delamination using the one-dimensional cross-section shown in Figure 1. Here, an energy-balance approach is employed in which the strain energy in the intact region ahead of the delamination front (U_i) is compared with the strain energy in the top- and bottom-substacks behind the delamination front (U_t and U_b, respectively):

$$G = (U_t + U_b) - U_i. \quad (1)$$

Here, G is the strain energy release rate, measured in J m^{-2}. For delamination to occur at a given interface, the energy released during delamination must be larger than the interface fracture toughness, G_c. In other words, the delamination condition $G \geq G_c$ must be satisfied. To find an expression for G in our multilayered stack, we must first determine what U_t, U_b, and U_i are in Equation (1). To do this, we start with a generalized equation for strain energy per unit area, U^*:

$$U^* = h \int \sum_{i=1}^{3} \sum_{j=1}^{3} \sigma_{ij} d\varepsilon_{ij}, \quad (2)$$

where the stress tensor (σ_{ij}) and strain tensor (ε_{ij}) are summed over the x-, y-, and z-directions, and h is the thickness of a given film. Under the assumption of linear elasticity and for equi-biaxial strain, the in-plane strains ($\varepsilon_{xx} = \varepsilon_{yy}$) are equal and related to the in-plane stress as:

$$\varepsilon_{xx} = \varepsilon_{yy} = \frac{1}{E}(1 - \nu)\sigma_{xx} \text{ and } \nu = \frac{\varepsilon_{xx}}{\varepsilon_{zz}} \quad (3)$$

where ν is Poisson's ratio and E is Young's modulus. Thus, the stresses and strains are proportional to each other and the stress and strain in the plane of a given layer can be described by the scalars σ and ε, respectively. Using Eq. 1 for equi-biaxial strained linearly elastic films, and noting that

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$\sigma_{zz} = 0$ and that there are no shear strains, the strain energy per unit area (U*) within a given layer is

$$U^* = h \int \sum_{i=1}^{3} \sum_{j=1}^{3} \sigma_{ij} d\varepsilon_{ij} = h \sum_{i=1}^{3} \frac{\sigma_{ii}}{2} \frac{\varepsilon_{ii}}{2} = h \frac{E\varepsilon^2}{2(1-\nu)}, (4)$$

In our system, some materials are not linearly elastic at ambient temperature; however, this is an appropriate assumption to make at the low temperatures used for delamination (T ≤ -30˚C). In particular, while EVA is viscoelastic at ambient temperature, its loss modulus, which quantifies the magnitude of viscous behavior, virtually disappears below the glass transition temperature (T_g) starting around -15˚C.[28] During this transition, the elastic modulus increases by orders of magnitude,[29] which in turn causes the rate at which strain energy builds up in response to temperature changes to increase dramatically as well. Consequences of this effect on the lift-off process will be discussed later.

From Equation (4), we move from a single layer to a multilayered stack. In general, this can cause the expression for strain energy to become considerably more complicated as each layer is constrained by the others. This constraint generates additional stress and strain energy that causes U to change not only layer to layer, but within each layer as well.[30] However, this interaction only becomes important when the thin layers are detached from the thick glass substrate, which will otherwise dominate the applied strain with its CTE. For our simplified four-layer stack (Table 1),

$$U_i = \frac{1}{2} \sum_{k=1}^{4} \frac{h_k E_k {\varepsilon_k}^2}{(1-\upsilon_k)}, (5)$$

$$U_b = \frac{1}{2} \frac{h_1 E_1 {\varepsilon_1}^2}{(1-\upsilon_1)}, (6)$$

$$U_t = \frac{1}{2} \sum_{k=2}^{4} \frac{h_k E_k {\varepsilon_k}^2}{(1-\upsilon_k)}, (7)$$

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where the index k represents the different layers of the structure.

Plugging Equation (5) – (7) into Equation (1), we see how the properties of individual layers can be adjusted to influence delamination. Of particular interest, the stressor layer provides a convenient lever to improve lift-off by increasing h and/or E until $G \geq G_c$ is achieved. To illustrate briefly, it was found that EVA with low vinyl acetate content (< 10 wt%) consistently and cleanly delaminated CdTe device stacks because of its sufficiently high E (~0.15 GPa at ambient temperature)[31] while EVA with high vinyl acetate content (~30 wt%, E ~ 0.01 GPa at ambient temperature,[31] commonly used in PV encapsulation) failed to produce any lift-off. It should be noted that the above equations have been developed to identify key material and system properties that can be tuned to control delamination to inform experimental directions and intuition; numerical predictions for strain energy in individual systems are left to the interested reader.

Here, we focus on in-plane strain (ε) and study its effect on lift-off quality. In our system, ε has several components: (1) ε_o – intrinsic strain between the CdTe film and glass substrate in the as-fabricated device; (2) ε_{lam} – compressive thermal strain that arises due to the CTE difference between each layer (Table 1) when the stack is cooled after laminating the stressor/handle backsheet to the device from the elevated lamination temperature (T_{lam}) to ambient temperature T_{amb} (~20˚C); (3) ε_{delam} – analogous (large) compressive thermal strain resulting from the sudden and non-homogenous decrease in temperature from T_{amb} to the delamination temperature (T_{delam}) of the cold bath; (4) ε_m – final strain term which captures all mechanical contributions, such as curvature about the z-axis and elongation/compression along the x-axis (Figure 1). Total strain in a given layer k can therefore be expressed as:

$$\varepsilon_k = (\varepsilon_o)_k + (\varepsilon_{lam})_k + (\varepsilon_{delam})_k + (\varepsilon_m)_k. \quad (8)$$

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Among these four contributions, the intrinsic strain (ε_o) and mechanical strain (ε_m) are fixed by the materials and processes employed during initial device fabrication. In principle, these can be manipulated. For example, it is well-known in CdTe that more aggressive $CdCl_2$ treatments make devices more susceptible to delamination.[32] However, in general it is desirable to use fabrication conditions that maximize device performance and independently control the delamination process. This control enables the ability to delaminate different thin-film stacks, which may require greater amounts of energy to delaminate. For a given device architecture, the thickness and physical properties (h, E, υ, CTE) of the stressor layer (EVA here) can be easily manipulated to increase strain in the film. Controlling lamination and delamination conditions (e.g. T_{lam} and T_{delam}) is another straightforward way to increase thermal strain and improve lift-off. In this work, we examine the impact of device architecture, T_{lam}, and T_{delam} on the delamination process.

3. Results and Discussion

Figure 2 quantifies the quality, or yield, of lift-off (measured in % area delaminated) as a function of lamination temperature for three different device architectures. In Figure 2a, we see improved yield with increasing T_{lam}, with performance saturating for T_{lam} > 150 ºC and decreasing above $T_{lam} \approx 170$ ºC. We believe that this decrease in delamination yield is caused by phase transitions in the PET/Kynar® handle, specifically melting in the Kynar® layer where $T_{melt} = 168^{\circ}C$.[26] However, it should be noted that the cooling was not precisely controlled and different cooling rates could also significantly influence the mechanics.

We also found that delamination yield was strongly influenced by device architecture. In particular, devices with no Au back contact had consistently higher delamination yields than identically prepared samples with Au back contacts. This is because in the latter, the crack is forced

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to first propagate through the ductile Au layer (where propagation is slowed and energy is lost due to plastic deformation)[33] before it can reach the brittle CdTe layer (where there is little to no plastic deformation). Once in the CdTe layer, the crack can easily propagate through to the weakened CdS/TCO interface and cause delamination. However, while the ductile Au back contact can slow crack propagation, it does not necessitate poor delamination. In fact, the devices with the highest delamination yields measured here (green in Figure 2a) had the Au layer present. The difference between the worst (Figure 2b) and best series (represented in Figure 2d) was the substrate used – AF45 and SLG, respectively. This is likely because the SLG substrate has a larger CTE mismatch with CdTe (SLG = 8.6, CdTe = 4.9, AF45 = 4.5 ppm C^{-1}) (Table 1), which increases the intrinsic strain (ε_o) in the as-fabricated devices and aids in lift-off when the system is thermally shocked. Under these conditions, lift-off is essentially perfect with the exception of minor edge effects (Figure 2d).

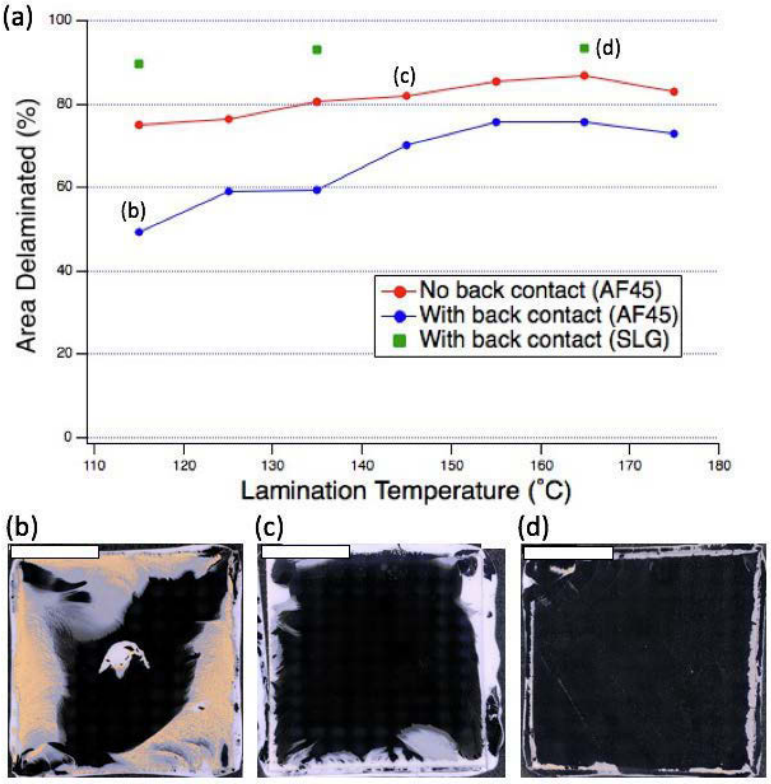

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Figure 2. (a) Plot of area delaminated as a function of T_{lam}. Delamination yield depends on the presence of a ductile (Au) back contact and the substrate used (AF45 vs. SLG) for T_{delam} = -196 ºC. (b) – (d) show representative images of delamination yield, with black representing clean lift-off. Scale bars are 5 mm.

Next, we varied T_{delam}, which was found to influence delamination *rate* rather than yield (Figure 3). By decreasing T_{delam}, we increase the quench depth relative to the glass transition temperature ($T - T_g$) of EVA. Below T_g, there is a dramatic increase in the elastic modulus of EVA (~100×),[29] which causes the rate at which strain energy builds up to increase much more quickly with changes in quench depth. Accordingly, the energy release rate (G), and thus growth rate of the delamination front, increases at a far higher rate after being cooled through the glass transition. At high T_{delam}, the modulus and quench depth are insufficient to build up adequate strain energy to initiate delamination, and we reach what is referred to here as the T_{delam} threshold, above which delamination will not occur.

For samples with no back contact (red in Figure 3), this value was determined by measuring the delamination rate at a series of T_{delam} (measured in 10˚C increments) and extrapolating to find the value at which delamination rate was zero. This was found to be T_{delam} = -28˚C (red dashed line in Figure 3), which was very close to the highest measured T_{delam} of -30˚C. It is interesting to note that at T_{delam} = -30˚C, a 1 cm^2 area delaminated in ~1.3 minutes, whereas at T_{delam} = -196˚C (liquid nitrogen), a 1 cm^2 area delaminated in only ~1.3 *seconds*. The T_{delam} threshold value for samples *with* back contacts was determined by testing high temperatures first, then decreasing T_{delam} until delamination was achieved, which was found to be T_{delam} = -46˚C (blue dashed line in Figure 3). This demonstrates that additional energy is required to initiate delamination in samples that have

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a ductile back contact, because of energy lost to plastic deformation in this layer, as discussed above.

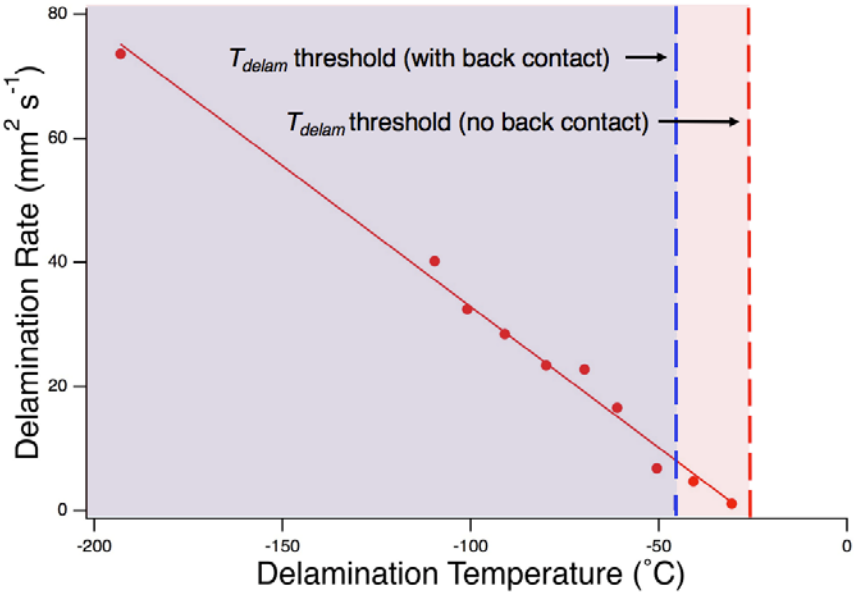

Figure 3. Plot of delamination rate as a function of T_{delam}. The highest possible T_{delam} to initiate delamination (T_{delam} threshold) is lower for samples with ductile back contact, implying that these require more energy to delaminate.

The ability to control delamination rate through T_{delam} can be extremely useful in process control. However, it should be noted that the delamination rates shown here are specific to the samples employed (device architecture, materials used) as well as the stressor/handle geometry. In particular, stress is concentrated at corners and edges; therefore, delamination preferentially initiates and propagates from these features. Handle shapes with sharp corners and high aspect ratios (i.e. rectangular strips) are therefore expected to delaminate more readily than those without stress concentrating geometries, such as circles. As demonstrated in the theoretical framework section above, the material properties of the stressor layer also play a crucial role in the lift-off

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process. Above, it was shown that the stressor layer must have a sufficiently high elastic modulus to induce delamination. However, if the modulus is too large (i.e. it is too stiff), there will not be adequate flexibility to allow for gradual propagation of the delamination front. For example, it was found that some epoxies, such as Hysol® 1C™ ($E \gtrsim 1$ GPa at ambient temperature),[34] produce clean delamination at very low T_{delam} (-196˚C), but at elevated temperatures ($T_{delam} \sim$ -80˚C), delamination only initiates at corners and does not propagate.

These types of considerations should be taken into account, particularly when attempting to lift off diverse polycrystalline thin-film stacks, as G_c (the energy required to delaminate) depends on many factors including device material, processing conditions, and device architecture. For example, processing conditions can lead to accumulations of 2-D materials at buried interfaces in some thin-film photovoltaic technologies, such as $CdCl_2$ in CdTe[1, 2] and $MoSe_2$ in CIGS.[13] This drastically reduces G_c, making the application of the lift-off technique presented here straightforward. For example, substrate CIGS device stacks can be cleanly delaminated in exactly the same manner as CdTe, with no further optimization to the technique or materials (Figure 4a-b). In fact, even large areas of CIGS (~3x3", this area being the largest attempted) have been cleanly lifted off using the same process (Figure 4c). However, it is unknown if similar 2-D material accumulations exist in all thin-film systems. Therefore, several suggestions are made to maximize the likelihood for successful lift-off: (1) use a growth substrate with relatively high CTE mismatch compared to the thin film, but not so high as to cause delamination during device growth; (2) delaminate in liquid nitrogen, which causes high thermal strain and is inert; (3) increase elastic modulus and/or CTE of stressor if unsuccessful.

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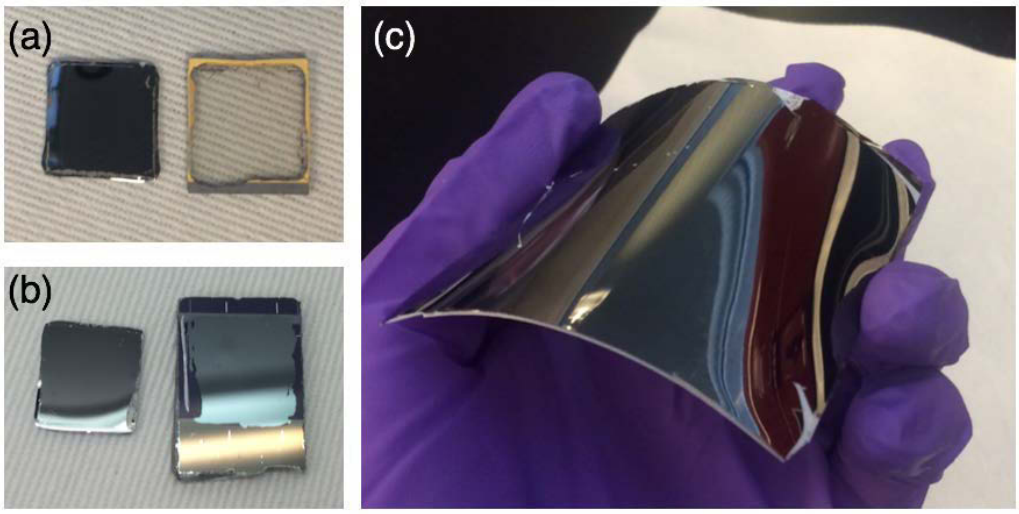

Figure 4. Images of delaminated (a) superstrate CdTe device with CdS/TCO interface exposed; (b) substrate CIGS device with CIGS/Mo interface exposed where delaminated areas are ~1.5x1.5 cm^2. (c) Large area (~3x3") delaminated CIGS on Kynar®/PET/EVA (KPE)[35] backsheet.

Finally, we compare device performance before and after lift-off measured under standard test conditions (1000 W m^{-2}, 25˚C, AM1.5G). Figure 5 compares the J-V behavior of the devices at various stages and the corresponding contacting geometries employed. Here, initial device efficiency was 14% (black curve in Figure 5a). Following lift-off, efficiency dropped to 10.7% (red curve in Figure 5a), due to a combination of a 100 mV decrease in open-circuit voltage (V_{oc}), a loss of 1.5 mA/cm^2 in short-circuit current density (J_{sc}), and a 5.2% drop in fill factor (FF). The decrease in J_{sc} observed here is a drastic improvement from our previous work in which J_{sc} dropped by almost 50% following lift-off due to device cracking.[36] Similar decreases in performance due to device cracking have also been identified in the early work (2010) of the Minemoto group.[37] In more recent work (2018), they have been able to largely eliminate this issue and achieve similar results of 10.2% lifted off CIGS.[5] In the current work, cracking was eliminated by using SLG substrates, which have a higher CTE mismatch with CdTe and allow for cleaner delamination, in conjunction with laser scribing prior to lift-off.[38]

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Comparison of quantum efficiency spectra (Figure 5e) show nominally identical behavior throughout the CdS/CdTe portion of the spectrum, reflecting the integrity of these layers after lift-off. As expected, there is a small loss of current below 400 nm, reflecting the lower band gap of ZnO/ZnO:Al relative to SnO_2:F/SnO_2. The decrease in *FF* can also be attributed to the new front contact, which is not well optimized. In particular, the sputtered ZnO/ZnO:Al layer has a sheet resistance of 59.5 Ω/square compared to 12.5 Ω/square for our original SnO_2:F/SnO_2, which is evidenced by the increased series resistance. Additionally, shadowing losses from contact probes during J-V measurements of post-delamination devices (substrate configuration) are not present in pre-delamination devices (superstrate configuration) (Figure 5b-c). By defining the device area with a metal (Ni) aperture (Figure 5d), both the shadowing and conduction limitations may be addressed, and we can fully recover our initial J_{sc} and nearly recover the original *FF* (green curve in Figure 5a). However, the Ni aperture also shades a substantial portion of the active cell and effectively creates a dark device in parallel with the illuminated device, drastically reducing V_{oc}. Thus, through optimization of the front contact and appropriate anti-reflection coating, it is expected that J_{sc} and *FF* can be restored to their original value and possibly even improved upon.

More complicated is the 100-mV loss in V_{oc} between pre- and post-delamination devices, which may reflect a loss in integrity of the $CdCl_2$ layer that appears important for passivation of this interface.[36] Alternatively, this loss may be the result of interface defects or the varied band offsets between the TCO and CdS before and after lift-off. Work is currently underway to further understand and address this issue. It should be noted though, that delamination provides unprecedented access and opportunity to modify and/or redesign the heterojunction and potentially boost voltage if the interface can be more effectively passivated.

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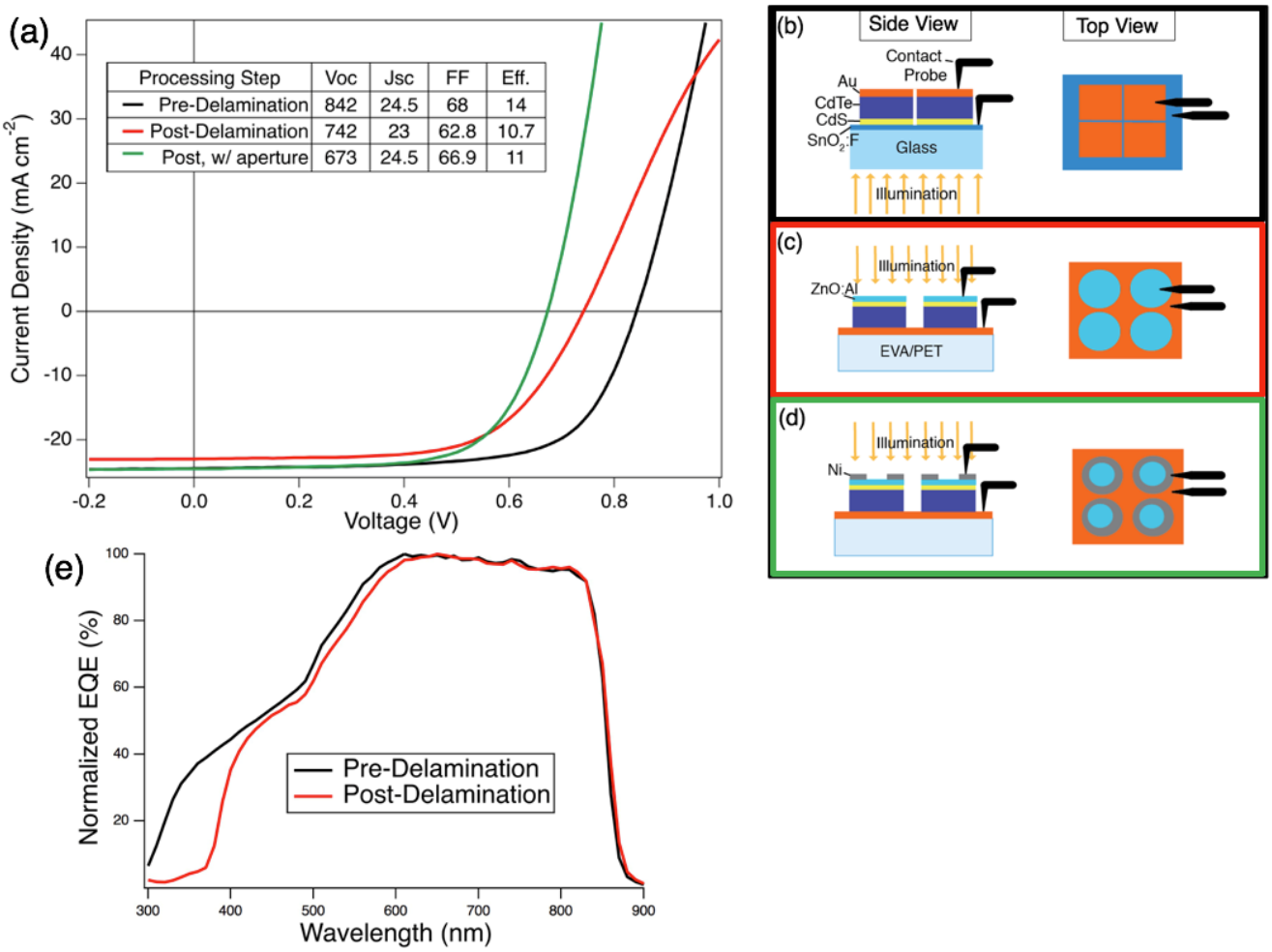

Figure 5. (a) J-V curves for a CdTe device before delamination (black curve), after delamination (red curve), and after delamination with Ni aperture (green curve). Illustrations of side and top view during J-V measurements for (b) superstrate pre-delamination device (black box), (c) substrate post-delamination device (red box), and (d) substrate post-delamination device with Ni aperture (green box). (e) Normalized external quantum efficiency (EQE) curves for pre- and post-delamination devices (black and red curve, respectively).

A major goal of this work is to increase the specific power (W kg^{-1}) of thin-film CdTe using commercially-manufacturable, high-efficiency cell technology. Specific power is directly proportional to the cell efficiency and inversely proportional to the device mass. We calculated a corrected post-delamination efficiency of 11.4% by correcting current density values in the post-

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delamination device (no aperture) to reflect the true J_{sc} of 24.5 mA cm^{-2} resulting from a measured device area of ~12 mm^2. The areal density of the post-delamination device was found to be 350 g m^{-2}. Our pre-delamination device on glass had 14% efficiency and an areal density of 7,830 g m^{-2}. Thus, we demonstrate the potential to maintain 80% of our efficiency while decreasing our areal density by over an order of magnitude, without significantly increasing cell production costs. This opens a new route for the possibility for low-cost PV with high specific power.[39] Furthermore, the resulting delaminated films are flexible, and the handle and stressor layers can be designed to fit the desired final application. The understanding developed here helps develop key parameters that should be considered while designing final lightweight packaging.

4. Conclusions

In this work, the thermo-mechanical lift-off of CdTe thin-films from glass growth substrates was explored both experimentally and theoretically. We developed simple equations to describe thermo-mechanical delamination of thin-film solar cells and found several tunable control parameters. We focused on controlling thermal strain through T_{lam} and T_{delam} and measured both delamination yield and rate as a function of these key parameters, respectively. However, there are many other parameters that can be tuned to achieve lift-off in diverse thin-film systems. Not only can strain be altered in numerous ways, but the stressor and handle material can be chosen to have higher CTE, elastic modulus, and/or thickness to improve delamination quality. Additionally, we found that better delamination can be achieved by modifying device architecture, such as removing the ductile back contact or choosing a substrate with a relatively high CTE mismatch compared with the thin-film device. Finally, we demonstrated an 11% efficient lifted-off device that retained

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~80% of its original efficiency while simultaneously reducing its areal density by over an order of magnitude.

Although not explored here, we note that this thermo-mechanical lift-off technique has the extremely important benefit of exposing previously buried regions of thin-film devices. In superstrate CdTe, delamination allows direct access to the heterojunction region, making it easily studied through standard surface analysis techniques.[1, 2, 40] Likewise, delamination of substrate CIGS films, which was also briefly demonstrated in this paper, allows for direct access to the previously buried CIGS/Mo interface. Therefore, the benefits of the lift-off technique developed in this paper are two-fold: (1) decouple final lightweight packaging from high-temperature growth requirements in order to enable high specific power PV at low costs,[39] and (2) enable fundamental studies of buried interfaces in a wide variety of thin-film device stacks.

5. Experimental Section

CdTe devices were grown in the superstrate configuration using either an alkali-free borosilicate glass (Schott AF45) or soda-lime glass (SLG). The glass was coated with a SnO_2:F/SnO_2 transparent conducting oxide (TCO) using chemical vapor deposition. 100 nm of cadmium sulfide (CdS) was deposited via radio frequency magnetron sputtering in an oxygen/argon ambient.[41] CdTe (~4 μm) was then deposited using close-spaced sublimation (CSS) in an oxygen/helium ambient with AF45 substrates held at 600°C and SLG substrates at 550˚C. Vapor-phase $CdCl_2$ annealing was also performed in a CSS configuration with the substrate temperature fixed at 415°C in an oxygen/helium ambient. Copper dopant was introduced either through evaporation (~3 nm)[42] or by soaking the device in a 0.1 mM $CuCl_2$ solution.[43] Finally, a gold contact was applied through

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evaporation and the device was activated by thermal annealing. The device architecture can be seen in the inset of Figure 6a.

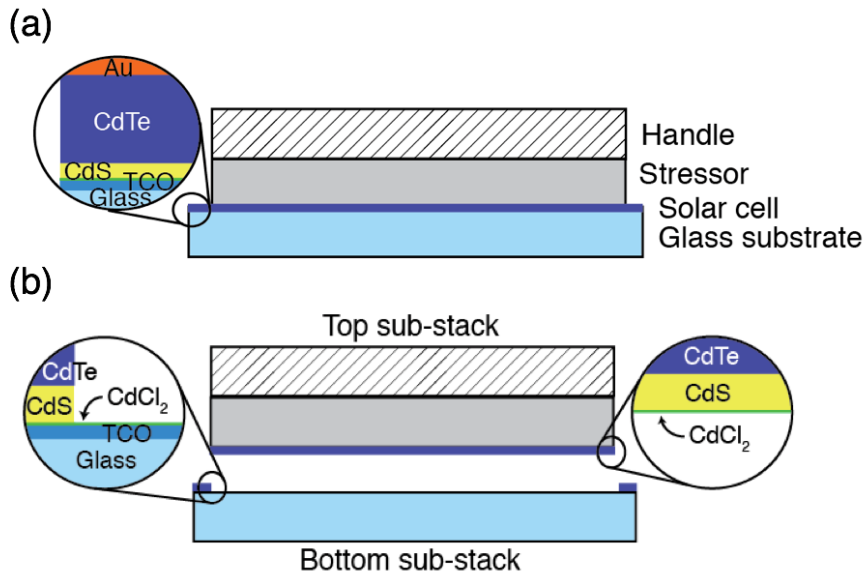

Figure 6. Schematic of stack (a) before delamination with stressor and handle applied to back of device (superstrate CdTe device architecture seen in inset), and (b) after delamination at the CdS/TCO interface, which is weakened by a monolayer accumulation of $CdCl_2$ (half monolayer shown on the bottom sub-stack in the right inset and top sub-stack in the left inset).

While this paper primarily focuses on delamination of CdTe solar cells, we briefly demonstrate the generality of the technique by delaminating CIGS device stacks in exactly the same manner, with no further optimization to the technique or materials. The CIGS devices delaminated here were grown in the substrate configuration on SLG. The glass was coated in ~0.8 µm of Mo via DC magnetron sputtering in an argon ambient. CIGS was co-evaporated using the three-stage process developed by Repins *et al.*[44] and CdS was then deposited using chemical bath deposition.[45] Next, RF sputtering was used to deposit zinc oxide in an oxygen/argon ambient, followed by aluminum-doped zinc oxide in an argon ambient. Devices were subsequently completed with e-beam deposited nickel/aluminum front contacts and photolithographic area definition. It should be noted

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that because the stressor and handle materials used here (described below) are opaque, further analysis using substrate CIGS devices was precluded from the current work.

The choice for a flexible packaging material is an analog to the polymeric backsheets employed commercially in silicon PV modules. These multilayer laminates include polyethylene-co-vinyl acetate (EVA) as an adhesive and insulating dielectric film(s) that protect the photovoltaic module from UV, liquid water, and weather. In our case, we used a "KPE" triple-layer backsheet consisting of Kynar® polyvinylidene fluoride (PVDF, ~30 μm),[46] polyethylene terephthalate (PET, ~130 μm), and low vinyl-acetate content EVA (~150 μm) with 9 μm of acrylate-based adhesive between each layer.[35] Here, we consider the "handle" as the combined Kynar®/PET bi-layer, and the "stressor" as the EVA layer. This backsheet was adhered to the back contact (Figure 6a) through vacuum lamination. During this process, the stack was pressed together with a constant pressure under vacuum for ~10 minutes, and simultaneously heated to a maximum lamination temperature, T_{lam}, which was varied from 115 to 175˚C. The stack was then removed and allowed to cool naturally to ambient temperature. Following lamination, a square perimeter was laser scribed into the CdTe film through the glass substrate using a Nd:YVO_4 laser. This step has been found to drastically reduce film cracking, which was identified as a major issue in previous work.[36] Next, the stack was submerged in a bath of temperature T_{delam}, ranging from -196˚C (liquid nitrogen) to -30˚C [ethyl alcohol (T_{freeze} = -114˚C) mixed with liquid nitrogen], to induce delamination.

By thermo-mechanically delaminating CdTe device stacks described above and using angle resolved x-ray photoelectron spectroscopy (ARXPS) to analyze the newly exposed CdS/TCO interface, Perkins *et al.* have found a half-monolayer accumulation of $CdCl_2$ on either side of the cleave[1] (Figure 6b). This accumulation of $CdCl_2$, which is a 2-D layered material bonded only through relatively weak van der Waals bonds, is thought to be critical to obtaining reproducible,

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clean delamination at the CdS/TCO interface. This layer is also thought to play an important role in maintaining open-circuit voltage in CdTe devices, as intentional removal of it (by rinsing with DI water) was observed to be detrimental to device performance.[36] Therefore, in order to preserve chemistry at the newly exposed CdS/TCO interface, most films (apart from those with varied T_{delam}) were lifted off in liquid nitrogen within a nitrogen-filled glovebox. Following lift-off, the top and bottom sub-stacks were withdrawn from the bath into a stream of dry nitrogen gas until room temperature was reached. Images of delaminated CdTe films were captured using a Keyence VHX5000 optical microscope and analyzed using ImageJ to quantify total delaminated area. Videos of delamination were also captured and analyzed frame by frame to determine delamination time, defined as the length of time between device immersion in the cold bath and completion of delamination (select videos included in Supplemental Information S1 and S2). Delamination times were then divided by the respective measured area to obtain delamination rates.

Because delamination occurs at the CdS/TCO interface, the front contact (TCO) is separated from the delaminated film and must be restored following lift-off. For this, a ZnO/ZnO:Al TCO bi-layer was sputtered, with no intentional heating, onto the delaminated film. A selective etch was then performed to expose the back contact by using circles of Shipley S1818® photoresist (diameter ~ 4 mm) as an etch mask and ferric chloride as the etchant. On a separate device, a thin (~50 nm) nickel aperture was evaporated on top of the ZnO/ZnO:Al bi-layer to define device area for more accurate current density measurements, before the back contact was subsequently exposed using the above method.

Supporting Information

Video S1. Video of delamination with bath temperature T_{delam} = -40˚C (.mp4)

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Video S2. Video of delamination with bath temperature T_{delam} = -80˚C (.mp4)

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REFERENCES

[1] Perkins, C. L.; Beall C.; Reese, M. O.; Barnes, T. M. Two Dimensional Cadmium Chloride Nanosheets in Cadmium Telluride Solar Cells, *ACS Appl. Mater. Interfaces* **2017**, 9, 20561-20565.

[2] Pookpanratana, S.; Khan, F.; Zhang, Y.; Heske, C. Chemical Structure of Buried Interfaces in CdTe Thin Film Solar Cells, in *2010 35th IEEE Photovoltaic Specialists Conference (PVSC)*, Honolulu, HI **2010**, 000024-000027.

[3] Antunez, P. D.; Bishop, D. M.; Luo, Y.; Haight, R. Efficient Kesterite Solar Cells with High Open-Circuit Voltage for Applications in Powering Distributed Devices, *Nat. Energy* **2017**, 2, 884-890.

Pursuant to the DOE Public Access Plan, this document represents the authors' peer-reviewed, accepted manuscript. The published version of the article is available from the relevant publisher.

[4] Chantana, J.; Arai, H.; Minemoto, T. Trap-Assisted Recombination for Ohmic-Like Contact at p-type Cu(In,Ga)Se2/back n-type TCO Interface in Superstrate-Type Solar Cell, *J. Appl. Phys.* **2016**, 20, 045302.

[5] Chantana, J.; Hirai, S.; Inoue, M.; Masuda, T.; Minemoto, T. Flexible Cu(In,Ga)Se2 Solar Cell with Superstrate-Type Configuration Fabricated by a Lift-Off Process, *Thin Solid Films* **2018**, 662, 110-115.

[6] Berg, M.; Kephart, J. M.; Munshi, A.; Sampath, W. S.; Ohta, T.; Chan, C. Local Electronic Structure Changes in Polycrystalline CdTe with CdCl2 Treatment and Air Exposure, *ACS Appl. Mater. Interfaces* **2018**, 10, 9817-9822.

[7] Su, Y.; Xin, C.; Feng, Y.; Lin, Q.; Wang, X.; Liang, J.; Zheng, J.; Lin, Y.; Pan, F. Band Alignment Rectification and Tunneling Effects in Al2O3 Atomic-Layer-Deposited on Back Contact for CdTe Solar Cell, *ACS Appl. Mater. Interfaces* **2016**, 8, 28143-28148.

[8] Konagai, M.; Sugimoto, M.; Takahashi, K.High Efficiency GaAs Thin Film Solar Cells by Peeled Film Technology, *J. Cryst. Growth* **1978**, 45, 277-280.

[9] Bedell, S. W.; Shahrjerdi, D.; Hekmatshoar, B.; Fogel, K.; Lauro, P. A.; Ott, J. A.; Sosa, N.; Sadana, D. Kerf-less Removal of Si, Ge, III-V Layers by Controlled Spalling to Enable Low-Cost PV Technologies, *IEEE J. Photovolt.* **2012**, 2, 141-147.

[10] Tiwari, A. N.; Romeo, A.; Baetzner, D.; Zogg, H. Flexible CdTe Solar Cells on Polymer Films, *Prog. Photovolt: Res. Appl.* **2001**, 9, 211-215.

[11] Tiwari, A. N.; Krejci, M.; Haug, F. –J.; Zogg, H. 12 8% Efficiency Cu(In,Ga)Se2 Solar Cell on a Flexible Polymer Sheet, *Prog. Photovolt: Res. Appl.* **1999**, 7, 393-397.

Pursuant to the DOE Public Access Plan, this document represents the authors' peer-reviewed, accepted manuscript. The published version of the article is available from the relevant publisher.

[12] Anegawa, T.; Oda, Y.; Minemoto, T.; Takakura, H. Comparison of Lift-Off Processes and Rear-Surface Characterization of Cu(In,Ga)Se2 Thin Films for Solar Cells, *J. Cryst. Growth* **2009**, 311, 742-745.

[13] Wada, T.; Kohara, N.; Negami, T.; Nishitani, M. Chemical and Structural Characterization of Cu(In,Ga)Se_2/Mo Interface in Cu(In,Ga)Se_2 Solar Cells, *Jpn. J. Appl. Phys.* **1996**, 35, L1253-L1256.

[14] Henderson, A. M. Ethylene-Vinyl Acetate (EVA) Copolymers: A General Review, in *IEEE Electr. Insul. Magazine.*, Vol. 9, Jan.-Feb., **1993**.

[15] DuPont, DuPont Elvax EVA resins Grade Selection guide, http://www.dupont.com//content/dam/dupont/products-and-services/packaging-materials-and-solutions/packaging-materials-and-solutions-landing/documents/elvax_molding_compounding_extrusion.pdf, accessed: November, 2018.

[16] Abrisa Technologies, SCHOTTAF45 Alkali free thin glass technical reference document, http://abrisatechnologies.com/specs/SCHOTT%20AF45%20Spec%20Sheet%20072102.pdf, accessed: November, 2018.

[17] Rouxel, T.; Sanglebúuf, J.-C. The Brittle to Ductile Transition of Soda-Lime-Silica Glass, *J. Non-Cryst. Solids* **2000**, 271, 224-235.

[18] NSG group, Properties of soda-lime silica float glass technical bulletin, https://www.pilkington.com/resources/ats129propertiesofglass20130114.pdf, accessed: November, 2018.

Pursuant to the DOE Public Access Plan, this document represents the authors' peer-reviewed, accepted manuscript. The published version of the article is available from the relevant publisher.

[19] Fang, T.-H.; Chang, W.-J. Nanomechanical Characteristics of SnO_2:F Thin Films Deposited by Chemical Vapor Deposition, *Appl. Surf. Sci.* **2005**, 252, 1863-1869.

[20] Quirk, J.; Harman, C. G. Properties of a Tin Oxide-Base Ceramic Body, in *Proceedings of* the *55th Annual Meeting, The American Ceramic Society*, Vol. 37, New York, N.Y. **1954**, 24-26.

[21] Deligoz, E.; Colakoglu, K.; Ciftci, Y. Elastic, Electronic, and Lattice Dynamical Properties of CdS, CdSe, and CdTe*, Phys. B* **2006**, 373, 124-130.

[22] Rumble, J. R.; Lide, D. R.; Bruno, T. J. *CRC Handbook of Chemistry and Physics : A Ready-Reference Book of Chemical and Physical Data*, CRC Press, Boca Raton, FL, USA **2017**, Ch. 12-13.

[23] Callister, W. D. *Materials Science and Engineering* 3rd edn, Wiley, New York, NY, USA **1994**, Ch. 6-8.

[24] Mark, J. E. *Physical Properties of Polymers Handbook*, Springer, New York, NY, USA **2006**.

[25] Harper, C. A. *Modern Plastics Handbook*, McGraw-Hill, New York, NY, USA **2000**.

[26] Professional Plastics, Kynar® 740 PVDF Material Data Sheet, https://www.professionalplastics.com/professionalplastics/Kynar740DataSheet.pdf, accessed: November, 2018.

[27] Yu, H.-H.; Hutchinson, J. W. Delamination of Thin Film Strips*, Thin Solid Films* **2003**, 423, 54-63.

Pursuant to the DOE Public Access Plan, this document represents the authors' peer-reviewed, accepted manuscript. The published version of the article is available from the relevant publisher.

[28] TA Instruments, Characterization of ethylene vinyl acetate copolymers by dielectric analysis, http://www.tainstruments.com/pdf/literature/TA107.pdf, accessed: November, 2018.

[29] Khonakdar, H. A.; Wagenknecht, U.; Jafari, S. H.; Hässler, R.; Eslami, H. Dynamic Mechanical Properties and Morphology of Polyethylene/Ethylene Vinyl Acetate Copolymer Blends, *Adv. Polym. Technol.* **2004**, 23, 307-315.

[30] Begley, M. R.; Hutchinson, J. W. *The Mechanics and Reliability of Films, Multilayers and Coatings*, Cambridge University Press, Cambridge **2017**, Ch. 5.

[31] DuPont, DuPont Elvax EVA resins thermal and mechanical properties comparison,

http://www.dupont.com//content/dam/dupont/products-and-services/packaging-materials-and-solutions/packaging-materials-and-solutions-landing/documents/elvax_adhesives_wax_blends.pdf, accessed: November, 2018.

[32] Burst, J. M.; Rance, W. L.; Barnes, T. M.; Reese, M. O.; Li, J. V.; Kuciauskas, D.; Steiner, M. A.; Gessert, T. A.; Zhang, K.; Hamilton, C. T.; Fuller, K. M.; Aitken, B. G.; Kosik Williams, C. A. The Effect of CdTe Growth Temperature and ZnTe:Cu Contacting Conditions on CdTe Device Performance, in *2012 38th IEEE Photovoltaic Specialists Conference (PVSC)*, Austin, TX **2012**, 000188-000191.

[33] Ritchie, R. O. Mechanisms of Fatigue-Crack Propagation in Ductile and Brittle Solids, *Int. J. Fract*. **1999**, 100, 55-83.

[34] Cease, H.; Derwent, P. F.; Diehl, H. T.; Fast, J.; Finley, D. Measurement of Mechanical Properties of Three Epoxy Adhesives at Cryogenic Temperatures for CCD Construction, Fermi National Accelerator Laboratory, Batavia, IL **2006**.

Pursuant to the DOE Public Access Plan, this document represents the authors' peer-reviewed, accepted manuscript. The published version of the article is available from the relevant publisher.

[35] FLEXcon, FLEXcon multiGUARD® KPE backsheet series, https://cdn.enfsolar.com/Product/pdf/Backsheet/5214745fa2ae8.pdf, accessed: November, 2018.

[36] Clayton-Warwick, D.; Kempe, M. D.; Dabney, M. S.; Barnes, T. M.; Wolden, C. A.; Reese, M. O. Decoupling Thin Film CdTe Growth from Packaging: Toward Record Specific Power in Low Cost Polycrystalline PV, in *2017 44th IEEE Photovoltaic Specialists Conference (PVSC)*, Washington D. C., USA, June, **2017**.

[37] Minemoto, T.; Abe, Y.; Anegawa, T.; Osada, S.; Takakura, H. Lift-off Process for Flexible Cu(In,Ga)Se_2 Solar Cells, *Jpn. J. Appl. Phys.* **2010**, 49, 04DP06.

[38] McGott, D. L.; Wolden, C. A.; Reese, M. O.; Mitigation of Crack Formation During Thermo-Mechanical Delamination of CdTe Solar Cells, in *2018 7th IEEE World Conference on Photovoltaic energy Conversion (WCPEC)*, Waikoloa, HI, USA, June, **2018**.

[39] Reese, M. O.; Glynn, S.; Kempe, M. D.; McGott, D. L.; Dabney, M. S.; Barnes, T. M.; Booth, S.; Feldman, D.; Haegel, N. M. Increasing Markets and Decreasing Package Weight for High-Specific-Power Photovoltaics, *Nat. Energy* **2018**, 3, 1002-1012.

[40] Meysing, D. M.; Reese, M. O.; Mahabaduge, H. P.; Metzger, W. K.; Burst, J. M.; Duenow, J. N.; Barnes, T. M.; Wolden, C. A. Chemical and Mechanical Techniques Enabling Diret Characterization of the CdS/CdTe Heterojunction Region in Completed Devices, in *2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC)*, New Orleans, LA **2015**.

[41] Meysing, D. M.; Wolden, C. A.; Griffith, M. M.; Mahabaduge, H.; Pankow, J.; Reese, M. O.; Burst, J. M.; Rance, W. L.; Barnes, T. M. Properties of Reactively Sputtered Oxygenated

Pursuant to the DOE Public Access Plan, this document represents the authors' peer-reviewed, accepted manuscript. The published version of the article is available from the relevant publisher.

Cadmium Sulfide (CdS:O) and their Impact on CdTe Solar Cell Performance, *J. Vac. Sci. Technol., A* **2015**, 33, 021203.

[42] Duenow, J. N.; Dhere, R. G.; Li, J. V.; Young, M. R.; Gessert, T. A. Effects of Back-Contacting Method and Temperature on CdTe/CdS Solar Cells, in *2010 35th IEEE Photovoltaic Specialists Conference (PVSC)*, Honolulu, HI **2010**, 001001.

[43] Mao, D.; Blatz, G.; Wickersham, C. E.; Gloeckler, M.; Correlative Impurity Distribution in Cadmium Telluride (CdTe) Thin-Film Solar Cells by ToF-SIMS 2D Imaging, *Sol. Energy Mater. Sol. Cells* **2016**, 157, 65-73.

[44] Repins, I.; Contreras, M. A.; Egaas, B.; DeHart, C.; Scharf, J.; Perkins, C. L.; To, B.; Noufi, R. 19.9%-Efficient ZnO/CdS/CuInGaSe$_2$ Solar Cell with 81.2% Fill Factor, *Prog. Photovolt.: Res. Appl.* **2008**, 16, 235-239.

[45] Contreras, M. A.; Romero, M. J.; To, B.; Hasoon, F.; Noufi, R.; Ward, S.; Ramanathan, K. Optimization of CBD CdS Process in High-Efficiency Cu(In,Ga)Se$_2$-Based Solar Cells, *Thin Solid Films* **2002**, 403 - 404, 204-211.

[46] Arkema, Kynar® resin physical and mechnical properties, https://www.extrememateials-arkema.com/en/product-families/kynar-pvdf-family/physical-and-mechanical-properties/, accessed: November, 2018.

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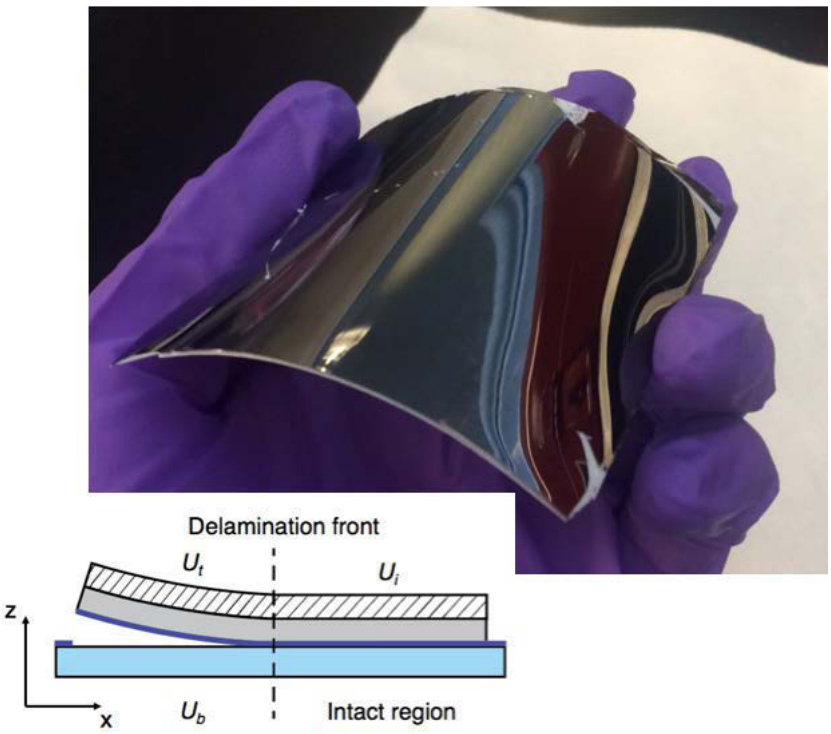

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