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Fixed Switching Frequency Predictive Control of an Asymmetric Source Dual Inverter System with a Floating Bridge for Multilevel Operation

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Abstract: This paper proposes a modified Modulated Model Predictive Control (MMPC) scheme to control an open-end winding induction motor drive using an asymmetric source dual inverter with one floating bridge. The control algorithm uses a modulation algorithm within the cost function optimization scheme to avoid variable switching frequency. The voltage of floating capacitor is regulated utilizing predefined redundant switching sequences as well as the voltage vector location is identified to improve calculation time. The proposed MMPC scheme enhances the output performance with comparison to model predictive control scheme. Experimental results are presented to verify theory and simulation results.

1. Introduction

Finite Set Model Predictive Control (FS-MPC) has been gained increasing attention for power converter applications [1, 2]. This control algorithm possesses merits over conventional control algorithms such as the ability to include constrains and nonlinearities, control multiple variables in a single loop and fast dynamic response [3]. Compared to a standard Space Vector Modulation (SVM) method, the need of dwell time calculations, sector and region determination or a switching sequence design can be ignored if the FS-MPC is adopted [4]. To accomplish a proper control by FS-MPC algorithm, a rigorous modelling of the load and the converter is essential. The working principle of FS-MPC algorithm is initially assigning all applicable converter switching states to load model such that all possible future system behaviours can be predicted. This is followed by an error calculation block, which is used to derive the error between the reference and the predicted future system behaviours. The minimum error value can be determined and that corresponding switching states can be selected for the next sampling period.

In the literature, the FS-MPC has widely applied for power converter topologies, such as two-level inverters [1], single-phase and three-phase multilevel converters and dual converters [4-6]. Apart from that, the control of matrix converter and active front end rectifiers can be successfully achieved by the FS-MPC [7, 8]. Furthermore, the FS-MPC has also been applied as fast current controller as well as torque and flux controller [9, 10]. In spite of all these advantages the predictive control has not been widely accepted for power electronics application due to the controller's switching nature. The controller applies only one switching state during a complete sample period can result in considerabely large harmonic distortions in the converter output. Additionally, the controller may choose the identical switching sequence for consecutive sample intervals thus the overall variable switching frequency can be expected.

To overcome the large output ripples and variable switching frequency, various methods have been addressed. For instance, the switching sequences have been rearranged to manipulate the pulse patterns [9]. The inclusion of modulation techniques and extending the prediction horizon to enhance converter output quality [11, 12]. In particular, an SVM method is integrated with the FS-MPC current controller for a dual three-phase converter [13]. For this approach, the dwell times of switching states are derived from solving an optimization problem. Nevertheless, multi-objective control will be significantly complex since it demands a solution for a multi-dimensional optimization problem. In order to cope with these constrains, a novel predictive control scheme is proposed in [12] where an appropriate modulation technique is utilized at the end of prediction.

The addressed MMPC control scheme has been modified and validated using the dual inverter system with a floating bridge, which is depicted in Fig.1(a). The traditional dual inverter topology employs two isolated DC power supplies thus the zero-sequence current circulation can be eliminated. The proposed topology utilizes only one DC source such that the volume and weight of the overall system can be reduced. In [14], authors present a single source dual inverter system where the common mode voltage is avoided by selecting the switching sequences for dual converter with identical common mode voltage. The challenges for this modulation are achieving sufficient voltage utilisation and multilevel voltage output.

In this paper, a fixed switching frequency predictive control method is used for the first time to control an asymmetric source dual inverter system to achieve multilevel voltage as well as to regulate the floating capacitor charge. Appropriate switching states are allocated into sequence to maintain the charge of the floating capacitor. Identification of the charging and discharging states along with charging limitations will help to reduce DSP calculation time by limiting the switching states. The challenges in the implementation of the proposed control method are analysed. The performance of the controller is compared with the traditional FS-MPC controller and verified with experimental results.

2. Proposed inverter system

In this paper, an asymmetric source dual inverter with a floating bridge is analyzed. This topology can save the requirements for isolated DC power sources. The floating capacitor is charged by applying suitable switching combinations. A diagram of the converter is shown in Fig. 1(a). The converter uses asymmetric DC-link voltage with a ratio of 2:1. This ratio is chosen in order to generate 9 phase voltage levels between the load [15, 16]. Compared with the proposed topology, when symmetric DC sources were applied, then the levels of phase voltages will decrease into 5 along with reduced voltage utilization of DC-link. Regarding the dual inverter topology, each one provides a voltage that is 180 degrees out of phase from the other. According to the structure of the inverters, the voltages generated by the dual inverters sum up between the load terminal. This phase shift is critical to accomplishing complete voltage utilization in comparison with a single-sided inverter. Otherwise, any difference in that specific phase shift will shrink the voltage utilization. The space vector diagram for the analyzed converter is demonstrated in Fig. 1(b). The diagram in Fig. 1(b) denotes the three-phase voltage using a single vector and obtained by assuming ideal asymmetric source dual inverter system. To regulate the voltage of floating bridge capacitor, the available switching states of the asymmetric source dual inverter are studied. The charge of the floating capacitor can be maintained by routing the floating DC link current across the capacitor. A switching state that makes the floating DC link current flow from the positive to the negative side of the capacitor will act to charge the floating capacitor otherwise the capacitor will be discharged. In the state diagram, all the charging and discharging states are marked as green and red. The numbers in the state diagram shown in Fig. 1(b) are the state of the top switches for each leg, where the numbers can be disintegrated into 1(1 0 0), 2(1 1 0), 3(0 1 0), 4(0 1 1), 5 (0 0 1), 6(1 0 1), 7(1 1 1) and 8(0 0 0). According to the state diagram shown in Fig. 1(b) the first number represent the switching state of the main converter and the second number represents the floating converter state, where 1 represents turn-on of the device and 0 represent turn off.

An instance of charging and discharging states are shown in Fig. 1(c), it can be seen from the figure that combination (11) make phase A current i_a flow into the positive terminal of the floating capacitor, while current i_a would act on the negative terminal of the floating capacitor if applies combination is (74). This implies that the sign of current i_a will determine either charging or discharging floating capacitor. Fig.1 (d) displays the angle of phase A voltage and current when reference vector locates at Sector I. The dark green circular sector in Fig.1 (d) represents the angle of phase voltage is at the division of $[0°, 60°]$. The light green circular sector indicates the angle of phase current, which is delayed by load power factor angle $\Delta\theta$. If the power factor angle within $-90°, 0°$ (motor drive application) then i_a would be always positive regardless of power factor variation. Therefore, combination (11) would charge the floating capacitor while (74) would discharge the floating capacitor. To achieve better results with more variation in power factor angle the floating DC link current is calculated for all redundant vectors associated with the reference voltage and an average DC link current is calculated. If the average current is positive then it will charge otherwise discharge the floating capacitor. The selection of applied redundant switching state will depend on the current state of the capacitor voltage.

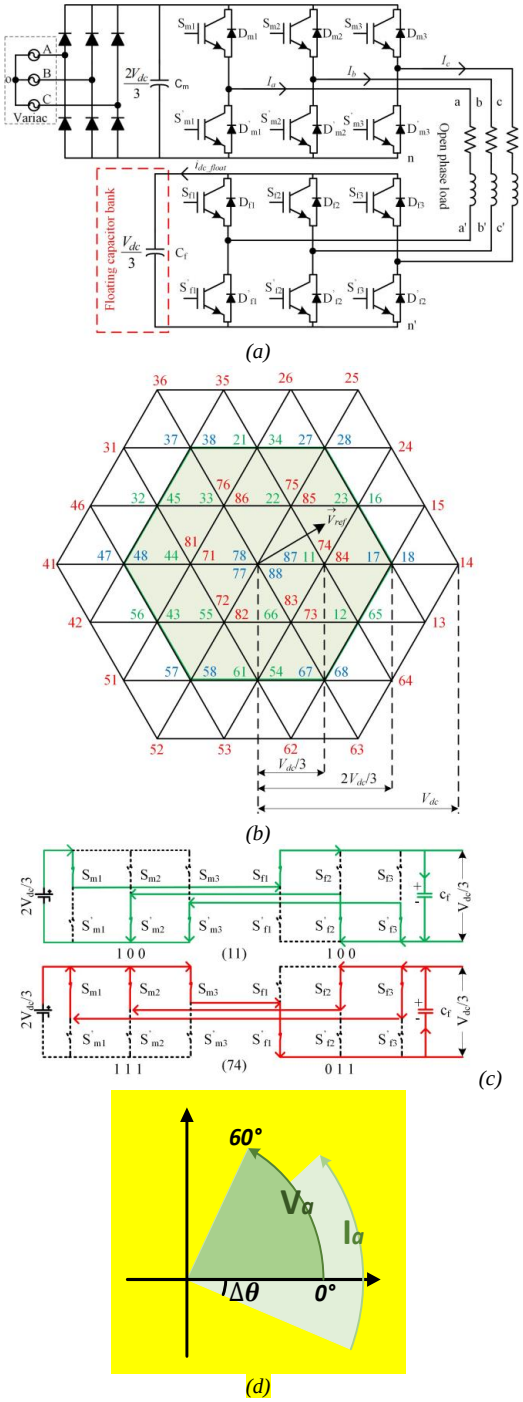
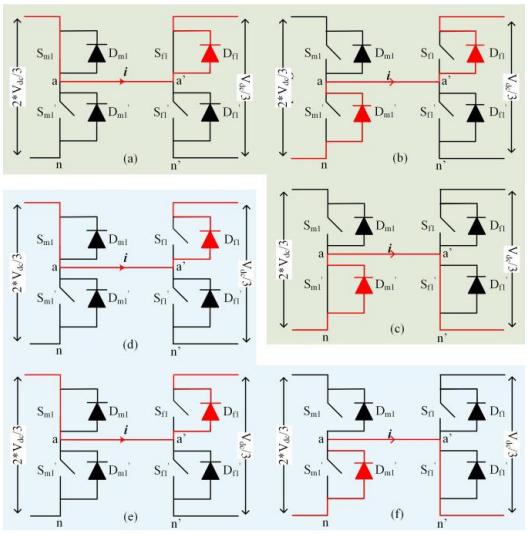
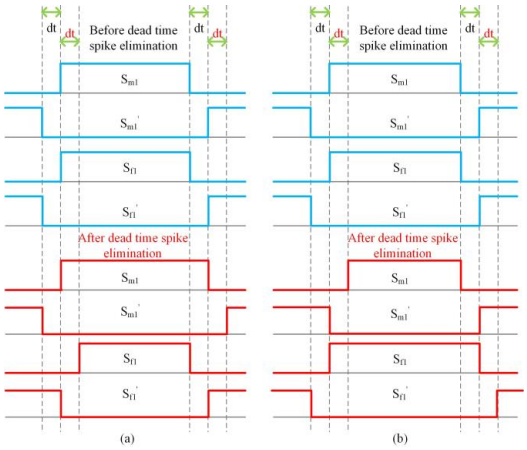


Fig. 1. *(a) Schematic of the proposed floating bridge topology (b) Space vector diagram of the asymmetric source dual inverter (voltage ratio 2:1) (c) Charging and discharging states circuit diagram (d) load angle at sector I.*



(a)



(b)

Fig. 2. *($a_{a\text{-}c}$) Effect of dead time interval, ($a_{d\text{-}f}$) three-step commutation to avoid dead time voltage spike (b) modification of switching pulses (b_a) positive load current (b_b) negative load current.*

The outer portion of the hexagon has only two charging states in each sector thus maintaining capacitor charge under all operating condition is not possible. A restriction on modulation index must be imposed to maintain floating capacitor charge, thus a reduction in the number of voltage level can be seen. The proposed inverter can mimic a three level converter waveform as long as the reference voltage locates within green hexagon [Fig. 1(b)]. This charging constrain is not depended on the loads since there are adequate redundant switching states to charge and discharge. This indicates that floating capacitor voltage can be fully regulated within this green hexagon regardless of load conditions.

The other challenge of dual inverter with asymmetric source is the unwanted voltage level during the dead-time interval. The dead-time indicates to the turn-on delay time between the top and bottom switches of a converter leg such that the short circuit of DC supply can be avoided. During dead-time period, the converter output voltage is determined according to the direction of load current. In an ideal scenario, the dead-time voltage state clamps to the voltage levels before or after the dead-time period. The asymmetric sources dual inverter exhibits distinct features over conventional inverters. During the dead-time period, the output voltage clamps to a different voltage level thus voltage spikes can be seen. Consequently, these voltage spikes during the dead-time period may not only introduce harmonic distortion in the output phase voltage but also to the load current. In order to avoid the dead-time spike for the dual inverter, one approach is to not select the switching state that clamps the phase voltage to an undesired voltage level during the dead-time period. However, this method could be applied to all the switching sequences for the proposed topology. Another approach is to postpone the dead-time period in both converters separately to ensure both the converter phase legs would not enter the dead-time period at the same instant.

To illustrate how long delay is required between the dual converter and which one of dual converter pulses will be delayed, the simplified converter diagrams in Fig. 2(a) are analysed. In the figure when the converter switching state is (11) and the current direction is positive. Under this case, diode (Df1) and switch (Sm1) are conducting. It can be observed that the current will still flow through the same devices if the converter with a floating bridge enters its dead-time first. Once the floating converter has recovered from its dead-time period, the present conducting devices will switch to diode (Dm1') and switch (Sf1'). The main converter will enter its dead-time. Hence, the phase voltage during the dead-time period will generate the identical voltage level as before the dead time period. The modification of the switching pulses is shown in Fig. 2(b).

The identification of the current direction needs to be fast to avoid unwanted voltage spikes during zero crossing. To achieve fast identification two anti-parallel SiC schottky diodes are used and the voltage drop between the diodes are compared by a comparator.

3. Control algorithms

The primary aim of this paper is to propose a modified MMPC algorithm for the dual inverter topology with one floating bridge. The performance of this modified MMPC algorithm will then compared to the performance of FS-MPC and traditional MMPC algorithm including performance, waveform quality and DSP calculation time.

3.1. Predictive control

Model predictive controller is used to predicts the capacitor voltage and load current for all switching state available for this converter. After that, the predicted value is compared to the reference value to determine error magnitude. The controller then selects the minimum error producing switching state and then applies that state to the converter. An implementation of the predictive control method on an R-L load is illustrated in Fig. 3(a).

The dual converter topology can generate 64 switching states in total, which can be witnessed in the space vector

diagram shown in Fig. 1(b). For charging the capacitor and achieving a three-level output voltage, only 24 states will be chosen. All the vectors on the outermost of hexagon and undesired states are neglected. To achieve desired control, an accurate model of converter and load is required. However, it has also been demonstrated that despite some variations in the parameters, the predictive controller will always choose the state to provide better tracking to the reference. It is worthy to mention that inaccurate model will cause larger ripple in the output waveform [17, 18]. The converter and load models are implemented in α-β reference frame. Therefore, the output voltage of the inverters can be expressed a function of switching states and the DC link voltage.

$$V_{\alpha_main} = S_{\alpha_m} V_{dc_main} \tag{1}$$

$$V_{\beta_main} = S_{\beta_m} V_{dc_main} \tag{2}$$

$$V_{\alpha_float} = S_{\alpha_f} V_{dc_float} \tag{3}$$

$$V_{\beta_float} = S_{\beta_f} V_{dc_float} \tag{4}$$

$$V_{\alpha} = V_{\alpha_main} - V_{\alpha_float} \tag{5}$$

$$V_{\beta} = V_{\beta_main} - V_{\beta_float} \tag{6}$$

Subscript α and β represent the two-phase stationary coordinate after applying Clarke's transformation. The main inverter and floating inverter are marked by the subscript 'main' and 'float', respectively. The modelling of the static *R-L* load in α-β reference frame is shown in (7).

$$V_{\alpha\beta} = Ri_{\alpha\beta} + L\frac{di_{\alpha\beta}}{dt} \tag{7}$$

where R and L are the load resistance and inductance. Equation (7) is used to calculate the predicted current value by decomposing the derivative term:

$$\frac{di_{\alpha\beta}}{dt} = \frac{V_{\alpha\beta}}{L} - \frac{Ri_{\alpha\beta}}{L} \tag{8}$$

$$\frac{i_{\alpha\beta}^{k+1} - i_{\alpha\beta}^{k}}{Ts} = \frac{V_{\alpha\beta}^{k}}{L} - \frac{Ri_{\alpha\beta}^{k}}{L} \tag{9}$$

$$i_{\alpha\beta}^{k+1} = \left(1 - \frac{RTs}{L}\right) i_{\alpha\beta}^{k} + \frac{Ts}{L} V_{\alpha\beta}^{k} \tag{10}$$

where $i_{\alpha-\beta}^{k}$ and $V_{\alpha-\beta}^{k}$ are the load current and voltage at present sample interval. T_s is the sample period and ($k+1$) is predicted value. The current flow from DC link to the floating capacitor is also identified for each switching state, as shown in (11). The prediction for floating capacitor voltage can be derived by evaluating the current equations for the capacitor, as shown in (12) and (13).

$$i_{dc_float} = S_{\alpha_float} i_{\alpha} + S_{\beta_float} i_{\beta} \tag{11}$$

$$i_{dc_float} = C\frac{dV_{dc_float}}{dt} \tag{12}$$

$$V_{dc_float}^{k+1} = \frac{Ts * i_{dc_float}^{k}}{C} + V_{dc_float}^{k} \tag{13}$$

where i_{dc_float} is the current flow into the floating bridge, C is the capacitance, $V_{dc_float}^{k}$ and $V_{dc_float}^{k+1}$ are the present and predicted capacitor voltages accordingly. To compensate for controller and dead time delays the voltage and currents are simply predicted two samples ahead. The two sample ahead predicted values are calculated utilizing one sample ahead predicted values, as expressed in (14 - 15). The two sample ahead prediction of control variable will compensate for the delays in control platform as well as reduce the effect of top and bottom switches interlocking dead time.

$$i_{\alpha\beta}^{k+2} = \left(1 - \frac{RTs}{L}\right) i_{\alpha\beta}^{k+1} + \frac{Ts}{L} V_{\alpha\beta}^{k+1} \tag{14}$$

$$V_{dc_float}^{k+2} = \frac{Ts * i_{dc_float}^{k+1}}{C} + V_{dc_float}^{k+1} \tag{15}$$

where $k+2$ states the predicted value at two samples ahead. The floating capacitor voltage has slowed transient and at steady state the capacitor voltage does not vary considerably in one sample period thus, $V_{dc_float}^{k+1}$ is presumed to be the current DC link voltage.

The converter output current is predicted at two samples ahead, but the reference is at present instant in time. To estimate the future reference values a vector angle compensation method is applied, as displayed in (16).

$$i^{*k+2} = i^{*k} e^{2j\omega T_s} \tag{16}$$

where $k+2$ is predicted value at two sample ahead, ω is the angular frequency of the reference variables as well as k is the present reference value. The controller has to deal with two variables with different nature, one is the load currents and the other is floating capacitor voltage. To achieve proper system performance a proper control of floating capacitor voltage is necessary as well the load current controller, thus an additional term is added with the capacitor voltage cost function to scale the capacitor voltage error amplitude same as the current amplitude. Thus, the controller will give equal importance to the different control variables. The design of the weighting factor is described in (20).

$$g_i = \sqrt{\left(i_{\alpha}^{*k+2} - i_{\alpha}^{k+2}\right)^2 + \left(i_{\beta}^{*k+2} - i_{\beta}^{k+2}\right)^2} \tag{17}$$

$$g_{v_float} = \lambda\sqrt{\left(V_{dc_float}^{*} - V_{dc_float}^{k+2}\right)^2} \tag{18}$$

$$g = g_i + g_{v_float} \tag{19}$$

$$\lambda = \frac{\left|i^{*}\right|}{V_{dc_float}^{*}} \tag{20}$$

Where g is the total cost function and λ is the weighted factor to normalize the floating voltage error in contrast with the current errors. Using (1-20) a model predictive floating capacitor voltage and current control for three-phase open-ended *R-L* load using a dual inverter with a floating bridge can be implemented, as shown in Fig. 3(a). In the figure, predictive model block predicts the currents and floating DC link voltage using (14) and (15). The predicted values are then read by the cost function minimization block and then compared with the reference values as indicated in (17–19) and then select the optimum switching sequence to minimize error.

3.2. Modulated model predictive control

Modulated Model Predictive Control (MMPC) involves a modulation technique inside the cost function optimization algorithm to enhance the output performance of converters. This control scheme inherently takes all the merits of the FS-MPC scheme without increasing the control complexity for multi-objective control. The control process can be summarized as:

- The reference currents and voltages are identified, and the current values are measured.
- The floating capacitor voltage and the load current are estimated.
- The cost function is evaluated for each applicable switching state.
- The duty cycles related to the cost function outcomes are derived.
- An individual cost function for each individual region utilizing three switching states and their corresponding duty cycles are determined.
- A switching sequence for modulation is obtained.
- The switching sequences to result in a minimum error for the next sampling period are implemented.

The MMPC algorithm selects a set of optimal switching sequence to minimize error at each sample instance, thus cost function calculation is different than the FS-MPC algorithm. To achieve the cost function for the specific triangle or region a cumulative cost function is defined. Each small triangle (region) has three different switching combinations as shown in Fig. 1(b). The cost function for these three different states are first calculated using (21 – 23), then the relative duty cycle time is calculated for every three switching state combinations as expressed in (24 – 26). The cost functions are then multiplied with associated duty cycle time for each switching combination. The final cost function is the addition of all three values as shown in (27). A flowchart of the control algorithm is shown in Fig. 3(c).

There are two methods to achieve control over capacitor voltage, the former scheme is to involve capacitor voltage control within the cost function minimization algorithm following the same manner as for the FS-MPC. The second method is to introduce it as a bang-bang controller within the modulation scheme. This is achieved by defining different switching table at the beginning of the program with redundant switching states. A floating DC link voltage comparator is defined after the modulated model predictive control to select the appropriate triangle to minimize error. Depending on the outcome of the comparator a set of redundant voltage vectors are selected to minimize error. Therefore, the requirement for predicting capacitor voltage can be avoided and the calculation duration can be shortened. Reducing calculation duration for predictive control schemes is one of the difficulties due to the characteristic of the controller. Thus, in this paper the capacitor control has been introduced inside modulation scheme.

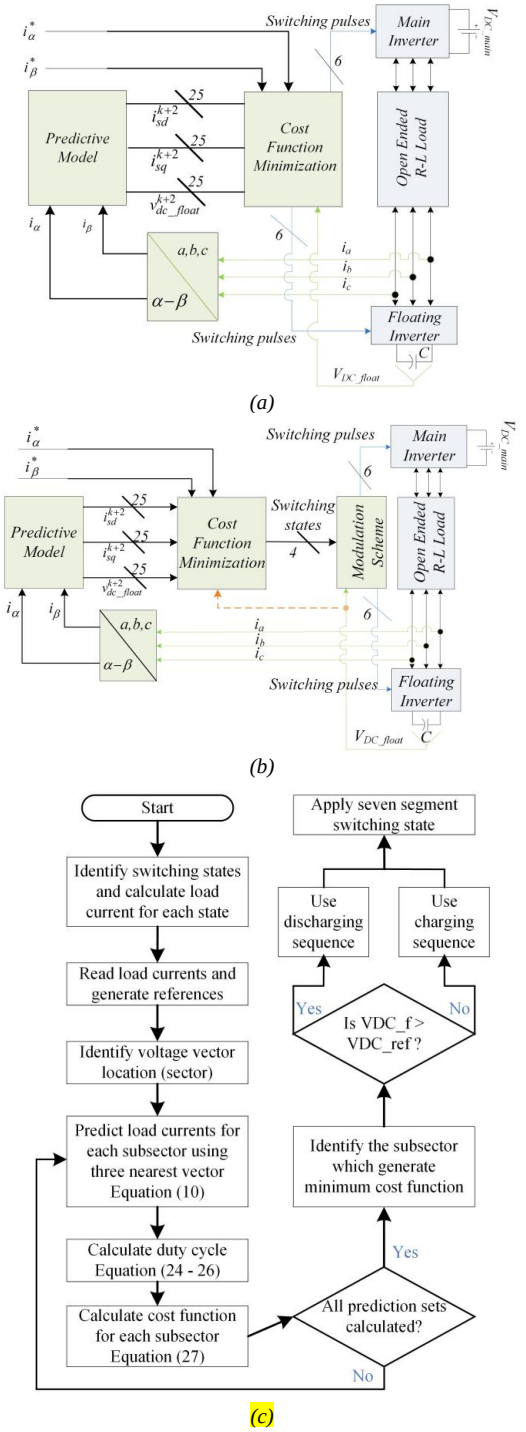


Fig. 3. *Block diagram of the controller (a) predictive controller (b) proposed MMPC as the current control of dual inverter with one bridge floating on an R-L load (c) flowchart of the proposed controller.*

The MMPC algorithm introduced in this paper is based on the traditional SVM scheme. A switching table is constructed to achieve the control. To explain the working process of the controller, the space vector diagram depicted in Fig. 1(b). In that figure, the reference voltage locates within region 1, sector I. Under this condition, the cost function for these three switching states (85 – 84 - 23) can be minimized such that these switching states will then be utilized to generate the minimum error at the next sampling interval.

The switching cost function for this specific region can be expressed using (21-23).

$$g_{85} = \sqrt{(i_\alpha^* - i_\alpha^{85})^2 + (i_\beta^* - i_\beta^{85})^2 + (V_{dc_f}^* - V_{dc_f}^{85})^2} \quad (21)$$

$$g_{23} = \sqrt{(i_\alpha^* - i_\alpha^{23})^2 + (i_\beta^* - i_\beta^{23})^2 + (V_{dc_f}^* - V_{dc_f}^{23})^2} \quad (22)$$

$$g_{84} = \sqrt{(i_\alpha^* - i_\alpha^{84})^2 + (i_\beta^* - i_\beta^{84})^2 + (V_{dc_f}^* - V_{dc_f}^{84})^2} \quad (23)$$

where g_{xy} is the cost function for the switching state combination 'xy' (here xy = 85, 23 and 84). In (21-24), i_α^{xy}, i_β^{xy} and $V_{dc_f}^{xy}$ represent α, β axis currents and the voltage of floating capacitor, respectively. The duty cycle is proportional to the cost function outcomes. For instance, the larger the cost function leads to the smaller the duty cycle. The duty cycles derivation for every switching state combination is displayed in (24-26). The total cost function derivation for this specific case is expressed in (27). A seven-segment switching sequence can be allocated once the region has been chosen to minimize error at the next sampling period. This segmentation is required to modulate the appropriate voltage, the sequences can be 84-85-23-74-23-85-84 as the reference voltage locates in the sector I as showed in Fig. 1(b).

$$t_{85} = \frac{g_{23}g_{84}}{g_{85}g_{23} + g_{85}g_{84} + g_{23}g_{84}} \quad (24)$$

$$t_{23} = \frac{g_{85}g_{84}}{g_{85}g_{23} + g_{85}g_{84} + g_{23}g_{84}} \quad (25)$$

$$t_{84} = \frac{g_{23}g_{85}}{g_{85}g_{23} + g_{85}g_{84} + g_{23}g_{84}} \quad (26)$$

$$G = g_{85}t_{85} + g_{23}t_{23} + g_{84}t_{84} \quad (27)$$

Lastly, output voltages of currently utilized switching states are evaluated to extend the prediction horizon. The output voltage is derived by multiplying the voltage vector with the duty cycle for that specific switching state. The derivation of the output voltage vector in α, β plane is expressed in (28-29). These voltages can be chosen to predict the control objectives at two sample intervals in advance.

$$V_\alpha(k) = [t_{85}V_{\alpha_85} + t_{23}V_{\alpha_23} + t_{84}V_{\alpha_84}] \quad (28)$$

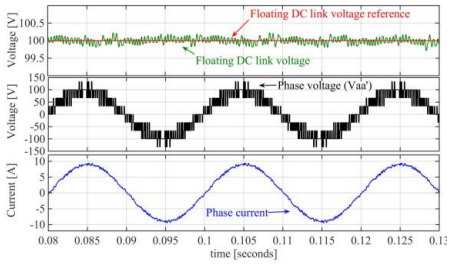
$$V_\beta(k) = [t_{85}V_{\beta_85} + t_{23}V_{\beta_23} + t_{84}V_{\beta_84}] \quad (29)$$

The load and the converter are modelled using (1-15) and the modulation method is expressed using (21-29). It is obvious that the MMPC demands extra calculations. For simplifying calculations, the term of capacitor voltage control is included in the modulation process. Hence, the requirements for predicting capacitor voltage and associated calculations can be eliminated. To further relieve the computational stress, the location of the reference voltage in the space vector diagram is identified. In this case, only the sector of the voltage vector is identified and then only the voltage vectors associated with the specific sectors are utilized to identify the optimum vector sequences. The controller has to deal with only 6 switching states rather than 25, thus the calculation time minimizes drastically and reduces the chances of selecting some other switching states which can introduce additional harmonics in the voltage waveform.

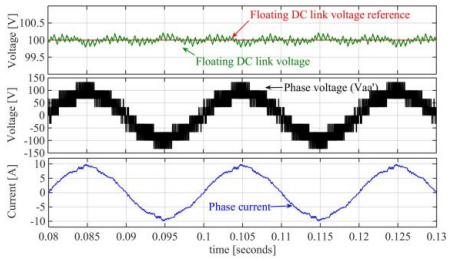
4. Results

4.1. Simulation results

The controllers were simulated using both PLECS and SIMULINK simulation platform to compare FS-MPC to proposed MMPC controller. The main converter was powered by a constant DC link of 200Volts. The reference floating DC link voltage was set to 100Volts. The dead-time value was set to 4µs, same as the experimental converter. The switches were considered ideal and the snubbers and chokes were ignored. To achieve results a 9Amps reference current was set to show the operation at multilevel mode, for both the control methods. The response of the FS-MPC controller is displayed in Fig. 4(a). From that figure, it shows that the converter is operating at multilevel mode and has control over floating capacitor voltage. The results for proposed MMPC control are shown in Fig. 4(b). The controller was also able to regulate the floating capacitor voltage and outputs multilevel voltage waveform. The main advantage of this controller is fixed switching frequency thus the harmonic distortion is much lower.



(a)



(b)

Fig. 4. *The response of the controller when 9A current was required from the system, (a) predictive control (b) proposed MMPC controller.*

Table I. Voltage and current THD (Simulation)

Modulation	Sampling (Average SW) frequency (kHz)	Load current THD (%)
FS-MPC	12.5 (2.8)	4.9
Proposed MMPC (Cap-charge in cost-function)	5 (5)	3.8
Proposed MMPC (Cap-charge in modulation)	5 (5)	3.8

Harmonic distortions for different controllers are shown in Table I. It can be seen that the FS-MPC scheme presents the highest load current harmonic distortion. The waveform quality of the FS-MPC scheme was improved by introducing modulation scheme inside predictive control algorithm. The results show better quality load currents, where THD reduced from 4.9% to 3.8% of the fundamental component. It can also be seen from Table I that the capacitor control inside modulation scheme or in cost function algorithm doesn't have a significant effect on output waveforms for proposed MMPC controller. All the waveform results shown in this paper were achieved using three-step commutation to avoid dead-time spike inherent with dual inverter with asymmetric sources [19 -20].

4.2. Experimental results

In this section the theory and simulation results are validated using laboratory setup. An experimental rig has been built, shown in Fig.5. An 'off the shelf' two-level power converter is utilized, these converters are produced by SEMIKRON named as SAKI modules. These converters are integrated with dead time circuit which varies from 4 – 4.1µs along with propagation delay of 0.1–0.2µs[4]. A current direction detection circuit was also designed to identify load current direction, to avoid dead-time spike[19]. The converter has been verified using an R-L load, load parameters are presented in Table II. The main inverter was powered by a constant DC link source of 200Volts where the reference of floating DC link voltage was kept constant at 100Volts for all the experimental results shown in this section. The performance of the FS-MPC controller was analyzed first. To show the results, a reference load current of 9Amps was applied to the controller. The results are shown in Fig. 6(a) it can be seen from the figure that the converter can achieve multilevel mode of operation.

To illustrate the dynamic response of the controller, a step change in the reference current was changed from 4A to 9A, shown in Fig. 6(b). The load current harmonic spectrum shows a wide range of harmonics resulting from the variable switching frequency of the predictive control algorithm, shown in Fig. 6(c). Finally, to improve waveform quality without compromising the characteristics of the predictive control algorithm, the proposed MMPC control was implemented. The multilevel operation of the converter is shown in Fig. 7(a). A dynamic response was imitated by applying a step change in reference currents, shown in Fig. 7(b).

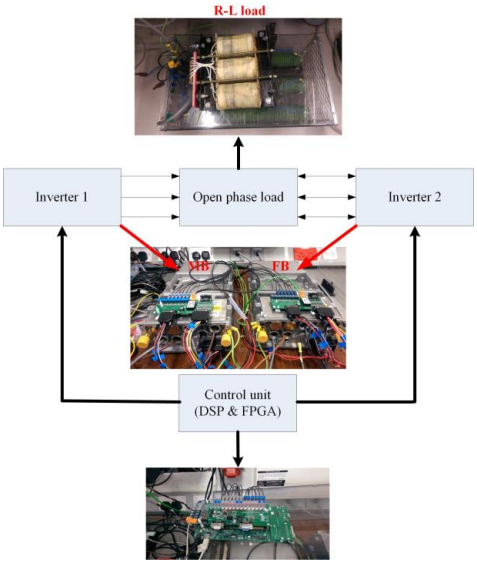


Fig. 5. *Experimental Converter and Control Platform.*

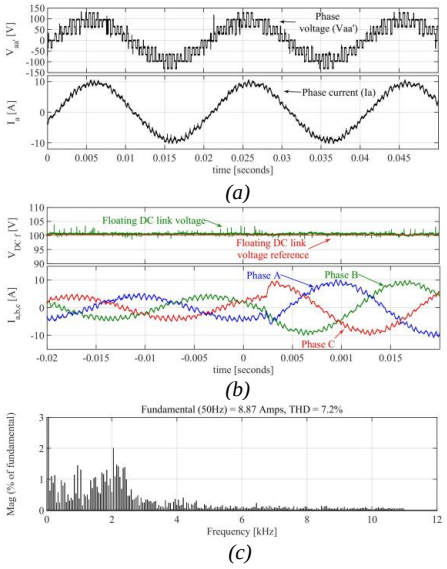


Fig. 6. *The response of the FS-MPC controller (a) phase voltage and current (b) floating DC link voltage and phase current when 9A current is demanded from the system (c) phase current harmonic spectrum.*

Table II. Parameters.

R-L Load		
Resistance	R	10.6 Ohm
Inductance	L	3.8e-3 H
DC link capacitance	C	4550µf
Main DC link	Vdc_main	200 Volts
Floating DC link	Vdc_float	100 Volts

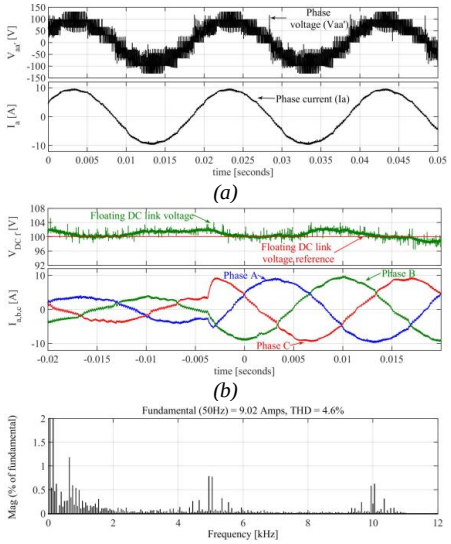


Fig. 7. *The response of the proposed MMPC controller (a) phase voltage and current (b) floating DC link voltage and phase current when* 9A current is required from *the system (c) phase current harmonic spectrum.*

A frequency spectrum of the load current for the proposed MMPC algorithm is shown in Fig. 7(c) as the dual inverter was operating at multilevel mode. From the frequency spectrum, it can be observed that the most of harmonics are clustering around the sampling frequency and the total harmonic distortion is lower than the traditional predictive control.

5. Control comparison

A comparison of control dynamics and their effect on load current for the predictive control strategies are shown in this section. A comparison of load currents and voltage harmonic distortions are shown in Table III. It can be seen from the table that the proposed MMPC controller achieves better current waveform quality than the FS-MPC control algorithm. The FS-MPC control shows the highest harmonic distortions due to the nature of the controller and the harmonics are clustering around lower frequency range thus a larger output filter will be required. The load current THD is improved more than 36% using proposed controller. The frequency spectrum suggests that most of the harmonics are clustering around the sampling frequency thus a much smaller filter will be required. The experimentally achieved THD values shown in Table III is much higher than the ones presented in Table I achieved using simulation platform. This is because ideal switches were considered for simulation and parasitic coupling capacitors are ignored. It can also be seen from Table I and Table III that a much higher sampling frequency is used for FS-MPC control algorithm, this is because the average switching frequency is much lower than sampling frequency for variable switching nature of the predictive control. A much higher sampling frequency can be used to achieve higher average switching frequency by keeping the same load, thus a faster DSP will be required for practical implementation. However, the trend of the frequency spectrum will remain the same. Thus in this experiment 12.5kHz sampling frequency was used.

Table III. Voltage and current THD (Experimental)

Modulation	Sampling (Average SW) frequency (kHz)	Load current THD (%)
FS-MPC	12.5 (3)	7.2
MMPC (Cap-charge in cost-function)	5 (5)	4.6
MMPC (Cap-charge in modulation)	5 (5)	4.6

A comparison of floating voltage control for all the controllers is shown in Fig. 8(a). It can be seen from Fig. 8(a) that the steady state voltage of the proposed controller has similar fluctuations due to the selection of three voltage vectors and does not change much either for floating voltage control inside modulation scheme or in cost function algorithm thus any method can be utilized. In this experiment the floating capacitor voltage control is integrated with modulation scheme to reduce DSP calculation time. There are couple of reasons for floating capacitor voltage fluctuation for proposed controller, one directly related to the sampling time. Sampling time for FS-MPC is 80µs and it can select either charging or discharging switching sequence within this sampling time without changing the output voltage state. Whereas for proposed controller sampling time is 200µs relatively large compared to FS-MPC. Moreover, the proposed controller selects a set of three vectors which contains charging and discharging sequences thus the capacitor voltage fluctuated more than the FS-MPC. The fluctuation in the capacitor voltage is still less than 3% which is acceptable thus no action has been taken. The response of the controllers for a step change in reference current amplitude is shown in Fig. 8(b). It can be seen that the FS-MPC has the fastest response of them all. The load currents were directly measured after the analog to digital conversion, where an average sampling method is used thus the currents in Fig. 8(b) for proposed MMPC controller is clean. The current for model predictive control show switching effect due to the digital conversion is sampling at 12.5 kHz and the converter was switching at much lower frequency. The computational time of the DSP board 'TMS3206713DSK' for different control algorithms is shown in Fig. 8(c). To achieve results a 'TMS3206713DSK' DSP board along with an FPGA 'ActelProasics 3' was used. The FPGA board is used for ADC conversion and for implementing delay time for the pulses. For all the control strategies, the FPGA has the same task, only to read an analog signal and convert to a digital signal along with the delaying of the pulses. The DSP program changes according to a control algorithm and the computational time for each control algorithm is then measured. The calculation time for proposed MMPC control algorithm is reduced by identifying the charging and discharging switching sequences, it can see seen that identification of the charging limit and the switching states leads to a significant reduction of calculation time. The traditional MMPC control with capacitor charging inside cost function requires additional equations and the calculation time is high.

To reduce the computational burden, the charging of capacitor was integrated with the modulation scheme and the outcome is outstanding, 30µs reduction in calculation time. The calculation time is further reduced by identifying the location of reference voltage within the space vector diagram. Identification of reference voltage position inside vector diagram enables the controller to deal with only 6 states rather than 25 thus reduces the calculation time significantly. The calculation time suggests that the proposed MMPC control can be implemented using lower power DSP/FPGA platforms.

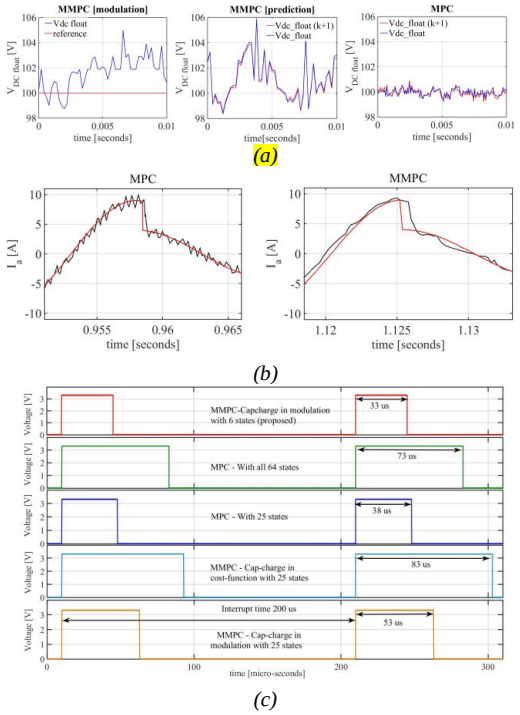


Fig. 8. *(a) Floating capacitor voltage control (b) the response of the control methods for a step change in amplitude of reference current (c) computational time for different controllers.*

6. Conclusion

In this paper, a modified MMPC is addressed and employed as load current controllers for a dual inverter topology with a floating bridge. The MMPC algorithm integrates a modulation algorithm within the predictive control scheme such that constant switching frequency of 5 kHz is achieved. It has been experimentally verified that the addressed algorithm can control the dual inverter and enhance the load current performance in comparison with the predictive control algorithm. It is critical to emphasize that the proposed algorithm can be regarded as an attractive alternative to conventional controllers due to its intuitive implementation and simplicity.

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