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Michael A. Derenge and Kenneth A. Jones

AFFILIATIONS

United States of America Army Research Laboratory, 2800 Powder Mill Road, FCDD-RLS-DE, Adelphi, Maryland 20783-1138, USA

ABSTRACT

In light of the necessity to anneal GaN to activate implanted dopants, the effects of the annealing temperature and time, the quality of the hydride vapor phase epitaxy grown GaN film, the quality of the annealing cap, and the effects of the stresses generated by the difference in the coefficients of thermal expansion of the film and the substrate are examined topographically using atomic force microscopy, and electrical measurements are made on Schottky diodes fabricated on the annealed samples. The results show that thermal decomposition begins at threading edge dislocations that form polygonized small angle grain boundaries during the annealing process; donor defects, probably nitrogen vacancies, are formed near the surface; and the donors are created more quickly when the annealing temperature is higher, the annealing time is longer, and the thermal stresses on the annealing cap are greater. The results suggest that the maximum annealing temperature is ∼1300 °C, and at that annealing temperature, the annealing time should not exceed 4 min.

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INTRODUCTION

It is important to be able to locally dope GaN because it can be used to lower its contact resistance.[1] It should be particularly useful for *p*-type material since the acceptor depths are particularly large. Buried *p*-type structures such as the current blocking layer in the current aperture vertical electron transistor (CAVET) could also be created by ion implantation.[2]

A primary challenge to activating the implants is to find a way to thermally activate the implanted ions without physically altering the surface or electrically altering the interior. Physically, Ga droplets can be formed[3] when N with its large vapor pressure evaporates preferentially; its vapor pressure is 100 MPa at ∼1195 °C.[4] Attempts have been made to physically restrain N from escaping using a crystalline or amorphous dielectric that covers the surface well, does not chemically react with it, does not readily evaporate at the annealing temperature, and can be selectively removed. Examples are sputtered SiO_2,[5] Si_3N_4,[6] or AlN,[7] but results show that they do not adhere very well. A large number of thermal etch pits were observed when annealed at 1200 °C when using a Si_3N_4 capping layer[6] and after annealing at 1300 °C when using AlN.[7] Ga droplets appeared on the surface when the GaN film was annealed at 1300 °C when a SiO_2 cap was used.[5] Using an epitaxial film that binds to the surface more strongly and binds more of the surface atoms is an attractive alternative if it can be selectively etched off. A metal organic chemical vapor deposition (MOCVD) epitaxially grown AlN film deposited at the usual growth temperature has been tried, but it cracked because it could not plastically accommodate the lattice mismatch between GaN and AlN.[8] We have developed a cap composed of a metal organic chemical vapor deposition (MOCVD) grown epitaxial AlN film deposited at a lower temperature that is not as strong because it contains a large number of defects that are able to accommodate the lattice mismatch and then reinforced the cap by sputtering a thick (1 μm) AlN film on top of the MOCVD film.[8–10] This more defective cap was easier to etch off after the anneal.[11]

However, retaining a relatively smooth surface is a necessary but possibly not sufficient condition for achieving device quality localized doping, as the implantation process could produce structural defects that are electrically active. One possibility is stacking faults that have been observed in annealed samples that were ion implanted at room temperature.[12] Modeling suggests that they create deep donors in GaN.[12] This could be one of the reasons why it has been difficult to activate p-type dopants.[13] This problem could possibly be avoided, or at least minimized, by implanting at higher temperatures. However, the annealing process could also create electrically active point defects. Given the high vapor

pressure of N, one example could be the N vacancy, N_V. Experimentation suggests that N_V is a donor with a donor energy, $E_D = 70$ meV.[14] Theory also shows that it forms more easily in p-type material.[15,16] Experimentation also suggests that N_V can form complexes in ion implanted and annealed samples.[17]

In this paper, we will explore the effects of annealing samples at different temperatures for different times using a dual AlN cap to protect the surface of (0001) GaN films grown on sapphire by hydride vapor phase epitaxy (HVPE). We also qualitatively examine the effects of the strains produced by thermal cycling by making measurements near the edges and closer to the center where the stresses are larger. Changes in the surface roughness are recorded using atomic force microscopy (AFM), and changes in the electrical properties are measured using capacitor/voltage (*CV*) and current/voltage measurements made on Schottky diodes fabricated on the samples. The surface topographs provide insight into the thermally induced movement of surface atoms and structural defects near or at the surface. Forward and reverse bias characteristics and carrier concentration distributions are interpreted in terms of possible electrically active point defect creation.

PROCEDURE

Twelve 10.5×11 mm^2 rectangular samples and four triangular samples with a circular hypotenuse and 10.5 mm sides were cut from an unintentionally doped, *c*-oriented, 10.5 μm thick GaN film grown by Ostendo by HVPE on a 2 in. sapphire substrate. During processing and/or measuring one side, the *x*-axis was oriented parallel to the intersection of the $(10\underline{1}0)$ and (0001) planes—the $[\underline{1}2\underline{1}0]$ direction. Two 5×5 μm^2 AFM topographs were taken, one at the edge and one near the center. With the exception of a few outliers, they were virtually the same both between edge and center and from sample to sample. The average RMS value for these measurements is 0.69 nm, and it is recorded in Table I for the as-grown sample.

One sample was withheld to be used as the standard, and the others had an annealing cap deposited on them, which was composed of an 80 nm AlN film grown by MOCVD at 800 °C and a 1 μm AlN film sputter deposited on top of it at 500 °C. The temperature the samples were annealed at, T_A, in a nitrogen atmosphere was 1150, 1200, 1250, or 1300 °C, and the annealing time, t_A, was 1, 2, 4, or 8 min. There was no sample annealed at 1150 °C for 1 min because the 16th sample was used as the standard. The caps were removed after the anneal in a 2M KOH solution heated to 25 °C for 16 h. The RMS value was determined again near the edge and near the center after the anneal, and this time there was a difference. The value for near the edge is entered into Table I as is the difference between the value for the center and the value for the edge, Δ_{RMS}.

100, 200, and 300 μm diameter mesas 1 μm high were created by etching the samples, and they were used to create 90, 170, and 270 μm NiAu lateral Schottky diodes. They were encircled by TiAlNiAu ohmic contact rings that were annealed at 750 °C for 30 s. The measurements on the different types of diodes were similar, so only measurements for the 170 μm diodes are included in this paper. Diodes in the columns or rows within 2 mm of the edge were considered to be edge diodes; the others were considered to be diodes near the center. Measurements were made on at least 10 diodes of each type.

CV measurements were made to determine the net donor concentration, n_d, as a function of the depth, *d*, beneath the surface, with d_o being the depth at zero bias. The median value of n_d for the diodes near the edge is recorded in the table. The same measurements were made for diodes near the center, and the median value for the diodes near the edge was subtracted from their median value, and the difference, Δn_d, is entered in the table. The

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TABLE I. Properties of the as-grown GaN films and Schottky diodes fabricated from them for samples annealed at different temperatures for different times and devices located at different positions on the sample.

T_A (°C)	t_A	RMS (nm)	Δ_{RMS} (nm)	n_d ($cm^{-3} \times 10^{16}$)	Δn_d ($cm^{-3} \times 10^{16}$)	G $(\Omega^{-1}\,cm)^2$	ΔG ($\Omega^{-1}\,cm^2$)	G_K ($\Omega^{-1}\,cm^2$)	ΔG_K ($\Omega^{-1}\,cm^2$)	J_l (A/cm^2)	ΔJ_l (A/cm^2)
20	…	0.69	…	0.52	0.02	281	−29.4	0.48	−0.47	0.0001	−0.0001
1150	2	0.73	−0.16	4.33	1.09	369	−76.3	0.02	0.01	0.11	0.85
1150	4	1.39	−0.48	3.30	2.11	309	26.9	0.35	−0.26	1.65	−1.40
1150	8	0.88	−0.27	5.42	−0.38	284	−10.7	4.95	−4.57	2.26	−1.11
1200	1	0.67	6.16	5.17	0.36	365	−7.1	0.27	−0.09	0.68	−0.14
1200	2	0.54	0.16	3.44	1.49	431	−32.9	0.36	0.42	0.11	2.09
1200	4	0.85	0.18	5.48	−2.26	381	−36.8	4.06	0.76	7.50	17.3
1200	8	1.03	5.00	5.63	0.16	286	6.2	1.77	2.09	7.01	15.8
1250	1	0.56	0.00	4.87	0.48	303	43.6	1.51	0.11	12.0	−7.19
1250	2	0.65	−0.15	5.28	−0.06	380	20.8	0.008	0.16	0.002	1.22
1250	4	0.57	1.34	4.87	0.71	310	32.0	1.88	2.02	6.60	17.0
1250	8	1.00	7.84	5.55	41.0	386	−106.0	5.24	7.58	31.5	33.2
1300	1	1.20	8.02	6.36	1.56	263	18.9	12.6	−0.75	120.0	−38.5
1300	2	1.47	3.68	5.12	900.0	324	−64.5	4.08	−1.27	1.89	32.6
1300	4	1.11	5.75	74.4	784.0	283	−63.6	1.33	1.23	6.90	14.3
1300	8										

forward and reverse iV curves are also recorded. The specific conductance, G, above the voltage knee, V_K, for the median iV curve for the diodes near the edge is calculated and recorded in the table. This value is subtracted from a similar conductance calculated for the median values for the diodes near the center, and this difference, ΔG, is recorded in the table. The specific conductance below the knee voltage, G_K, and the difference, ΔG_K, are also calculated and recorded. The reverse leakage current density at −5.0 V, J_l, is recorded in the same way. J_l refers to the median diode near the edge, and ΔJ_l refers to the difference in the median leakage current density for the diodes at the center and those at the edge. n_d, Δn_d, G, ΔG, G_K, ΔG_K, J_l, and ΔJ_l are also determined for the standard sample, and those results are listed in the first row of Table I.

RESULTS AND DISCUSSION

First, we consider the effects of T_A and t_A on RMS roughness measured on topographs taken near the edge of the sample. As shown in Table I, except for the sample annealed at 1200 °C for 1 min that failed catastrophically as shown in Fig. 1(c), the RMS roughness is relatively unaffected by the anneal for the samples annealed at $T_A = 1150$, 1200, or 1250 °C and $t_A = 1$, 2, or 4 min. For the samples that are annealed at 1250 °C, it took a t_A of 8 min for the step flow growth pattern on the surface to disappear, as shown in Fig. 1(a). Surface diffusion would have to occur, but it is not clear what the mechanism is given that the annealing cap was still intact, but that does not preclude some N being lost by diffusion through the cap. The topograph of the sample annealed at 1150 °C for 8 min, which is displayed in Fig. 1(b), shows that defects might play a role in the out-diffusion of N, as, while retaining the step growth pattern, it also displays small hexagonal pits arrayed in lines parallel to the ⟨11$\underline{2}$0⟩ directions. These pits were observed in the vast majority of samples where the step flow growth pattern remained intact, but they were most easily seen in the sample annealed for the longest time and the lowest temperature. This can be explained by their growing larger with time at an annealing temperature that has little effect on the surface topology. This suggests that there is a strong escaping tendency of the N even at relatively low annealing temperatures when there is a sufficiently long annealing time, and defects are present to enable its escape even when a cap is used. That N does preferentially evaporate even at these lower annealing temperatures has been demonstrated by direct evaporation experiments utilizing weight changes,[18] Raman spectroscopy,[19] and Rutherford backscattering spectroscopy (RBS).[20] In each case, the researchers were able to detect N evaporation at 900 °C, and it became significant at annealing temperatures above 1000 °C.

It is likely that the pits are etch pits for threading edge dislocations (TED).[21] We theorize that the lines represent small angle grain boundaries created by the polygonization of TEDs, as described schematically in Fig. 2. The topograph in Fig. 1(c) for the sample that apparently had a loose cap showed that, given the chance, the film will decompose along these polygonized grain boundaries. The deep grooves are approximately parallel to ⟨11$\underline{2}$0⟩ directions and make angles of ∼60° with each other. The relaxation of the film caused by the polygonization process helps to explain the observation in our earlier work that annealing heterostructure GaN films tends to reduce their x-ray rocking curve peak width.[8]

The RMS roughness for the center of the sample tends to be a little rougher for the same T_A and t_A as shown in Table I where the difference between the RMS values between the topographs from the center and the edge of the same sample, Δ_{RMS}, is listed. The difference is particularly large for the higher T_A and longer t_A. This suggests that the cap is not as tight near the center as it is near the edge. This could be because the shear stress created by the difference in the thermal coefficient of expansion (TCE) of the film and the substrate is larger near the center where edge effects do not have to be considered. Given that the induction field is larger than the rotating graphite susceptor, which is larger than the sample it is heating, we believe that the temperature variation between the center and edge is minimal, so it is unlikely that the greater roughness in the center can be solely attributed to the center of the sample being heated to a higher temperature.

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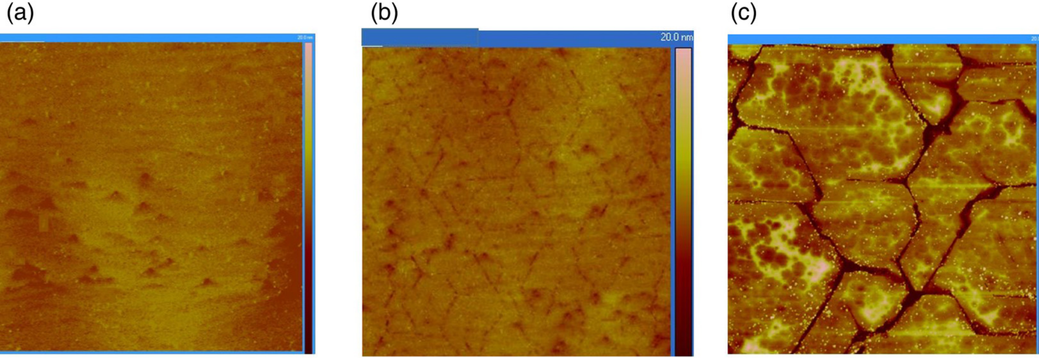


FIG. 1. 5 × 5 μm^2 AFM micrographs of the sample (a) located near the edge and annealed at 1250 °C for 8 min that illustrates the transition from step flow growth to a rougher surface, (b) located near the edge and annealed at 1150 °C for 8 min that illustrates step flow growth, as well as the lines, composed of small hexagonal thermal etch pits, that are parallel to ⟨11$\underline{2}$0⟩ type directions, and (c) located near the center and annealed at 1200 °C for 1 min that illustrates what happens to the surface when the annealing cap has poor adhesion.

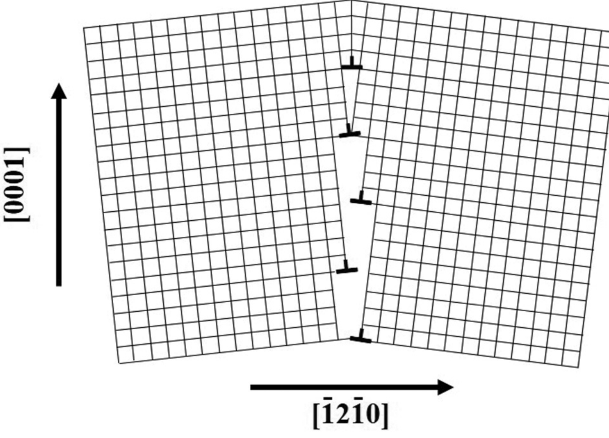
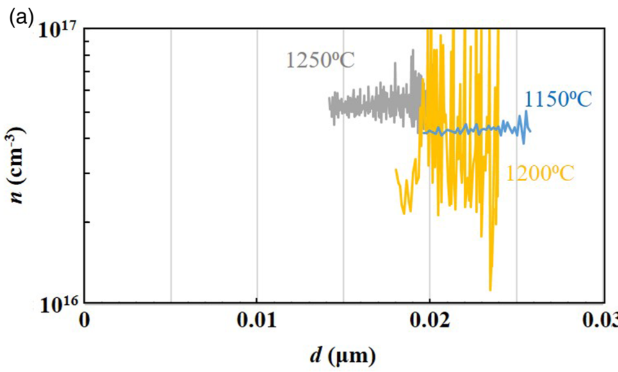


FIG. 2. A schematic of the tilt boundary responsible for the lines parallel to the ⟨11$\bar{2}$0⟩ directions.

The net donor concentration, n_d, determined as a function of the distance from the interface, d, for the diodes near the edge was determined from CV curves, and the results are listed in Table I and displayed in Fig. 3. The mean value of n_d is relatively unaffected by the anneal for the samples annealed at $T_A = 1150$, 1200, or 1250 °C for $t_A = 1$, 2, or 4 min; the values range from 3 to 5×10^{16} cm^{-3}. This is larger than the value of 5.2×10^{15} cm^{-3} for the as-grown sample. This difference can be attributed to activation and cleaning processes stimulated by the anneal.

Of more significance is the observation that while n_d remains constant, d tends to decrease as T_A or t_A increases. As is shown in Fig. 3(a), d decreases as T_A is raised from 1150 to 1200 to 1250 °C. This can be accounted for by donors being created near the surface where they will not be directly detected given that CV measures n_d at the end of the depletion layer, so the device would have to be forward biased to measure n_d for $d < d_o$. For anneals when T_A reaches 1250 °C and t_A is 4 or 8 min, and for all anneals at 1300 °C, however, n_d is larger at d_o for some cases, and it decreases as d increases. The distinguishing factor is the position of the diode. As shown in Fig. 3(b), n_d for the diodes near the edge have a lower more uniform concentration for diodes annealed for 8 min at 1250 °C, while those near the center have a larger more variable concentration that increases toward the surface. This increase is suggestive of donors being created by the out-diffusion of N leaving N_V behind. The effect is larger toward the center where larger stresses are created by the TCE difference; the larger the stress, the less able the annealing cap is to prevent the preferential evaporation of the N. All of the diodes annealed at 1300 °C show the same trends with the trends being more dramatic as t_A increases.

The discussion of the forward JV characteristics displayed in Figs. 4 and 5 is divided up into the specific conductance above and below the knee voltage. We will discuss how they are affected by the annealing temperature and time, and the position of the Schottky diode being measured. It is interesting to note that V_K itself can be affected by some of these parameters. For example, V_K



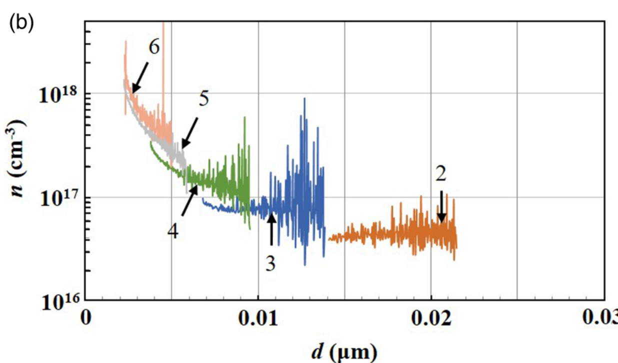


FIG. 3. n_d vs d plots for (a) diodes near the edge that are annealed for 2 min at 1150, 1200, or 1250 °C and (b) diodes annealed at 1250 °C for 8 min that are located 2, 3, 4, 5, and 6 mm from the edge.

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is larger for the annealed samples compared to the one that is as-grown. The average value for the latter is 0.83–0.92 V, whereas it is frequently greater than 1 V for the annealed samples. This can be attributed to the voltage created by the piezoelectric effect[22] of the GaN film put into lateral compression by the difference in the TCE, with the one for sapphire being larger than the one for GaN. Figure 5 also shows that V_K is larger for the diodes fabricated near the center of the sample than they are near the edge. This can be explained by the lateral stresses being larger toward the center away from stress lowering by edge effects.

The results in Table I show that G for diodes near the edge is initially increased by annealing. It is larger for the sample annealed for 2 min at 1150 °C, and the increase is even larger after the 1200 and 1250 °C anneals. These results are also demonstrated in Fig. 4 where the JV curves for the diode with the largest and smallest currents along with the median current for all of the diodes near the edge are plotted. This can be attributed to the mobility being increased by annealing out some of the structural damage as has been suggested by the reduction in rocking curve widths.[8]

The results in Table I and Fig. 4 also show that G for the diodes annealed for 2 min at 1300 °C is comparable to G for the as-grown sample. This can be explained by the creation of point defects that scatter the electrons, thus canceling out the reduction of scattering by structural defects that have been reduced by the

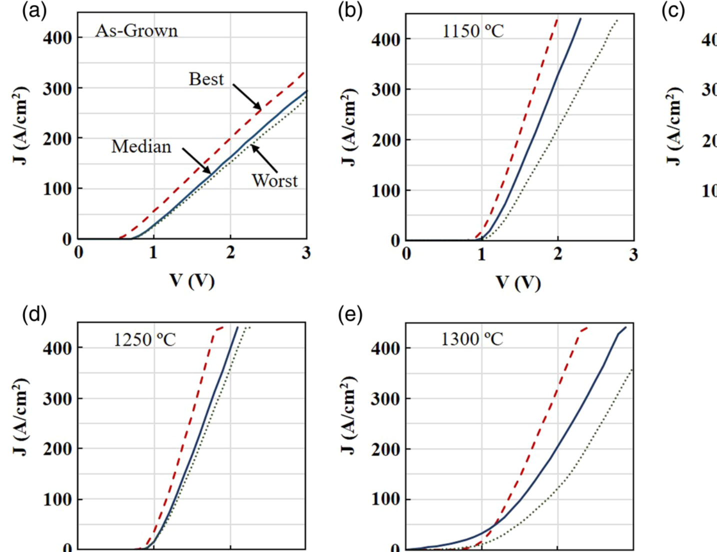

FIG. 4. The forward *iV* curves for a diode near the edge with the largest (short-dashed curve) or smallest (dotted curve) current along with the median value (solid curve) for all of the diodes near the edge for samples that were (a) as grown, or annealed for 2 min at (b) 1150, (c) 1200, (d) 1250, or (e) 1300 °C.

anneal. Given that the point defects seem to be N_V, which are donors[14–16] that should increase *G*, not reduce it, the creation of N_V must be a more complex process, such as forming complexes,[17] for the creation of N_V to have a negative effect on *G*.

The results from Table I show that usually *G* is larger after the 2 min anneal than it is after it is for a 1 min anneal, and then it drops with annealing time after it has reached its maximum value. The only exception is the outlier for the sample annealed at 1250 °C for 8 min.

These results are also corroborated in Fig. 5 where the *iV* curves for the diode with the largest and smallest current, and the median *JV* curve for all of the diodes near the edge that were annealed at 1250 °C for 1, 2, 4, or 8 min. Although the *G* is smaller for the samples annealed at 1300 °C, they show the initial increase from the 1 to 2 min anneal, and then it drops for the 4 min anneal. There are no data for the 8 min anneal because the contact has become more ohmic than Schottky. Thus, the annealing process cannot be used in this T_A/t_A region.

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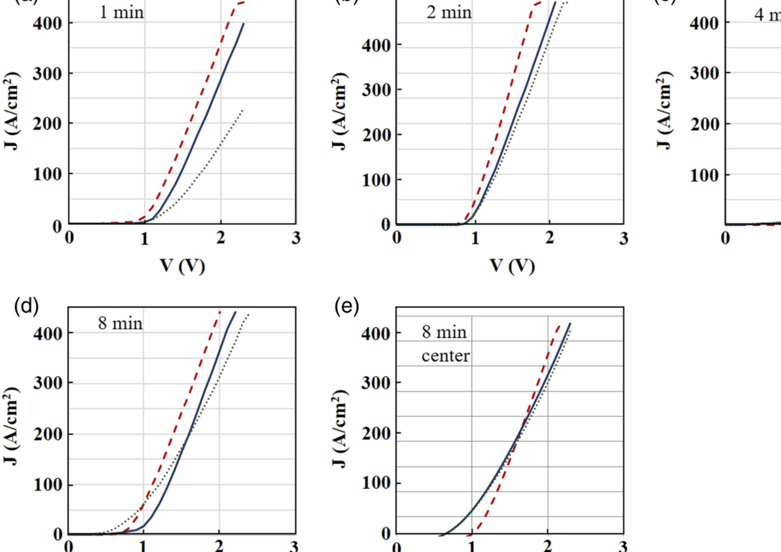


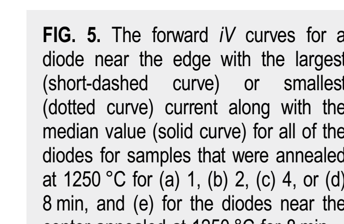
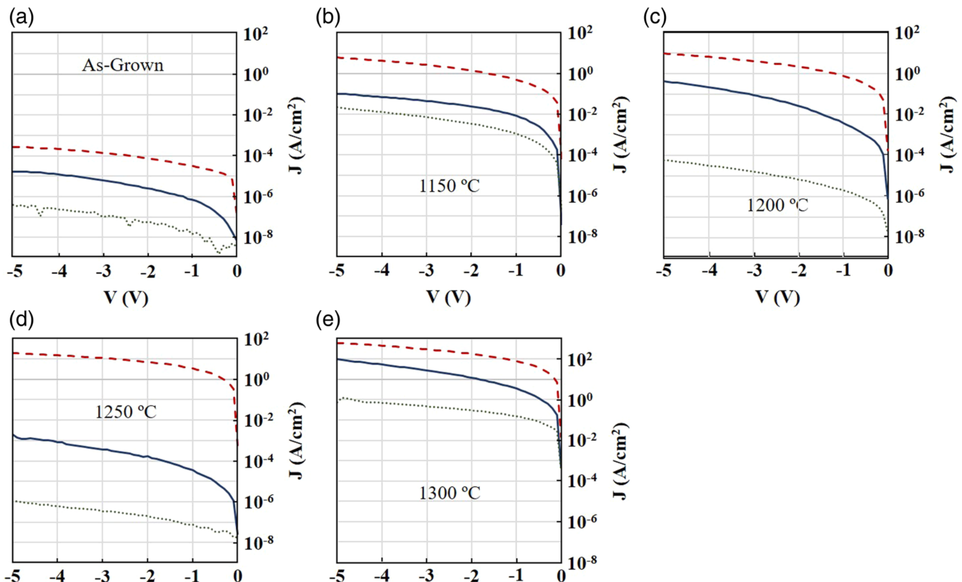


FIG. 5. The forward *iV* curves for a diode near the edge with the largest (short-dashed curve) or smallest (dotted curve) current along with the median value (solid curve) for all of the diodes for samples that were annealed at 1250 °C for (a) 1, (b) 2, (c) 4, or (d) 8 min, and (e) for the diodes near the center annealed at 1250 °C for 8 min.



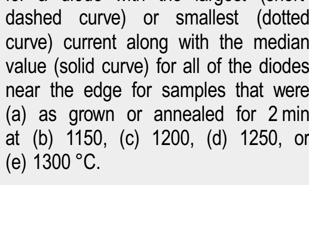


FIG. 6. The reverse leakage currents for a diode with the largest (short-dashed curve) or smallest (dotted curve) current along with the median value (solid curve) for all of the diodes near the edge for samples that were (a) as grown or annealed for 2 min at (b) 1150, (c) 1200, (d) 1250, or (e) 1300 °C.

Table I and Fig. 5(e), where the diode with the lowest and highest currents as well as the median *JV* for all of the diodes near the center of the sample annealed at 1250 °C, show that there is a substantial reduction in *G* for the diodes near the center compared to those at the edge. This difference can be explained by the larger TCE induced stresses at the center of the sample enhancing the ability to create more N_V by reducing the ability of the annealing cap to prevent the preferential evaporation of N. This leads to a reduction in *G*; this means that there is a smaller acceptable annealing region in T_A/t_A when the GaN film is compressively stressed.

As demonstrated in Table I and seen in Fig. 5, annealing the samples has little effect on the conductance below the knee, G_K, for the 1 and 2 min anneals when T_A is 1150 or 1200 °C. However, after that, it usually increases with both T_A and t_A. This can be

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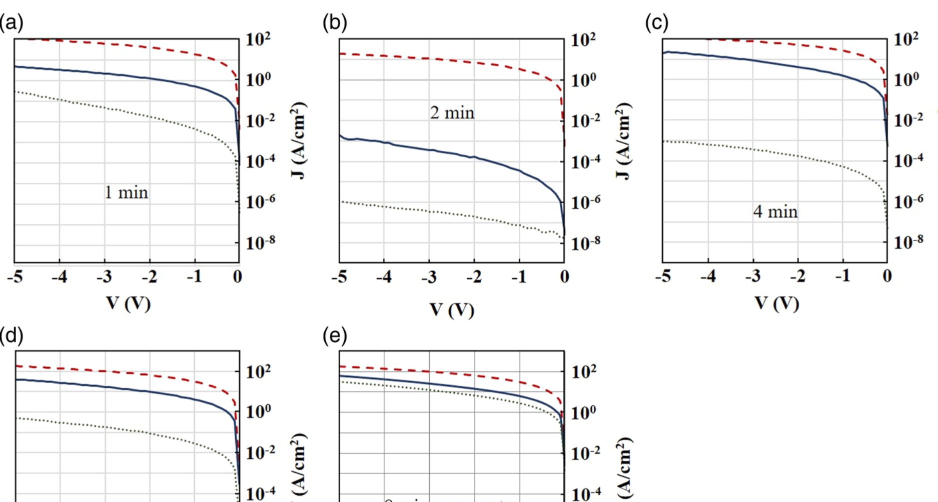

FIG. 7. The reverse leakage currents for a diode with the largest (short-dashed curve) or smallest (dotted curve) current along with the median value (solid curve) for all of the diodes for samples that were annealed at 1250 °C for (a) 1, (b) 2, (c) 4, or (d) 8 min, and (e) for the diodes near the center annealed at 1250 °C for 8 min.

attributed to a larger forward tunneling current, which could be enabled by the donor states created by the N_V and/or complexes formed by them.

Also, the sample position has little effect for the 1 and 2 min anneals when T_A is 1150, 1200, or 1250 °C, but in most cases, G_K is larger for the diodes near the center. This is consistent with G_K being larger where the stress is higher because it reduces the effectiveness of the cap enabling more N evaporation thereby creating more N_V and N_V related defects where more tunneling can occur. For the 4 and 8 min anneals, G_K is larger for the diodes near the center when $T_A = 1200$ or 1250 °C, and the difference is larger at 1250 °C or when $t_A = 8$ min. t_A appears to be the more significant parameter except at $T_A = 1300$ °C, where T_A is the dominant parameter, which is consistent with it being the upper limit for the annealing temperature.

As seen in Table I and Fig. 6, capped annealing at any T_A has a very significant effect on the reverse biased current. Even annealing the sample at 1150 °C increases J_l from 10^{-5} to 10^{-1} A/cm^2 at −5 V. Again, we attribute this to the formation of N_V very near the surface. As pointed out earlier, N_V related defects enable forward tunneling; they likewise will also enable tunneling in the reverse direction.

One can observe in Table I and Fig. 7 that there is a general tendency for J_l to increase with t_A, but J_l for the 1 min anneal is larger than it is for the 2 min anneal for all but the $T_A = 1150$ °C anneals. This is likely due to the changes in J_l produced by our changes in t_A being less sensitive than changes created by our changes in T_A. The more frequently observed increase in J_l with t_A can also be explained by increases of N_V with increasing t_A.

J_l is also affected by the position of the diode; this can be seen in Table I and Fig. 7(e). There is a general tendency for J_l to be larger for diodes near the center, but this is more likely to be true for the diodes annealed at higher temperatures and for longer times. The dominant changes in J_l produced by the changes in position can also be explained by stresses being larger near the center leading to an increase in N_V because they are less able to prevent the preferable evaporation of N.

CONCLUSIONS

Capped GaN samples can be annealed up to a temperature of 1300 °C for a time as long as 8 min without forming relatively large hexagonal thermal etch pits, but a little but detectable surface deterioration can occur even when the cap adheres well. However, there are some substantial changes in the electrical properties of the Schottky diodes fabricated on them. In some cases, the surface appears to begin to deteriorate at threading edge dislocations that form small angle grain boundaries created by polygonization during the annealing process as is suggested by the thermal etch pits aligned along $\langle 11\underline{2}0 \rangle$ directions that are observed in some AFM topographs of samples annealed for shorter times at lower temperatures. Given the large vapor pressure of nitrogen, it is likely that the etch pits are formed by the preferential evaporation of N. This produces defects with donorlike properties near the surface, as is suggested by the shorter depletion layer widths as determined from *CV* measurements that were observed for samples annealed at higher temperatures for longer times. These *CV* curves show that the carrier concentration increases toward the surface and increases with T_A and t_A at higher temperatures and longer times. The annealing does have an initial positive effect, as the conductance above the voltage knee increases with T_A up to 1250 °C with the shorter time anneals and up to 1200 °C when they are longer. It is likely due to an increase in the mobility caused by the annealing out of some crystalline defects, as at the higher T_A and longer t_A the G drops probably because at least some of the N_V created by the annealing create N_V complexes. The G below V_K increases as T_A and t_A increase suggesting that there is a donor induced forward leakage current. The effect is much more pronounced for reverse leakage currents as they increase orders of magnitude even for lower T_A and shorter t_A. The position of the sample also affects the results. In a few instances, the AFM micrograph from the center shows considerable deterioration that most likely is due to poor cap adhesion when it relaxed to reduce the stresses created by the differential in the thermal coefficient of expansion of the sapphire substrate and the AlN cap. That there is considerable compressive stress in the film is shown by the positive shift in V_K, of ∼0.3 V produced by the piezoelectric induced charge. For the samples with the smooth surfaces, the diodes in the center tend to have a smaller G above V_K, larger G below V_K, larger reverse leakage current, and larger carrier concentration at the higher T_A and longer t_A.

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