Thermal Links and Microstrip Transmission Lines in SPT-3G Bolometers

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Abstract In this work, we have measured the properties of membrane-suspended bolometer thermal links and microstrip transmission lines in the transition-edge sensor arrays for the third-generation camera for South Pole Telescope (SPT-3G). A promising

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technique for controlling the end point of the release etch that defines the thermal link has been developed. We have also evaluated the microstrip loss in our detectors by measuring the optical efficiency of detectors with different lengths of microstrip line. The loss tangent is sufficiently low for the use in multi-chronic pixels for cosmic microwave background instruments like SPT-3G.

Keywords Transition-edge sensor · XeF_2 etch · Microstrip loss · Cosmic microwave background · South Pole Telescope

1 Introduction

The SPT-3G cosmic microwave background (CMB) experiment [1,2] is designed to make precise measurements of CMB polarization [3], with the goal of measuring the energy scale of inflation, the number of neutrino species, and the sum of masses of neutrinos [4,5]. The SPT-3G camera has $\sim$ 16, 000 transition-edge sensors (TESs) [6,7] on ten 150-mm-diameter wafers. Each pixel in the camera measures two linear polarizations in three bands. In order to successfully fabricate such a large array of TESs [8–11], it is important to develop a strategy for controlling the performance of key components of the camera pixels.

Figure 1a shows a scanning electron microscope (SEM) image of one SPT-3G pixel. The millimeter-wavelength signal is first received by a broadband sinuous antenna [12, 13] at the center of the pixel. The signal is then split into three bands centered around 95, 150 and 220 GHz by quasi-lumped-element filters [14–16] and transferred to the bolometer islands through superconducting Nb microstrip lines [17]. The bolometer island is a suspended structure supported by four low-stress silicon nitride (SiN) legs which serve as the weak thermal link to the detector substrate. (Details of the island

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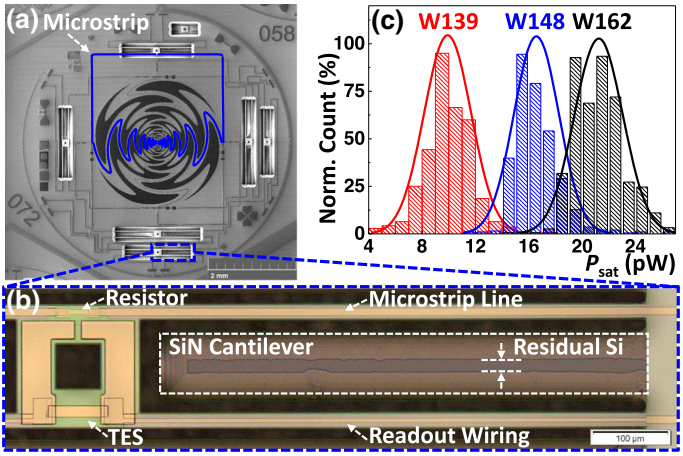

Fig. 1 **a** SEM image of a detector pixel. **b** Detailed image shows the SiN cantilever area around the detector island. **c** P_{sat} distribution of bolometers from three representative SPT-3G wafers (Color figure online)

and two of four supporting SiN legs are shown in Fig. 1b.) The thermal link is designed to provide a detector saturation power (P_{sat}) roughly 2 times of the expected loading from the sky, telescope and cold optics. A 20 Ω Ti/Au load resistor is used to absorb the signal and change the temperature of the island. Finally, the change in temperature of the island is measured by a TES on each island and read out by a frequency-division multiplexing system [18,19]. Details about the fabrication of the SPT-3G detector arrays can be found in our previous publications [8–10].

The bolometer thermal link is a key component because for a given TES transition temperature the thermal conductivity of the link determines P_{sat}. The XeF_2 release etch [20] that defines the legs is difficult to control due to the lack of direct observation

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of the progress under the legs and an obvious end point marker. In our detectors, there is a rectangular area (SiN cantilever area in Fig. 1b) between the two legs that was prepared without Nb ground layer on top of the SiN substrate, so that the Si under the SiN is visible during the thermal link defining process and we found that the width of the residual Si under a SiN cantilever (Fig. 1b) around the thermal link is directly related to the thermal conductance of the link. The width of this Si residue can be monitored in real time and used to choose the end point for the etch. The concept has been verified by measuring wafers with identical TES T_c but different releasing etch times in the SPT-3G receiver. Details are presented in Sect. 2. Microstrip transmission lines are an another key component because loss in the microstrip reduces the optical efficiency [21]. In order to evaluate the actual microstrip loss on the detector wafers, we fabricated and tested test pixels with different microstrip lengths. Details are given in Sect. 3.

2 Detector P_{sat}

The SPT-3G camera provides a unique opportunity for investigating the effect of fabrication parameters because ten detector wafers with different fabrication conditions can be measured simultaneously [22] with similar optical loading. Figure 1c shows the representative measured P_{sat} distributions of low, medium and high P_{sat} detector wafers deployed in 2017. (Results for all three bands are included.) All three wafers have similar scatter in P_{sat}, but the average P_{sat} varies from 10 to 21 pW. Similar distributions can also be observed in all other wafers of the focal plane. The P_{sat} can be described as [23–25]:

$$P_{sat} = K \times ({T_c}^n - {T_b}^n), \tag{1}$$

where K represents the thermal conductance of the weak thermal link, n is the index for thermal conductivity ($n = 1$ indicates that electrons are the main thermal carrier, while $n = 3$ means that phonons are the main thermal carrier) and T_b is the bath (i.e., wafer or wafer holder) temperature. To simplify the discussion, we assume K is inversely proportional to the leg length [10], $T_b = 0.280$ K for all ten detector wafers measured together in the SPT-3G cryostat, and n is similar for all wafers because all thermal links have the same film structure. In this case, only T_c and K contribute to the variation in P_{sat} for different wafers. It is worth mentioning that the situation could be much more complicated in reality. For example, slight changes to the thermal link surface roughness could change K and n significantly. It is also important to keep in mind that K and T_c have too be adjusted to achieve a relatively low thermal conduction ratio $G(T_c) = \mathrm{d}P_{sat}/\mathrm{d}T = nKT_c^{n-1}$, because $G(T_c)$ is directly related to the phonon noise equivalent power (NEP) [26]. A higher NEP may significantly slow down the telescope mapping speed. However, this is not the main focus of this manuscript and it will not change the main conclusion. More thermal link-related discussion can be found in previous publications [27,28]. In the following discussion, n will be fixed at 2.9 based on our previous detector testing [9].

Figure 2a shows the average T_c values of the ten deployed wafers. The main difference between wafer batches in Fig. 2a is the TES film configuration. For example, a Ti/Au bilayer TES was used for Batch D, while a Ti/Au/Ti/Au configuration was

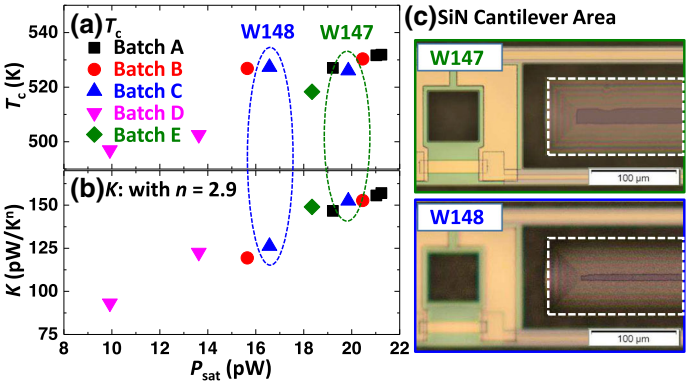

Fig. 2 Average **a** T_c and **b** calculated K values (with $n = 2.9$) as a function of the P_{sat} values of different SPT-3G wafers. **c** The residual Si under the SiN cantilever approximately shows the amount of etching during release of the detectors. The symbols/colors of the data points represent different wafer fabrication batches (Color figure online)

used for the rest of the batches, resulting in T_c about 25 mK higher than for Batch D. This demonstrates that the TES T_c can be tuned within a small range by modifying the TES film configurations [10,29,30]. Similar T_c within a given wafer batch provides a good opportunity to investigate the properties of the weak thermal link. Figure 2b shows the average K values calculated from Eq. (1) for the ten wafers. There is a clear difference in K even within the same wafer batch, which suggests that the legs are etched by different amounts during the releasing process. The XeF_2 etching process that is used to release the legs can be affected by many factors, such as the heating history of the wafers (changes film stress) and oxidation of exposed Si in the area being etched. Taking W147 and W148 in Batch C as an example (blue triangles in Fig. 2a, b), they were released with a similar number of XeF_2 etching cycles, but the calculated K value of W148 is about 20% lower than that of W147. Interestingly, there is a significant difference in the width of the residual Si under the SiN cantilever (see Fig. 2c) for these two wafers, which suggests that the lateral dimension of the residual Si can be used as an end point marker for the releasing process. It is worth mentioning that the wafers were rotated during breaks in the XeF_2 etching process to improve the etching uniformity across the wafer. Slightly different etching speed can be observed between the center and edge pixels of the wafer. Since this difference is rather constant between wafer to wafer, the progress of the center pixel can still be considered as a marker for the whole wafer.

The width of the residual Si has an important limitation as an end point marker because we have to assume that the XeF_2 etching selectivity between Si and SiN is the same for all wafers. In reality, the selectivity may vary significantly due to changes in process pressure, cooling capacity and the amount of remaining XeF_2 crystals in the cylinder [20]. Because of the uncertainty of our XeF_2 etch, we can only qualitatively evaluate the end point for wafers released in one batch. For example, both of the wafers in Batch A were released until there was no residual Si under the cantilever and, as expected, they show similar P_{sat} and K. However, all K values for Batch A wafers are

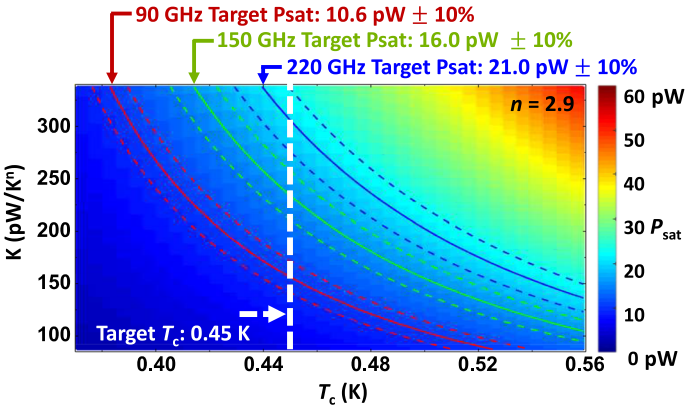

Fig. 3 P_{sat} as a function of the T_{c} and K, for $n = 2.9$, and target parameters for future SPT-3G detectors (Color figure online)

about 20% higher than that for W148, which has some Si under the cantilever and therefore should have higher K values. The XeF_2 etching selectivity must be slightly different, resulting in faster etching of the Si in Batch A. The origin of this phenomenon is not clear, and related investigation is still in progress.

According to measurements of the current SPT-3G focal plane, the overall detector P_{sat} is higher than the optimal values and the detector parameters have been modified for the coming deployment in 2018 [2]. According to Eq. (1), a lower detector P_{sat} can be achieved by reducing thermal link K, TES T_{c} or both of them. Because the 2017 detector design leg length and releasing degree are approaching their limitations, it is reasonable to lower the target TES T_{c} to 0.45 K from 0.50 K so that the tolerance for the thermal conductance can be higher. In the future SPT-3G detector fabrication, the bolometer leg length will be defined after acquiring the TES T_{c} from a wafer from the same batch. The leg length can then be chosen to provide appropriate thermal link K values based on the calculated P_{sat} phase diagram (Fig. 3) with TES T_{c} in x-axis and K in y-axis. Detailed discussion about the detector fabrication optimization can be found in a separate work [2,11].

3 Detector Microstrip Loss

The attenuation of the microstrip transmission lines (with SiO_x dielectric layer) that connect the antenna to filters and detectors directly affects the optical efficiency of a pixel. In order to measure the microstrip loss, we fabricated test pixels with three different microstrip lengths: $z_{\mathrm{S}} = 10494\ \mu\mathrm{m}$; $z_{\mathrm{M}} = 17929\ \mu\mathrm{m}$; and $z_{\mathrm{L}} = 22804\ \mu\mathrm{m}$ (see Fig. 4a, b). Pixels without inline filters were also fabricated to investigate the filter losses; in these pixels, the microstrip lines are 295 μm longer than in pixels with filters.

Figure 4a, b is the pixel design for microstrips with length of z_{S} and z_{L}, respectively. Figure 4c shows the optical efficiency ratio between different test pixels ($\eta_{\mathrm{a}}/\eta_{\mathrm{b}}$) as a function of the microstrip length difference ($z_{\mathrm{a}} - z_{\mathrm{b}}$). Optical efficiency measurements

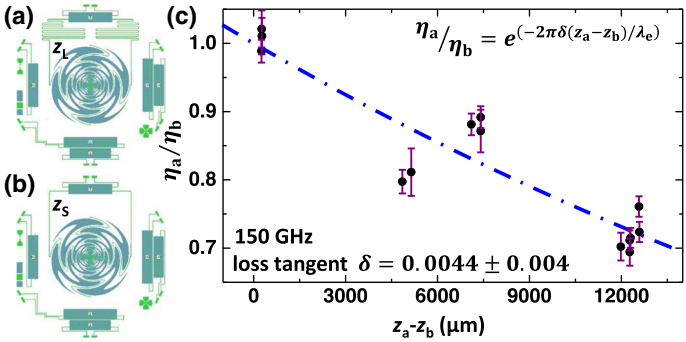

Fig. 4 The testing pixel designs with **a** long and **b** short microstrip lines. **c** Detector optical efficiency ratio (η_a/η_b) as a function of the microstrip length difference ($z_a > z_b$) (Color figure online)

are described in [21]. Comparing efficiency ratios removes any constant losses that are not associated with the microstrip lines, e.g., losses in the antennas and in the coupling scheme used for the measurements. There is no significant difference between the results from pixels with and without inline filters, so the filter loss must be small. We fit the efficiency ratios to a simple microstrip loss model [17]:

$$\eta_a/\eta_b = e^{(-2\pi\delta(z_a-z_b)/\lambda_e)}, (z_a > z_b) \tag{2}$$

where δ is the loss tangent (assuming $\tan(\delta)$ is small, so $\delta \approx \tan(\delta)$) and $\lambda_e \approx 1061\ \mu m$ is the effective wavelength in the microstrip for 150 GHz. The fitting result (blue line in Fig. 4c gives $\delta = 0.0044$ which is about two times higher than the lowest reported values (around 0.002) [17,31]. This corresponds to a microstrip loss of about 24% at 150 GHz in our detector pixels. The optimization is still in progress. We currently concentrate on looking for alternative dielectric layer and improving the microstrip etching process.

4 Conclusion

In this work, we briefly summarized the P_{sat} measurement results of the ten detector wafers in SPT-3G. The thermal conductivity of the bolometer legs on these wafers has been calculated based on these results. We found that the thermal conductivity is very sensitive to the XeF_2 etch used to release the bolometer island, but some control is possible if the width of the residual Si under a SiN cantilever around the legs is used to monitor the release and to choose the end point. We also measured the loss in the microstrip transmission lines and filters on the detector wafers by fabricating test pixels with different microstrip line lengths, and with and without filters. The filters have negligible loss. The microstrip line has a loss tangent of 0.0044, which gives about 24% degradation in optical efficiency in our 150 GHz pixels. These results will help us to optimize the process for future detector design and fabrication.

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