An Active Modulation Scheme to Boost Voltage Utilisation of the Dual Converter with a Floating Bridge

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***Abstract*—This paper proposes a capacitor voltage regulation method for the dual converter with a floating bridge for aerospace applications. This topology has previously been reported, but with a constrained voltage utilisation factor due to the need for capacitor voltage regulations. In this paper, the effect of switching states on the voltage variation of capacitor is quantitatively modelled and an enhanced space vector modulation scheme with current feedback is proposed to achieve an active control of the floating capacitor voltages. This proposed method also allows further exploitation and utilisation of converter voltage. The relationship between the allowed modulation index of dual converter and load power factor is obtained and expressed using a fitted polynomial equation. The advantages of the proposed method include boosted voltage utilisation and superior performance in term of capacitor voltage balance. These advantages have been proven through simulation and experimental results on RL loads as well as with an open-end winding induction motor. The proposed modulation scheme can boost the converter voltage utilisation by at least 10% while achieving full four-level operation. More importantly, the higher available voltage allows extending the constant torque region of the motor, the further beginning of field weakening operation could be postponed.**

***Index Terms*—Dual converter, more electric aircraft, multilevel converters, space vector modulation, voltage regulation**

I. Introduction

As to the push towards more electric aircraft (MEA) intensifies, aerospace systems are undergoing a transition from hydraulic, mechanical, and pneumatic power system into an integrated electric power system [1]–[3]. The MEA initiative can offer significant improvements in terms of the system efficiency and weight loss while reducing costs and emissions [4]–[6].

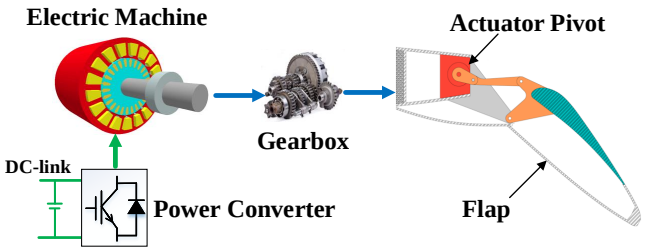

Fig. 1. EMA architecture for secondary flight surface

Considering this scenario, electromechanical actuators (EMAs) for flight control surface represent a key aspect of the MEA concept [7]. Indeed, on modern aircraft, EMAs are progressively replacing the bulky and more expensive hydraulic actuators in order to achieve higher reliability, flexibility and reduced weight [8], [9]. In Fig.1, the basic architecture of an EMA is depicted. The power converter feeds an electric machine, which is mechanically coupled to a step-down gearbox acting on the flight control surface pivot. Since the DC-link voltage is typically fixed for aerospace applications, the base speed of the electrical machine is limited by the supplied voltage from power converter. For this reason, new power converter topologies as well as adapting advanced modulation schemes for increasing the voltage utilisation are being intensively investigated [1]–[3], [10], [11].

Multilevel converters are one of the most promising solutions for MEA drive applications due to their reduced dv/dt, better power quality and lower losses compared to traditional two-level converters. Many multilevel converter topologies have been developed and among them, the dual converter topology has received increasing attention for MEA applications. This mainly results from its redundancy [11], fault-tolerance ability [12], [13] and the possibility of generating more voltage levels [14], [15]. The dual converter employs two standard two-level converters connecting to an open-end winding machine [16], [17]. With the same number of switching devices of a three-level diode-clamped converter, the dual converter can achieve four-level voltages when the voltage ratio of two converters' supplies is 2:1. Apart from that, the dual converter has higher availability since it has 64

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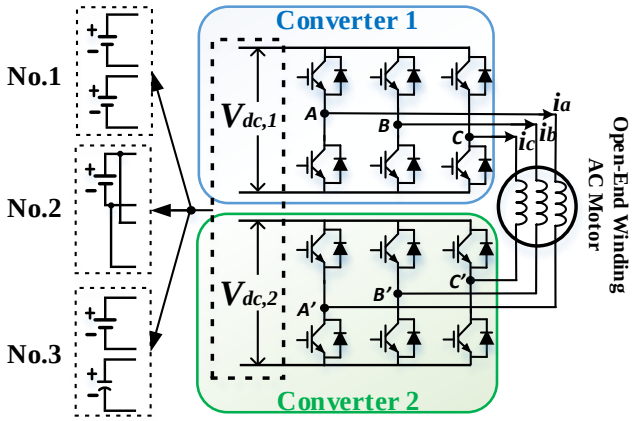

Fig. 2. Three configurations of dual converter topology

switching states while only 27 states can be generated by a three-level diode-clamped converter.

Generally, dual converters have three different configurations according to their power supply arrangement, i.e. the dual converter with two isolated voltage supplies (No.1), with a common DC-link (No.2), and with a DC-link and a floating bridge (No.3), as shown in Fig.2. The first configuration (No.1) is capable of multilevel operation but it needs a bulky transformer to achieve isolation [18], [19]. This would increase the volume and weight of system significantly, which is not desired in aerospace applications. The second configuration (No.2) has the highest degree of fault tolerance while it is suffered from zero-sequence current circulating [20]. In order to suppress zero-sequence current, it may degrade from the multilevel to the two-level operation [14], [18], [19], [21]. The last configuration (No.3) comprises the merits of other two configurations in terms of multilevel output capability due to avoiding zero-sequence current circulation and no need of isolation circuitry since one bridge is floating. This paper will mainly focus on this configuration.

One major challenge of the chosen configuration is to regulate the floating capacitor's voltage to a desired value. In the past decades, various methods to regulate capacitor voltage have been proposed for multilevel converters, such as diode-clamped converters [1], [22], flying capacitor converters [23] and cascaded H-bridge converters [24], [25]. However, there is no comprehensive study regarding the voltage regulation methods for dual converters. In [18], [19], [26], [27], the dual converter is considered as a whole multilevel converter for modulation. The effect of switching states on capacitor voltage is analysed but the direction of phase current is ignored in [18]. More importantly, their analysis neglects the consideration of load power factor angle. The actual current acting on the floating capacitor would vary depending on the power factor angle [27]. According to conclusions in [18], [26], [27], due to the limitation of voltage regulation and achieving multilevel operation at the same time, the voltage utilisation of this dual converter configuration is constrained to the DC-link voltage. Under this condition, the capacitor voltage, which can be substantially beneficial for aerospace applications, is under-utilised.

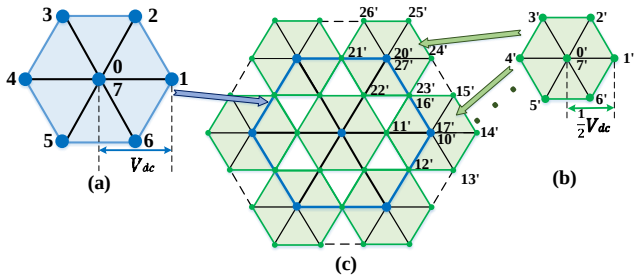

Fig. 3. Space Vector Diagram by (a): CON 1; (b): CON 2; (c): Resulted by dual converter

The other type of voltage regulation method for the chosen configuration is allocating active power flow and reactive power flow into the converter with a dc-link and the converter with a floating capacitor, respectively [28], [29]. The maximum floating capacitor voltage that can be regulated depending on power factor angle is defined in [28]. However, the main drawback of this method is causing undesirable voltage steps in the converter output. Due to the decoupled voltage control for two converters, the resulted voltage on load is unpredictable. These undesirable voltage steps would deteriorate output performance, which makes this configuration less attractive.

In this paper, the voltage regulation method of the dual converter with a floating bridge is comprehensively studied for the first time. The instantaneous currents acting on the capacitor by all applicable switching states are analysed and the impact of load power factor is taken into consideration. Compared to previous voltage regulation methods, the proposed method can boost converter voltage utilisation by at least 10.1% and achieve multilevel operation at the same time. The paper will be organized as follows. The basic operation principle of dual converter is covered in Section II. In Section III, the effect of switching process on the voltage variation of floating capacitor is discussed. After that, the modulation scheme to regulate capacitor voltage along with its regulation capability is proposed in Section IV. The simulation and experimental results on an open-end winding induction motor as well as RL loads are displayed in Section V and Section VI, respectively. The potential benefits resulting from the application of the proposed method to an electric drive for EMA are finally investigated in Section VII. In particular, the advantages associated with the extension of the constant torque region due to the improved voltage utilization is analysed.

II. Principle of Operation

Considering the dual converter with a floating bridge of configuration 2 (No.2) in Fig.2, the voltage ratio ($V_{dc,1}/V_{dc,2}$) of the two voltage sources is selected to be 2:1, in order to achieve a four-level operation. As shown in Fig.2, Converter 1 (CON 1) is supplied by a DC-link with a voltage of V_{dc} and Converter 2 (CON 2) is powered by a floating capacitor at the voltage of $\frac{1}{2}V_{dc}$.

Fig.3 shows the voltage vector diagram of a dual converter. One dot represents one switching vector in Fig.3 and it can be expressed by several switching states, which are known

as redundant states. For a two-level converter as shown in Fig.3 (a) and (b), the 8 switching states (0-7 or 0'-7') form 7 different vectors in the plane. Since the dual inverter employs two 2-level inverters, there are $8^2 = 64$ applicable switching states.

For the dual inverter, the phase voltage applied to the electrical loads is the voltage difference produced by the two converters (CON 1 in Fig.3 (a) and CON2 in Fig.3 (b)). The resulted space vector diagram in Fig.3 (c) can be drawn as small hexagons in Fig.3 (a) around vectors on the large hexagon in Fig.3 (b). The voltages applied to the supplied load thus can be represented with the switching states of both converters. For instance, switching state (15') represents '1'(100) for CON 1 and '5'(001) for CON 2. With the voltage ratio of 2:1, Fig.3 (c) demonstrates that this dual inverter produces 37 vectors from 64 switching states and the phase voltage applied to the electrical machine is a 4-level voltage.

III. Effect of the Switching Vector

A. Types of Switching Vector

During the modulation process, the phase current i_a, i_b and i_c as shown in Fig.2 would charge or discharge the floating capacitor (FC) and result in a voltage variation. The 37 space vectors shown in Fig.3 (c) can be categorized into three different types: type I for the vector with redundancy states that make the phase current act on both the positive and negative polarity of the FC, type II for the vector only have either one case of current flow and type III for the vector has no effect on the voltage variation of FC.

These three types of space vector are demonstrated in Fig.4. The line colour in Fig.4 implies the flow path of different phase current. Green colour represents the path of current i_a, red indicates the path of current i_b and blue shows the path of current i_c. In Fig.4 (a) and (b), the type I vector that has switching states (16') and (23') are shown. The current i_b flows into the '+' polarity of FC in the case of (23') where flows into the '-' polarity of FC in the state of (16'). The former case is denoted as '$+i_b$' whereas the latter one is represented by '$-i_b$'. This vector belongs to type I because it has redundancy states that could make phase current act on both the positive and negative polarity of the FC. In contrast, the vector with state (14') in Fig. 4 (c) is categorised into type II since it only could make the current i_a act on the negative pole of FC. There is no current acting on the FC when the type III vector is applied, such as (27') in Fig. 4 (d). Under this condition, the FC voltage would remain constant.

Following this classification manner, 37 switching vectors of the dual inverter are denoted in sequence in Fig.5. The summary of three vector types I, II, III and their corresponding current flow into FC I_{fc_typeI}, I_{fc_typeII}, $I_{fc_typeIII}$ are detailed in Table I. The sign '$\pm$' means the phase current could act on both the positive and negative polarity of the FC.

B. Phase Current Act on FC

Within the hexagon of CON 1 in blue line in Fig.5, space vectors are associated with type I and III. The type III switching states are essentially the same ones of CON 1. The

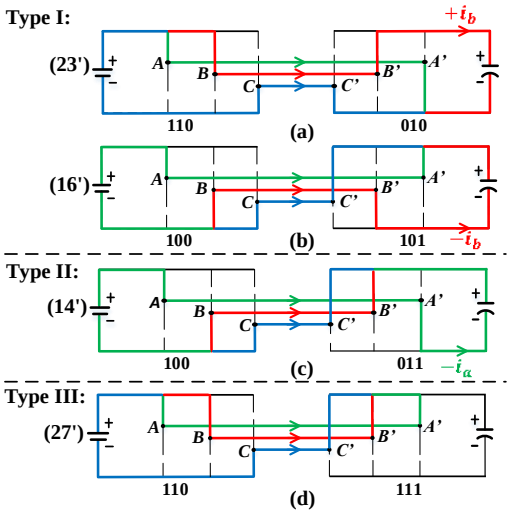

Fig. 4. Cases of different phase current act on floating capacitor

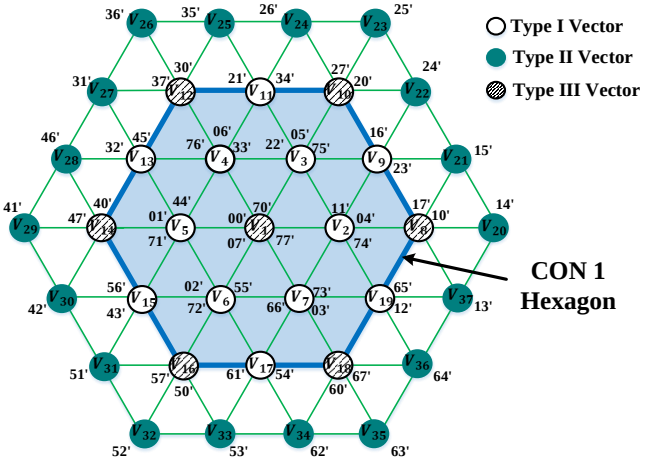

Fig. 5. Types of vector for the dual converter

type II vector locates on the outmost of vector diagram. In the following part, the current acting on the FC within CON1 hexagon and the area beyond that are discussed in sequence. Due to the symmetry of the three-phase system, the Sector I of space vector diagram by dual converter is considered, as displayed in Fig.6. Generally, the objective of converter modulation process is to synthesise the demand voltage vector V_{ref}. The synthesis process is based on 'voltage-second balancing' principle, which can be expressed by (1), where V_0, V_1, V_2 are three applied space vectors and d_0, d_1, d_2 are their corresponding duty cycle of a switching period T_s, respectively. Additional, the definition of Modulation Index (M.I.) is given in (2), where $V_{dc,overall}$ refers to the sum of voltages of dual converter $V_{dc,1}$ and $V_{dc,2}$ in Fig.2.

$$\begin{aligned} V_{ref} &= V_0 * d_0 + V_1 * d_1 + V_2 * d_2 \\ 1 &= d_0 + d_1 + d_2 \end{aligned} \tag{1}$$

$$M.I. = \sqrt{3} * V_{ref} \Big/ V_{dc,overall} \tag{2}$$

TABLE I
CURRENT ACT ON THE FC BY THREE TYPES OF VECTOR

Sector	Vector Type (current flow I_{fc})		
	I (I_{fc_typeI})	II (I_{fc_typeII})	III ($I_{fc_typeIII}$)
1	$V_2(\pm i_a)$, $V_3(\pm i_c)$, $V_9(\pm i_b)$	$V_{20}(-i_a)$, $V_{21}(+i_c)$, $V_{22}(-i_a)$, $V_{23}(+i_c)$	$V_1(0)$, $V_8(0)$, $V_{10}(0)$
2	$V_3(\pm i_c)$, $V_4(\pm i_b)$, $V_{11}(\pm i_a)$	$V_{23}(+i_c)$, $V_{24}(-i_b)$, $V_{25}(+i_c)$, $V_{26}(-i_b)$	$V_1(0)$, $V_{10}(0)$, $V_{12}(0)$
3	$V_4(\pm i_b)$, $V_5(\pm i_a)$, $V_{13}(\pm i_c)$	$V_{26}(-i_b)$, $V_{27}(+i_a)$, $V_{28}(-i_b)$, $V_{29}(+i_a)$	$V_1(0)$, $V_{12}(0)$, $V_{14}(0)$
4	$V_5(\pm i_a)$, $V_6(\pm i_c)$, $V_{15}(\pm i_b)$	$V_{29}(+i_a)$, $V_{30}(-i_c)$, $V_{31}(+i_a)$, $V_{32}(-i_c)$	$V_1(0)$, $V_{14}(0)$, $V_{16}(0)$
5	$V_6(\pm i_c)$, $V_7(\pm i_b)$, $V_{17}(\pm i_a)$	$V_{32}(-i_c)$, $V_{33}(+i_b)$, $V_{34}(-i_c)$, $V_{35}(+i_b)$	$V_1(0)$, $V_{16}(0)$, $V_{18}(0)$
6	$V_7(\pm i_b)$, $V_8(\pm i_a)$, $V_{19}(\pm i_c)$	$V_{35}(+i_b)$, $V_{36}(-i_a)$, $V_{37}(+i_b)$, $V_{20}(-i_a)$	$V_1(0)$, $V_{18}(0)$, $V_8(0)$

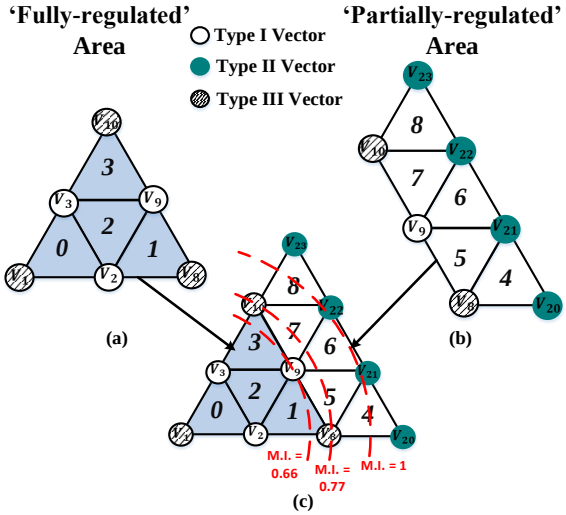

Fig. 6. Space vector diagram within a) 'Fully-regulated Area' of Sector I; b) 'Partially-regulated Area' of Sector I; c) Section I

For the purpose of minimising output harmonic distortion, the nearest three vectors (NTV) method is adopted. For instance, if reference vector locates within region 2 in Fig. 6 (a), the nearest three vectors V_2, V_8, V_9 are applied in (1). In Fig.6 (a) of region 0-3, each has at least one type I vector and no existence of type II vector. The current flow to floating capacitor (FC) can be can be modelled as shown in (3), where the current I_{fc_typeI} can be found in the Table I and d_{typeI}, $d_{typeIII}$ are the duty cycle for type I and type III vector, respectively.

$$Region0-3: I_{fc} = d_{typeI} * (\pm) I_{fc_typeI} + d_{typeIII} * 0 \quad (3)$$

From (3), it is obvious that the sign of current flow into FC can be selected flexibly thus the area in Fig.6 (a) is called 'Fully-regulated Area'. If the reference vector operates beyond the CON 1 hexagon in Fig.5, the type II vector is unavoidably involved. In Fig.6 (b), there are at least one type II vector in each region and even absence of type I vector for region 4 and 8. For this case, the current flow to floating capacitor (FC) can be modelled by (4) and (5), where current I_{fc_typeII} can be found in the Table I and d_{typeII} is the duty cycle for type II vector.

$$Region5-7: I_{fc} = d_{typeI} * (\pm) I_{fc_typeI} + d_{typeII} * I_{fc_typeII} \quad (4)$$

$$Region4, 8: I_{fc} = d_{typeII} * I_{fc_typeII} \quad (5)$$

From (4) and (5), it can be deduced that due to the existence of type II vector, then the current act on the FC cannot be completely manipulated, especially for region 4 and 8 in (5). Therefore, the area in Fig.6 (b) is denoted as 'Partially-regulated Area'.

C. Charge Variation of FC

When a switching state (mn') is applied, the variation of FC voltage $\Delta V_{fc_mn'}$ and charge $\Delta Q_{fc_mn'}$ can be represented, where C is the capacitance of FC and $T_{mn'}$ is the switching time of state (mn').

$$\Delta Q_{fc_mn'} = C * \Delta V_{fc_mn'} = \int_0^{T_{mn'}} I_{fc}(sector)\, dt \quad (6)$$

Accordingly, the charge variation of FC by three types of vector ΔQ_{fc_typeI}, ΔQ_{fc_typeII}, $\Delta Q_{fc_typeIII}$ can be expressed by (7) where T_{typeI} (= d_{typeI}*T_s), T_{typeII} (= d_{typeII}*T_s) are the switching time for type I and type II vector, respectively.

$$\begin{aligned} \Delta Q_{fc_typeI} &= \int_0^{T_{typeI}} I_{fc_typeI}(sector)\, dt \\ \Delta Q_{fc_typeII} &= \int_0^{T_{typeII}} I_{fc_typeII}(sector)\, dt \\ \Delta Q_{fc_typeIII} &= 0 \end{aligned} \quad (7)$$

Recent research related to the dual converter only considered the movement of reference vector within the 'Fully-regulated Area' [18], [26], [27]. This refers to the CON 1 hexagon in Fig.5, which means only the main DC-link voltage, 66% of the overall voltage, is utilised. It cannot be denied that the regulation capability is constrained within 'Partially-regulated Area'. In particular, an active modulation scheme that requires the feedback of phase current is necessary.

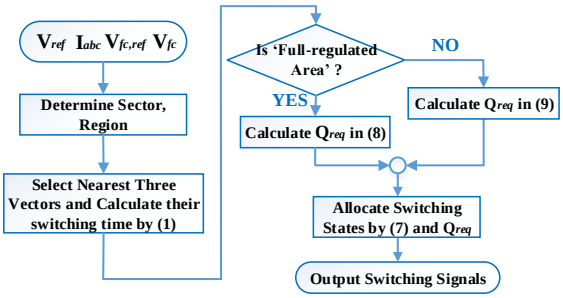

Fig. 7. Flowchart of proposed regulation method

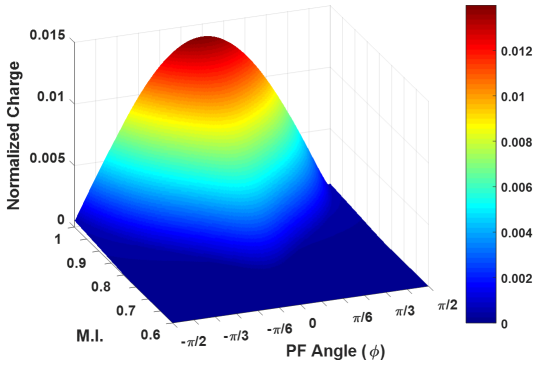

Fig. 8. Maximum Charge variation of FC over a switching period

IV. Proposed Voltage Regulation Method

A. Working Principle

Regarding 'Fully-regulated Area', the voltage of FC could be fully regulated since the sign of current flow into FC can be chosen according to the regulation need. The required charge to balance capacitor voltage is represented by 'Q_{req}' in (8) when reference vector locates within 'Fully-regulated Area' and where V_{fc}, $V_{fc,ref}$ is the FC voltage and the reference FC voltage, respectively.

$$Q_{req} = C * (V_{fc} - V_{fc,ref}) \tag{8}$$

Therefore, the switching states' allocation of type I vector can be determined based on (7) and (8). Once the reference vector enters 'Partially-regulated Area', the type II vector is involved and its charge variation on FC can be calculated by (7). Then, in this case, Q_{req} can be expressed by (9).

$$Q_{req} = C*(V_{fc}-V_{fc,ref}) + \int_0^{T_{typeII}} I_{fc_typeII}(sector)\, dt \tag{9}$$

In summary, the proposed FC voltage regulation mechanism can be demonstrated by the flowchart shown in Fig.7. Initially, the nearest three vectors (NTV) and their switching time are obtained after the sector and region of V_{ref} is determined. The required charge 'Q_{req}' can be calculated by (8) or (9) depending on the V_{ref} is in 'Fully-regulated Area' or 'Partially-regulated Area'. Based on the overall consideration of corresponding current flow in Table I with the information of current I_{abc}, the switching states of type I vector can be allocated by (7) to compensate the Q_{req}. Finally, the switching signals for dual inverter can be generated.

B. Resulted Charge Variation of FC

Following the proposed modulation method depicted in Fig.7, the maximum charge variation over a switching period by the proposed method is showed in Fig.8. The x-axis is the modulation index (M.I.) from 0.6 to 1 and y-axis is power factor (PF) angle from $-\pi/2$ to $\pi/2$.

The charge is normalised by the phase current amplitude. In Fig.8, it can be observed that the charge variation on FC is generally low at lower modulation indexes region and large at higher modulation indexes region. In particular, the charge variation of FC over a switching period is zero when M.I. is smaller than 0.66, which is denoted as 'Fully-regulated area' in Fig.6. Additionally, the charge variation is relatively large when power angle is around 0, i.e. power factor is 1, whereas relatively small when power angle is around $-\pi/2$ and $\pi/2$, i.e. power factor is 0. In summary, the allowable modulation index may be increased when power factor decreases.

C. Voltage Utilisation Boundary

As mentioned above, manipulating two redundant switching states of type I vector defines the voltage regulation capability. When the reference vector enters 'Partially-regulated Area', the type II vector is introduced. The voltage regulation boundary of the proposed method is determined by the comparison of the absolute value of resulted charge by type I vector $|Q_{fc_typeI}|$ and by type II vector $|Q_{fc_typeII}|$ over a fundamental cycle of the reference vector V_{ref}, as shown in below:

$$\begin{aligned} |Q_{fc_typeI}| &= \sum \int_0^{2\pi} \left| \int_0^{T_{typeI}} I_{fc_typeI}\ (sector) dt \right| d\theta \\ |Q_{fc_typeII}| &= \left| \sum \int_0^{2\pi} \left(\int_0^{T_{typeII}} I_{fc_typeII}\ (sector) dt \right) d\theta \right| \end{aligned} \tag{10}$$

For a certain modulation index (M.I.) and a power factor (PF) angle, if $|Q_{fc_typeI}|$ is larger than $|Q_{fc_typeII}|$, this means the charge caused by type II vector can be fully compensated by the charge resulted from type I vector over a fundamental cycle. In this case, the voltage level of FC can be maintained. Otherwise, if $|Q_{fc_typeI}|$ is smaller than $|Q_{fc_typeII}|$, the FC voltage could not be regulated. For instance, when M.I. is between 0.66 and 0.77 as shown in Fig.6 (c), the reference vector would pass by Region 1, 5, 6, 7, 3 of Sector I in sequence. Therefore, the involved vectors are V_2, V_9, V_3 of type I vector and V_{21}, V_{22} of type II vector. Their resulted charges on the FC over Sector I could be derived by (11) where θ is the angle of reference vector. The switching time T_{V_2}, T_{V_9}, T_{V_3}, $T_{V_{21}}$, $T_{V_{22}}$ are simply obtained

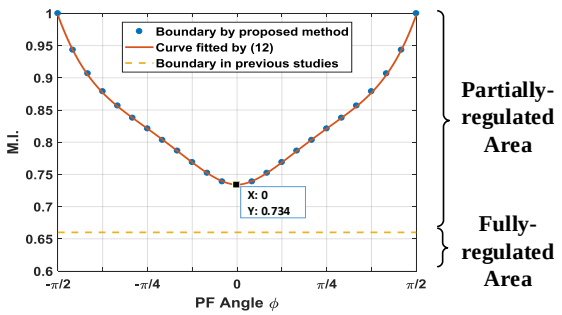

Fig. 9. The controllable area of FC voltage verse power factor angle

by multiplying their corresponding duty cycles through (1) by a switching period T_s.

$$|Q_{fc_typeI}| = \int_0^{\frac{\pi}{3}} \left| \int_0^{T_{V_2}} i_a \, dt \right| d\theta + \int_0^{\frac{\pi}{3}} \left| \int_0^{T_{V_9}} i_b \, dt \right| d\theta + \int_0^{\frac{\pi}{3}} \left| \int_0^{T_{V_3}} i_c \, dt \right| d\theta \quad (11)$$

$$|Q_{fc_typeII}| = \left| \int_0^{\frac{\pi}{3}} \left(\int_0^{T_{V_{21}}} i_c \, dt \right) d\theta + \int_0^{\frac{\pi}{3}} \left(\int_0^{T_{V_{22}}} -i_a \, dt \right) d\theta \right|$$

Fig.9 displays the boundary between allowable M.I. and PF angle (ϕ) by the proposed voltage regulation method in the blue dots. In particular, the minimum value of 0.734 is occurred at the PF angle of 0 since $|Q_{fc_typeII}|$ would exceed $|Q_{fc_typeI}|$ once the M.I. increases beyond that threshold value. In addition, the red curve displays that the analytical boundary is fitted by using 'curve fitting' toolbox inside Matlab. The fitted equation can be written as:

$$M.I.(\phi) = 0.133 * |\phi| - 0.353 * (|\phi|)^2 + 0.33 * (|\phi|)^3 + 0.005 * (|\phi|)^4 + 0.734 \quad (12)$$

Equation (12) provides a mathematical approach to derive the maximum voltage utilisation according to load PF factor. Regarding previous studies, the voltage utilisation of the dual converter with a floating bridge is constrained as 66% of the overall voltage. In contrast, as shown in Fig.9, the minimum M.I. by the proposed method is 0.734 at 0 PF angle (unity PF) and the maximum value is 1 at $\pm\pi/2$ PF angle (zero PF). This means the voltage utilisation of this topology can be increased by at least 10.1%. Additionally, the method proposed in [18] is considered as the 'benchmark method' and would be chosen to compare with the proposed method in the following.

V. Simulation Results

A simulation model of motor drive system with dual converter for aerospace applications is built within PLECS (standalone) environment. The detailed parameters of induction machine and power converter are shown in Table II. The deadtime is selected since it is the minimum value allowed by the power converters employed in the practical experiment. In order to minimize the potential affect of deadtime on the modulation process and FC charging and discharging, the switching frequency of 5kHz is chosen thus deadtime only occupies approximately 2% of one switching cycle (i.e. 200 μs). The system performance by the proposed modulation scheme and the benchmark method are simulated and compared. A guideline of FC sizing for a given voltage ripple requirement is presented.

TABLE II
Machine and Converter Parameters

Power Converter		Induction Motor	
Main DC-link voltage	540 V	Stator resistance	1.2 Ω
FC voltage	270 V	Rotor resistance	1.01 Ω
Main DC-link capacitance	1250 μF	Rated current (RMS)	14.23 A
FC Capacitance	3250 μF	Power factor (at full load)	0.80
Switching frequency	5 kHz	No-load current (RMS)	5.77 A
Deadtime	4.1 μs	Power factor (at no load)	0.03

A. Control Schematic

Fig.10 depicts the closed-loop control schematic of an open-end drive system. This system consists of the main converter (CON 1) supplied by a DC-link, sub converter (CON 2) supplied by an FC, and an open-end winding induction machine connected mechanically with a DC machine through a shaft. The elegant field orientation control is applied where 'Nested loop' of outer speed and flux control with inner current control loop is adopted. The speed control loop is designed for minimizing the speed error and it provides the reference value of stator q-axis current I^*_{sq}, which represents one of the two inputs of the q-axis current controller ('Inner Current Control' in Fig.10). The q-axis current controller is a proportional-integral (PI) controller that generates the stator q-axis reference voltage V^*_{sq}. Considering the flux control loop (i.e. 'Outer Flux Control' of Fig.10), its output consists in the reference d-axis current I^*_{sd}, which is applied as input to the d-axis current controller ('Inner Current Control' in Fig.10). The latter provides the output of stator d-axis voltage reference V^*_{sd}. Both the voltage reference signals in the rotating dq frame (i.e. V^*_{sq} and V^*_{sd}) are referred in the stationary $\alpha\beta$ reference frame using the stator flux electric angle θ_e. Hence, the reference voltage vector V_{ref} is generated at the output of the coordinate transformation block and it is employed by the SVM modulator for modulation purpose.

The SVM modulator in grey colour in Fig.10 is the core part of whole control system. It take the responsibilities of modulating reference vector and achieving voltage regulation of FC at the same time. The switching vectors are derived from the modulation process and switching states are allocated according to the need of regulating FC voltage, as described in Fig.7.

In Fig.11, the performance of dual converter drive system using the proposed method in blue colour and the bench-

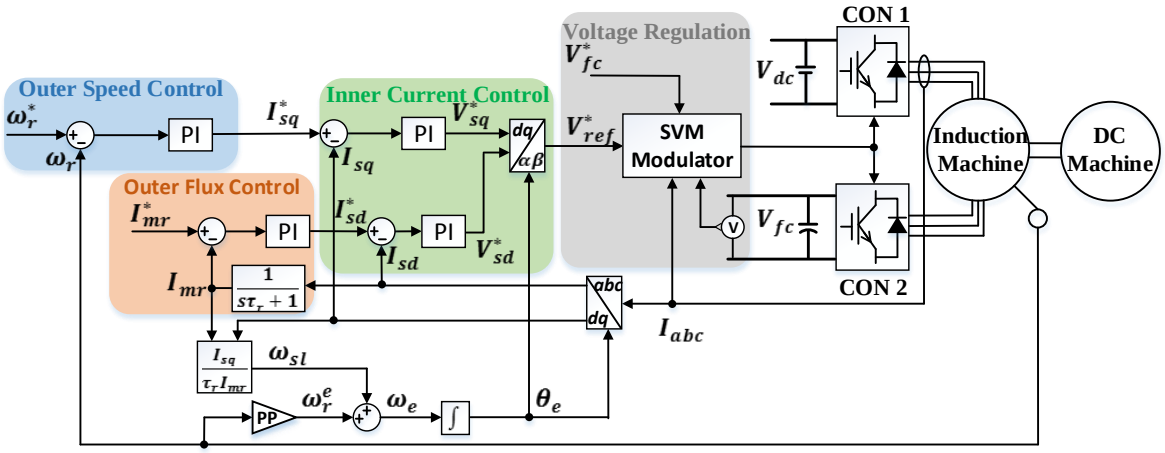

Fig. 10. Control schematic of the motor drive system

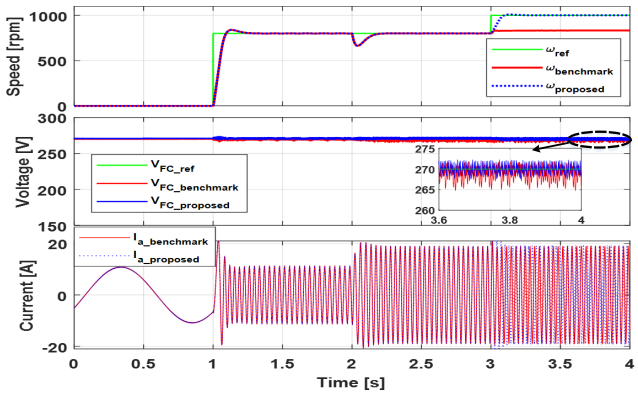

Fig. 11. Simulated drive performance comparison at 72 N*m load torque

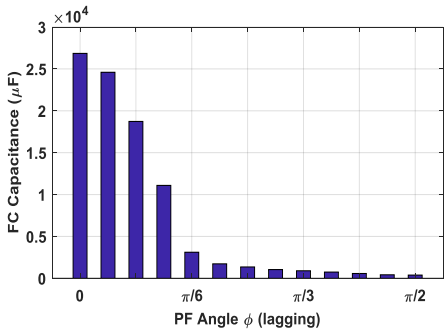

Fig. 12. Recommended capacitance size for a specified voltage ripple demand

mark method in red colour is demonstrated for comparison. The simulation condition is to give a step speed reference ω_{ref}=800rpm at 1s, and a step load torque T_L=72 N*m at 2s. In the first subplot of Fig.11, it displays that the speed performance is nearly matched by two methods before 2s. After that, the speed reference ω_{ref} is increased to 1000rpm at 3s. The drive system by the proposed method can follow the speed while by the benchmark method could not. Since speed is proportional to the supplied voltage, this validates that the proposed method can boost voltage utilisation compared to using the benchmark method. Regarding FC voltage in the second subplot of Fig.11, the proposed method shows superior performance over the benchmark method in terms of more accurate and stable voltage regulation of FC. The mean value of FC voltage is 269.90V and the peak-to-peak ripple is 4.68V. In contrast, mean value of FC voltage and the peak-to-peak ripple is 268.32V and 7.25V by the benchmark method, respectively. Due to superior performance of voltage regulation, the current THD (total harmonic distortion) using the proposed method is 3.2%, which is improved slightly compared to 3.4% by using the benchmark method as shown in the third subplot of Fig.11.

B. Sizing of FC

If the amplitude of phase current I_{phase} is known, the size of floating capacitor (FC) 'C_{req}' can be derived by (13) for a given voltage ripple requirement ΔV_{max}. One essential item in this equation is the normalised charge variation Q_{norm}, which can be found in Fig.8.

$$C_{req} = \frac{Q_{norm} * I_{phase}}{\Delta V_{max}} \tag{13}$$

Equation (13) should provide sufficient guidelines to size the FC when the desired voltage requirement and operation condition is informed. For instance, the peak-to-peak voltage ripple requirement is set to 2% of FC voltage, which is 5.4V for 270V. If the modulation index is 0.76 and the maximum current I_{phase} is 20.1A, the recommended FC sizing C_{req} is depicted in Fig.12. For a fully-loaded machine with load power factor of 0.80 as indicated in Table II, the capacitor capacitance should be chosen at least $3022\mu F$. The chosen capacitance in the simulation as well as experiment is 3250 μF as indicated in Table II, which is slightly larger than $3022\mu F$. From the third subplot of Fig.11, the peak-to-peak ripple of FC is 4.68V that accounts for 1.73% of 270V. This result meets the requirement of 2% FC voltage.

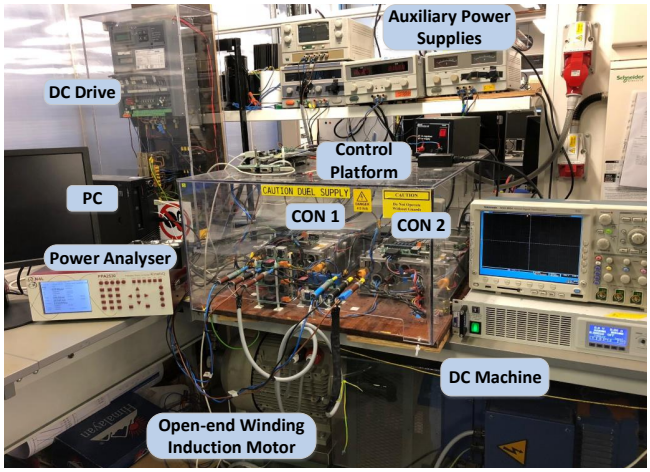

Fig. 13. Experimental rig setup

VI. Experimental Results

In this section, the motor drive prototype as shown in Fig.13 is carried out in the real experiment. The converter voltage utilisation and FC performance by the proposed method and the benchmark method are compared. In particular, the analytical relationship of converter voltage utilisation verse load power factor angle in Fig.9 is tested. Since the power factor (PF) of induction machine is relatively low, the validation experiment for high PF condition is conducted by a series of RL loads.

In Fig.13, the chosen power converters are 'off-the-shelf' two-level converters produced by SEMIKRON. These converters have integrated gate drivers with DC-side capacitor of 1250μF capacitance, RC snubber, and input-output common mode choke. Additionally, the DC-side of converter is paralleled with Y-capacitor in order to suppress EMI. The control platform consists of a Digital Signal Processor (DSP) and a field-programmable gate array (FPGA) board. The DC machine is connected mechanically to the open-end winding induction motor to act as a load. It is operated under torque control using an industrial DC drive, thus variable load torque on the induction motor is applicable. The power analyser N4L-PPA2530 is applied to measure the load power factor angle.

A. Performance Comparison

In Fig.14, the motor drive performance comparison by the proposed method and the benchmark method are displayed. The test condition is setting reference speed to 800 rpm then increasing to 1000 rpm at 1s. In the first subplot of Fig.14, after 1s, the drive system by the proposed method in red line still can follow reference speed in green line but the drive system by the benchmark method in blue line could not. The reason is revealed in the second subplot of Fig.14. The speed reference of 1000 rpm requires higher voltage supply than 66% of the overall voltage. This validates that the proposed modulation method can boost converter voltage to supply on the electric loads. In the third subplot of Fig.14, the measured FC voltage by the benchmark method in blue colour has a peak-to-peak ripple of 8.6V and the average value is around 266.7V. It is obvious that the proposed modulation scheme in red colour

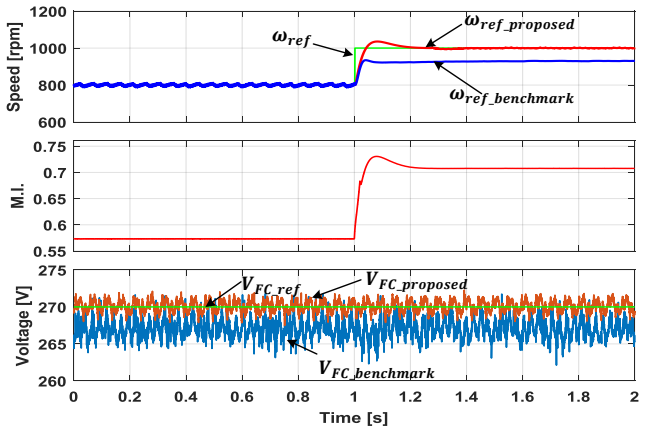

Fig. 14. Experimental drive performance comparison when PF factor = 0.5 and the capacitance of FC is 3250μF

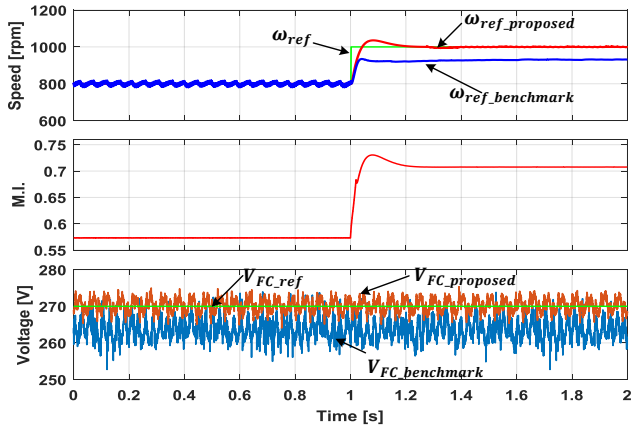

Fig. 15. Experimental drive performance comparison when PF factor = 0.5 and the capacitance of FC is 1250μF

presents superior FC voltage regulation performance with 4.3V ripple and the mean value of 270.0V approximately. This indicates the size of the FC could be smaller for a given voltage ripple requirement if the proposed modulation scheme is applied, which agrees with the results in the simulation.

In addition, another experimental comparison is carried out by adopting lower capacitance of FC (i.e. 1250μF). Besides that, the test conditions maintain the same as previous. Compared to Fig.14, peak-to-peak ripples of FC voltage in Fig.15 have significantly increased. The measured FC voltage by the benchmark method has a peak-to-peak ripple of 19.8V and the average value is around 262.4V. In contrast, the proposed modulation scheme still presents superior FC voltage regulation performance with 9.9V ripple and the mean value of 269.8V approximately.

B. Boundary Validation

In order to validate the analytical voltage regulation capability under specific power factor, an open-loop V/f control is adopted. During test, the magnitude of voltage reference is increased gradually. When the FC voltage starts to reduce below the reference value, this means that the maximum allowed modulation index was achieved. Fig.16 displays results

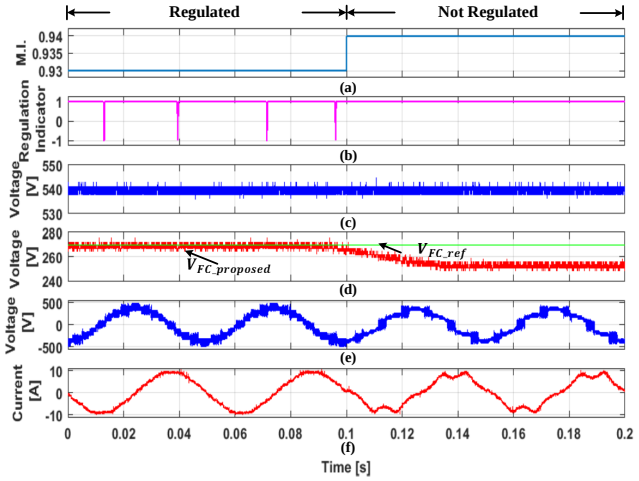

Fig. 16. Motor drive performance a) M.I; b) Regulation indicator; c) DC-link voltage; d) FC voltage; e) Phase voltage; f) Phase current when PF = 0.03

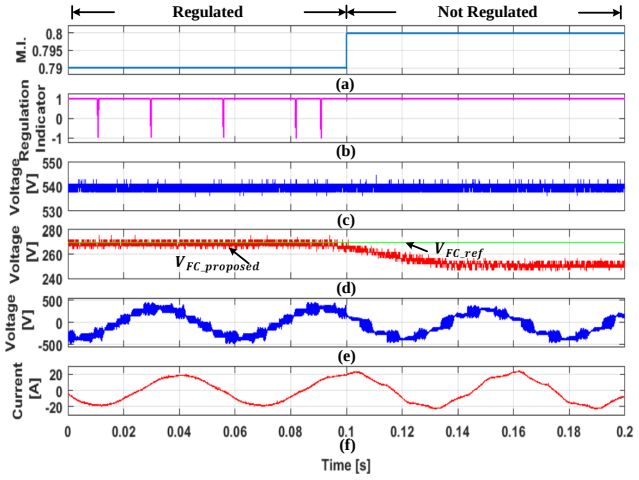

Fig. 17. Motor drive performance a) M.I; b) Regulation indicator; c) DC-link voltage; d) FC voltage; e) Phase voltage; f) Phase current when PF = 0.80

when the induction motor is operated under no load where RMS of phase current is 5.77A. The experimental results for a fully-loaded induction motor with phase current of 14.23A (RMS) are reported in Fig. 17. These two load conditions are corresponded to load power factor of 0.03 and 0.80 as shown in Table II, respectively.

In Fig.16 (a), the dual inverter works at 0.93 modulation index (M.I.) from 0 to 0.1s and then it is increased to 0.94 at 0.1s. The regulation indicator is referred to 'Q_{req}' in (8) and (9). It displays '1' as '$Q_{req} < 0$' while '-1' if '$Q_{req} > 0$'. During 0 - 0.1s, the regulation indicator in Fig.16 (b) is '1' for the most of time duration while '-1' for small portion of time duration. This means the capability of capacitor voltage regulation closes to its limitation. The Fig.16 (d) indicates the voltage of floating capacitor can be regulated around reference value (270 V) at M.I. = 0.93. In addition, the phase voltage in Fig.16 (e) has distinct 7-level, which is characteristic of expected 4-level inverter performance. However, when M.I. rises up to 0.94, the regulation indicator is '1' constantly which

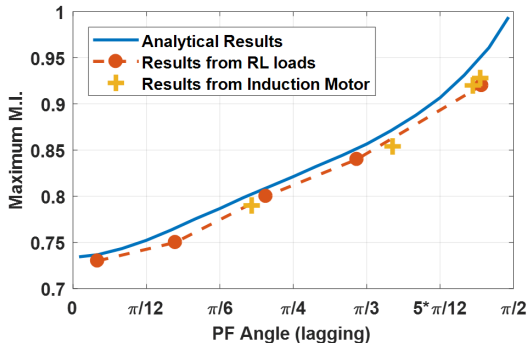

Fig. 18. Comparison of voltage capability results

TABLE III
THE BASE SPEED COMPARISON

	The Benchmark Method		The Proposed Method	
Load Condition	Max. M.I.	Base Speed	Max. M.I.	Base Speed / (boosted)
No load	0.66	987 rpm	0.96	1434 rpm / (45.3%)
Fully load	0.66	839 rpm	0.79	1018 rpm / (21.3%)

means the dual inverter has operated beyond its regulation capability. As expected, the capacitor voltage is decreasing below the level of reference voltage. Consequently, undesired phase voltage steps and distorted phase current waveform can be demonstrated in Fig.16 (e) and (f), respectively. Regarding the fully-loaded induction motor, the experiment follows the same manner as for no-load test. Fig.17 display the maximum modulation index of inverter is 0.79 at the load power factor of 0.80.

In Fig.18, the results of voltage utilisation verse load power factor from experimental results are recorded and compared with outcomes in the analytical study. The experimental results are slightly smaller than the analytical boundary of voltage regulation capability, but these two outcomes agree generally. This mismatch may result from dead-time thus a more advanced dead-time compensation is worthy to develop in the further studies.

VII. IMPLEMENTATIONS OF THE PROPOSED METHOD ON AN EMA ELECTRIC DRIVE

As previously highlighted, one of the key benefits arising from the adoption of the proposed method consists in a better utilization of the available DC-link voltage. This advantage can be exploited in EMA aerospace applications where the DC-link voltage is fixed and field weakening operations are often required for motors [30]. This indicates that they need to operate beyond the base speed, which is related to the voltage supplied by power converter. The higher available voltage resulting from the employment of the proposed method allows extending the torque constant region of the motor (i.e. higher value of base speed). Thus, the beginning of the field weakening operations is postponed and the rated torque can be developed on a wider range of speed.

In Table III, the comparison between the benchmark and the proposed methods is reported in terms of base speed

improvement for the machine under test. The base speed refers to the maximum speed that machine could operate without reducing the field current (i_d). As shown in Table III, the maximum modulation index of dual converter is 0.66 by the benchmark method, despite the load condition. In contrast, the proposed method can make the dual converter to supply 96% and 79% of the overall voltage when the machine works at no-load and fully-load condition, respectively. This significant enhancement of the voltage utilisation reflects on the machine's base speed. For a no-load machine, the base speed can be boosted by 45.3% if the proposed modulation scheme is utilised. In addition, the improvement percentage of base speed is 21.3% for a fully-loaded machine, as indicated in Table III. This boosted base speed could allow the machine to minimize its weight and volume considerately, which is critical for aerospace applications.

VIII. Conclusion

In this paper, the dual converter with a floating bridge for aerospace applications is studied and an implementation instance of flight surface control on MEA is given. In order to regulate the voltage of FC, the instantaneous current that acts on the FC is analysed. After a quantified modelling of charge variation of FC by switching states, an active space vector modulation scheme with current feedback is proposed. In particular, the capability of regulating the floating capacitor voltage is defined and a fitted polynomial equation is derived to express this relationship. Compared to the benchmark method that previously presented, benefits of the proposed modulation scheme that have been validated in both simulation and experiment include:

1) Superior FC voltage regulation performance in term of more accurate average value and less voltage ripple;
2) Boosted base speed for electric machines with a fixed DC link voltage;
3) Boosted voltage utilisation of converter by at least 10.1% and achieving four-level operation;

Using this modulation scheme, the advantages of dual inverter with a floating bridge can be fully exploited and make it more competitive among other multilevel inverter topologies for aerospace applications.

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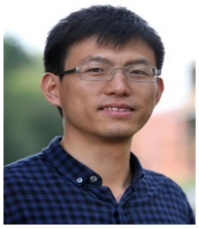

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