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The fabrication of nanoscale Bi_2Te_3/Sb_2Te_3 multilayer thin film-based thermoelectric power chips

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Abstract

In this paper, we report our method of fabricating nanoscale multilayered Bi_2Te_3/Sb_2Te_3 thin film-based integrated thermoelectric devices, and detail the voltage and power produced by the device. The multilayered Bi_2Te_3/Sb_2Te_3 thin film was grown via e-beam evaporation; it had 20 alternating Bi_2Te_3- and Sb_2Te_3-layers, each layer being 1.5 nm thick. We characterized the film using high-resolution transmission electron microscopy (HRTEM), revealing its excellent cross-sectional structure without any obvious interface defects. The Bi_2Te_3/Sb_2Te_3 multilayer films were investigated by synchrotron x-ray scattering. An integrated device including 128×256 thermoelectric elements was fabricated from the multilayered film. An open-circuit voltage of 51 mV and a maximum power of 21 nW were produced from this 30 nm-thick Bi_2Te_3/Sb_2Te_3 multilayer TE device. We found that the nanoscale multilayer structure significantly affects the voltage and power produced. The fabrication of the integrated thermoelectric devices is compatible to that of generating standard integrated circuits (ICs), and is scalable for producing higher voltage and power, or achieving solid-state cooling for on-chip applications.

Key words: Bi_2Te_3/Sb_2Te_3 multilayer thin films, thermoelectric device, microfabrication

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I. INTRODUCTION

Thermal-to-electrical energy conversion and solid-state cooling have been widely investigated in thermoelectric (TE) thin-film materials and devices [1-12]. The thermoelectric effect is the appearance of an electric field along a temperature gradient established in a material. The inverse effect, the so-called the Peltier effect, can be used for refrigeration. Thermoelectric generators (TEGs) and thermoelectric refrigeration devices (TRDs) are extremely simple, and their operation does not need any moving parts or bulk fluids. The performance of these TE devices can be much superior to their vapor- and gas-based-counterparts, offering promising prospects for fully solid-state and environmentally benign energy- conversion (producing clean energy), or for cooling. The performance of TE devices is quantified by a dimensionless figure-of-merit, ZT, where Z is a measure of a material's thermoelectric properties, and T is the absolute temperature. ZT is defined as $ZT = S^2\sigma T/\kappa$, where σ is the electrical conductivity, κ is the thermal conductivity, and S is the Seebeck coefficient. The value of ZT can be increased in three interdependent ways: Increase σ, decrease κ, and increase S. Notably, good thermoelectric materials require an unusual simultaneous combination of electrical- and thermal-properties: High electrical conductivity σ, high Seebeck coefficient S, and low thermal conductivity κ. Nanostructured materials can have thermoelectric merit significantly greater than the same bulk materials, due to the quantum confinement of electrons, as well as to their higher impedance to phonon transport [13-17]. The overlap of the electron quantum states of the nanostructures assure anisotropic electron conduction, and a high Seebeck coefficient, while, at the same time, reducing thermal conductivity by scattering phonons from the nanostructures.

Bismuth telluride (Bi_2Te_3) and antimony telluride (Sb_2Te_3) have been investigated extensively investigated [18-25], and were found to be excellent thermoelectric materials for applications in generating thermoelectric power and solid-state cooling.

II. Experimental Details

We grew thin films of nanoscale Bi_2Te_3/Sb_2Te_3 multilayers (MLs) using e-beam evaporation, and from them fabricated integrated thermoelectric devices with the Bi_2Te_3/Sb_2Te_3 multilayer (ML) thin film, using microfabrication techniques. The TE device was designed to have 32,768 TE elements, which are connected electrically in series, and thermally in parallel for attaining maximal output voltages (Fig. 1a). The TE elements were arranged as 128 (row) × 256 (column) in the TE device (Fig. 1b), wherein the end of the TE elemental chain was connected to two metal contacts for electrically connecting the device to the outside. Each column also can be characterized through the metal pads.

We grew the Bi_2Te_3/Sb_2Te_3 multilayer thin film via electron-beam evaporation at room temperature. Solid bismuth (III) telluride, and antimony (III) telluride (99.999 % purity from Alfa Aesar Company, were used as the source materials for growing the Bi_2Te_3 and Sb_2Te_3 nanolayers, respectively. The multilayer (ML) film was deposited sequentially so to have a periodic structure consisting of 20 alternating layers of Bi_2Te_3 and Sb_2Te_3 wherein each layer was 1.5 nm thick (a total thickness of 30 nm) (Fig. 2a). The substrate holder was rotated at the speed of 20 RPM during the deposition. The process chamber had a background pressure of 2×10^{-7} Torr. An INFICON deposition monitor controlled the thicknesses of the layers. The

thickness was calibrated and confirmed using high-resolution transmission electron microscopy (HRTEM).

The TE device has three layers: A multilayer (ML), a metal layer to contact the top of the ML, and a metal layer to contact the bottom of it; it was fabricated using the process of layer-by-layer microfabrication. We used ultra-violet (UV) lithography for patterning in fabricating the devices. Three pieces of photo masks were designed for generating the TE device, and were fabricated by Photo Sciences, Inc. Shipley SPR 220 photo-resist was used in the UV lithography, and lift-off process was used to pattern the layers. As the substrates, we used three-inch-diameter n-type <100> silicon wafers (Virginia Semiconductor, Inc.). The silicon wafers were about 350-μm-thick with a resistivity of about 3 Ω·cm. The wafers initially were oxidized at 1100 ^{o}C for 60 minutes so to obtain a 0.5-μm-thick silicon dioxide layer using wet thermal-oxidation. The first layer patterned on the oxidized silicon substrate was a Cr/Au/Ni layer for the metal contact of the bottom of the Bi_2Te_3/Sb_2Te_3 multilayer (ML), including 5-nm-thick chromium (Cr), 500-nm-thick gold (Au), and 40-nm-thick nickel (Ni); then a 30-nm-thick Bi_2Te_3/Sb_2Te_3 multilayer (ML) was patterned, wherein the bottom of ML was connected to the first metal layer; the third layer was a Ni/Au layer for the metal contact of the top of the Bi_2Te_3/Sb_2Te_3 multilayer (ML), including 40-nm-thick nickel (Ni) and 500-nm-thick gold (Au).

Using high-resolution transmission electron microscopy (HRTEM), we analyzed the cross-section morphology of Bi_2Te_3/Sb_2Te_3 multilayer, and its interface with the silicon substrate. We prepared the TEM samples by the In-situ Lift-out method using a dual-beam FIB (FEI Helios 600 dual beam FIB). The FIB's TEM membranes were imaged in a JEOL 2100F, high-resolution

analytical transmission-electron microscope at 200 k. The Bi_2Te_3/Sb_2Te_3 multilayer films were investigated by synchrotron x-ray scattering. X-ray scattering was performed at Beamline X6B of the National Synchrotron Light Source, Brookhaven National Laboratory, with x-ray wavelength 0.65 Å and a 640-element Si strip detector having resolution of 0.01° in scattering angle 2θ. The fabricated device was imaged in a JEOL JSM-6610LV scanning electron microscope. All thermal annealing was performed under a vacuum of 1×10^{-4} Torr. We used two Ferrotec thermoelectric modules: The Peltier cooler model 9500/071/040 B, and 9500/127/085 B (Ferrotec Company) to heat the top of TE device and cool the device's substrate during our measurements of the output voltage and current from the fabricated device, respectively. Fig. 3a shows the simple setup on a probe station for the measurements. The TE device was sandwiched between the two TE modules during the measurement (Fig. 3b). The bottom one is biased to cool the substrate of the TE device, and the top one is biased to heat the device's top surface. The bottom cooler model was held on the metal substrate holder of the probe station by vacuum on the back, the fabricated TE device was put on the bottom cooler model, and then the top cooler model was put on the TE device, covering all the TE elements, but leaving the metal pads and the two major metal contacts uncovered, which were adjusted using an optical microscope. The TE device was connected to an outside load-resistor with adjustable resistances through two probes for our characterization of the output voltage and power produced from the device. The two probes also can employ the metal pads under the optical microscope for characterizing each two columns of TE elements. The output voltage of the TE device was measured as a function of the electrical current flowing in the resistor whilst varying the resistance. A DC power source provided the DC voltage for the two Ferrotec thermoelectric modules. Both modules were biased at 2A and 5V, which allows the top surface of the TE device to be heated at about 60 ^{o}C, and the

bottom surface of the device substrate to be cooled to temperature of about 20 ^{o}C. An Agilent multimeter and an Agilent pico amp meter were used together for the electrical characterization of the fabricated TE devices.

III. Results and Discussion

Figures 2b, c, and, d show the HRTEM image of a cross section of the electron-beam-evaporated Bi_2Te_3/Sb_2Te_3 multilayer (ML) thin film. Fig. 2b shows the film as grown without annealing, while Fig. 2c shows the film after being annealed at 100 ^{o}C for one hour. Fig. 2d is an enlarged image of the film after this annealing process. The TEM shows that the electron-beam-evaporated multilayer films have excellent cross-sectional structure without any obvious interface defects.

The Bi_2Te_3/Sb_2Te_3 multilayer films were investigated by synchrotron x-ray scattering. Most illuminating is the comparison of annealed to unannealed films using x-ray reflectivity (Fig. 4), in which oscillations arise from the contrast between alternating regions of material density. The x-ray reflectivity from the unannealed sample has the uniform q dependence of a featureless, smooth film with little internal structure. By comparison, the unannealed sample shows reflectivity that has a broad maximum above and local minimum below the annealed one, at 0.35 and 0.12 Å^{-1} respectively. This is consistent with the nominal 1.5 nm thickness of each layer. A more subtle oscillation with 0.022 Å^{-1} periodicity in consistent with the 30 nm total film thickness. Fine oscillations are further interference effects from interlayer density boundaries. After annealing at 200 ^{o}C, all maxima and oscillations essentially disappear, and all of the

contrast from the multilayer structure has been removed. This shows that substantial mixing between the Bi_2Te_3 and Sb_2Te_3 phases has taken place, destroying the layer interfaces.

Figs. 5a, b, c, and d show the SEM images of the fabricated TE device. Fig. 5a is a SEM image of some elements in the fabricated TE device; these images correspond to individual elements as indicated schematically in Figs. 1a and b. The active area of the device is 1.6 cm × 1.3 cm. Figs. 5b and c show the enlarged view of the TE elements. The Bi_2Te_3/Sb_2Te_3 multilayer in each TE element is about 30 μm (length) × 40 μm (width) × 30 nm (thickness). The active area of each TE element, the overlapping area of the two contact metal layers is about 20 μm (length) × 30 μm (width). Fig. 5d shows the SEM image of TE elements connected to the metal pads, which can be addressed by probes for characterizing each of the two columns of TE elements.

Fig. 6 shows the variation of output voltage and power produced from the TE device versus the load current. An open-circuit voltage of 51 mV, a short-circuit current of 1.7 μA, and a maximum power of 21 nW were produced from the 30 nm-thick Bi_2Te_3/Sb_2Te_3 multilayered TE device. The straight line shows the measured voltage versus the electrical current measured in the load resistor, and the power was calculated from the voltage multiplied by the current. The total resistance of the TE device is about 30 kΩ, which comes mainly from the contact metal layers. Each TE element has an average resistance of 0.92 Ω (0.87Ω (Metal) + 0.05Ω (ML)), and produces an average open-circuit voltage of 1.56 μV. The metal layer has a sheet resistance of about 0.3 Ω/□, so generating about 95% of the resistance of the entire device. The electrical current or power will increase if the sheet resistance of metal layer decreases with depositing thicker metal layers. Fig. 7 shows the dependence of the open-circuit voltage on the annealing

temperatures. The voltage value declines with increasing annealing temperatures, and is down to almost zero when the annealing temperature rises to about 200 ^{o}C. Thermal annealing fostered inter-diffusion between the Bi_2Te_3- and Sb_2Te_3-nanolayers [23], so decreasing the effect of the interface on the open-circuit voltage. Since the open-circuit voltage directly is related to the Seebeck coefficient of the multilayered materials, it is considered that the multilayer structure can enhance the Seebeck coefficient. Fig. 8 plots the variation in the resistivity of ML versus the annealing temperatures. The resistivity decreases at annealing temperatures of less than about 160 ^{o}C, and then increases with higher ones. The open-circuit voltage values obtained from the fabricated TE power chip are also compatible with those achieved by other researchers [21], but the active TE film in this chip is only 30 nm thick, which is much smaller than the film thickness used by other researchers.

IV. Conclusions

We successfully fabricated a 30 nm-thick Bi_2Te_3/Sb_2Te_3 multilayer thin-film-based integrated device encompassing 128×256 thermoelectric elements using microfabrication techniques. HRTEM and X-ray scattering measurements confirm the multilayer structure. An open-circuit voltage of 51 mV, and a maximum power of 21 nW were produced from the 30 nm-thick Bi_2Te_3/Sb_2Te_3 multilayer TE device. The TE device is scalable to produce higher voltage and power with increasing thickness of the ML. We also found that the nanoscale multilayer structure had a significant effect on the voltage and power produced. When the multilayer structure or the interface becomes weaker due to interdiffusion caused by thermal annealing between the Bi_2Te_3 and Sb_2Te_3 layers, the voltage and the power become smaller. The measurements in this research are obtained under ambient conditions, and are simple. Fabrication

of the integrated thermoelectric devices is compatible with the standard fabrication of integrated circuits (IC) fabrication, and is scalable for producing higher voltage and power, or achieving solid-state cooling for applying on-chip temperature monitoring and for stabilizing surface temperature.

Acknowledgements

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Figure Captions

Fig. 1. (a) Working principle for an integrated TE device, wherein the Sb_2Te_3/Sb_2Te_3 multilayer (ML) TE elements are connected electrically in series, and thermally in parallel; (b) arrangement of TE elements in the TE devices; and, (c) picture of the fabricated TE device.

Fig. 2. (a) Schematic of the cross-section of Sb_2Te_3/Sb_2Te_3 multilayer (ML); (b) HRTEM image of the cross-section of Sb_2Te_3/Sb_2Te_3 multilayer (as-grown); (c) HRTEM image of the cross-section of Sb_2Te_3/Sb_2Te_3 multilayer (annealed at 100 ^oC for one hour); (d) an enlarged HRTEM image of the cross-section of Sb_2Te_3/Sb_2Te_3 multilayer (annealed at 100 ^oC for one hour).

Fig. 3. (a) Setup for characterizing the fabricated TE device on a probe station; (b) enlarged view of the setup, where the TE device was sandwiched between two TE modules; the bottom one is biased to cool the substrate of TE device, while the top one is biased to heat the top surface of this device.

Fig. 4. X-ray reflectivity data shows that annealing the Bi_2Te_3/Sb_2Te_3 (BT/ST) films at 200 ^oC for one hour washes out the contrast between layers. Oscillations visible in the unannealed sample data are not observed for the annealed film.

Fig. 5. (a) SEM image of some elements in the fabricated TE device; (b) SEM image of an enlarged view of TE elements; (c) SEM image of a TE element, wherein the multilayer (ML) film, the top and bottom metal contact layers are labeled; and, (d) SEM image of the TE elements connected to the metal pads.

Fig. 6. Variation of output voltage and power produced from the TE device versus the load current.

Fig. 7. Variation of the open-circuit voltage versus the annealing temperatures.

Fig. 8. Variation of the resistivity of ML versus the annealing temperatures.

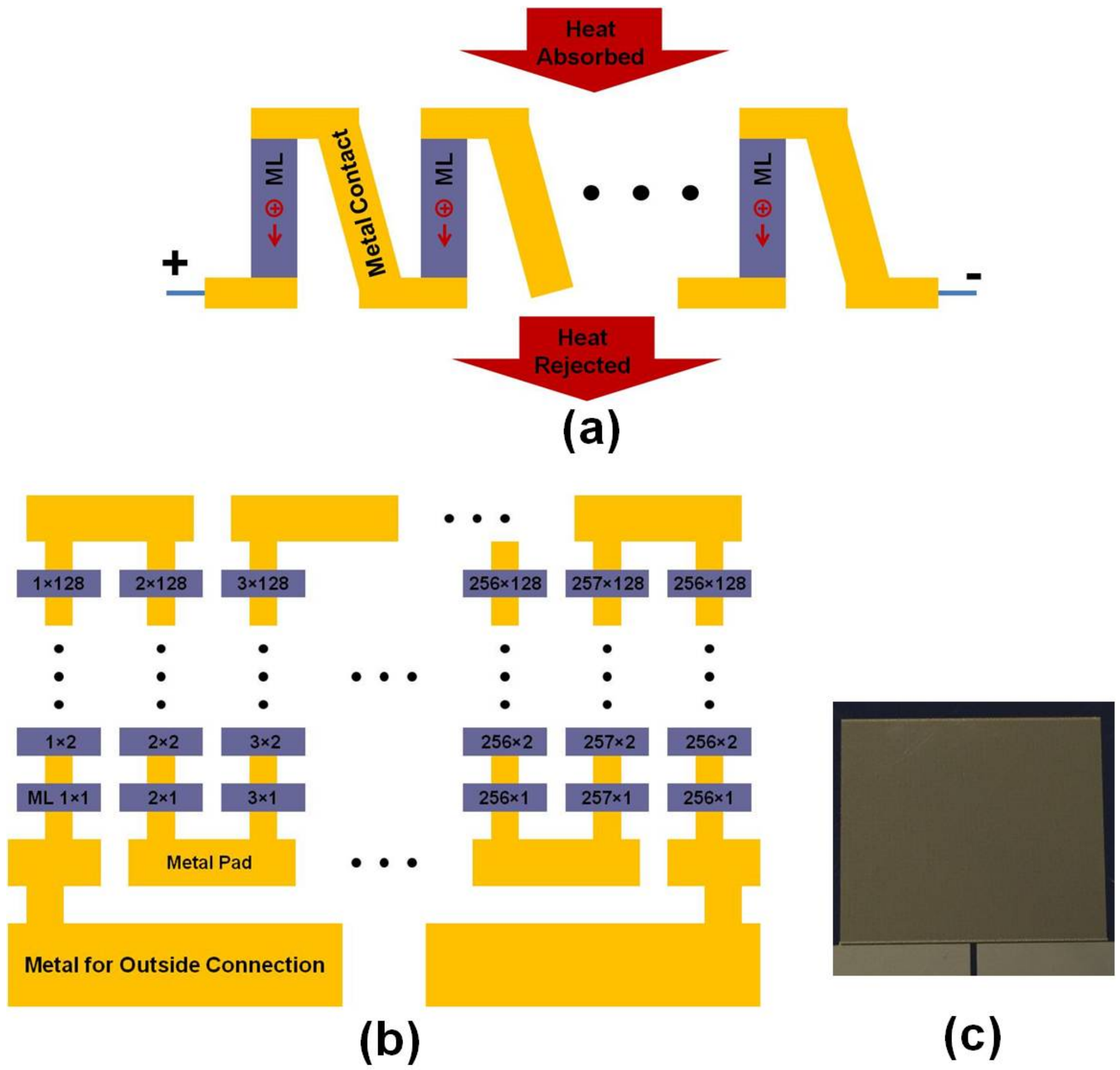
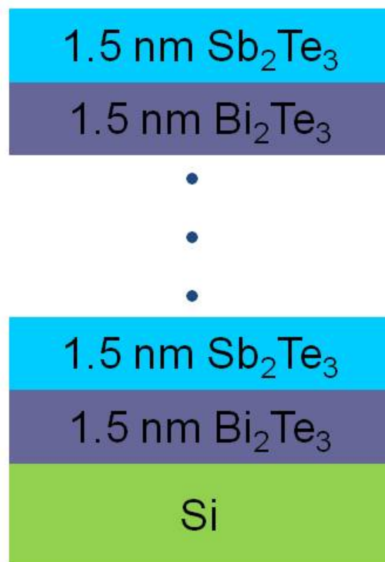


Fig. 1



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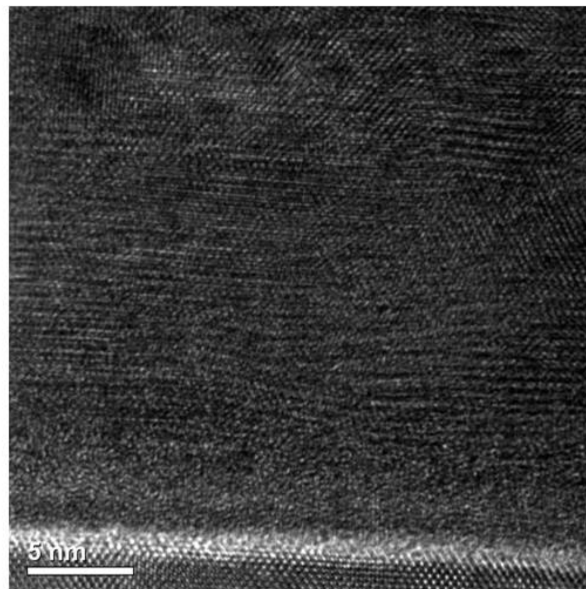

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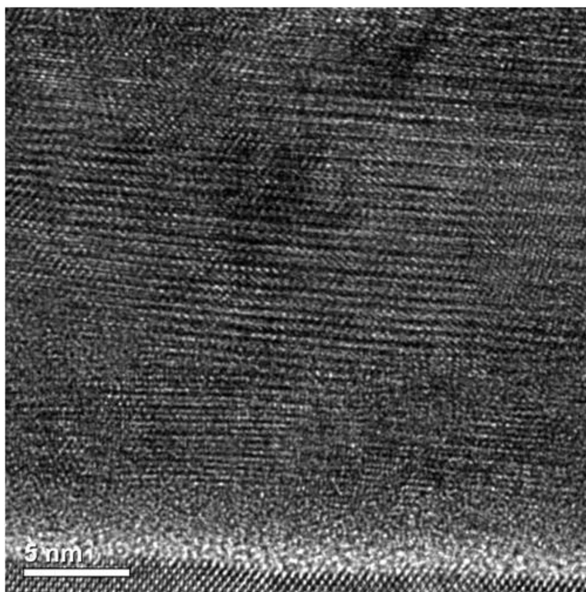

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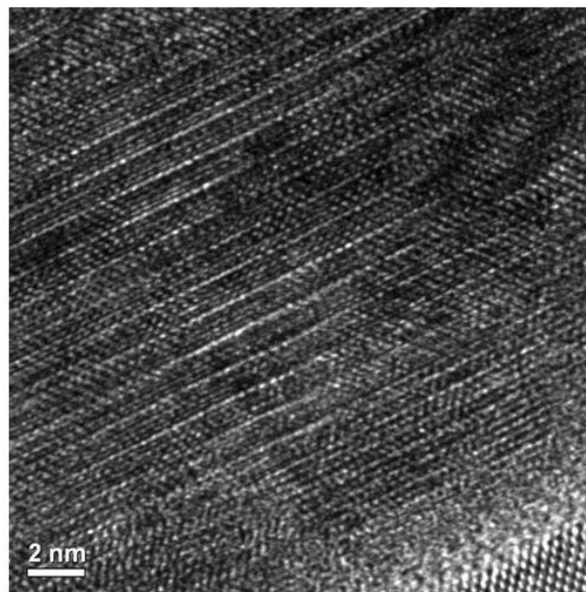
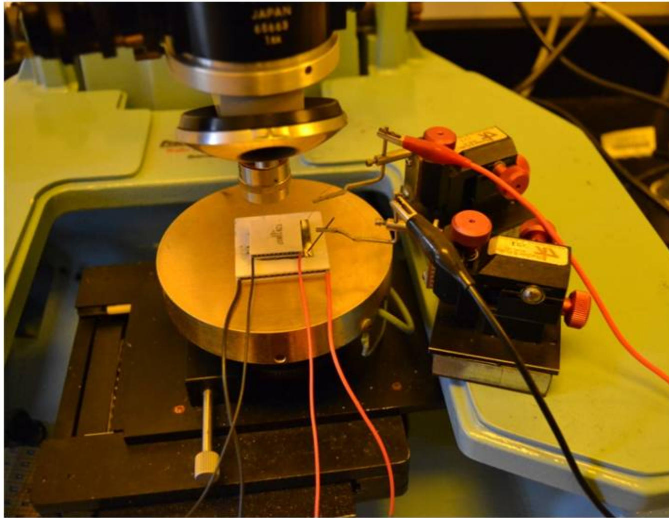


(d)

Fig. 2



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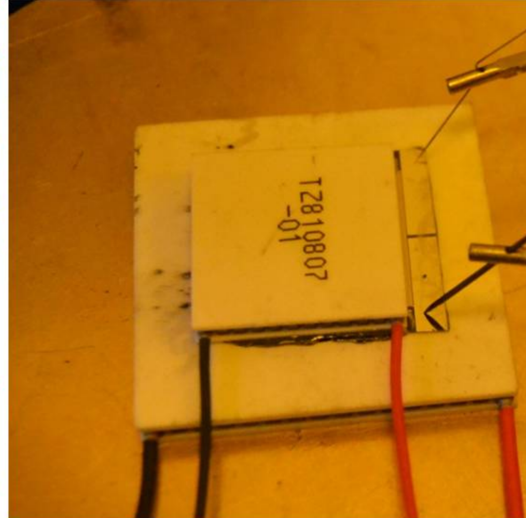

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Fig. 3

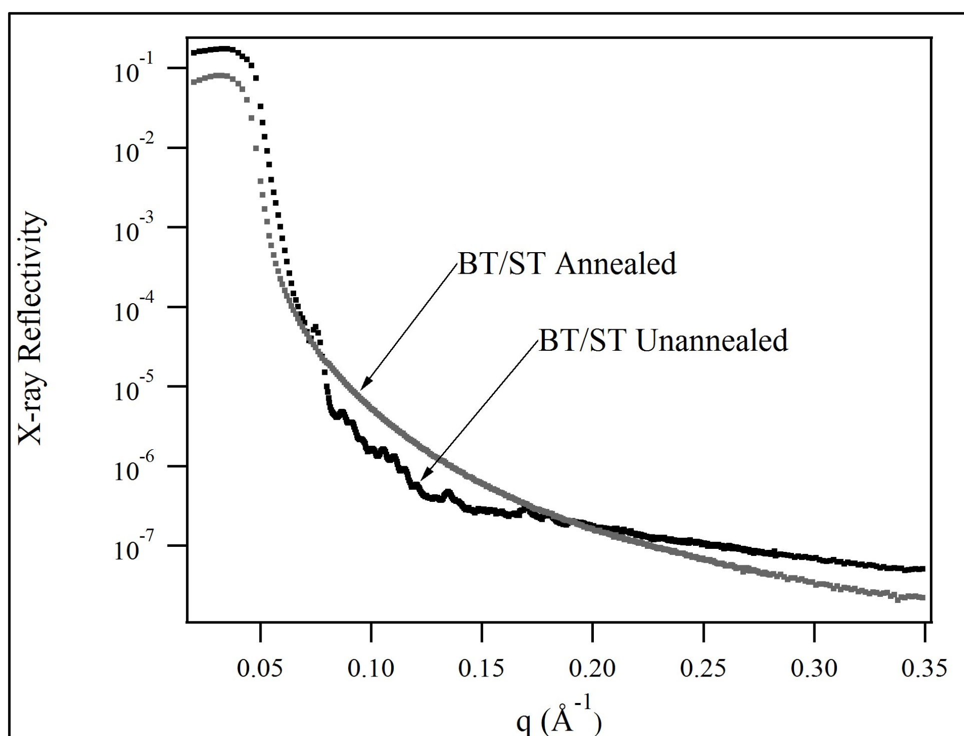

Fig. 4

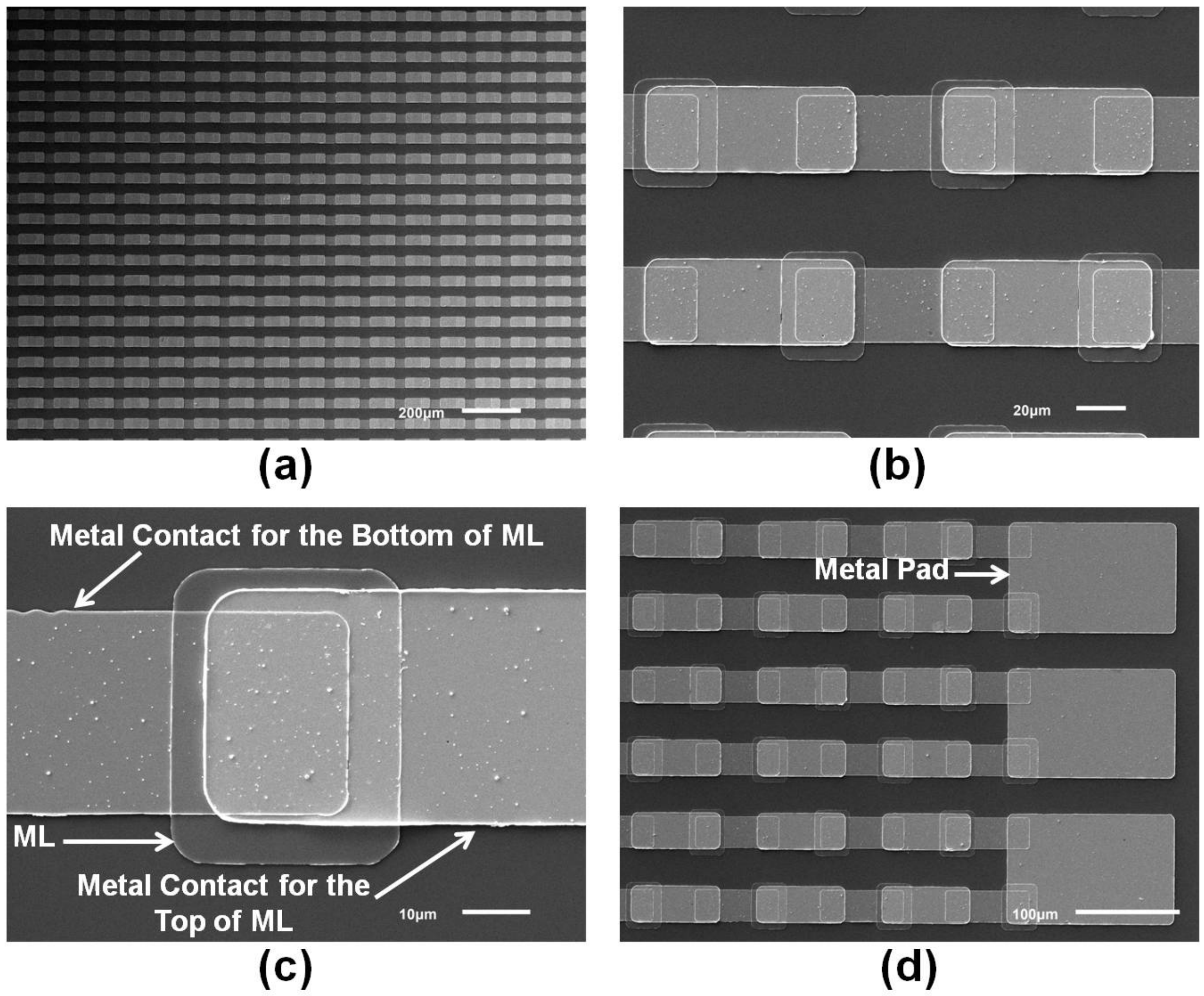

Fig. 5

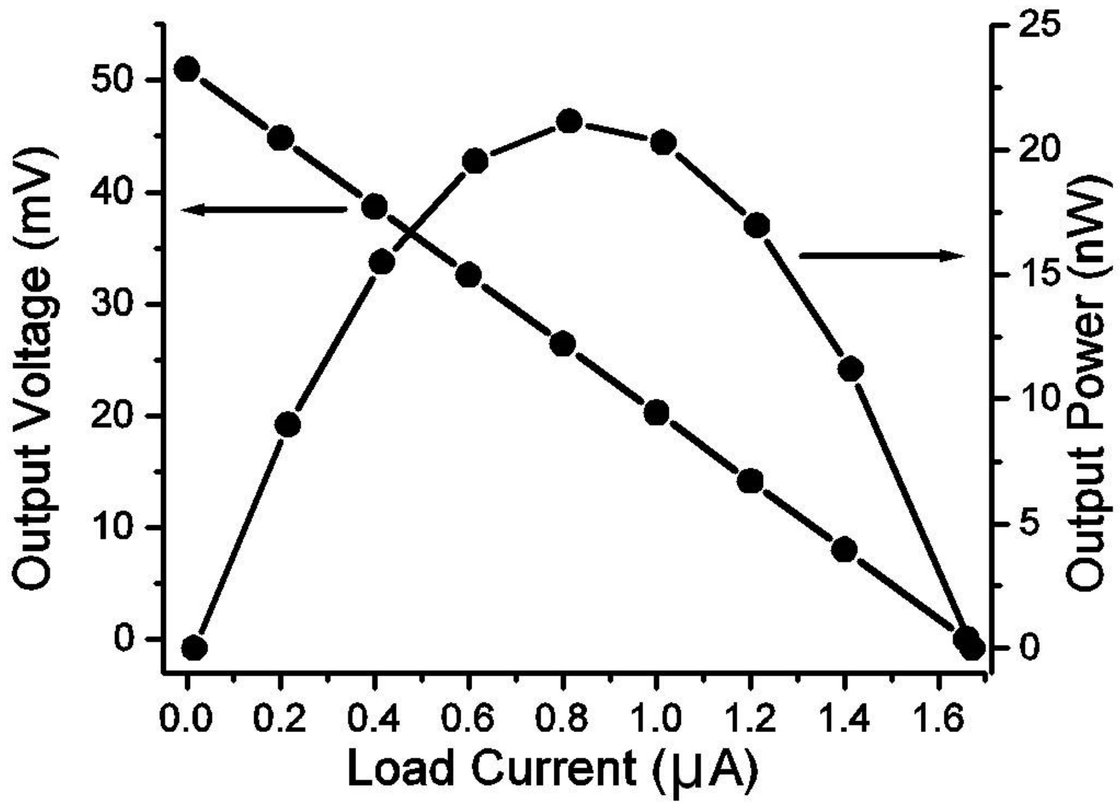

Fig. 6

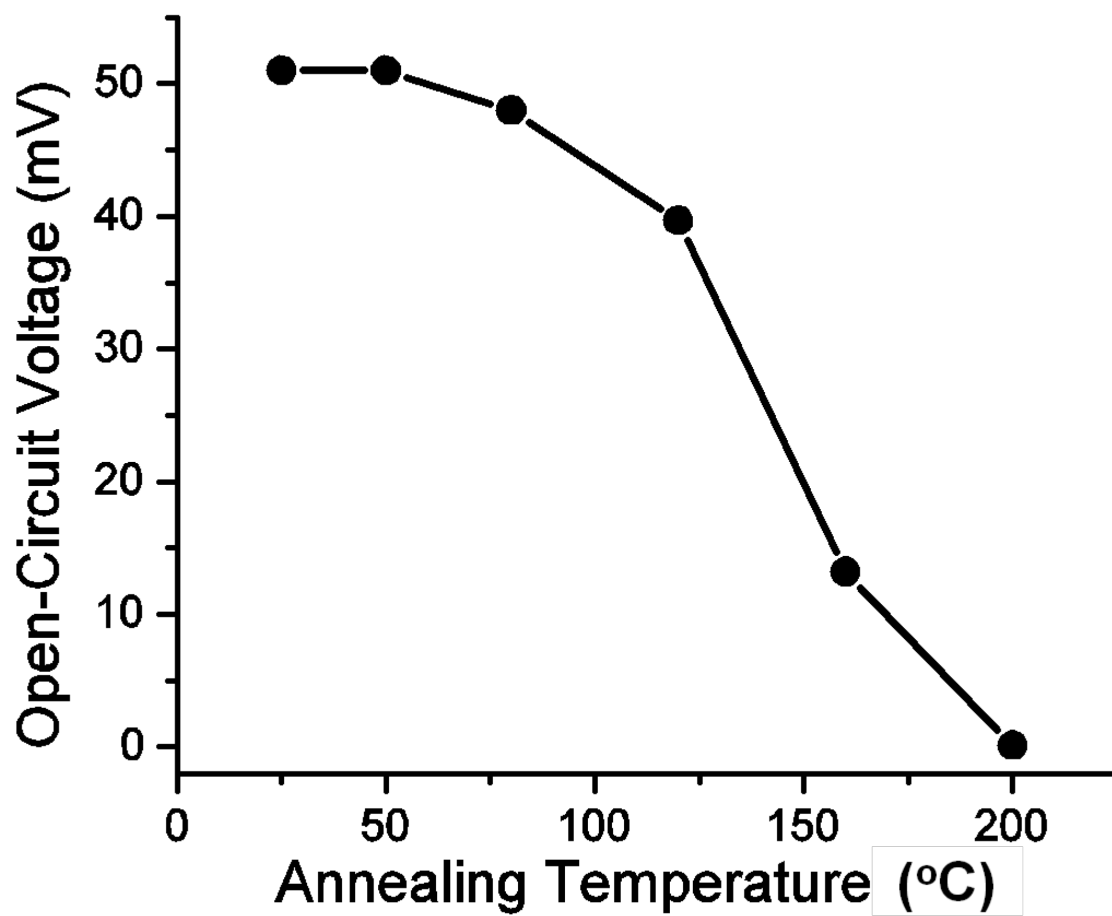

Fig. 7

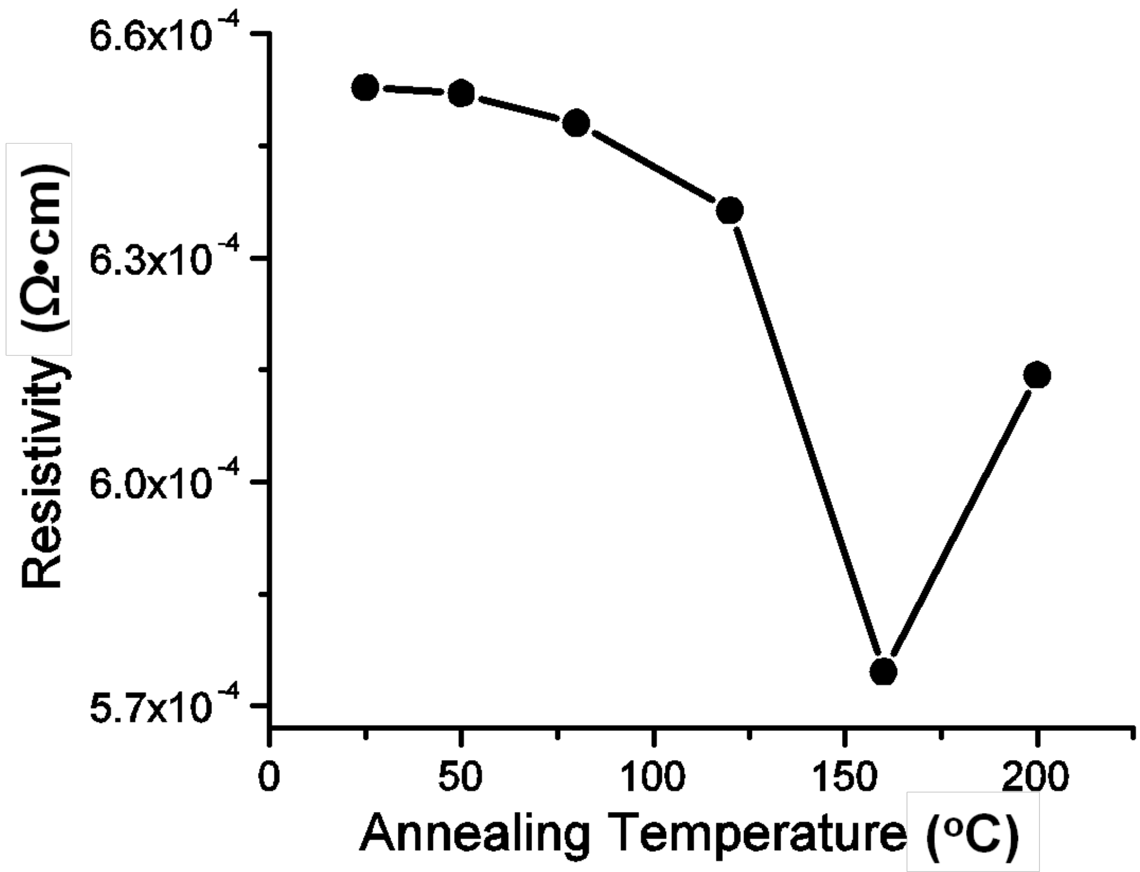

Fig. 8