A Generalized Precharging Strategy for Soft Startup Process of the Modular Multilevel Converter-Based HVDC Systems

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***Abstract*-The modular multilevel converter (MMC) has become the most attractive converter technology for medium/high-power applications, specifically for high-voltage direct current (HVDC) transmission systems. One of the technical challenges associated with the operation and control of the MMC-based system is to precharge the submodule (SM) capacitors to their nominal voltage during the startup process. In this paper, considering various SM circuits, a generalized precharging strategy is proposed for the MMC-based systems, which can implement soft startup from dc or ac side. The proposed precharging strategy can be applicable for various SM circuits and MMC configurations. The proposed startup strategy does not require extra measurements and/or auxiliary power supplies. The charging current is controlled by adjusting the changing rate of the number of blocked and bypassed SM capacitors. Based on the proposed startup strategy, the startup processes of MMC/MMC-HVDC systems with various SM circuits are analyzed and a generalized startup procedure for various MMC-HVDC systems is proposed. In addition, the uncontrollable steady-state SM capacitor voltages of various MMC-based systems are analyzed and the associated precharging time is also investigated. Performance of the proposed strategy for various MMC-HVDC systems is evaluated based on time-domain simulation studies in the PSCAD/EMTDC software environment and experimental results based on a scaled-down prototype.**

***Index Terms*— Modular Multilevel Converter (MMC), High Voltage Direct Current (HVDC), Soft Startup Precharging Process, Precharging the SM Capacitors**

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NOMENCLATURE

N	Number of SMs per arm.
N_C	Number of SM capacitors per arm.
N_{BLK}	Number of blocked SM capacitors per arm.
N_{BY}	Number of bypassed SM capacitors per arm.
V_{LL}	Amplitude of the ac-side line-to-line voltage.
V_{dc}	DC-bus voltage.
V_C^{nom}	Nominal voltage of SM capacitor.
V_{arm}	Voltage across each arm.
$V_C^{\mathrm{I,SS}}$	Uncontrollable steady-state SM capacitor voltage during Stage I.
V_C^{ini}	Initial SM capacitor voltage for controllable start-up.

I. INTRODUCTION

The modular multilevel converter (MMC) has become the most attractive converter topology for medium/high voltage applications, especially for voltage-sourced converter high-voltage direct current (VSC-HVDC) transmission systems because of its modularity and scalability [1].

One of the main technical challenges associated with the control and operation of the MMC systems is to smoothly precharge the submodule (SM) capacitors to their nominal voltage during the converter startup process. Considering various MMC systems based on different SM circuits, which have been investigated to block the dc-side short-circuit faults [2]–[4], precharging process becomes even more complicated. For the MMC-based drive systems, precharging the capacitors during startup process is carried out by absorbing power from the dc-side voltage source, while the MMC-HVDC system can be charged from the ac grid.

The existing startup methods are mainly based on using additional power supplies and/or complex control methods while only considering one type of SM circuit topology. In [5], [6] and [7], the proposed startup methods only consider half-bridge MMC systems and charge the SM capacitors from the dc-side voltage source. In [8] and [9], an auxiliary voltage source is employed to charge the SM capacitors individually, which adds to the system complexity and cost. In [10], [11], [12] and [13], closed-loop startup control methods are applied to charge the SM capacitors from ac or dc side. However, those closed-loop methods only consider the MMC based on half-bridge SMs and employ additional PI controllers, which limitis the application range and increase control complexity.

Reference [14] investigates the startup issue of a clamp-double SM-based MMC-HVDC system and proposes a grouping sequentially controlled charge method. However, the method is specifically applicable to the MMC with clamp-double SMs and additional control effort is needed to group and charge the SM capacitors. An offshore integrated MMC multi-terminal HVDC system has been investigated in [15], which analyzed the startup process of multi-terminal MMC-HVDC system from the view of system level.

To address the startup challenges of various SM circuits and MMC-based systems, a generalized precharging strategy is proposed in this paper to charge the SM capacitors of the MMC-based systems during startup process, suitable for different startup conditions, i.e., ac- and dc-side startups. Based on the proposed precharging strategy, a generalized startup procedure for various MMC-HVDC configurations is proposed. The proposed strategy is based on adjustment of the number of blocked and bypassed SM capacitors in conjunction with the conventional capacitor voltage sorting algorithm, without using any auxiliary power supplies and/or additional feedback control loop. By using the proposed procedure, the SM capacitors can be charged smoothly to their nominal voltage and the inrush charging current can be limited. The proposed strategy is also applicable to black start applications [8]. In this paper, the uncontrollable steady-state SM capacitor voltages of various MMC-based systems are also analyzed and determined. The effectiveness of the proposed startup strategy is verified by both simulation and experimental results under ac- and dc-side startup processes.

This paper is structured as follows. Section II proposes a generalized precharging strategy. Section III develops the startup procedures for various MMC configurations and determines the uncontrollable steady-state voltages for various SM circuits and MMC configurations under different startup conditions. A generalized startup procedure for various MMC-HVDC systems is developed in Section IV. Section V analyzes the precharging time. The simulation and experimental results of the proposed startup strategy are presented in Sections VI and VII, respectively. Section VIII concludes this paper.

II. The Proposed Precharging Strategy

A schematic diagram of an MMC is shown in Fig. 1. The MMC consists of two arms per phase where each arm comprises N series-connected, nominally identical, half-bridge (HB) submodules (SMs), and a series-connected inductor. The details of operation of the MMC have been described in [1] and are not repeated here.

To start up an MMC, two stages need to be considered:

- Uncontrollable precharging (Stage I): During this stage, the SMs are not controllable and all the switches are blocked. The charging current from either the ac or the dc side flows through the anti-parallel diodes to charge the SM capacitors to an uncontrollable steady-state voltage $V_C^{\mathrm{I,SS}}$. Since the system is uncontrollable, to limit the inrush charging current, a current-limiting resistor arranged in the dc side, ac side, or the arm loops is employed [7], [10], [14].
- Controllable precharging (Stage II): Subsequent to an initial voltage built-up across each SM capacitor in Stage I, the SMs can be controlled to be in the inserted, bypassed, or blocked state.

For the proposed precharging strategy, two operating states are defined:

- Blocked SM capacitor (charging state): In an HB SM, both S1 and S2 are off, and its equivalent circuit is shown in Fig. 2. During this state, the SM capacitor is only charged when the arm current is positive.
- Bypassed SM capacitor (bypassing state): In an HB SM, S1 is off and S2 is on, and its equivalent circuit is shown in Fig. 2. Ideally, the SM capacitor voltage is kept unchanged.

The idea of the proposed precharging strategy is based on control of the number of blocked and bypassed SM capacitors in conjunction with the conventional SM capacitor voltage sorting algorithm. In this way, all SM capacitors can be charged to their nominal voltage V_C^{nom}. When the MMC is connected to a dc voltage source at its dc side or to an ac voltage source at its ac side, a steady-state voltage V_{arm} is established across each arm, as shown in Fig. 3. Each SM capacitor is charged to a certain voltage level, which is usually less than its nominal value during Stage I. For the HB SM, the blocked SM capacitors are charged through the anti-parallel

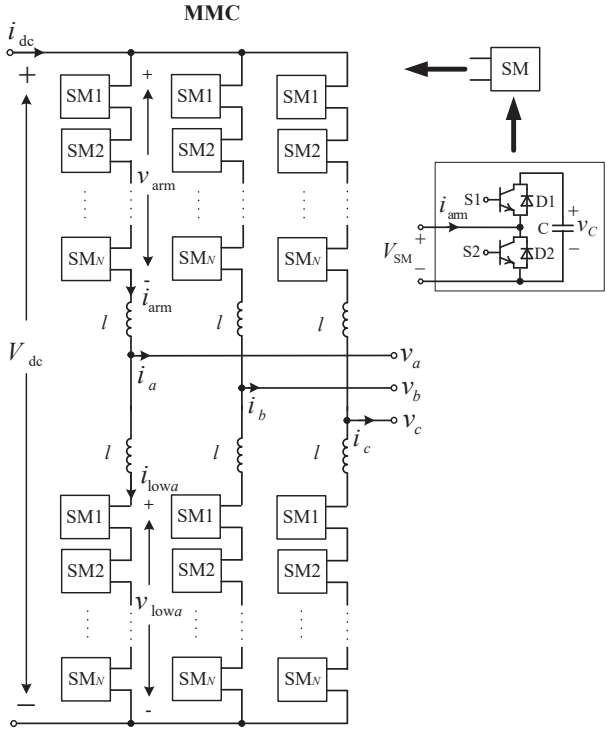

Fig. 1. Schematic representation of an MMC.

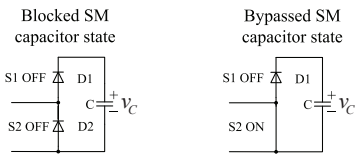

Fig. 2. The equivalent circuit of an HB SM under blocked and bypassed SM capacitor states.

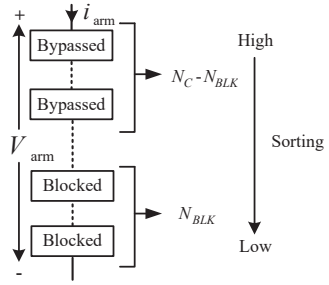

Fig. 3. The proposed precharging strategy for an arm.

diode of S1, when the arm current is positive. When the arm current is negative, the charging current flows through the anti-parallel diode of S2. Thus, the positive arm voltage can charge the capacitors during the blocked SM capacitor state. During Stage II, assuming all SMs are controllable, $N_{\rm BLK}$ SM capacitors out of N_C SM capacitors of each arm are blocked and $N_{\rm BY}$ (where $N_{\rm BY} = N_C - N_{\rm BLK}$) SM capacitors are bypassed during startup process to charge the SM capacitors. N_C is the total number of SM capacitors in each arm, where $N_C = N$ for the HB-MMC system. The relationship between SM capacitor number N_C and SM number N of each arm is given by

$$N_C = \begin{cases} N, & \text{HB, FB, UFB,} \\ 2N, & \text{CD, 3LCC, 5LCC.} \end{cases} \tag{1}$$

As shown in Fig. 3, when all the SM capacitors are charged to their nominal voltage $V_C^{\rm nom}$, the corresponding reference value of $N_{\rm BLK}$ is given by

$$N_{\rm BLK}^{\rm ref} = \frac{V_{\rm arm}}{V_C^{\rm nom}}, \tag{2}$$

where $V_{\rm arm}$ depends on various operating conditions and will be discussed in the following sections. The corresponding $N_{\rm BY}^{\rm ref}$ is equal to $(N_C - N_{\rm BLK}^{\rm ref})$. To balance the capacitor voltages/energy during the startup precharging process, the conventional sorting algorithm is employed [16]. In each arm, $N_{\rm BY}$ SM capacitors with the highest voltages are bypassed while $N_{\rm BLK}$ SM capacitors with the lowest voltages are blocked while enabling sorting balance algorithm during the startup precharging process. After startup process, $N_{\rm BLK}^{\rm ref}$ SM capacitors support the charging voltage $V_{\rm arm}$ while the sorting algorithm maintains the capacitor voltages/energy of all SMs at the same level.

Besides the HB SM, other SM circuits including the full-bridge (FB), the unipolar-voltage full-bridge (UFB), the clamp-double (CD), the three-level/five-level cross-connected (3LCC/5LCC) SMs can be also used for the purpose of dc-fault blocking [2], [4], [17]. Although the circuit topologies of the aforementioned SMs differ from the HB SM, the capacitors in these SMs can be controlled either in the blocked (charging) or bypassed state when all conducting switches are always turned on, which have the same behavior of the HB SM.

Considering various SM circuits, a general startup precharging procedure is developed and described in Fig. 4, in which $V_C^{\rm ini}$ is the initial voltage of SM capacitors for controllable startup. In case of the fault-blocking SMs, the conducting switches are turned on. In this way, all SMs become equivalent to the HB SMs and the SM capacitors can be controlled as either in the blocked or the bypassed state. After all capacitor voltages reach their steady-state values, the current-limiting resistor is bypassed and the number of the blocked SM capacitors $N_{\rm BLK}$ is controlled from N_C to $N_{\rm BLK}^{\rm ref}$ smoothly while, in conjunction with the capacitor voltage sorting algorithm, the number of bypassed SM capacitors is changed from zero to $N_{\rm BY}^{\rm ref}$. The changing rate of $N_{\rm BLK}$ limits the inrush charging current. The reference value of $N_{\rm BLK}$ is determined by (2) to charge the SM capacitors to their nominal voltages.

III. Startup Procedures for Various MMC Configurations

A. DC-Side Startup

Due to a positive dc-bus voltage on the dc side of the MMC in Fig. 1, a positive arm voltage is generated and given by,

$$V_{\rm arm} = \frac{V_{\rm dc}}{2}. \tag{3}$$

Regardless of the SM circuit topology, the charging current is positive to charge the SM capacitors. To charge the SM capacitors to their nominal voltage, the corresponding reference number of the blocked SM capacitors is

$$N_{\rm BLK}^{\rm ref} = \frac{V_{\rm arm}}{V_C^{\rm nom}} = \frac{V_{\rm dc}}{2V_C^{\rm nom}}. \tag{4}$$

Before starting up, during Stage I, all SM capacitors can be charged to the uncontrollable steady-state voltage $V_C^{\rm I,SS}$. Then, when all SM circuits are controllable, the precharging process will enter into Stage II. Under this condition, the initial voltage of all SM capacitors for controllable startup ($V_C^{\rm ini}$) is equal to $V_C^{\rm I,SS}$, which is given by

$$V_C^{\rm I,SS} = V_C^{\rm ini} = \frac{V_{\rm dc}}{2N_C}, \tag{5}$$

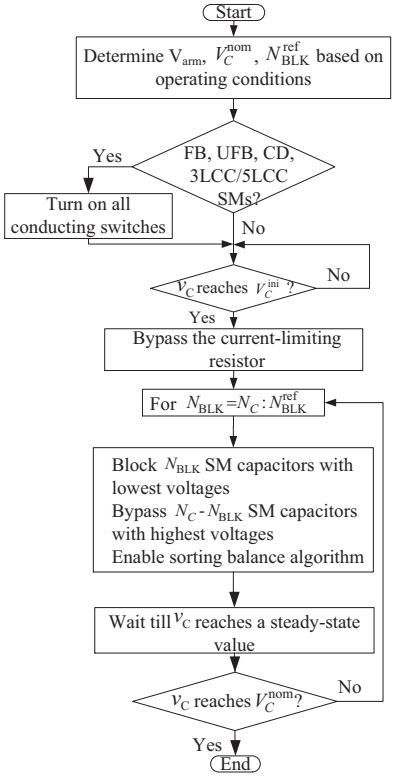

Fig. 4. Flowchart of the proposed startup strategy of the MMC.

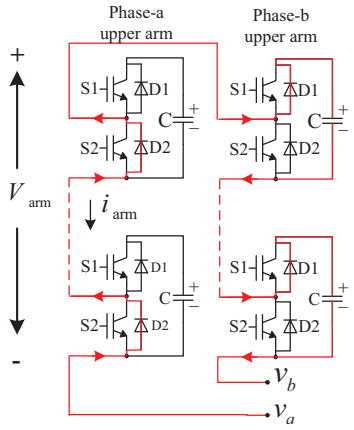

Fig. 5. HB-MMC charged from ac side.

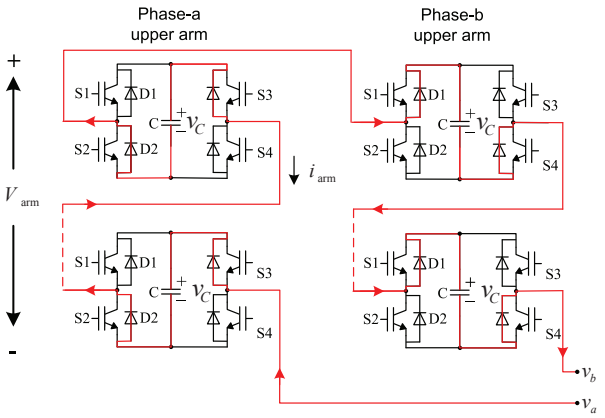

Fig. 6. FB-MMC charged from ac side.

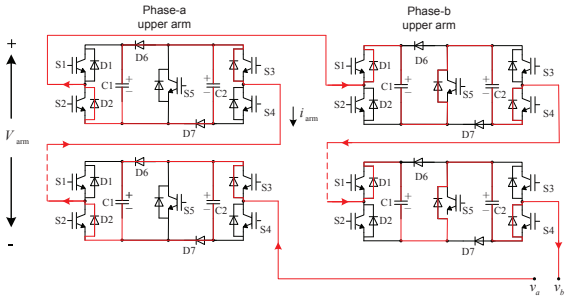

Fig. 7. CD-MMC charged from ac side.

which is only half of the nominal capacitor voltage.

If the dc-bus voltage is not at its nominal value, the MMC can be still started up by choosing appropriate N_{BLK} based on (4). Thus, by the proposed startup strategy, a black start [8] can be realized with a low dc-bus voltage (i.e., $V_{\text{dc}} = 2V_C^{\text{nom}}$ and $N_{\text{BLK}}^{\text{ref}} = 1$).

B. AC-Side Startup

When the ac side of the MMC is connected to an ac grid/voltage source, the arm voltage is determined by the ac-side line-to-line voltage and the SM circuit topologies.

1) Startup Procedure for the HB-MMC: For the HB-MMC, the charging circuit can be regarded as an uncontrolled rectifier. When v_{ab} is positive, the current flows from phase-a upper arm to phase-b upper arm. Due to the HB SM circuit, the current flows through the anti-parallel diodes of the SMs in the phase-a upper arm, charging the SM capacitors of phase-b upper arm, as shown in Fig. 5. Thus, the maximum available charging voltage in each arm is $V_{\text{arm}} = V_{\text{LL}}$, where V_{LL} is the amplitude of the ac-side line-to-line voltage.

To charge the SM capacitors to their nominal voltage, the reference number of blocked SM capacitors is $N_{\text{BLK}}^{\text{ref}} = \frac{V_{\text{LL}}}{V_C^{\text{nom}}}$ based on (2). For the HB-MMC, before starting up, at the end of Stage I, all SM capacitors are charged to the uncontrollable steady-state voltage $V_C^{\text{I,SS}}$. Under this condition, $V_C^{\text{I,SS}}$ and the initial voltage of all SM capacitors for controllable startup (V_C^{ini}) are equal, which are given by

$$V_C^{\text{I,SS}} = V_C^{\text{ini}} = \frac{V_{\text{LL}}}{N_C}. \tag{6}$$

By properly controlling N_{BLK} from N_C to $N_{\text{BLK}}^{\text{ref}}$, the SM capacitors can be smoothly charged to their nominal voltages.

2) Startup Procedure for the FB-MMC: For the FB-MMC, during Stage I, the ac-side current uncontrollably charges the SM capacitors in both phase-a and phase-b arms, as shown in Fig. 6. Thus, during uncontrollable precharging stage, when blocking all SMs, the maximum available charging voltage across each arm is $\frac{V_{\text{LL}}}{2}$. The steady-state SM capacitor voltage during Stage I is

$$V_C^{\text{I,SS}} = \frac{V_{\text{LL}}}{2N_C}. \tag{7}$$

After Stage I, when all SMs are controllable, the conducting switches (i.e., $S4$ in Fig. 6) are turned on. The ac-side current flows through the anti-parallel diodes of one arm and charge the SM capacitors in the other arm, which has similar charging behavior of the HB-MMC. The SM capacitors are charged to the initial voltage $V_C^{\text{ini}} = \frac{V_{\text{LL}}}{N_C}$ for controllable startup, which is the same as that of the HB-MMC. Thus, when all SM capacitors are charged to their nominal voltage, the corresponding reference number of the blocked SM capacitors can be chosen the same as that of the HB-MMC, i.e., $N_{\text{BLK}}^{\text{ref}} = \frac{V_{\text{LL}}}{V_C^{\text{nom}}}$. For the UFB, 3LCC, and 5LCC SMs in [4], similar procedures are applied.

3) Startup Procedure for the CD-MMC: For the CD-MMC, during Stage I, the ac-side current uncontrollably charges the SM capacitors in both phase-a and phase-b arms, as shown in Fig. 7. However, when the arm current is negative, every two capacitors connected in parallel in each SM are charged. The equivalent number of SM capacitors in charging loop is $\frac{N_C}{2} + N_C = 1.5N_C$, which support the line-to-line voltage. Thus, at the end of Stage I, all SM capacitor voltages reach to the uncontrollable steady-state voltage

$$V_C^{\text{I,SS}} = \frac{V_{\text{LL}}}{1.5N_C}. \tag{8}$$

Subsequent to Stage I, when all SMs are controllable, all conducting switches (i.e., $S5$ in Fig. 7) are turned on and the SM capacitor voltages reach the initial voltage $V_C^{\text{ini}} = \frac{V_{\text{LL}}}{N_C}$ for controllable startup, which is the same as that of the HB-MMC. Therefore, the startup procedure for the CD-MMC is similar to that of the FB-MMC.

4) Startup Procedure for the Hybrid MMC: As shown in Fig. 8, for a hybrid MMC consisting of N_{HB} HB and N_{FB} FB SMs in each arm [4], [17], the HB SMs are charged only when the arm current is positive while FB SMs are charged when the arm current is either positive or negative

during Stage I. Therefore, the capacitors in the FB SMs are charged doubled compared to the other capacitors in the HB SMs. Consequently, the HB and FB SM capacitor charges are respectively expressed by,

$$Q_{\text{HBSM}} = Q_{p,\text{HB}} + Q_{n,\text{HB}}, \tag{9}$$

$$Q_{\text{FBSM}} = Q_{p,\text{FB}} + Q_{n,\text{FB}}, \tag{10}$$

where, Q_p and Q_n are the charges of the associated SM capacitor when the arm current is in its positive and negative half cycle, respectively. For the same positive arm current, $Q_{p,\text{HB}} = Q_{p,\text{FB}}$. Since the capacitor in the HB SM is bypassed when the arm current is negative, $Q_{n,\text{HB}} = 0$. Assuming that the charges of the HB and FB SM capacitors are the same during positive and negative half cycle, $Q_{p,\text{FB}} = Q_{n,\text{FB}}$. Therefore, the uncontrollable steady-state capacitor voltage during Stage I can be expressed by,

$$2V_{C,\text{HB}}^{\text{I,SS}} = V_{C,\text{FB}}^{\text{I,SS}}. \tag{11}$$

Considering the steady-state condition, when phase-a current is negative, the capacitors in FB SMs of phase-a and those in HB and FB SMs of phase-b support the line-to-line voltage V_{LL}. Similar situation happens when phase-a current is positive. Thus, the second relationship of uncontrollable steady-state capacitor voltage during Stage I is

$$N_{\text{HB}}V_{C,\text{HB}}^{\text{I,SS}} + 2N_{\text{FB}}V_{C,\text{FB}}^{\text{I,SS}} = V_{\text{LL}}. \tag{12}$$

Base on (11) and (12), the uncontrollable steady-state capacitor voltages of the HB and FB SMs are respectively described by,

$$V_{C,\text{HB}}^{\text{I,SS}} = \frac{V_{\text{LL}}}{N_{\text{HB}} + 4N_{\text{FB}}}, \tag{13}$$

$$V_{C,\text{FB}}^{\text{I,SS}} = \frac{2V_{\text{LL}}}{N_{\text{HB}} + 4N_{\text{FB}}}. \tag{14}$$

Subsequent to Stage I, when all SMs are controllable, all conducting switches in the FB SMs are turned on and, consequently, each SM capacitor can be charged to $V_C^{\text{ini}} = \frac{V_{\text{LL}}}{N_C}$, which is the same as that of the HB-MMC.

For other SM circuits, the startup procedure is similar to that of the HB-FB hybrid MMC. The only difference is the uncontrollable steady-state SM capacitor voltage $V_C^{\text{I,SS}}$ during Stage I, which depends on the number of various types of SMs and their circuit topologies.

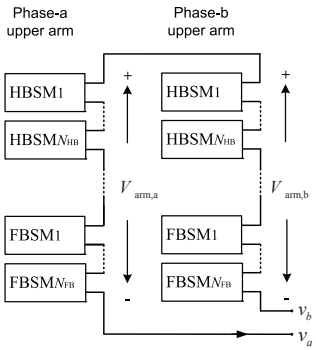

Fig. 8. Hybrid MMC.

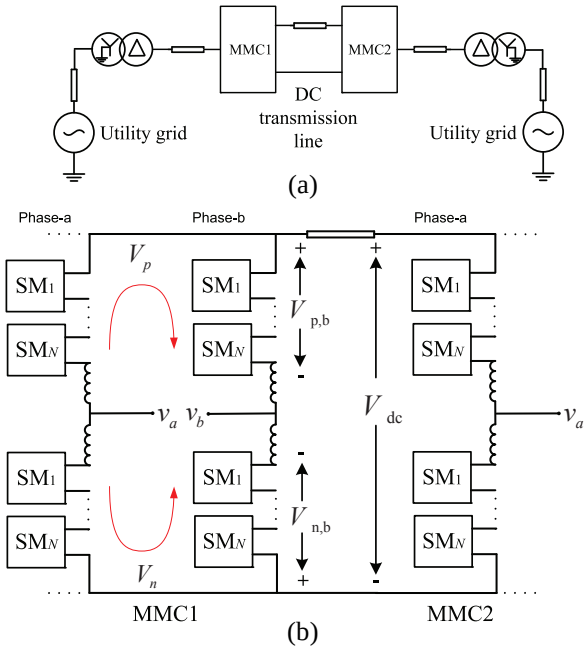

Fig. 9. Schematic representation of the MMC-HVDC system: (a) single-line diagram and (b) circuit diagram.

IV. Startup Procedures for the MMC-HVDC Systems

In this paper, the following startup process of the MMC-HVDC system of Fig. 9 is investigated. The ac side of MMC-1 is connected to an ac grid/voltage source. Once MMC-1 starts up from its ac side and the dc-bus voltage is built up, MMC-2 can start up from its dc side. Thus, MMC-1 experiences an ac-side startup process while MMC-2 starts up from its dc side. A generalized startup procedure for various MMC-HVDC systems is proposed as follows:

- Step 1, when an ac grid is connected to MMC-1, the SM capacitors in MMC-1 are uncontrollably precharged to a steady-state voltage $V_{C,\text{MMC1}}^{\text{I,SS}}$ during Stage I, as discussed in Section III-B. At the same time, a dc-bus voltage V_{dc}^{I} generated by MMC-1 can charge the SMs in MMC-2 to an uncontrollable steady-state voltage $V_{C,\text{MMC2}}^{\text{I,SS}} = \frac{V_{\text{dc}}^{\text{I}}}{2N_C}$ based on (5).
- Step 2, when the SMs in MMC-1 become controllable after the steady-state voltage $V_{C,\text{MMC1}}^{\text{I,SS}}$ established, if there are SMs with fault-blocking capability in MMC-1, their conducting switches are turned on. Consequently, the new steady-state capacitor voltages of MMC-1 become $V_{C,\text{MMC1}}^{\text{ini}} = \frac{V_{\text{LL}}}{N_C}$ and the steady-state dc-bus voltage becomes $V_{\text{dc}}^{\text{II}} = V_{\text{LL}}$. The established dc-bus voltage charges the SM capacitors of MMC-2 to a new steady-state voltage $V_{C,\text{MMC2}}^{\text{ini}} = \frac{V_{\text{dc}}^{\text{II}}}{2N_C} = \frac{V_{\text{LL}}}{2N_C}$ based on (5).
- Step 3, when all SMs of MMC-1 and MMC-2 are controllable and all conducting switches are turned on, the current-limiting resistor is bypassed and the number of blocked (bypassed) SM capacitors is controlled from N_C to $N_{\text{BLK}}^{\text{ref}}$ to charge the SM capacitors to their nominal voltages.

The uncontrollable steady-state capacitor voltage and dc-bus voltage during Stage I are determined by the types of SM circuits and discussed in the following.

TABLE I
THE STEADY-STATE VALUES FOR VARIOUS MMC-HVDC SYSTEMS

	HBSM	FB/UFB/ 3LCC/5LCCSM	CDSM
$V_{C,\mathrm{MMC1}}^{\mathrm{I,SS}}$	$\frac{V_{\mathrm{LL}}}{N_C}$	$\frac{V_{\mathrm{LL}}}{2N_C}$	$\frac{V_{\mathrm{LL}}}{1.5N_C}$
$V_{C,\mathrm{MMC1}}^{\mathrm{ini}}$	$\frac{V_{\mathrm{LL}}}{N_C}$	$\frac{V_{\mathrm{LL}}}{N_C}$	$\frac{V_{\mathrm{LL}}}{N_C}$
$V_{\mathrm{dc}}^{\mathrm{I}}$	V_{LL}	0	$\frac{V_{\mathrm{LL}}}{3}$
$V_{\mathrm{dc}}^{\mathrm{II}}$	V_{LL}	V_{LL}	V_{LL}
$V_{C,\mathrm{MMC2}}^{\mathrm{I,SS}}$	$\frac{V_{\mathrm{LL}}}{2N_C}$	0	$\frac{V_{\mathrm{LL}}}{6N_C}$
$V_{C,\mathrm{MMC2}}^{\mathrm{ini}}$	$\frac{V_{\mathrm{LL}}}{2N_C}$	$\frac{V_{\mathrm{LL}}}{2N_C}$	$\frac{V_{\mathrm{LL}}}{2N_C}$
$N_{\mathrm{BLK,MMC1}}^{\mathrm{ref}}$	$\frac{V_{\mathrm{LL}}}{V_C^{\mathrm{nom}}}$	$\frac{V_{\mathrm{LL}}}{V_C^{\mathrm{nom}}}$	$\frac{V_{\mathrm{LL}}}{V_C^{\mathrm{nom}}}$
$N_{\mathrm{BLK,MMC2}}^{\mathrm{ref}}$	$\frac{V_{\mathrm{LL}}}{2V_C^{\mathrm{nom}}}$	$\frac{V_{\mathrm{LL}}}{2V_C^{\mathrm{nom}}}$	$\frac{V_{\mathrm{LL}}}{2V_C^{\mathrm{nom}}}$

As shown in Fig. 9, the steady-state dc-bus voltage is calculated by

$$V_{\mathrm{dc}} = V_{p,b} - V_{n,b}, \tag{15}$$

where, $V_{p,b}$ and $V_{n,b}$ are the sum of steady-state SM capacitor voltages within their corresponding arms.

For the HB-MMC-HVDC system, $V_{p,b} = V_{\mathrm{LL}}$ and $V_{n,b} = 0$ based on the current direction of Fig. 9. Thus, the dc-bus voltage during Stage I is $V_{\mathrm{dc}}^{\mathrm{I}} = V_{\mathrm{dc}}^{\mathrm{II}} = V_{\mathrm{LL}}$.

For the FB-MMC-HVDC system, when all conducting switches are off, $V_{p,b} = V_{n,b} = \frac{V_{\mathrm{LL}}}{2}$ and, consequently, $V_{\mathrm{dc}}^{\mathrm{I}} = 0$ based on (15). Thus, the SMs in MMC-2 cannot be charged due to the zero dc-bus voltage. Once all conducting switches in MMC-1 are turned on, a steady-state dc-bus voltage $V_{\mathrm{dc}}^{\mathrm{II}} = V_{\mathrm{LL}}$ is produced and the SMs in MMC-2 can be charged from its dc side, which is similar with the HB-MMC-HVDC system. Similarly for UFB, 3LCC, and 5LCC SMs, prior to turning on the conducting switches, $V_{\mathrm{dc}}^{\mathrm{I}} = 0$.

For the CD-MMC-HVDC system, as shown in Fig. 9, based on (15), the steady-state voltage generated by MMC-1 during uncontrollable stage is calculated by

$$V_{p,b} = N_C V_{C,\mathrm{MMC1}}^{\mathrm{I,SS}} = N_C \frac{V_{\mathrm{LL}}}{1.5N_C}, \tag{16}$$

$$V_{n,b} = \frac{N_C V_{C,\mathrm{MMC1}}^{\mathrm{I,SS}}}{2} = \frac{N_C}{2}\frac{V_{\mathrm{LL}}}{1.5N_C}, \tag{17}$$

$$V_{\mathrm{dc}}^{\mathrm{I}} = V_{p,b} - V_{n,b} = \frac{1}{3}V_{\mathrm{LL}}. \tag{18}$$

The steady-state values of the dc-bus voltage, capacitor voltages, and the number of blocked SM capacitors are summarized in Table I.

For the hybrid MMC-HVDC system consisting of N_{HB} HB SMs and N_{FB} FB SMs, prior to turning on the conducting switches in FB SMs, based on (15), the dc-bus voltage during Stage I is calculated by

$$V_{p,b} = N_{\mathrm{HB}} V_{C,\mathrm{HB}}^{\mathrm{I,SS}} + N_{\mathrm{FB}} V_{C,\mathrm{FB}}^{\mathrm{I,SS}}, \tag{19}$$

$$V_{n,b} = N_{\mathrm{FB}} V_{C,\mathrm{FB}}^{\mathrm{I,SS}}, \tag{20}$$

therefore,

$$V_{\mathrm{dc}}^{\mathrm{I}} = V_{p,b} - V_{n,b} = N_{\mathrm{HB}} V_{C,\mathrm{HB}}^{\mathrm{I,SS}}. \tag{21}$$

The above analysis is applicable to the hybrid MMC-HVDC systems with other types of SM circuits. Once all conducting switches are turned on, the charging procedure becomes similar to that of the HB-MMC-HVDC system.

V. PRECHARGING TIME ANALYSIS

To estimate the precharging time, the equivalent charging circuit is derived, as shown in Fig. 10. The precharging time is determined by the impedance of charging circuit, especially by circuit resistance and capacitance. The arm inductor is used to smooth the charging current and can be neglected during the precharging time analysis. As shown in Fig. 10, the equivalent resistance $R_{\mathrm{eq,arm}}$ includes the resistances of inductors and transmission lines, the current-limiting resistance, the conduction resistances of semiconductor switches, and equivalent series resistances (ESRs) of capacitors. The equivalent capacitance $C_{\mathrm{eq,arm}}$ can be derived by energy balance. When N_{BLK} capacitors are blocked and charged, the steady-state capacitor voltage is $\frac{V_{\mathrm{arm}}}{N_{\mathrm{BLK}}}$. The sum of energy stored in the SM capacitors is equal to the energy stored in the equivalent capacitor, which is described by:

$$\frac{1}{2}C_{\mathrm{eq,arm}}V_{\mathrm{arm}}^2 = \frac{N_{\mathrm{C}}}{2}C\left(\frac{V_{\mathrm{arm}}}{N_{\mathrm{BLK}}}\right)^2. \tag{22}$$

The equivalent arm capacitance is

$$C_{\mathrm{eq,arm}} = \frac{CN_{\mathrm{C}}}{N_{\mathrm{BLK}}^2}. \tag{23}$$

A. DC-Side Precharging

For dc-side precharging, V_{arm} is half of the dc-bus voltage, as shown in Fig. 10(a). During uncontrollable charging stage, all capacitors are inserted and $N_{\mathrm{BLK}} = N_{\mathrm{C}}$. The capacitor voltage can be expressed as

$$v_{\mathrm{C}}(t) = \frac{V_{\mathrm{arm}}}{N_{\mathrm{C}}} - \frac{V_{\mathrm{arm}}}{N_{\mathrm{C}}}e^{-\frac{t}{R_{\mathrm{eq,arm}}C_{\mathrm{eq,arm}}}}, \tag{24}$$

where $C_{\mathrm{eq,arm}} = \frac{C}{N_{\mathrm{C}}}$ based on (23) and $V_{\mathrm{arm}} = \frac{V_{\mathrm{dc}}}{2}$.

During controllable charging stage, for any arbitrary N_{BLK}, the steady-state SM capacitor voltage is $\frac{V_{\mathrm{dc}}}{2N_{\mathrm{BLK}}}$. When the number of the blocked SM capacitors is changed from $N_{\mathrm{BLK}}+1$ to N_{BLK}, the SM capacitor voltage is described by:

$$v_{\mathrm{C}}(t) = \frac{V_{\mathrm{arm}}}{N_{\mathrm{BLK}}} - \frac{V_{\mathrm{arm}}}{N_{\mathrm{BLK}}\,(N_{\mathrm{BLK}}+1)}e^{-\frac{t}{R_{\mathrm{eq,arm}}C_{\mathrm{eq,arm}}}}, \tag{25}$$

where $C_{\mathrm{eq,arm}}$ is calculated by (23).

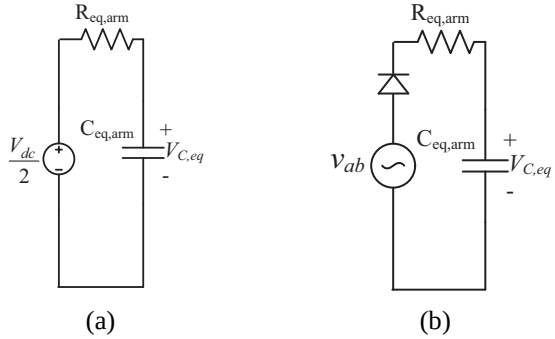

Fig. 10. The equivalent circuit of (a) dc-side and (b) ac-side precharging.

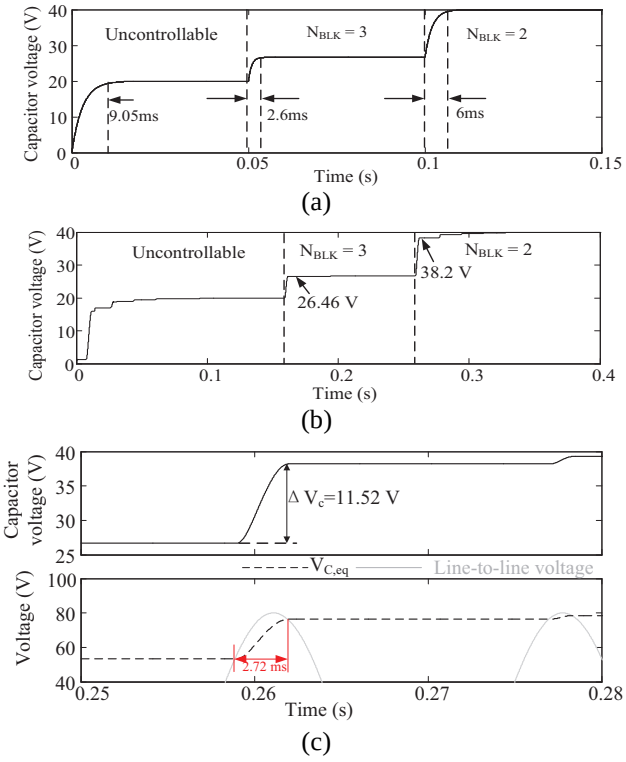

Fig. 11. The simulation results of precharging time analysis (a) dc-side precharging, (b) ac-side precharging, and (c) zoom in view of (b).

The time constant of the circuit of Fig. 10(a) is defined as $\tau_{\text{eq,arm}} = R_{\text{eq,arm}} C_{\text{eq,arm}}$. When charging time t = $3\tau_{\text{eq,arm}}$, $e^{-\frac{t}{\tau_{\text{eq,arm}}}}$ is less than 0.05 and, as an assumption, the steady-state condition is reached.

To verify the precharging time analysis, the simulation results of dc-side precharging are shown in Fig. 11(a) based on a HB-MMC system which consists of 4 SMs in each arm. For the uncontrollable precharging stage, the current-limiting resistor is inserted into the charging loop. The equivalent resistance $R_{\text{eq,arm}}$ is 12 Ω. For the controllable precharging stage, when the current-limiting resistor is bypassed by the circuit breaker, the $R_{\text{eq,arm}}$ is 2 Ω. The SM capacitor is 1000 μF. The dc source voltage is 160 V. During the controllable precharging stage, the N_{BLK} is gradually reduced from 4 to 2.

- Uncontrollable stage: $C_{\text{eq,arm}} = \frac{1000\times4}{4^2}\mu$F. The time constant is 3 ms. After 9 ms ($3\tau_{\text{eq,arm}}$), the capacitor voltage can reach its steady-state value, as shown in Fig. 11(a).
- $N_{\text{BLK}} = 3$ during controllable charging: $C_{\text{eq,arm}} = \frac{1000\times4}{3^2}$ μF. The time constant is 0.89 ms. After 2.67 ms ($3\tau_{\text{eq,arm}}$), the capacitor voltage can reach its steady-state value.
- $N_{\text{BLK}} = 2$ during controllable charging: $C_{\text{eq,arm}} = \frac{1000\times4}{2^2}$ μF. The time constant is 2 ms. After 6 ms ($3\tau_{\text{eq,arm}}$), the capacitor voltage can reach its steady-state value.

B. AC-Side Precharging

For ac-side precharging, during the uncontrollable precharging stage, the current-limiting resistor and all capacitors in the fault-blocking SMs are inserted in the charging circuit loop before turning on the conducting switches. During the controllable precharging stage and all conducting switches are on, the MMCs with various SMs have the same behavior of the HB-MMC and the associated equivalent circuit is shown in Fig. 10(b). The capacitors are charged only when the line-to-line voltage is higher than the voltage of equivalent capacitor $V_{\text{C,eq}}$. If the time constant of the equivalent circuit of Fig. 10(b) is small, the capacitors can be charged to their steady-state voltages within one line cycle. If the time constant of the equivalent circuit is large, multiple line cycles are required to charge the capacitors to their steady-state voltages.

The simulation results are shown in Figs. 11(b) and (c) based on the HB-MMC system used in dc-side precharging analysis. The RMS value of the line-to-line voltage is 56.6 V and the arm inductance is 5 mH. During the controllable precharging stage, N_{BLK} is gradually reduced from 4 to 2. As shown in Figs. 11(b) and (c), when $N_{\text{BLK}} = 3$, the time constant is small (0.89 ms) and the capacitors can be charged to their steady-state voltage within one cycle. When $N_{\text{BLK}} = 2$, the time constant is large (2 ms) and two cycles are needed to charge the capacitors to their steady-state voltage. As shown in Fig. 11(c), during the first cycle, the capacitor voltage is charged to 38.2 V within 2.72 ms, which is less than the steady-state voltage 40 V. Once the line-to-line voltage is less than $V_{\text{C,eq}}$, the charging process stops and the second cycle is needed to charge the capacitors.

VI. Study Results

In this section, performance of the proposed strategy for various MMC-HVDC systems with different SM circuits is evaluated based on simulation studies in the PSCAD/EMTDC software environment. The study system parameters are the same as those used in [4].

A. Startup Process of an MMC from the DC Side

Figure 12 shows the startup process of the HB-MMC system from its dc side. During Stage I, the SMs are uncontrollable and the current-limiting resistor is inserted to limit the charging current. The SM capacitor voltages are charged to their uncontrollable steady-state voltage $V_C^{\text{I,SS}} = \frac{V_{\text{dc}}}{2N_C} = 1.5$ kV at $t = 0.5$ s. During Stage II, the SMs are controllable and the current-limiting resistor is bypassed. From $t = 0.5$ s, as shown in Figs. 12(a) and (c), the number of blocked SM capacitors is dynamically controlled from $N_C = 20$ to $N_{\text{BLK}}^{\text{ref}} = \frac{V_{\text{dc}}}{2V_C^{\text{nom}}} = \frac{60kV}{2\times3kV} = 10$ to charge the SM capacitors to their nominal voltage. The arm currents are limited by the changing rate of N_{BLK}, as shown in Fig. 12(b). As expected, the startup process of the MMCs and the hybrid MMCs based on the SMs with fault-blocking capability is similar to that of the HB-MMC.

B. Startup Process of an MMC from AC Side

In Fig. 13, the ac-side startup process of the HB-MMC system is shown. During Satge I (prior to $t = 1$ s), the current-limiting resistor is inserted to limit the charging current. The SM capacitor voltages are charged to their uncontrollable steady-state voltage $V_C^{\text{I,SS}} = \frac{V_{\text{LL}}}{N_C} = 2.1$ kV. After Stage I, the SMs are controllable and the current-limiting resistor is bypassed at $t = 1$ s. The number of blocked SM capacitors

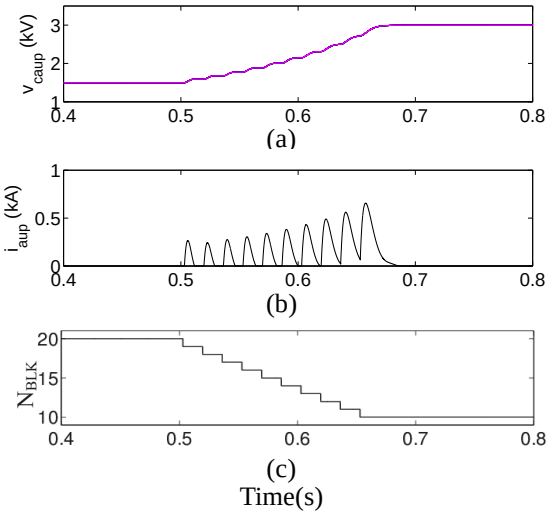

Fig. 12. DC-side startup process of the HB-MMC system: (a) SM capacitor voltages of the phase-a upper arm, (b) phase-a upper arm current, and (c) the commanded number of blocked SM capacitors within each arm.

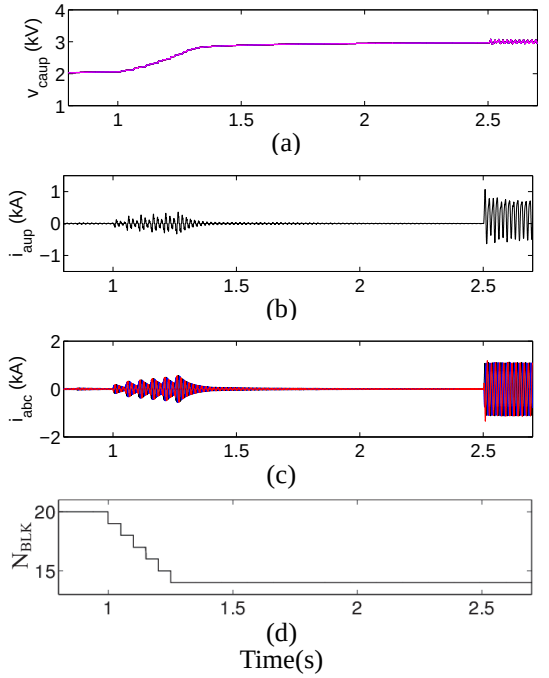

Fig. 13. AC-side startup process of the HB-MMC system: (a) SM capacitor voltages of the phase-a upper arm, (b) phase-a upper arm current, (c) ac-side three-phase currents, and (d) the commanded number of blocked SM capacitors within each arm.

is being changed from $N_C = 20$ to $N_{\text{BLK}}^{\text{ref}} = 14$ to charge the SM capacitors to their nominal voltage, as shown in Figs. 13(a) and (d). The arm and ac-side currents are limited by the changing rate of N_{BLK}, as shown in Figs. 13(b) and (c). After the startup process, the MMC starts to transfer power between ac and dc sides at $t = 2.5$ s.

The ac-side startup process of the FB-MMC system is illustrated in Fig. 14. During Stage I (prior to $t = 0.5$ s), the SMs are uncontrollable and the SM capacitor voltages are charged to their steady-state voltage $V_C^{\text{I,SS}} = \frac{V_{\text{LL}}}{2N_C} = 1.1$ kV. After Stage I, all conducting switches are turned on at $t = 0.5$ s. Consequently, the SM capacitors are charged to their new steady-state voltage $V_C^{\text{ini}} = \frac{V_{\text{LL}}}{N_C} = 2.1$ kV at $t = 1$ s, which is the same as that of the HB-MMC. At $t = 1$ s, the current-limiting resistor is bypassed, and the number of blocked SM

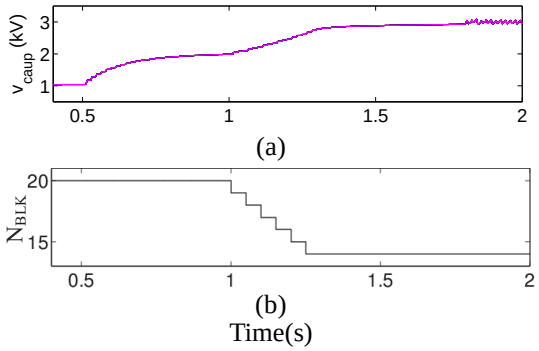

Fig. 14. AC-side startup process of the FB-MMC system: (a) SM capacitor voltages of the phase-a upper arm and (b) the commanded number of blocked SM capacitors within each arm.

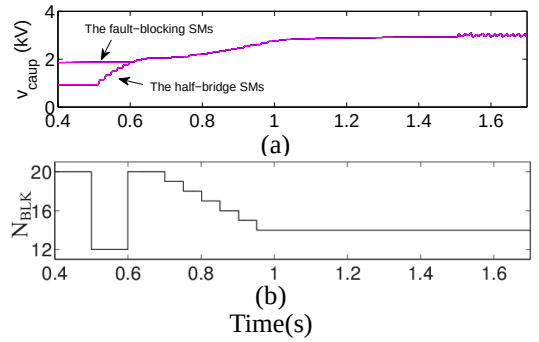

Fig. 15. AC-side startup process of the hybrid MMC system based on HB SM ($N_{\text{HB}} = 12$) and UFB SM ($N_{\text{UFB}} = 8$): (a) SM capacitor voltages of the phase-a upper arm, and (b) the commanded number of blocked SM capacitors within each arm.

capacitors is being dynamically controlled from $N_C = 20$ to $N_{\text{BLK}}^{\text{ref}} = 14$ to charge the SM capacitors to their nominal voltage, as shown in Fig. 14. The arm and ac-side currents are limited by the changing rate of N_{BLK}. After the startup process, the MMC starts to transfer power between its ac and dc side at $t = 1.8$ s. For the UFB, 3LCC, and 5LCC SM-based MMC systems, the startup process is similar to that of the FB-MMC.

The startup process of the CD-MMC is also similar to that of the FB-MMC. However, the uncontrollable steady-state capacitor voltage during Stage I is different. For the CD-MMC, $V_C^{\text{I,SS}} = \frac{V_{\text{LL}}}{1.5N_C} = 1.4$ kV.

For the hybrid MMC consisting of $N_{\text{HB}} = 12$ HB and $N_{\text{UFB}} = 8$ UFB SMs in each arm, the uncontrollable steady-state voltages of the HB and UFB SMs respectively reach $V_{C,\text{HB}}^{\text{I,SS}} = 0.96$ kV and $V_{C,\text{UFB}}^{\text{I,SS}} = 1.9$ kV around $t = 0.5$ based on (13) and (14), as shown in Fig. 15. Subsequent to Stage I, when all conducting switches are turned on while setting $N_{\text{BLK}} = N_{\text{HB}} = 12$ between 0.5 s and 0.6 s, the SM capacitors of the HB and UFB SMs are charged to the same steady-state voltage $V_C^{\text{ini}} = 2.1$ kV at $t = 0.6$ s. After the SM capacitor voltages reach the same value, the current-limiting resistor is bypassed and N_{BLK} is controlled from $N_C = 20$ to $N_{\text{BLK}}^{\text{ref}} = 14$ to charge the SM capacitors to their nominal voltage, as shown in Fig. 15.

C. Startup Process of the MMC-HVDC System

Figure 16 illustrates the startup process of the HB-MMC-HVDC system. Prior to $t = 0.6$ s, both MMC-1 and MMC-2 are in uncontrollable stage while $V_{\text{dc}}^{\text{I}} = V_{\text{dc}}^{\text{II}} = V_{\text{LL}} = 42$ kV, in which the SMs of the two MMCs are charged to the

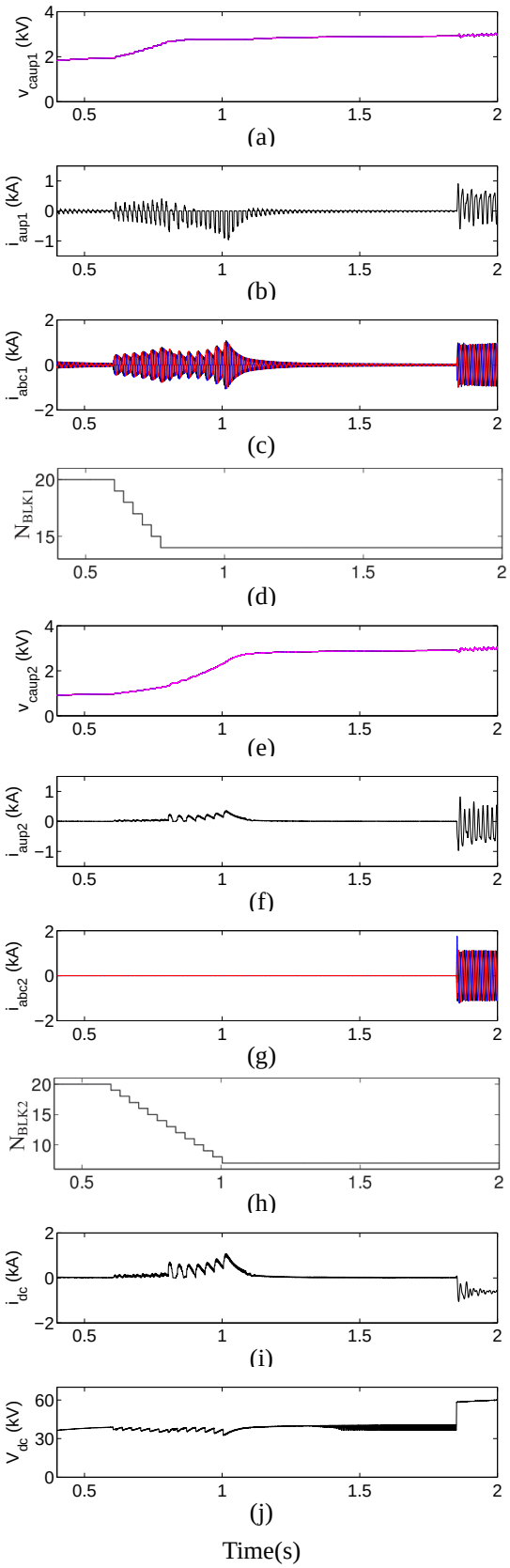

Fig. 16. The startup process of the HB-MMC-HVDC system: (a) SM capacitor voltages of the phase-a upper arm of MMC-1, (b) and (c) phase-a upper arm and ac-side currents of MMC-1, (d) the commanded number of blocked SM capacitors of MMC-1, (e) SM capacitor voltages of the phase-a upper arm of MMC-2, (f) and (g) phase-a upper arm and ac-side currents of MMC-2, (h) the commanded number of blocked SM capacitors of MMC-2, (i) dc current, and (j) dc-bus voltage.

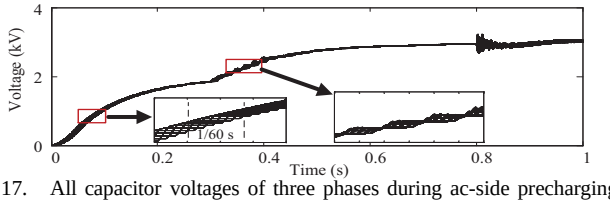

Fig. 17. All capacitor voltages of three phases during ac-side precharging.

uncontrollable steady-stage voltage $V_{C,\mathrm{MMC1}}^{\mathrm{I,SS}} = \frac{V_{\mathrm{LL}}}{N_C} = 2.1$ kV and $V_{C,\mathrm{MMC2}}^{\mathrm{I,SS}} = \frac{V_{\mathrm{LL}}}{2N_C} = 1.1$ kV, respectively, as shown in Figs. 16(a) and (e). After $t = 0.6$ s, both SMs are controllable and the current-limiting resistor is bypassed. The number of blocked SM capacitors is being changed from $N_C = 20$ to $N_{\mathrm{BLK}}^{\mathrm{ref}}$ ($N_{\mathrm{BLK}}^{\mathrm{ref}} = 14$ for MMC-1 and $N_{\mathrm{BLK}}^{\mathrm{ref}} = 7$ for MMC-2) to charge the SM capacitors to their nominal voltages, as shown in Figs. 16(a), (d), (e), and (h). The arm and ac-side currents are limited by the changing rate of N_{BLK}, as shown in Figs. 16(b), (c), (d), (f) and (h). Subsequent to the startup process, the MMC-HVDC system starts to transfer power between two ac systems at $t = 1.8$ s.

For the dc-side precharging, the capacitors of three phases are charged simultaneously. For ac-side precharging, the line-to-line voltages can charge all capacitors within one line cycle. Thus, all capacitors in three phases can be charged almost simultaneously, which will not lead to triple precharging time. As shown in Fig. 17, all capacitors can be charged to their nominal voltage almost at the same time.

In Fig. 18, the startup process of the FB-MMC-HVDC system is shown. As shown in Fig. 18(a), the SMs in MMC-1 are precharged to the uncontrollable steady-state voltage

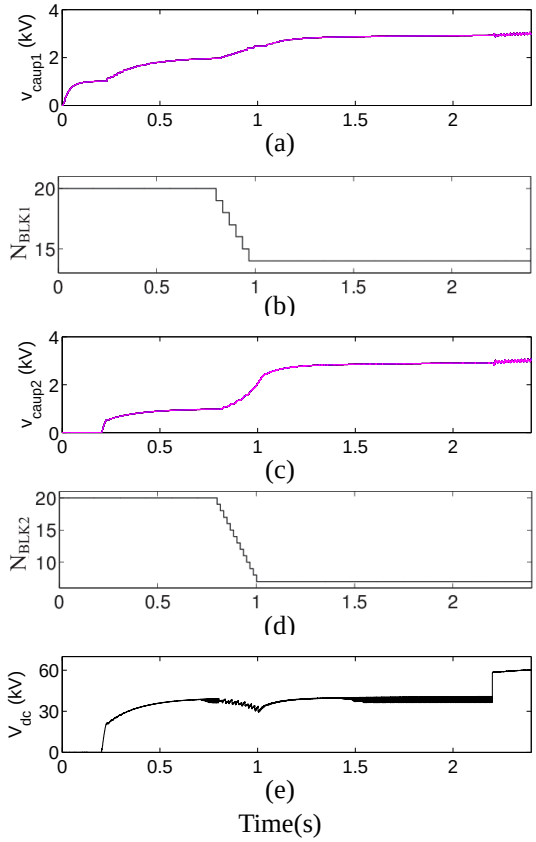

Fig. 18. The startup process of the FB-MMC-HVDC system: (a), (b), (c), and (d) SM capacitor voltages and the commanded number of blocked SM capacitors of the phase-a upper arm of MMC-1 and MMC-2, and (e) dc-bus voltage.

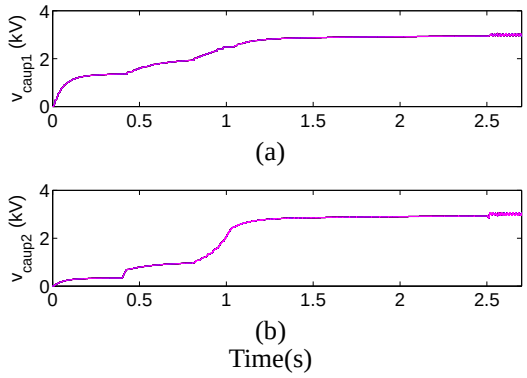

Fig. 19. SM capacitor voltages of the phase-a upper arm during the startup process of the CD-MMC-HVDC system: (a) MMC-1 and (b) MMC-2.

$V_{C,\mathrm{MMC1}}^{\mathrm{I,SS}} = 1.1$ kV (prior to $t = 0.2$), while the steady-state voltage of the SMs in MMC-2 is zero due to $V_{\mathrm{dc}}^{\mathrm{I}} = 0$. After $t = 0.2$ s, the conducting switches of the SMs in MMC-1 are turned on and the SM capacitors of MMC-1 are charged to the new steady-state voltage $V_{C,\mathrm{MMC1}}^{\mathrm{ini}} = 2.1$ kV around $t = 0.8$ s. At the same time, the steady-state dc-bus voltage rises up to $V_{\mathrm{dc}}^{\mathrm{II}} = V_{\mathrm{LL}} = 42$ kV, which charges the SMs in MMC-2 to the steady-state voltage $V_{C,\mathrm{MMC2}}^{\mathrm{ini}} = 1.1$ kV around $t = 0.8$ s, as shown in Fig. 18(c). After $t = 0.8$ s, the SMs in both MMCs are controllable and the current-limiting resistor is bypassed. The number of blocked SM capacitors is being controlled from N_C to $N_{\mathrm{BLK}}^{\mathrm{ref}}$ to charge the SM capacitors to their nominal voltage, as shown in Fig. 18. For the UFB, 3LCC, and 5LCC

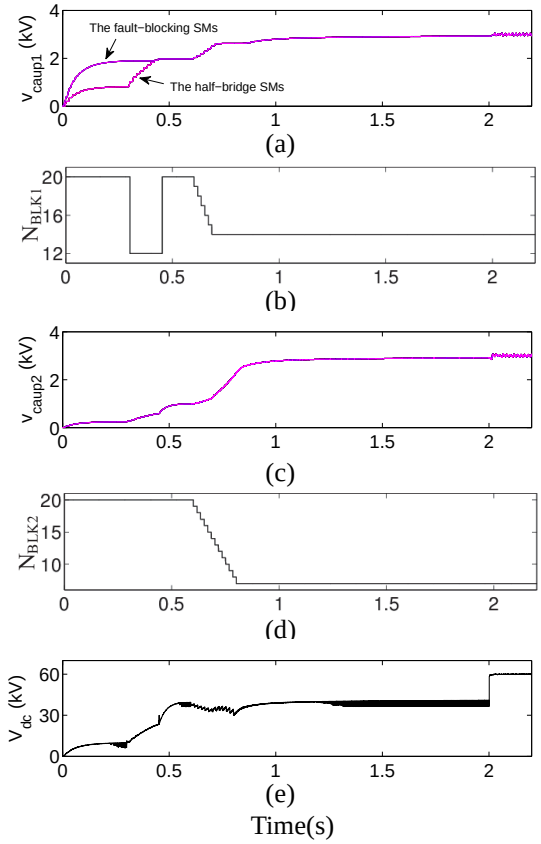

Fig. 20. The startup process of the hybrid MMC-HVDC system with HB SMs ($N_{\mathrm{HB}} = 12$) and UFB SMs ($N_{\mathrm{UFB}} = 8$): (a), (b), (c), and (d) SM capacitor voltages and the commanded number of blocked SM capacitors of the phase-a upper arm of MMC-1 and MMC-2, and (e) dc-bus voltage.

SM-based MMC-HVDC systems, the startup process is similar to that of the FB-MMC-HVDC system.

For the CD-MMC-HVDC system, the startup process is similar to that of the FB-MMC-HVDC system. The difference is the dc-bus voltage $V_{\mathrm{dc}}^{\mathrm{I}} = \frac{1}{3}V_{\mathrm{LL}} = 14$ kV. Thus, $V_{C,\mathrm{MMC2}}^{\mathrm{I,SS}} = 0.35$ kV, as shown in Fig. 19.

In Fig. 20, the startup process of the hybrid MMC-HVDC system is shown, which consists of $N_{\mathrm{HB}} = 12$ HB and $N_{\mathrm{UFB}} = 8$ UFB SMs. At $t = 0.3$ s, the SMs in MMC-1 are precharged to the uncontrollable steady-state voltage $V_{C,\mathrm{HB}}^{\mathrm{I,SS}} = 0.96$ kV for the HB SMs and $V_{C,\mathrm{UFB}}^{\mathrm{I,SS}} = 1.9$ kV for the UFB SMs based on (13) and (14), while the uncontrollable steady-state voltage of the SMs in MMC-2 is $V_{C,\mathrm{MMC2}}^{\mathrm{I,SS}} = \frac{V_{\mathrm{dc}}^{\mathrm{I}}}{2N_C} = 0.29$ kV due to $V_{\mathrm{dc}}^{\mathrm{I}} = 11.5$ kV based on (21), as shown in Figs. 20(a) and (e). From $t = 0.3$ s, all conducting switches of the SMs in MMC-1 are turned on and the number of blocked SM capacitors of MMC-1 is changed to $N_{\mathrm{BLK1}} = N_{\mathrm{HB}} = 12$ so that the SM capacitors of the HB and UFB SMs of MMC-1 are charged to the same steady-state voltage $V_{C,\mathrm{MMC1}}^{\mathrm{ini}} = 2.1$ kV, as shown in Figs. 20(a) and (b). Once the capacitor voltages of the HB and UFB SMs in MMC-1 reach the same voltage 2.1 kV, $N_{\mathrm{BLK1}} = 20$. At the same time, $V_{\mathrm{dc}}^{\mathrm{II}} = V_{\mathrm{LL}} = 42$ kV and, consequently, $V_{C,\mathrm{MMC2}}^{\mathrm{ini}} = 1.1$ kV, as shown in Figs. 20(c) and (e). Subsequent to $t = 0.6$ s, the current-limiting resistor is bypassed and the number of blocked SM capacitors is being changed from N_C to $N_{\mathrm{BLK}}^{\mathrm{ref}}$ to charge the SM capacitors to their nominal voltage.

VII. Experimental Verification

TABLE II
The System Parameters of the Experimental Prototype

SM type	Full-bridge
Number of SM per arm	4
SM capacitor	1000 μF
Arm filter inductor	5 mH
Current-limiting resistor	17.5 Ω

A scaled-down prototype has been built to verify the proposed precharging strategy. The main circuit parameters are listed in Table II. The photo of the experimental prototype is shown in Fig. 21. The prototype configurations of ac-side precharging and dc-side precharging are shown in Figs. 22(a) and (b), respectively. For ac-side precharging, the ac-side line-to-line voltage is 50 V and the nominal capacitor voltage is 35V. For dc-side precharging, the dc source voltage is 160

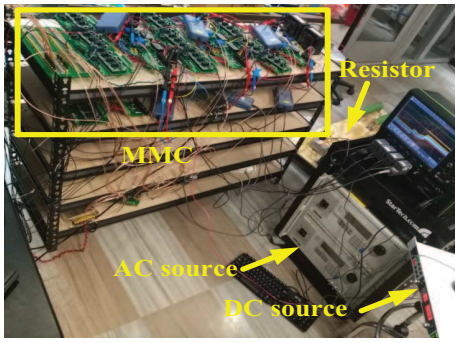

Fig. 21. The experimental prototype

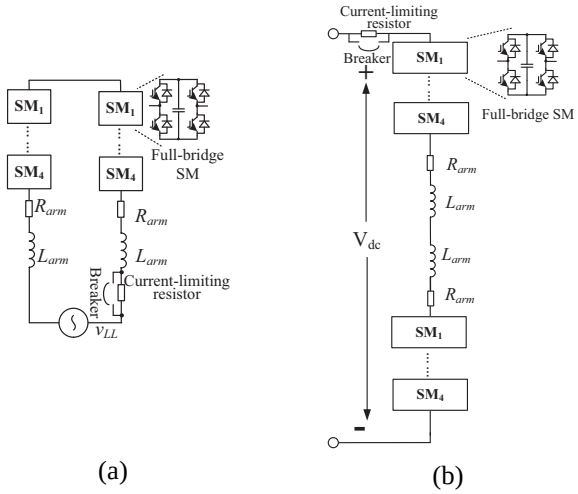

Fig. 22. The experimental prototype configuration of the FB-MMC (a) charging from ac source, and (b) charging from dc source.

V and the nominal capacitor voltage is 40 V. As shown in Fig. 23, when N_{BLK} is gradually reduced from 4 to 2, the SM capacitors can be charged smoothly to their nominal voltages. Thus, the experimental results of Fig. 23 verify the effectiveness of the proposed precharging strategy.

VIII. Conclusion

In this paper, a generalized precharging strategy is proposed for the MMC-based systems built upon various SM circuits under ac- and dc-side startup conditions. The uncontrollable steady-state capacitor voltages of various MMC-based systems are investigated for potential use of SM design. Based on the proposed precharging strategy, a generalized soft start procedure for various MMC-HVDC configurations is also proposed. The proposed startup strategy can smoothly charge the SM capacitors without using any additional feedback control loop, extra measurements and/or auxiliary power supplies. Moreover, the proposed strategy is also applicable to the black start applications. Effectiveness of the proposed strategy for various MMC/MMC-HVDC systems under ac- and dc-side startup conditions, is evaluated based on time-domain simulation studies in the PSCAD/EMTDC software environment and experimental results. The study results demonstrate the proposed strategy can charge the SM capacitors smoothly and limit the inrush charging current during the startup process for various MMC and MMC-HVDC configurations under different startup conditions.

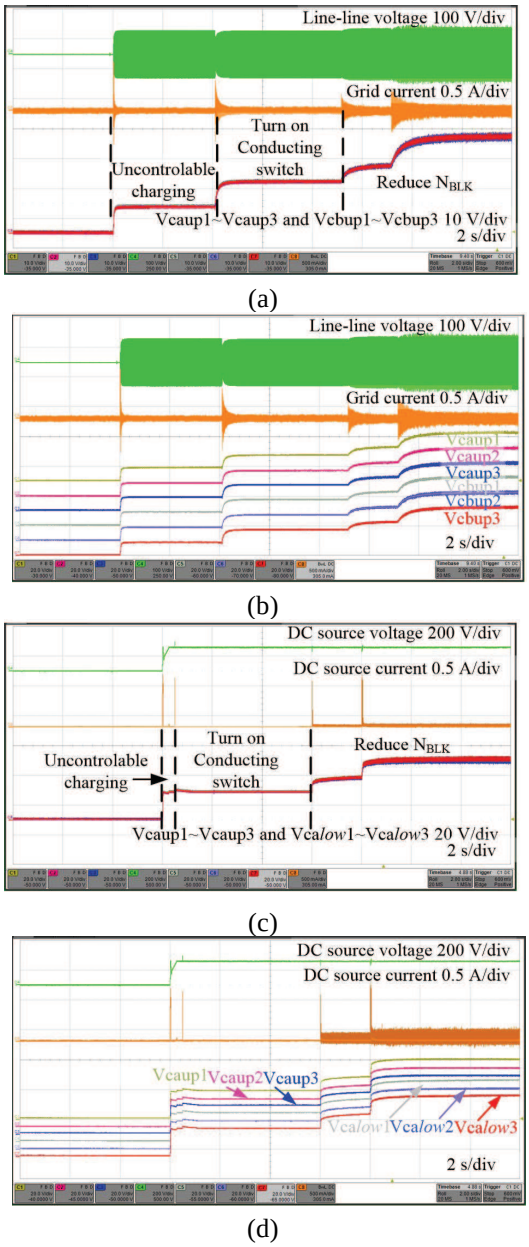

Fig. 23. The experiment results of the FB-MMC: (a) and (b) charging from ac source, (c) and (d) charging from dc source.

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