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Feasibility of a “4H” X-ray camera based on GaAs:Cr Sensor

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ABSTRACT: A multilayer stacked X-ray camera concept is described. This type of technology is called ‘4H’ X-ray cameras, where 4H stands for high-Z ($Z > 30$) sensor, high-resolution (less than 300 micron pixel pitch), high-speed (above 100 MHz), and high-energy (above 30 keV in photon energy). The components of the technology, similar to the popular two-dimensional (2D) hybrid pixelated array detectors, consists of GaAs:Cr sensors bonded to high-speed ASICs. 4H cameras based on GaAs also use integration mode of X-ray detection. The number of layers, on the order of ten, is smaller than an earlier configuration for single-photon-counting (SPC) mode of detection [Z. Wang, *JINST* **10** (2015) C12013]. High-speed ASIC based on modification to the ePix family of ASIC is discussed. Applications in X-ray free electron lasers (XFELs), synchrotrons, medicine and non-destructive testing are possible.

KEYWORDS: 4H X-ray camera; Integration mode; Stacked hybrid 2D detector architecture; GaAs:Cr Sensor.

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1. Introduction

Material characterization and discoveries on the mesoscale require both an intense source of penetrating illumination and detectors that can effectively capture the signals. In X-ray free electron lasers (XFELs), relativistic electrons move through a straight undulator and emit coherent X-rays in a single pass. Several features of XFELs have made them indispensable in structure determination of polycrystalline and non-periodic materials [1]: the energies of photons exceed a few keV that allow 3D structure determination (in contrast to 2D surface imaging); the number of photons reaches 10^{12} to 10^{13} per pulse (10^{10} - 10^{11} photons per μm^2); individual photon pulses last a few to 100 fs that remove motion blur due to thermal or ballistic atomic motion; and transverse coherent length is comparable to X-ray absorption length, which can be 10's of microns.

Two-dimensional (2D) hybrid pixelated area detectors (PADs) are among the most widely used detector architectures so far in XFEL applications [2, 3]. Examples of 2D hybrid PADs include CS-PAD [4], AGIPD [5], Keck PAD [6], LPD [7], JUNGFRU [8] and others. A pixelated semiconductor X-ray sensor (front end) is bonded to a pixelated application specific integrated circuit (ASIC) back end in a 2D hybrid PAD. X-rays produce electron-hole pairs in the semiconductor sensor. The induced electric charge are collected from the front end as signals and turned into digital signals by the ASIC. The hybrid architectures allow flexible selections of sensors and ASIC to meet different detection needs in XFEL experiments ranging from photon counting, spectroscopy, imaging, to their combinations such as spectroscopic imaging. Although the sensor selection has been tilted towards high-resistivity silicon, larger atomic number (Z) sensors such as GaAs:Cr and CdTe have seen increased uses in particular in synchrotron facilities. The highest XFEL photon energy is currently below 30 keV and silicon sensor is sufficient. Some other salient features of

2D hybrid X-ray imagers include large dynamic range, good signal-to-noise/contrast, fast data processing, digital data output, compatibility with industrial CMOS and bonding processes. Steady advances in scalable, low-cost bonding technologies also favor 2D hybrid PAD development. One of the notable development is the low-temperature direct bonding interconnect (DBI) technology that allows pixel pitch below 10 micron, or a bonding density exceeding 1 million connections per square centimeter by Zipotronix (recently acquired by Tessera Technologies, Inc.).

Motivated by the detector needs for higher energy XFELs such as the proposed MaRIE XFEL facility with a minimum photon energy of 30 keV and up to 126 keV in the third harmonic, as well as faster PADs for high-energy X-ray experiments in synchrotrons, we describe the concept of a ‘4H’ camera based on 2D hybrid architecture. Here ‘4H’ is defined as high-Z ($Z > 30$) sensor, high-resolution (less than 300 micron pixel pitch), high-speed (above 100 MHz frame-rate equivalent in burst mode), and high-energy (above 30 keV in photon energy). The proposed high-Z sensor will be GaAs:Cr developed by Tomsk State University (TSU). The proposed ASICs will be based on the ePix family of integrated circuits under development by SLAC. Other existing ASICs may also be used with some modifications. Below, we first discuss the working principle of a 4H camera based on a *stacked multilayer* PAD, followed by the discussions on GaAs:Cr sensors and then an ASIC possibility.

1.1 The design principle

A multilayer detector concept for XFEL applications was described recently [9]. In the earlier work, the use of silicon sensors for high-energy photons (42 keV and above) was emphasized. Due to the combination of Compton scattering physics for high-energy X-ray photons in silicon, the simultaneous requirements of high detection efficiency and high speed, single-photon counting (SPC) mode of detection is preferred. To achieve SPC mode in XFELs requires silicon sensor thickness to be below 100 μm and even thinner ASICs to minimize the attenuation of X-rays in ASICs. In this work, we propose the use of GaAs sensor instead. As shown in Fig. 1, Compton scattering fraction in GaAs is less than 5% for photon energies less than 80 keV and the X-ray attenuation is dominated by photoelectric absorption (PE). This fact allows the design of multilayer stacked detector configuration that operates in the integration (INT) mode, similar to the existing 2D hybrid PADs using silicon. A comparison of the N -layer stacked design with a single-layer design is summarized in Table.1.

1.2 Multilayer stacked configuration

Two multilayer stacked configurations with a fixed total GaAs thickness of 1000 μm are compared in Fig. 1. The first configuration corresponds to an individual GaAs sensor thickness of 250 μm . The second configuration corresponds to a layer thickness of 100 μm . In both cases, the total GaAs thickness is fixed at 1000 μm , which gives more than 50% of X-ray attenuation for photon energies exceeding 60 keV.

Another interesting observation is that relatively thick ASIC layer (assumed to be primarily silicon) of around 100 μm thick can be used. This is due to the large discrepancies in X-ray attenuation in Si and in GaAs. The full X-ray attenuation in Si ASIC is less than 5% in both cases. Since we have assumed constant GaAs sensor thickness for different layers in Fig. 1, the amount

Table 1. A comparison of a single-layer with an N -layer 2D hybrid detector. N_0 is the number of X-ray photons. u_d is a characteristic charge drift time. M_d is the number of dark pixels for a single-layer camera.

Parameters	Single-layer	N -layer
Sensor thickness per layer	T_0	T_0/N
Sensor response time	T_0/u_d	T_0/Nu_d
Dynamic range	N_0	N_0/N
Plasma effect	$\propto N_0$	$\propto N_0/N$
Full depletion bias	V_0	$\geq V_0/N$
Spatial resolution	pixel size	pixel size
Radiation hardness	excellent	excellent
Dark pixels	M_d	NM_d
Bonding	solder bumps/DBI	DBI preferred

of X-ray collected in the first layer is several times the second layer and so forth. In practice, layer thicknesses may be adjusted for different layers to allow comparable X-ray absorption for each layer or N_0/N photons per layer as listed in Table. 1. There are advantages to do so. For example, the X-ray induced signals in each layer will be better matched to the dynamic range of the ADC and allow reduced ADC dynamic range in each layer. The adjustable sensor thickness scheme depends on how thin of a GaAs and ASIC is practically achievable, which will be discussed in Sec. 2.3 below.

2. GaAs:Cr sensor

2.1 Recent thick ($> 500 \mu\text{m}$) sensor development

Previous investigations showed that pixelated sensors based on chromium compensated gallium arsenide (GaAs:Cr) are promising for high-energy X-ray imaging [10, 11, 12]. Detector-grade GaAs:Cr materials were obtained from low-resistivity gallium arsenide (n-GaAs) compensated with Cr atoms using high-temperature annealing. Chromium atoms, which are deep acceptors, diffuse in n-GaAs and compensate both shallow and deep (EL2-centers) donors. As a result, high-resistivity GaAs:Cr are formed with highly uniform resistivity distribution and uniform electric field distribution across the full sensor thickness [13]. The GaAs:Cr processing technology developed by TSU allows sensor thickness up to 1 mm while maintaining resistivity of about $10^9 \text{ Ohm}\cdot\text{cm}$ [14]. Compared to semi-insulating (SI) liquid encapsulated Czochralski (LEC) GaAs sensors, in which fluctuations of count rate are observed due to instability of electric field, GaAs:Cr sensors by TSU can maintain more stable count rate. This property permits the use of simple methods of flat field correction to obtain high quality X-ray images, which has been confirmed experimentally [11].

GaAs:Cr PADs have also been demonstrated using HEXITEC [10] and Medipix3RX ASICs [11]. The energy resolution for 60 keV photons is as small as 3 keV. It was shown that radiation hardness of GaAs:Cr sensors irradiated with 12 keV X rays exceeds 300 Mrad [15]. Experimentally, it was also found that there is no polarization effects in GaAs:Cr sensors if the photon flux density is in the range of 9×10^7 to $1.5 \times 10^{10} \text{ photons}/(\text{s}\cdot\text{mm}^2)$, which compares favorably with Cd(Zn)Te sensors.

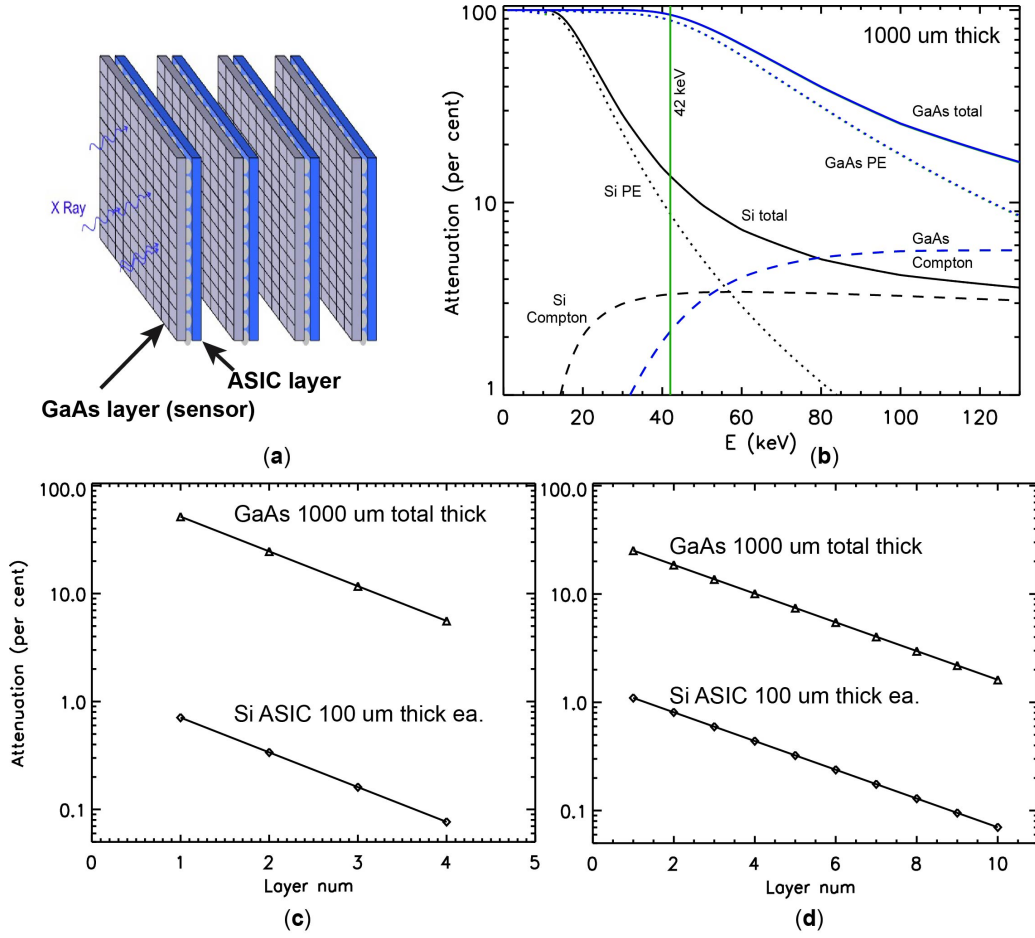


Figure 1. (a). A high-Z (GaAs) multiple layer camera concept that consists of 4 separate pixelated detectors; (b). Comparison of X-ray energy-dependent attenuation due to photoelectric absorption (PE), incoherent (Compton) scattering and total scattering (the sum of PE, incoherent and coherent scattering) in Si and GaAs sensors. The sensor thickness is 1000 μm . At 42 keV, PE still dominates the attenuation in GaAs, while Compton scattering is substantial in Si. (c). X-ray attenuation in each layer for a 4-layer detector structure with GaAs sensor (250 μm thick) bonded to ASIC, which is assumed to be mostly Si of 100 μm thick. (d). X-ray attenuation in each layer for a 10-layer detector structure with GaAs sensor (100 μm thick) bonded to ASIC, which is assumed to be mostly Si of 100 μm thick.

2.2 Thin GaAs:Cr area sensors – 100 to 300 μm thick

The multilayer stacked 4H camera concept motivates examination of the sensor response time for sensor thicknesses below 300 μm . We first study the theoretical charge collection and therefore the sensor response time as a function of GaAs:Cr thickness and pixel size. Fig. 2a shows the calculated electron drift time from cathode to anode in GaAs:Cr sensors as a function of active layer thickness for a mean electric field strength of 5 kV/cm. At this value of electric field strength, the electron drift velocity in GaAs:Cr reaches the maximum around 8.7×10^6 cm/s. The calculation of drift velocity was carried out using an equation given in [15], with the mean value of electron Hall mobility in GaAs:Cr of 4000 $\text{cm}^2/\text{V}\cdot\text{s}$, which correspond to drift mobility of 2500 $\text{cm}^2/\text{V}\cdot\text{s}$. It was found that 100 μm sensor can approach an theoretical operating speed below 2 ns, and 250

μm thick sensor an theoretical response time less than 5 ns.

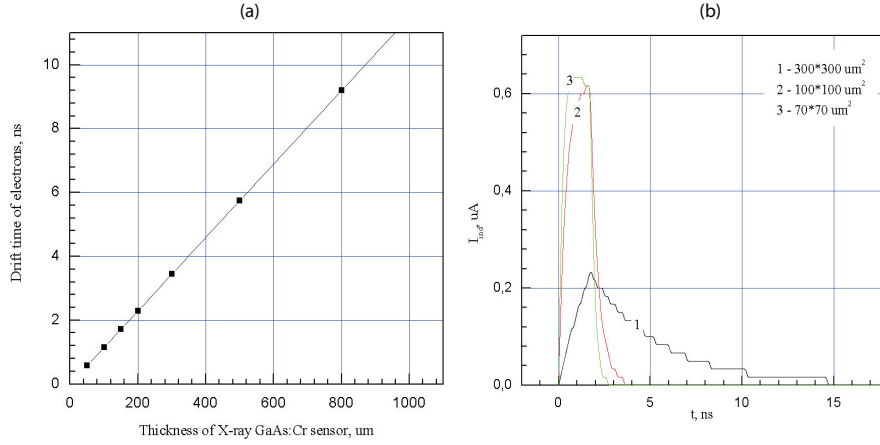


Figure 2. (a) Electron drift time in GaAs:Cr sensors as a function of sensor thickness; (b) Temporal response of 150 μm thick GaAs:Cr sensors with different pixel sizes.

The output pulse shape and therefore the sensor time response are also affected by pixel capacitance, input resistivity of pre-amplifier and others. In Fig. 2b, the pixel capacitance was calculated for the active layer thickness of 150 μm and different pixel sizes: 70×70 , 100×100 , $300 \times 300 \mu\text{m}^2$. The input resistance of the preamplifier was 60 kOhm. The preamplifier's input capacitance was ignored here. We also assumed that the electron lifetime is 20 ns and the hole lifetime is 1 ns. It can be seen that to obtain the operating speed of 2 ns, the pixel size should be no more than $100 \times 100 \mu\text{m}^2$ for a 150- μm thick sensor.

The results of experimental investigation of pulse characteristics of GaAs:Cr PAD sensors with different bias voltages are presented in Fig. 3. Alpha particles (5.5 MeV) from an ^{241}Am source were used to generate electron-hole pairs.

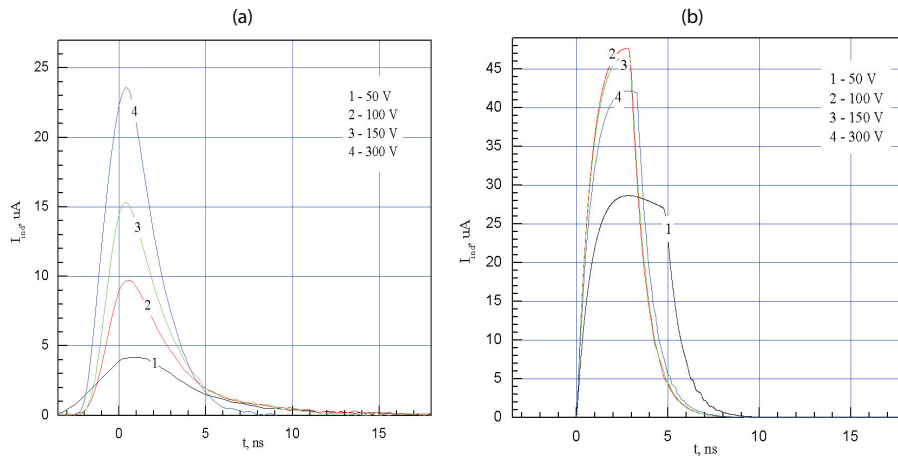


Figure 3. Experimental (a) and calculated (b) dependencies of induced current pulse width on applied bias when a 250 μm thick GaAs:Cr PAD is irradiated from the cathode side with 5.5 MeV alpha-particles.

The active area of GaAs:Cr PAD sensors was 0.1 cm^2 . The distance between the α -source and

the sensor was 1 cm. The stopping distance of the alpha-particle with an initial 5.5 MeV energy in GaAs doesn't exceed 25 μm . The total energy loss of an 5.5 MeV α -particle after going through 1 cm of air and 0.2 μm metal film (Au) is estimated to be 1.3 MeV. The polarity of applied bias on the irradiated contact was chosen so that electrons drifted across the full sensor thickness. The signal from the sensor was magnified by a preamplifier (analog bandwidth $\Delta F_{\text{amp}} = 1$ GHz, gain ratio $K = 21$ dB, input resistance $R_{\text{in}} = 224$ Ohm) and was recorded with Tektronix 3552 oscilloscope (analog bandwidth $\Delta F_{\text{amp}} = 500$ MHz).

The experimental results in Fig. 3 indicate that the durations of the measured pulses exceed the calculated values of 2-3 ns. The measured current pulse amplitudes I_{ind} do not saturate as expected from the calculations. The measurements are lower than the calculated values of I_{ind} for the same bias voltages. As discussed previously [16], one possible cause of the differences may be due to the plasma effect caused by heavily ionizing alpha particles.

To further elucidate the differences in electron-hole generation and collection between α -particles and high-energy photons, Fig. 4 shows the experimental charge collection efficiency (CCE) of GaAs:Cr PAD sensors irradiated with different ionizing radiations. It can be seen that the CCE values of GaAs:Cr PAD sensor irradiated with alpha particles are much smaller than the CCE values of high-energy photons at similar bias voltages. One possible explanation is related to higher concentration of electron-hole pairs along the track of an alpha particle. The electron-hole plasma cloud screens the external electric field, and as a result, the electron-hole recombination rate and charge loss increase. It's been estimated that the plasma screening time could takes up to 30% of nonequilibrium charge carrier lifetime [17] and a significant decrease in the CCE values for alpha particles are anticipated. Since high-energy X rays has a smaller stopping power that alpha particles, the plasma effect can be much less (up to a factor of 10^3). Furthermore, in the multilayer stacked configuration, the incoming X-ray flux can be divided into N layers as shown in Table. 1, which can in-turn reduce the charge density by a factor of N . Both the lower charge density for individual X-ray photons and the multilayer configuration will be useful features to reduce plasma shielding effects and enhance charge collection in high-energy X-ray imaging.

2.3 Some practical issues with thin sensors

The thinnest GaAs wafer from TSU is around 250 μm for the time being. Thinner GaAs wafers are too fragile mechanically to perform direct flip-chip bonding with an ASIC. There are two possible approaches to obtain GaAs pixelated sensors around 100 μm in thickness: a.) To directly grow epitaxial GaAs: Cr layer on an ASIC; and b.) To apply backside thinning process after flip-chip bonding of a thicker GaAs: Cr pixel sensors to an ASIC. The growth of an epitaxial GaAs:Cr on an silicon ASIC (~ 100 μm thick) has never been attempted before. The backside thinning process is well-known and no fundamental issue is expected to implement. The latter requires the industrial accessible flip-chip bonding process prior to backside etching of GaAs: Cr pixel sensor. In short, backside thinning approach is feasible to achieve 100 to 250 μm sensor thickness for the multilayer stacked configuration as shown in Fig. 1.

To minimize the X-ray losses to ASIC and bonding pads that are exposed to X-rays in a multilayer configuration, it is also desirable to minimize the material use in bonding. Current technologies to manufacture GaAs: Cr material and sensors developed by TSU, produce sensors with dimensions of 70×70 mm² with a pitch of 35 μm and a thickness of the sensitive layer up

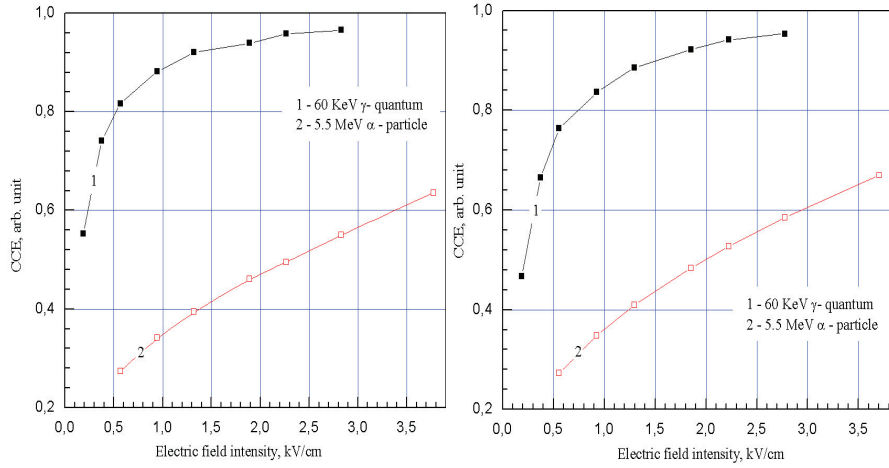


Figure 4. Experimental CCE dependences on bias of GaAs:Cr PAD sensors irradiated with different ionizing radiations: 1 - 60 keV gamma-quanta, 2 - 5.5 MeV alpha-particles. (Left) 520 μm sensor thick and (Right) 540 μm sensor thick.

to 1 mm. The sensors are suitable for further assembly with ASIC by flip-chip (pixel sensors) or ultrasonic wire bonding (microstrip sensors). In-house capabilities at TSU can be combined with industrial partners to accomplish the goal.

3. Application Specific Integrated Circuits (ASICs)

In 2D hybrid X-ray PADs, signals generated in individual pixels are processed in parallel and in sequential steps: signal integration (for INT mode), filtering, sampling, and storage. In many cases, the storage is performed in the analog domain (analog memories or capacitors in each pixel) before sampling and digital storage. Signals with repetition rates up to one MHz (LCLS, LCLS-II) can be read out continuously frame by frame, and they require thus only few single memory elements. Higher repetition rates usually operate in burst mode with high frequency pulse trains (around 5 MHz at the Eu-XFEL) separated by long idle times in which the detectors can be readout. Burst-mode sources require at least the same number of memory elements per pixel as the number of image frames. Here we discuss the feasibility of using burst mode for a 4H camera to achieve 100 MHz frame rate for around 10 frames of images.

3.1 SLAC X-ray Signal Processors (SXSP) family of ASICs

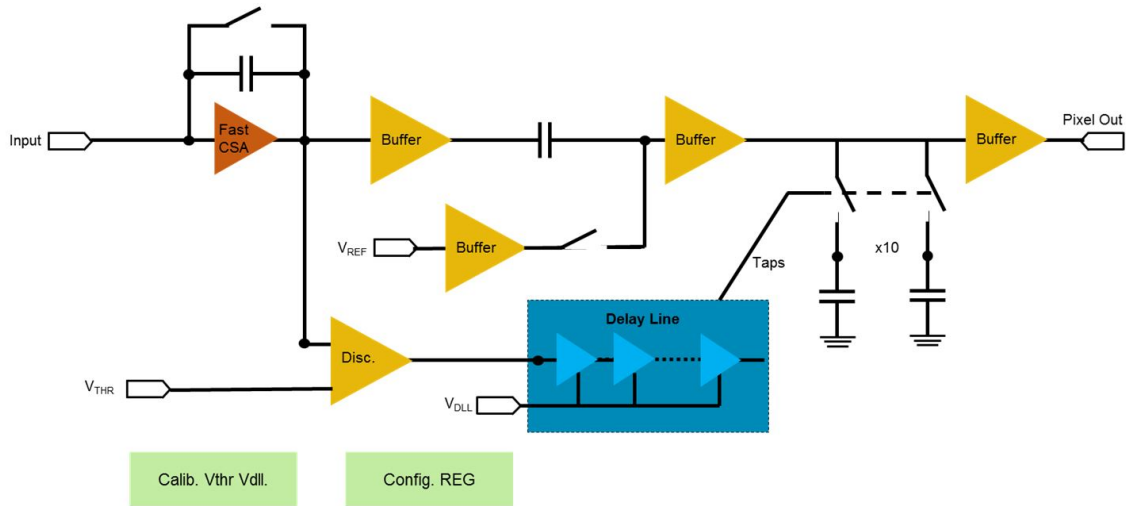
SLAC X-ray Signal Processors (SXSP) family consists of three categories of ASICs: one that measures energies for imaging or spectroscopy (ePix) [18], one that is designed for fast timing for time-of-flight applications (tPix) and one that is dedicated to photon counting applications (cPix). Each category has several variants and a total of 12 variants have been or are under development. Specifications of a selection of ePix platform based ASICs are reported in Table 2. ePix100 is optimized for ultra-low noise imaging applications, ePix10k is optimized for high dynamic range imaging applications, while ePixS is optimized for spectroscopy. tPix is instead optimized for sub-nanosecond time-of-flight (ToF) applications.

Table 2. ePix Platform based ASICs specifications and performance.

ASIC	ePix100	ePix10k	ePixS	tPix
Mode of op.	INT	INT (auto ranging)	INT	ToF
Pixel size (μm^2)	50×50	100×100	500×500	100×100
Array size (pixels)	352×384	176×192	10×10	176×192
Frame rate	5 kHz	5 kHz	30 kHz	1 kHz
	(120 Hz w/o ADC)	(120 Hz w/o ADC)		
Dynamic range	220 ke^-	22 Me^-	22 ke^-	2 keV (thresh.)
Dynamic range (8 keV ph)	100	10k	10	1
ENC (r.m.s.)	50 e^-	120 e^-	8 e^-	N/A
Time res.	N/A	N/A	N/A	100 ps/ $1 \mu\text{s}$ 1 ns/ $10 \mu\text{s}$

3.2 ePix Δ : an ultrafast ASIC concept for imaging at above 100 MHz frame-rate in burst mode

Among the variant of the ePix ASICs under study, one in particular has potential to meet the needs of experiments requiring ultra-high frame-rate imaging for short burst. As an example, recording shockwave propagation in high-energy density experiments would benefit from a camera capable of acquiring few (10-30) frames at intervals from 10ns down to 300ps. Based on the ePix platform and reusing some of the solutions adopted in tPix, ePix Δ features fast analog waveform capturing per pixel on an array of storage capacitors. A movie would be constructed by taking the difference between successive data points. Fig. 2 show a simplified block diagrams of the pixel architecture of ePix Δ ,

**Figure 5.** The simplified block diagram of the ePix Δ pixel (charge integrating configuration).

Operating synchronously with the XFEL source, a wide-bandwidth charge integrator extracts the signal from a fast sensor over the entire burst. A Correlated Double Sampler subtracts baseline variations and kTC from the amplifier output which is the sampled using a delay line with con-

trollable delays onto an array of capacitors. A master Delay Locked Loop in the periphery of the ASIC allows programmable delays from 10 ns down to 300 ps, similar to the one developed for the tPix ASIC (100ps). The number of recorded frames will depend on the storage depth, which will impose a trade off with the pixel size. In this particular configuration in which the charge preamplifier is not reset between subsequent frames the integral of the subsequent frames is recorded and the difference is extracted during the readout phase. Alternatively a wide-band trans-impedance preamplifier can be used to record frames independently. Both alternatives have interesting characteristics and impose different trade-offs among settling time, current consumption and input signal range. The trade-offs are largely dependent on the amplifier architectures. To study these dependences, a charge pre-amplifier (Fig. 6a) composed of a fast common source stage and a follower has been designed and simulated using an ideal model for the sensor with collection time of 700 ps. Some initial results are here reported to underline the dependences.

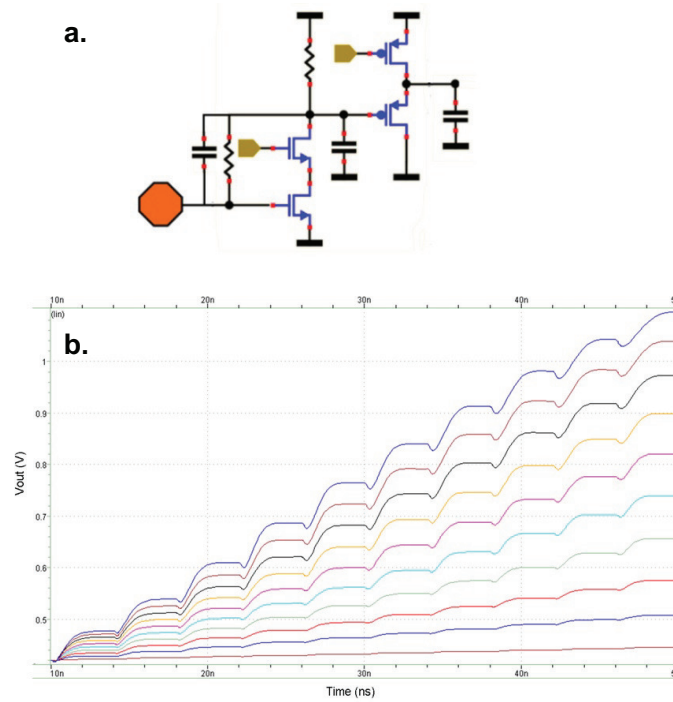


Figure 6. a) Simplified block diagram of the test charge preamplifier. b) Output response after 10 pulses at different values of charge (1.3fC – 32.5fC).

The feedback capacitor was sized to integrate up to 10 pulses of 32.5fC (25ph@30keV) at a burst rate of 250MHz (Fig. 6b). Adopting a stacked approach with 4-10 layers properly thinned in order to obtain a uniform photon distribution, these specification should allow a dynamic range of 100ph-250ph at 30keV. In this particular configuration the preamplifier consumes $180\mu\text{A}$ of current. To run the same amplifier keeping the same dynamic range at a burst rate of 500MHz the current consumption increase up to $400\mu\text{A}$. Instead to run the amplifier with increased dynamic range up to 100ph at 30keV (400ph-1000ph at 30keV, adopting a stacked approach with 4-10 layers) keeping the rate constant, require a current of $282\mu\text{A}$. Like in the other variants of ePix ASICs the in-pixel digital activity is minimal to avoid potential sources of cross-talk. Sources

operating in burst mode have usually long idle time between bursts allowing long time for the read-out of the pixel information. Analog-to-digital conversion will be done outside the chip. When using ePixΔ minimizing digital activity and thus components in the beam path also minimize X-ray attenuation.

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