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On Field-Effect Photovoltaics: Gate enhancement of the power conversion efficiency in a nanotube/silicon-nanowire solar cell

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Abstract

Recent years have seen a resurgence of interest in crystalline silicon Schottky junction solar cells distinguished by the use of low density of electronic states (DOS) nanocarbons (nanotubes, graphene) as the metal contacting the Si. Recently, unprecedented modulation of the power conversion efficiency (PCE) in a single material system has been demonstrated in such cells by the use of electronic gating. The gate field induced Fermi level shift in the low DOS carbon serves to enhance the junction built-in potential, while a gate field induced inversion layer at the Si surface, in regions remote from the junction, keeps the photocarriers well separated there, avoiding recombination at surface traps and defects (a key loss mechanism). Here we extend these results into the 3rd dimension of a vertical Si nanowire array solar cell. A single wall carbon nanotube layer engineered to contact virtually each n-Si nanowire tip extracts the minority carriers, while and an ionic liquid electrolytic gate drives the nanowire body into inversion. The enhanced light absorption of the vertical forest cell results in a 100 mW/cm^2, AM1.5G short-circuit current density of 35 mA/cm^2 and associated power conversion efficiency of 15%. These results highlight the use of local fields as opposed to surface passivation as a means of avoiding front surface recombination. A deleterious electrochemical reaction of the silicon due to the electrolyte gating is shown to be caused by oxygen/water entrained in the ionic liquid electrolyte. While encapsulation can avoid the issue, a non-encapsulation based approach is also implemented.

Introduction

Active modulation of the power conversion efficiency (PCE) in a solar cell by electronic gating has recently been demonstrated, varying the PCE over a broad range spanning ~4 to 11%.[1] This was in a planar nanotube/silicon Schottky junction solar cell in which a liquid electrolyte acted as a capacitive electrolytic gate to induce the modulation. Two principle mechanisms for the action of the gate were identified: 1) modulation of the junction built-in potential due to a gate induced modulation of the nanotube Fermi level (the idea that motivated the work) and 2) modulation of an electric field induced across the Si depletion layer, where the electrolyte made direct contact with the Si through the naturally porous nanotube film. The important role of this electrolyte induced field was highlighted in a follow-on paper where the nanotube film was patterned as a grid to occupy only a fraction of the Si surface, while the electrolyte extended across the entire surface.[2] In the device regions where only the electrolyte contacted the Si, the effect of the gate field was reminiscent of the inversion layers induced in so called "grating metal-insulator-semiconductor" (MIS) cells developed in the 1970s-1980s.[3,4,5] In those early

devices the "grating" consisted of *widely separated* metal lines, which formed Schottky junctions with the underlying Si at the front surface of the cell, while a dielectric incorporating (fixed) trapped charge, deposited over and between the grid lines, created a field that produced the inversion layer at the Si surface. That field confined the minority carriers to the inversion layer, allowing their diffusion to the grid lines where they were collected, while simultaneously repelling the majority carriers. Keeping the photocarriers apart at the surface is particularly important because it avoids photocarrier recombination at surface defects: a key loss mechanisms in solar cells.

The use of such inversion layers in solar cells was pioneered by R. L. Call who in fact first tried to exploit an electronic gate using a gate dielectric and transparent electrode over the regions between grid lines to create the inversion,[6] but who abandoned the effort due to the difficulties of obtaining pinhole free dielectrics over the large areas needed.[7] That led him to replace the gate electrode with trapped charge within the dielectric itself to induce the inversion (a development greatly advanced in the grating MIS cells advanced by Godfrey and Green[3,4]). Recently Zettl and coworkers, exploiting the high quality dielectrics made available by atomic layer deposition, returned to the use of a dielectric/transparent conductor gate to create the inversion, where they made the interesting point that if the collection electrodes are made sufficiently narrow, the gate field can even induce an inversion layer between metal-semiconductor pairs that do not otherwise form Schottky junctions, thus permitting their use in potential solar cells.[8] We note that this benefit extends to electrolytic gates as well, which have the additional advantage of a large gate lever arm due to the high capacitance afforded by their naturally thin Debye layers. Electrolytes also possess another advantage: easy filling of nooks and crannies; a feature that we exploit in the present work.

The cells discussed above were all planar devices; however, a well known method to improve solar cell performance is front surface texturing to enhance light trapping. Exceptional light trapping is provided in vertical Si nanowire (SiNW) array solar cells, recently reviewed by Garnett *et al*.[9] and by Li.[10] However, despite the greatly improved light absorption in such devices the best PCEs reported until quite recently hovered around 10%.[11,12,13,14] The exception is carefully passivated SiNW p-n junction cells recently reported to exhibit a PCE~17%.[15] These however require the high temperature processing associated with emitter diffusion and creation of the thermal oxide passivation layer, both requiring temperatures of 850^{o}C. Here we demonstrate a nanotube/SiNW junction solar cell in which the nanotube layer contacts predominantly the tips of the nanowires in an etched Si nanowire array. By exploiting a volume filling, liquid electrolyte gate we attain a one sun, AM1.5G, PCE of ~15%, with room for further optimization. No processing step in our device fabrication exceeded 80^{o}C.

Results and Discussion

A schematic cross-section of the cell architecture (not to scale) and the wiring diagram for gating and testing is shown in Figure 1a. Figure 1b shows a scanning electron microscopy (SEM) image (45^{o} tilt) of nanowires etched from a Si wafer (process adapted from Peng *et al.*[16]). Figure 1c shows an SEM image (45^{o} tilt) of ~1.5 μm long SiNWs with the single wall nanotube (SWNT) layer. Contact to the SWNT layer was made by an Au/Cr frame, situated on a front surface oxide (200 nm), which surrounded the SiNW region and defined the active area of the cell. The electrolyte used was a drop of 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl) imide (EMI-BTI) ionic liquid. This is indicated in Figure 1a

as having a spheroidal air interface but such a shape would act to concentrate the radiation so, as was the case with our planar cells,[1,2] care was taken to spread the drop to ensure a flat air interface over the region of the cell window. The gate electrode consisted of a coiled Pt wire onto which a thick layer of SWNTs had been deposited, placed within a 2 mm inner diameter polyethylene tube. The small tube was filled with the EMI-BTI electrolyte, retained there by capillary forces. The SWNTs on the Pt wire provided a high surface area electrode to avoid limiting the gate capacitance. The end of this gate electrode was touched to the electrolyte drop (over the Au pad to avoid shadowing light from the active area) connecting the electrolyte reservoirs. Note that this "remote" gate electrode improves on the previous design[1,2] where the gate electrode occupied front surface "real estate" of the Si (thus, in principle, precluding that area's availability for light capture).

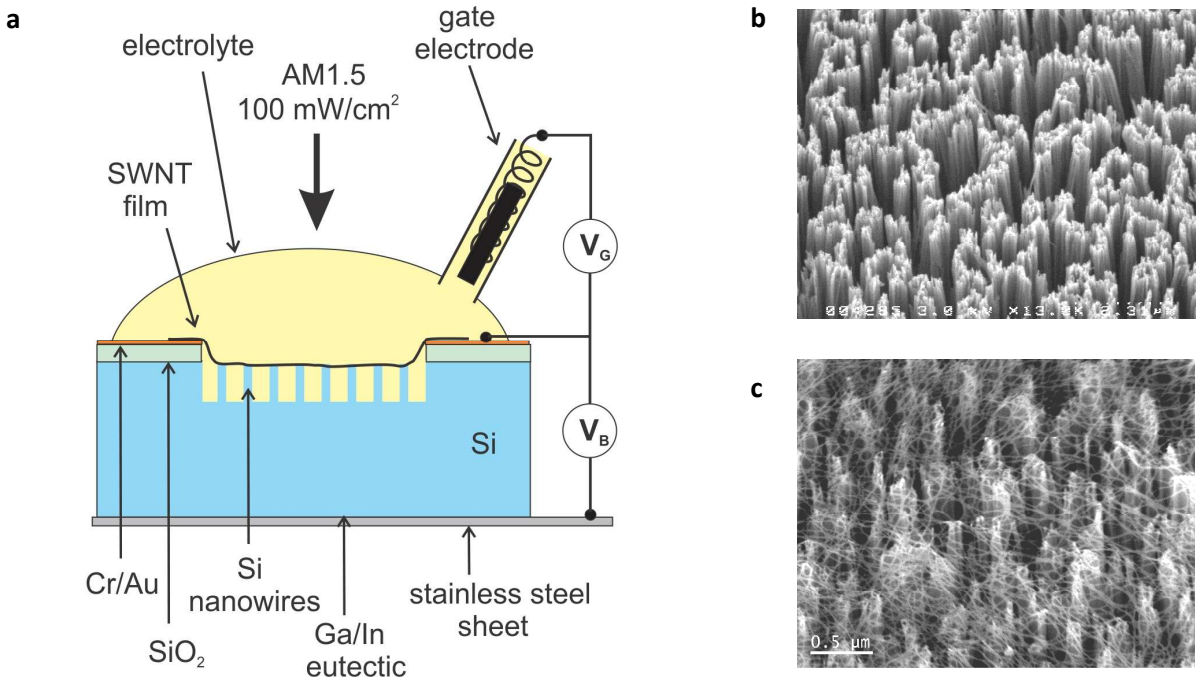

Figure 1. (a) Schematic of the gated SWNT/SiNW devices. V_G is the gate voltage applied to the gate electrode relative to the nanotube junction electrode while V_B is the cell bias voltage applied to the nanotube junction electrode relative to the backside contact used in the device J-V characterization. The semi-spheroidal shape of the electrolyte air interface is for illustration purposes. Care was taken to create a flat interface across the active region to avoid light concentration. (b) SEM image of the typical etched nanowires used in these studies. (c) The SWNT coated SiNWs. Note the contact of the nanotubes to the top of effectively every nanowire.

Figure 2 compares the reflectance of electrolyte coated SWNT/Si structures at near normal incidence. The reflectance for planar Si, both without, and with nanotube film layers (at two thicknesses) are also shown for reference. The reflectivity of the SWNT/SiNW array is exceptionally low, below 4% across the relevant (above bandgap) solar spectrum for Si.

Schottky junction solar cells only became competitive with p-n junction cells once it was realized that a thin insulating passivation layer (the I in so called MIS cells) between the metal and the semiconductor was critical to maximizing performance.[17] The modern understanding of the role of this layer is concisely summarized by Har-Lavan *et al.*[18] with a comprehensive review given by Tung[19]. For carbon nanotube/*planar*-Si cells the benefits of a thin native oxide passivation was noted in the supporting information of Wadhwa *et al.*[2] and studied in some detail for double walled carbon nanotube/planar-Si cells by Jia *et al.*[20] Such passivation is also critical for the SWNT/SiNW cells. If such oxide layers become too thick, however, they present a tunneling barrier that degrades the cell performance. An initially poor performance of SWNT/SiNW cells tested immediately after the nanotube layer deposition suggested that the native oxide had grown too thick during the device fabrication steps. Accordingly, a brief BOE etch of the SiNWs, through the porous SWNT network, was implemented (stripping away the oxide), followed by an oxide regrowth in the ambient air under AM1.5 illumination at 100 mW/cm^2. Figure 3 shows J-V curves for a SWNT/SiNW cell (no EMI-BTI) as a function of time in ambient air/illumination following the BOE etch. The initial measurements exhibited very poor performance; however, the short circuit current density, J_{SC}, open circuit voltage, V_{OC}, and fill factor, FF, were all seen to improve with time up to ~96 h, after which the trends reversed. The series resistance, R_S, obtained from the slope at the highest forward bias was found to grow monotonically while still being low enough at ~96 h that the native

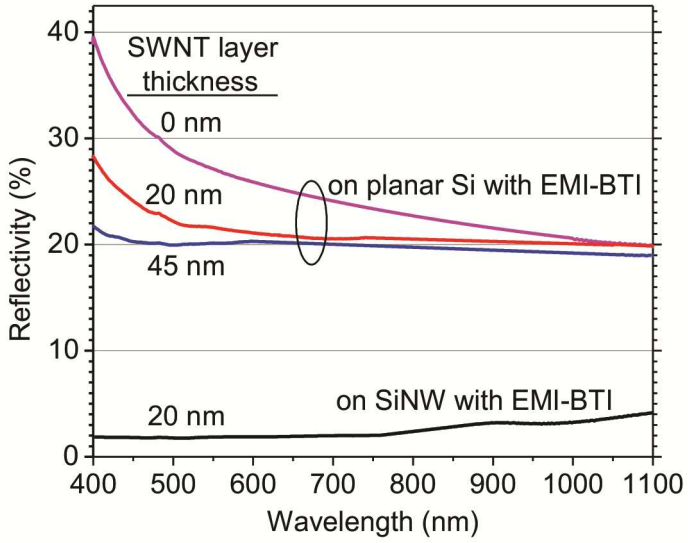

Figure 2. Reflectance of EMI-BTI coated silicon structures (planar and SiNW) with the nanotube layer thicknesses indicated.

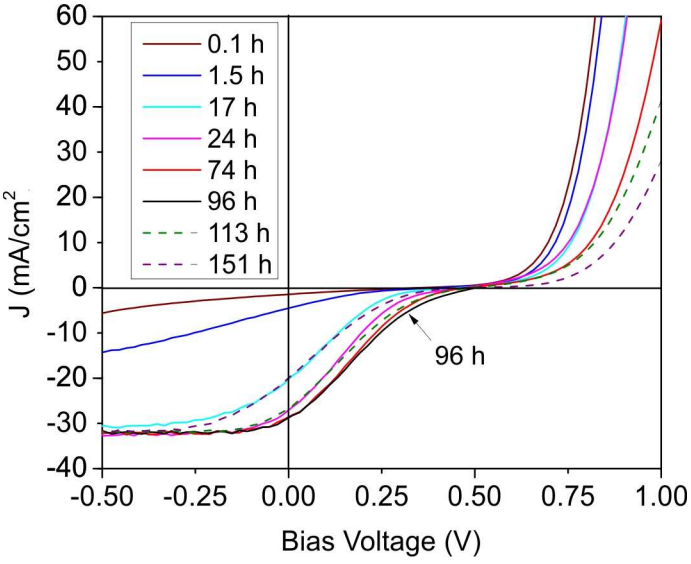

Figure 3. SWNT/SiNW cell J-V curves under 100 mW/cm^2, AM1.5 illumination in ambient atmosphere at the indicated times following the final SiNW BOE etch. Solid lines are for improving fill factors while dashed lines are for degrading fill factors.

device performance was maximized at that time. In contrast to these SWNT/SiNW devices, SWNTs on planar Si devices attained their optimum performance after only 2 h of air oxidation (also under illumination).[2] Initially mysterious, this large disparity in the time scale for optimum oxidation between the planar and SiNW devices is explained upon recognizing that the Si oxidation is a photo-accelerated process.[21, 22] All the devices were oxidized under AM1.5 illumination (initially with the purpose of more thoroughly drying them following the BOE wet etch). Since the oxidation is photo-accelerated it depends on the photon absorption cross-section. The devices are particularly sensitive to the oxide thickness in the vicinity of the SWNT/Si junctions where hole extraction takes place. Compared to the planar Si, the tips of the SiNWs present a small cross-section for the light absorption (of order 30 nm) while the shear SiNW sidewalls present a surface nearly parallel to the photon flux, and constitute a much larger area, for the same incident light intensity. Preliminary studies have also been done with larger diameter Si nanopillar (230 nm diameter) based devices, fabricated by reactive ion etching in a modified Bosch process. The larger cross-section for photon capture at the tops of the pillars (where the SWNT/Si junctions reside) exhibit an optimum performance for the photo-accelerated oxidation intermediate between the 2 h for the planar devices and the 96 h for the SiNW devices providing further corroboration the roll of light exposure during the oxidation.

For the both the planar and the SiNW based devices the electrolytic gating was also found to be optimized when the native (ungated) device was optimized. It has been shown that water also plays an active role in Si oxidation[23] so it was reasoned that its exclusion by the hydrophobic ionic liquid covering the Si would terminate further silicon oxide formation once the electrolyte was added (this proved a naive idea, as discussed further below).

The effect of EMI-BTI electrolyte gating at gate voltages (V_G applied to the gate electrode) of +1.0, 0, and -1.0 V under 100 mW/cm^2, AM1.5 illumination are shown in Figure 4. The gate voltage induced modulation of the SWNT Fermi level relative to that of the n-Si, serves to modulate the built-in potential (V_{BI}) at the junction as indicated by the dramatic shift of the open circuit voltage (V_{OC}) from 0.15 V (at V_G = +1.0 V) to 0.58 V (at V_G = -1.0 V). At the performance degrading gate voltage of V_G = +1.0 V, positive electrolyte ionic charge driven to the bare Si surface attracts majority carriers (electrons, in the n-Si) to the Si surface and into the nanowires. Screened by these excess majority carriers from the positive ionic charge, photogenerated holes can

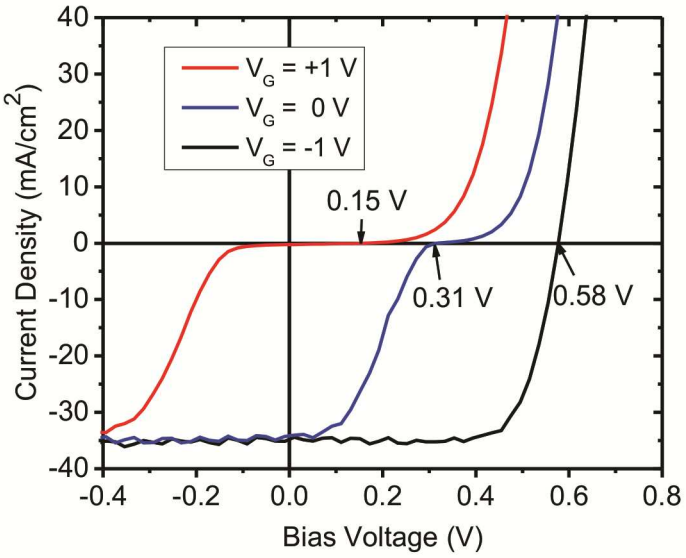

Figure 4. J-V curves for a SWNT/SiNW cell at the indicated gate voltages.

also approach the Si surface resulting in an enhanced surface recombination. Combined with the simultaneous decrease in the built-in potential in the SiNWs at their junctions with the nanotubes the recombination losses lead to a fill factor that is essentially zero. At the gate voltage of V_G = -1.0 V, negative electrolyte ionic charge at the Si surface repels the majority carriers creating an inversion layer at the surface and in the major fraction of the SiNWs avoiding the surface recombination. Combined with the enhanced V_{BI} in the SiNW at the SiNW/SWNT junctions the fill factor becomes 0.76 maximizing the cell performance. The 35 mA/cm^2 short circuit current density here is much greater than that in the planar, gated SWNT/Si cells (25mA/cm^2)[1], consistent with the additional light absorption due to the vertical SiNW array.

Two distinct methods were explored to deposit the SWNT layer: ultrasonic spraying from an ethanol suspension and transfer of a pre-formed SWNT film made by the filtration route.[24] Purely sprayed SWNT layers had to be made substantially thicker than what is seen in Figure 1c to attain low resistance continuity to the Au/Cr electrode. In our experience, however, photons absorbed in the nanotubes contribute negligibly, if at all, to the power generation, so that thicker nanotube layers degraded cell performance.[2] A good compromise was to spray a thin layer of nanotubes followed by the transfer of a 10 nm thick filtration fabricated film. The roughly optimized quantity of nanotubes deposited by the combined method had a surface nanotube concentration of ~1.3 μg/cm^2, approximately equivalent to that in a 20 nm thick, entirely filtration formed and transferred film; however, the transfer of a 20 nm thick film without the sprayed layer did not yield devices that performed as well as the combination. Table 1 compares the performance of several SWNT/SiNW cells at V_G = -1.0 V for which the principle intentional differences were the deposition method and thickness of the SWNT layer. Device D (J-V curve shown in Figure 4) was the best, for which the power conversion efficiency was 15.1%. Cell series resistances were estimated from fits to the J-V measurements at high forward bias. As seen from Table 1 devices with a thicker net SWNT layer, exhibited poorer performance. Light absorption by the thicker nanotube films cannot fully explain these differences since higher J_{sc} corresponds to a greater quantity of light making it into the Si, but cells A and C, which possess different SWNT layer thicknesses, have the same J_{sc} while cell B having an intermediate SWNT layer thickness possesses a slightly lower J_{sc}. Differences in the Jsc are likely dominated by differences in the lengths and spacing of the SiNWs and their agglomeration during processing, which are difficult to control with precision, but which control the Si reflectance and thus the light making it into the Si. To explain the other differences in the performance characteristics between the wholly transferred versus the partially spray deposited films we note that thicker filtration fabricated SWNT films possess a greater mechanical stiffness. When such a film is transferred across vertical nanowires whose heights vary, that stiffness limits the films ability to conform over short length scales, preventing contact to the shorter nanowires. This motivated the use of the mixed sprayed/transferred films and is consistent with the data in the Table. Indeed it is this ability of the nanotubes to touch and extract photocurrent from most nanowire tips (Figure 1c), while providing a direct (non-tortuous), low impedance pathway to the gold electrode (along with the gate induced inversion that avoids surface recombination) that serves to explain the dramatically improved performance in these cells over most other Si nanowire forest based cells reported to date.

Table 1. Performance characteristics for gated (-1.0 V) SWNT/SiNW array cell devices with distinct SWNT layers.

SWNT/SiNW device	V_{OC} (V)	Jsc (mA/cm^2)	FF	R_S ($\Omega \cdot cm^2$)	PCE (%)	SWNT deposition notes
A	0.58	32.5	0.74	1.36	13.9	20 nm transferred
B	0.58	32.0	0.73	0.71	13.5	5 nm sprayed/25 nm transferred
C	0.58	32.5	0.71	0.71	13.2	45 nm transferred
D	**0.58**	**34.4**	**0.76**	**0.64**	**15.1**	**10 nm sprayed/10 nm transferred**

Recently Jung *et al.* criticized the use of ionic liquid electrolytes as suffering from the "volatility of the incorporated liquid media".[25] However, modern ionic liquids possess vapor pressures at room temperature that are some 13 orders of magnitude lower than that of water,[26] so volatility is decidedly *not* a problem. They also argued that the appropriate framework for nanotube/Si cells is heterojunction solar cells.[25] However, this ignores the ~1/3 metallic nanotubes existing in the mixed metallic/semiconducting nanotube layers typically used in these devices. The analogy with metal-insulator-semiconductor Schottky junction cells is more appropriate in this case.

While volatility of the ionic liquid electrolyte is not a problem, such electrolyte gated cells do suffer a serious problem analogous to one that plagued initially very promising liquid junction Si solar cells: chemical reactions at the Si surface degrade cell performance.[27] In the gated cells such degradation was accelerated by the applied gate voltage so that when held, even for minutes at V_G= -1.0 V the J-V curves already began to exhibit an increasing series resistance and decreasing fill factor. Such characteristics for the degradation suggested a continued growth of the oxide layer between the SWNTs and the Si surface implying that water/oxygen had access to the Si surface despite the hydrophobicity of the electrolyte.

Although the as-received, EMI-BTI electrolyte was always stored, and sampled from an inert atmosphere glove box (argon, H_2O, O_2 each < 0.1 ppm), cyclic voltammetry measurements on the electrolyte performed within the glove box revealed an electrochemical window of only 2.7 V, greatly reduced from its literature reported window of 4.4 V, but consistent with its being contaminated with water.[28] Drying a sample of the electrolyte over activated molecular sieves (3 Å and 4 Å) for 48 h increased this window by ~600 mV. Upon repeating the measurement on the dried EMI-BTI now removed from the glove box into the lab ambient atmosphere, the electrochemical window began to narrow again over the course of a few hours. To test a device in a greatly reduced water background we proceeded as follows. A device received a final BOE etch followed by optimal oxidation in ambient atmosphere. To terminate further oxidation and to evaporate residual surface water the device was placed into an argon glove box, where it was stored for 4 days while a sample of the electrolyte was dried in the activated molecular sieve. At the end of this time the active cell area was saturated with the dried electrolyte and J-V measurements were periodically recorded under illumination, in the glove box, with the gate voltage initially maintained at a constant V_G = -0.75 V. No degradation in any of the J-V characteristics was observed even after 5 hours at this gate voltage. The gate voltage was subsequently raised to V_G = -1.0 V for an additional 5 hours with still no degradation observed. The device was subsequently moved into the

laboratory ambient atmosphere, and retested. Degradation became noticeable within one hour of exposure to the ambient atmosphere (at V_G = -1.0 V), becoming progressively worse with further exposure. These experiments strongly implicate water as the source of the degradation in ambient atmosphere and indicate that by avoiding it degradation can be overcome in the gated cells.

One means to avoid ambient water is to encapsulate the cells in an inert atmosphere as must presently be done for other water/oxygen sensitive systems (e.g. organic solar cells). Alternatively, a thin dielectric barrier layer coating the nanotubes and SiNWs at the junctions where they contact may be sufficient to prevent oxidation due to water entrained in the electrolyte. In an attempt to create such a barrier we turned to atomic layer deposition (ALD) of Al_2O_3. ALD deposited aluminum oxide has received increasing interest as a Si surface passivation layer since the availability of commercial ALD systems.[29] The layer by layer deposition of vapor phase reactants (sequentially trimethyl aluminum and water) implies a conformal coating even through the pre-deposited nanotube layer. Prior to growth of the Al_2O_3 the SWNT/SiNW device underwent a final BOE etch, followed by oxidation in ambient for the time that optimized device performance (96 h). Al_2O_3 was grown for 110 reactant cycles at a substrate temperature of 80° C.[30] Ellipsometry performed on such a film deposited on a flat silicon witness chip under these conditions gave a film thickness of 8.8 nm. The inset in Figure 5 shows an SEM image of the Al_2O_3 coated device. Bright spots in the image are enhanced secondary emission from where the SiNW tips underlie the dielectric coated nanotubes. Figure 5 shows the J-V curves for the device before and after electrolyte addition at gate voltages for the latter of zero and -1.0 V. At V_G = -1.0 V the open circuit voltage, short circuit current density and fill factor were, V_{OC} = 0.62 V, J_{SC} = -33.4 mA/cm^2, FF = 0.73 resulting in a PCE of 14.8%. The slightly lower J_{SC} and PCE over the uncoated device is likely due to an increased light scattering due to the coating (inset Fig. 5). The Al_2O_3 layer also affords some performance benefits. Note the improved fill factor for the V_G = 0 V curve in Fig.

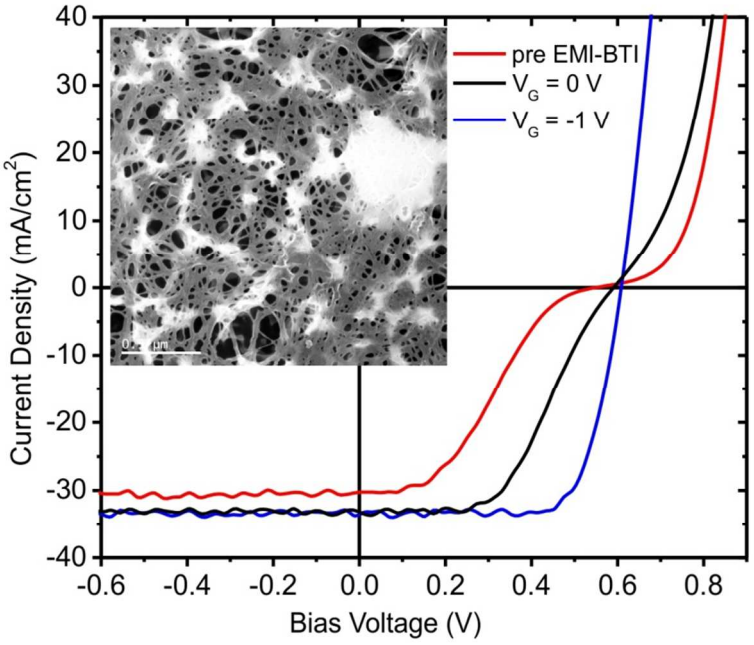

Figure 5. J-V curves for the ALD Al_2O_3 dielectric coated SWNT/SiNW cell without electrolyte (red) and with the electrolyte at the indicated gate voltages (black, blue). The enhanced photocurrent on addition of the electrolyte is attributed to refractive index matching reducing the scattering. Inset: top view SEM image of the dielectric coated SWNTs atop the SiNWs (scale bar 0.5 μm). Bright spots are enhanced secondary emission from the tips of the underlying SiNW tips.

5 compared to that for the uncoated device in Fig. 4, as well as the increase in the V_{OC} at V_G = -1.0 V. Such benefits of passivation are generally associated with a reduced surface state density, which also reduces the Fermi level pinning, permitting the larger shift in the V_{OC}.

Measurement of parasitic gate currents can quantify the reactions occurring at the Si surface, some portion of which should correspond to deleterious Si oxidation (other electrolyte or impurity reactions that don't degrade the SWNT/Si interface may also occur). For SWNT/SiNW devices without the ALD dielectric coating the steady state gate current at V_G = -1.0 V in the non-dried electrolyte was typically 2.7 μA. For the dielectric coated device this was reduced by a factor of 60 to 45 nA. Unfortunately, this was still a factor of ~110 greater that observed for the device measured in the glove box using the dried electrolyte for which the gate current was 0.4 nA, and while the rate of degradation of the coated device was greatly reduced over the uncoated device, it still began to evidence degradation over the course of several hours (measured in the ambient lab atmosphere in the non-dried EMI-BTI electrolyte). This implies that the ALD layer remains permeable to water at the thickness used. A thicker layer may prevent this, although a hydrophobic coating (e.g. Parylene) may be preferred to the naturally hydrophilic oxide in such an application.

Conclusions

Given that encapsulation or a better optimized barrier layer should prevent the electrochemical degradation, we finally consider other aspects of our present devices that could limit their performance (suggesting means to increase their PCEs beyond the present 15%). One limitation concerns excess recombination at the back contact. It has long been known that a back surface field induced by appropriate doping of the Si at the device back contact can reduce recombination there, with corresponding improvements in the device performance.[31] Another factor also limiting the PCE in our present design is the device geometry. In the present construction the Si wafer thickness (550 μm) is large relative to the active area width (2 mm) meaning that photocarriers created near the edge of the active window region have an appreciable cross-section for escape out the sides of that region, thereby contributing to the losses. Capturing those carriers could significantly boost the device PCE. Quite recently PCEs comparable to what we demonstrate here were obtained from planar, chemically charge transfer doped nanotube/Si solar cells exploiting a TiO_2 antireflection coating.[32] The broad band reflectance due to that coating was not as low as our vertical NW arrays (Fig. 2), exhibiting a minimum of 5% at 600 nm, but rising smoothly on either side of the minimum to over 10% at 500 nm and 800 nm, respectively and to over 20% at the extremes of the relevant solar spectrum (400-1100 nm). The comparable performance, despite our reduced reflectance, suggests that their devices exhibited lower losses which could be due to the more optimized geometry in their thinner (400 μm) wafers possessing a larger active cell area (15 mm^2 vs. our 8 mm^2) reducing carrier leakage out the sides of their active region. Another future improvement concerns the liquid electrolyte: in practice solar cells must generally be tilted making the flow of a fluid ionic liquid problematic. This could readily be overcome by the addition of a cross-linkable gellating compound. In conclusion, our results here, along with the clear strategies available for further device improvement bode well for the continued, remarkably rapid advance of such nanotube/Si devices since they were first reported in only 2007.[33]

Methods

The substrate was diced from a 500 μm thick, <100>, n-Type (phosphorous, 0.5-0.7 Ohm·cm) silicon wafer possessing a 200 nm thick thermal oxide. Onto the surface of the oxide was defined a square 12×12 mm^2 Au/Cr (60/10 nm) pad, possessing a 2×4 mm^2 rectangular window at its center. This Au/Cr pad served several functions: it provided an etch mask for a BOE etch of the oxide in the window and for the Si nanowire etch, limiting the nanowires to the window area (the backside and other areas protected by photoresist); the Au/Cr pad served as the electrical contact to the nanotubes that were draped as a thin film from the Au/Cr layer down across the tops of the SiNWs; and finally, it provided a literal shadow mask, limiting the collimated, simulated solar radiation to the window area in which the SiNWs were defined. The nanotube layer, when sprayed, had to be made rather thick (substantially thicker than in Fig. 1c) to ensure low resistance continuity to the Cr/Au electrode. But in our experience photons absorbed in the nanotubes contribute little to the power generation, so that thicker nanotube layers degraded cell performance.[2] A good compromise was to spray a layer of nanotubes of the approximate density shown in Fig. 1c followed by the transfer of a 10 nm thick nanotube film made by the filtration method discussed by Wu *et al*.[24] Ohmic contact between the Si wafer backside and a stainless steel sheet was made by a gallium-indium (Ga/In) eutectic spread between the two. Illumination was provided by a 150W xenon lamp (Oriel 6255) in an Oriel 6136 housing powered by a model 8500 power supply. An Oriel 81094 AM1.5G filter approximated the solar spectral distribution. Light from the inhomogeneous source was focused into the acceptance aperture of a 150 mm long, fused silica Homogenizing Rod (Edmund Optics P65-837) by a 50 mm diameter fused silica lens with a 65 mm focal length. The output face of the Homogenizing Rod was imaged in the horizontal focal plane of the sample by a 50 mm diameter, 100 mm focal length fused silica lens after rotation by 90 degrees with a broad band mirror (Newport 66225). The intensity at the sample plane was adjusted to 100 mW/cm^2 by translation of the 65 mm FL lens, cutting down on the fraction of the light entering the Homogenizing Rod. Homogeneity of the light intensity over the ~1 cm^2 central region of the homogenized beam at the sample plane was measured to be within 5%. Reflectance spectra were recorded at near normal incidence in a Perkin-Elmer Lambda 900 dual beam spectrophotometer using a silver mirror reference. The 3 Å and 4 Å molecular sieves (1:1, Fisher Scientific) were activated for 3 hours at 210 °C. Electrochemical analysis of the EMI-BTI (electrochemical grade, >99.5%, Covalent Associates) was performed in a glove box using a PARSTAT 2273 potentiostat/galvanostat (Princeton Applied Research). Cyclic voltammetry measurements were performed at a scan rate of 0.05 $V \cdot s^{-1}$ in a standard one compartment electrochemical cell using a glassy carbon disk electrode (GC, 3 mm diameter, 0.077 cm^2) as the working electrode, a silver wire as the pseudo reference electrode, and a Pt flag as the counter electrode. The GC working electrode was polished on soft lapping pads (Buehler, Illinois) with alumina slurries of size 0.5 and 0.05 μm, respectively.

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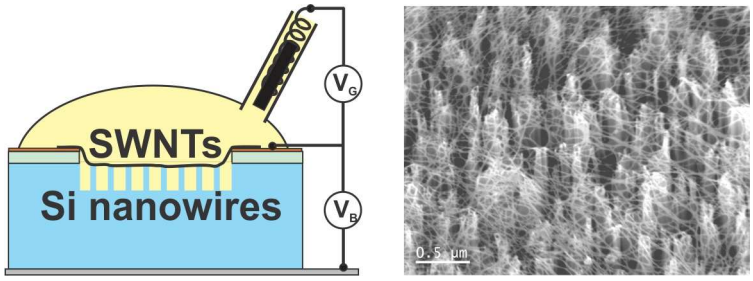
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