Temperature Dependent Short Circuit Capability of Silicon Carbide (SiC) Power MOSFETs

Zhiqiang Wang[1], *Student Member*, *IEEE*, Xiaojie Shi[1], *Student Member*, *IEEE*,
Leon Tolbert[1, 2], *Fellow*, *IEEE*, Fred Wang[1, 2], *Fellow*, *IEEE*, Zhenxian Liang[1, 2], *Senior Member*, *IEEE*,
Daniel Costinett[1, 2], *Member*, *IEEE*, and Benjamin J. Blalock[1], *Senior Member*, *IEEE*

1. Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN 37996, USA
2. Power Electronics and Electric Machinery Group, Oak Ridge National Laboratory, Knoxville, TN 37932, USA

Abstract—**This paper presents a comprehensive short circuit ruggedness evaluation and numerical investigation of up-to-date commercial silicon carbide (SiC) MOSFETs. The short circuit capability of three types of commercial 1200 V SiC MOSFETs is tested under various conditions, with case temperatures from 25 °C to 200 °C and DC bus voltages from 400 V to 750 V. It is found that the commercial SiC MOSFETs can withstand short circuit current for only several microseconds with a DC bus voltage of 750 V and case temperature of 200 °C. The experimental short circuit behaviors are compared and analyzed through numerical thermal dynamic simulation. Specifically, an electro-thermal model is built to estimate the device internal temperature distribution, considering the temperature dependent thermal properties of SiC material. Based on the temperature information, a leakage current model is derived to calculate the main leakage current components (i.e. thermal, diffusion, and avalanche generation currents). Numerical results show that the short circuit failure mechanisms of SiC MOSFETs can be thermal generation current induced thermal runaway or high temperature related gate oxide damage.**

Index Terms—**Silicon carbide (SiC) MOSFETs, short circuit capability, electro-thermal model, leakage current, thermal runaway**

I. INTRODUCTION

Featuring higher breakdown voltage, increased operating temperature, higher thermal conductivity, and lower switching and conduction loss, SiC devices (especially enhancement-mode SiC MOSFETs) are expected to be widely used in future transportation applications, e.g. electric vehicles and the “more electric” aircraft [1]–[8]. While achieving higher power density (due to limited space and carrier capability) and high temperature electrical design (due to inherent harsh environment), the ability to guarantee the reliability and safety becomes critical [9]–[12]. One of the key reliability issues is the short circuit capability of SiC power MOSFETs.

Recently, several research efforts have focused on the short circuit capability testing of 1200 V SiC power MOSFETs. In [13], the short circuit capability of 1200 V / 100 mΩ SiC MOSFETs with active areas of 3.5 mm × 3.5 mm are studied and analyzed at 400 V DC bus voltage, 10 V / 15 V positive gate bias, and 25 °C case temperature. It is shown that the short circuit withstand time (SCWT) is around 80 μs at 10 V gate voltage and 50 μs at 15 V. Similar investigation of 1200 V commercially available devices is reported in [14], with a DC bus voltage of 400 V, gate voltage of +18 / 0 V, and case temperatures of 90 °C and 150 °C. A major concern of these testing results is that the short circuit test conditions may not represent the real application scenarios of 1200 V SiC MOSFETs that usually has a positive gate voltage as high as 20 V and DC bus voltage greater than 600 V. A more practical evaluation of short circuit capability can be found in [15] and [16] with 600 V DC bus voltage, 20 V / -5 V gate voltage, and 25 °C case temperature. However, the temperature dependent short circuit characteristics and associated failure mechanisms have not been investigated. In addition, it is still unclear what the key limiting factor (DC bus voltage level, temperature, fault type, device type, etc.) of short circuit capability is.

The paper is organized as follows: Section II presents the short circuit capability testing results of three types of commercial SiC MOSFETs under different case temperatures, DC bus voltages, and fault types. In Section III, the temperature dependent short circuit characteristics are summarized, and the associated failure mechanisms are analyzed based on the derived electro-thermal model and leakage current model. Section IV concludes the paper.

II. SHORT CIRCUIT CAPABILITY EVALUATION

Three types of commercially available discrete 1200 V SiC MOSFETs with TO-247 package are investigated in this work, as shown in Table I. These devices have the same on-state resistance, while their current ratings and die sizes are different.

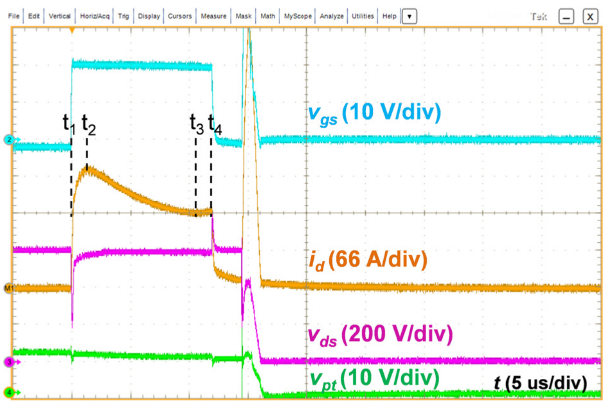
Table I. SiC MOSFETs under test [19]–[22]

Device Types / Parameters	CREE		ROHM
	1st Generation (1G)	**2nd Generation (2G)**	
Rated Voltage / Current	1200 V / 24 A (100 °C)	1200 V / 20 A (100 °C)	1200 V / 28 A (100 °C)
On-Resistance	80 mΩ	80 mΩ	80 mΩ
Normalized Die Area	1.59	1.0	1.21

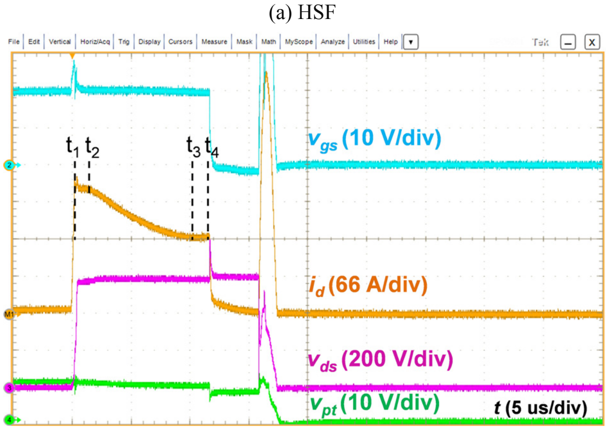
The test circuit configuration and hardware test setup for short circuit capability evaluation have been introduced in part II of [17]. The devices will be tested under different fault types, i.e. hard switching fault (HSF) and fault under load (FUL) condition [18]. In order to prevent the potential damage of the whole test setup when the device under test (DUT) fails, a solid state circuit breaker (SSCB) with a proper short circuit protection threshold is employed in the DC link. In addition, the DUT is heated by a controlled hot plate at the bottom side of the test board to evaluate its temperature dependent short circuit characteristics, and the device case temperature is monitored by a K-type thermocouple with a time constant of around 0.8 s (at 65 ft / s air velocity) / 20 s (at still air).

A. CREE 1G SiC MOSFETs

Fig. 1(a) and (b) show the short circuit transient waveforms of the CREE 1G SiC MOSFETs under HSF and FUL condition, with DC bus voltage V_{dc} = 600 V, gate voltage v_{gs} = + 20 / - 2 V, and case temperature T_c = 25 ºC, where v_{ds}, i_d, and v_{pt} are the drain-source voltage, drain current of the DUT, and the protection signal from the SSCB, respectively. The overall short circuit behavior under both fault types is similar and can be divided into four stages.



(a) HSF



(b) FUL

Fig. 1. Short circuit capability of CREE 1G SiC MOSFET with V_{dc} = 600 V and T_c = 25 ºC.

Stage I [t_1 ~ t_2]: When a short circuit occurs at t_1, the drain current increases quickly due to small inductance in the main power loop. Meanwhile, the device enters from linear region to active region, with a saturated drain-source voltage close to the DC bus voltage. The current keeps increasing in this stage due to positive temperature coefficient of MOS channel mobility up to 600 K [23].

Stage II [t_2 ~ t_3]: The device conducts in saturation as the full DC bus voltage appears across it. This involves considerable power loss, and as a consequence the semiconductor junction temperature increases rapidly due to self-heating. The temperature rise leads to reduction in the MOS channel (and drift region) carrier mobility, and thus the short circuit current presents a negative slope. The device can be successfully turned off if the semiconductor temperature is within safe range.

Stage III [t_3 ~ t_4]: As junction temperature continues increasing, the *di/dt* of the short circuit current waveform changes to be positive. This is likely because the decreasing rate of MOS channel electron current is lower than the rising rate of leakage current induced by thermally assisted impact ionization.

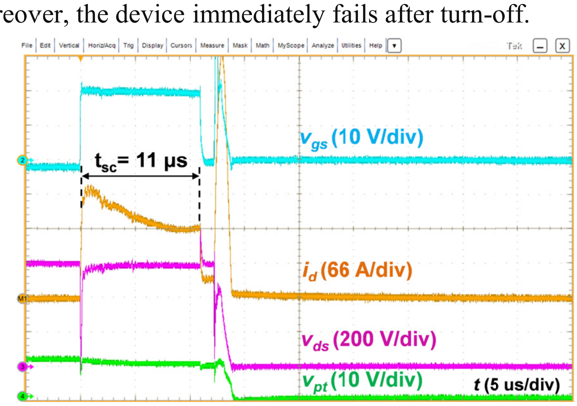
Stage IV [t_4 ~]: When the device is switched off at t_4, a tail leakage current remains after the turn-off process and eventually leads to a thermal runaway phenomenon and device failure. This failure mode, occurring after a delay time from the device turn-off, has been reported by some authors in Si field-stop IGBTs [24].

The short circuit withstand time t_{sc} (from t_1 to t_4) is 12 μs under HSF, and 11.5 μs under FUL. The slightly lower SCWT for FUL is associated with the higher peak fault current caused by a gate voltage spike during the fault transient. The short circuit critical energy E_c, defined by (1), is around 1.18 J for both cases.

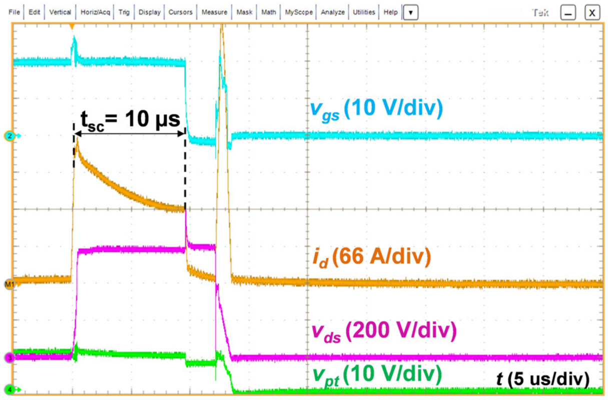
$$E_c = \int_{t_1}^{t_4} V_{ds} \cdot I_d \, dt. \tag{1}$$

The high temperature short circuit capability of the CREE 1G SiC MOSFETs is also evaluated with DC bus voltage V_{dc} = 600 V, gate voltage v_{gs} = + 20 / - 2 V, and case temperature T_c = 200 ºC, as shown in Fig. 2. Compared to Fig. 1, several observations can be made regarding the current waveforms: 1) the SCWT decreases slightly from 12 μs (25 ºC) to 11 μs (200 ºC) under HSF, and 11.5 μs (25 ºC) to 10 μs (200 ºC) under FUL; 2) the peak fault current point (occurring at time t_2) moves towards fault starting moment (at t_1); 3) the delay time to failure becomes shorter.

The CREE 1G SiC MOSFETs are further tested at an elevated voltage level, V_{dc} = 750 V, while keeping other conditions the same as Fig. 2. As shown in Fig. 3, the SCWT is significantly reduced to 7 μs under HSF and 6.6 μs under FUL. Moreover, the device immediately fails after turn-off.

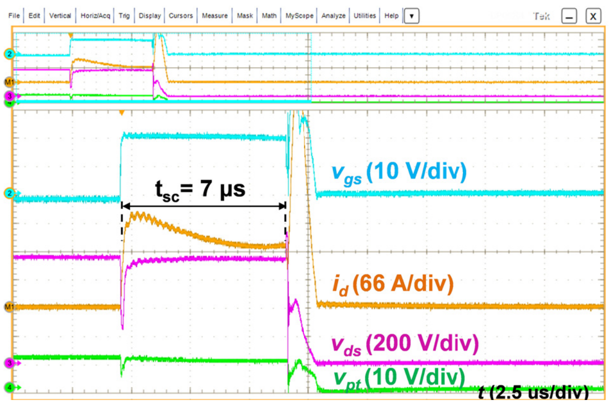


(a) HSF

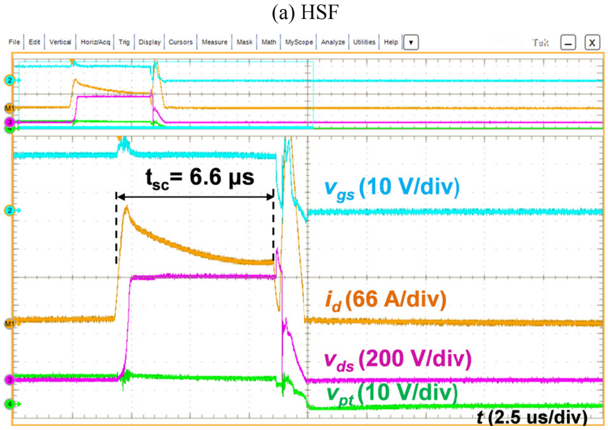


(b) FUL

Fig. 2. Short circuit capability of CREE 1G SiC MOSFETs with V_{dc} = 600 V and T_c = 200 ºC.



(a) HSF



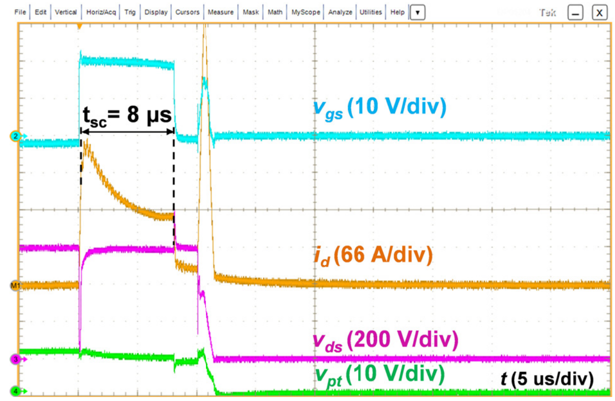
(b) FUL

Fig. 3. Short circuit capability of CREE 1G SiC MOSFETs with V_{dc} = 750 V and T_c = 200 ºC.

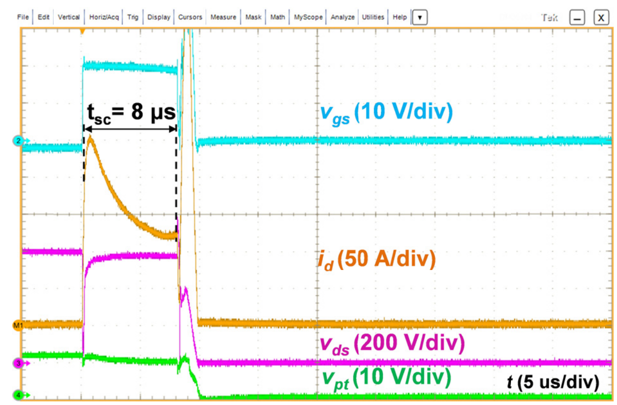
B. CREE 2G SiC MOSFETs

The short circuit capability of the second generation SiC MOSFETs from CREE has also been evaluated using the power stage. Given that HSF and FUL have nearly the same short circuit characteristics, only HSF testing results are presented hereafter.

Fig. 4(a) and (b) show the HSF short circuit transient waveforms under case temperatures of 25 ºC and 200 ºC respectively, with DC bus voltage V_{dc} = 600 V and gate voltage v_{gs} = + 20 / - 2 V. The overall short circuit behavior is the same as 1G SiC MOSFETs, while the SCWT becomes much shorter. Moreover, the SCWT stays unchanged at different case temperatures, which is around 8 µs.



(a) 25 ºC



(b) 200 ºC

Fig. 4. Short circuit capability of CREE 2G SiC MOSFETs under different case temperatures when V_{dc} = 600 V.

The CREE 2G SiC MOSFETs are further tested at a higher stress condition, with a DC bus voltage of 750 V and case temperature of 200 ºC. As can be observed in Fig. 5, the SCWT is as low as 5 µs, which is quite challenging for the design of protection circuits.

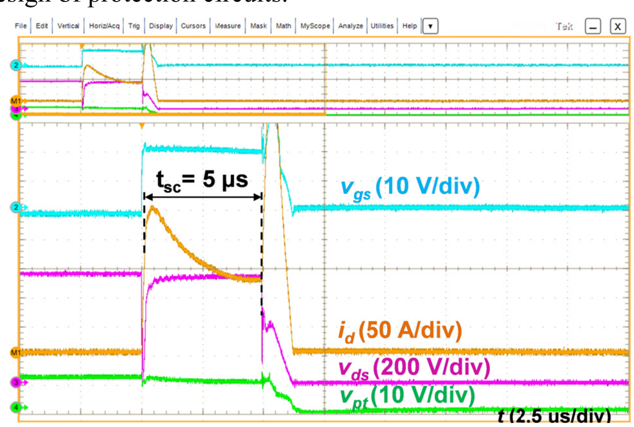


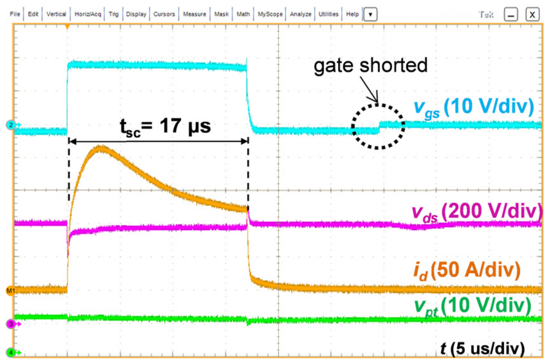
Fig. 5. Short circuit capability of CREE 2G SiC MOSFET with V_{dc} = 750 V and T_c = 200 ºC.

C. ROHM SiC MOSFETs

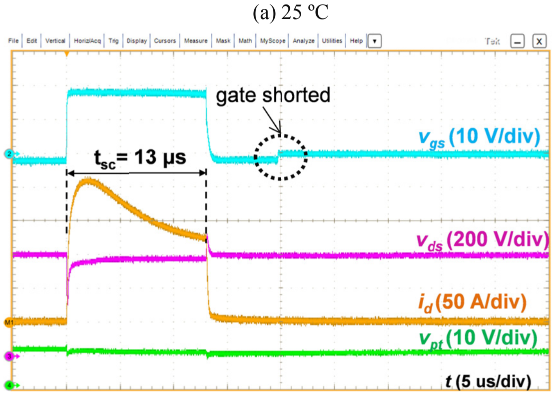
Short circuit tests have been conducted for the SiC MOSFETs from ROHM. The positive gate bias is set at 18 V, as recommended by the device manufacturer [25]. Fig. 6(a) and

(b) show the HSF short circuit transient waveforms under case temperatures of 25 ºC and 200 ºC respectively, with DC bus voltage V_{dc} = 600 V and gate voltage v_{gs} = + 18 / - 2 V. The short circuit behavior before device turn-off is similar to that of the CREE SiC MOSFETs; however, the SCWT is much longer. Different from the CREE devices, while the drain current can be successfully switched off, the gate and source terminals are shorted together after a delay following device turn-off.

In order to identify the key limiting factor, the ROHM SiC MOSFETs are further tested at a higher DC bus voltage (750 V) and positive gate bias (20 V), while keeping the case temperature at 200 ºC. As shown in Fig. 7, the devices still present a delayed failure at the gate-source junction. The SCWT is around 10 µs at V_{dc} = 750, which is higher than the CREE 1G and 2G SiC MOSFETs. Nevertheless, the SCWT is close to that of the CREE 1G SiC MOSFETs when the positive gate bias is increased to 20 V.

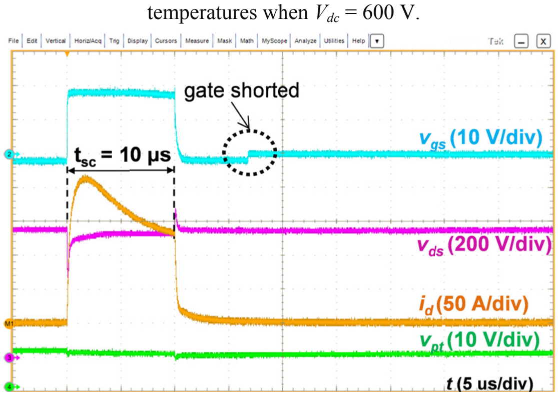


(a) 25 ºC

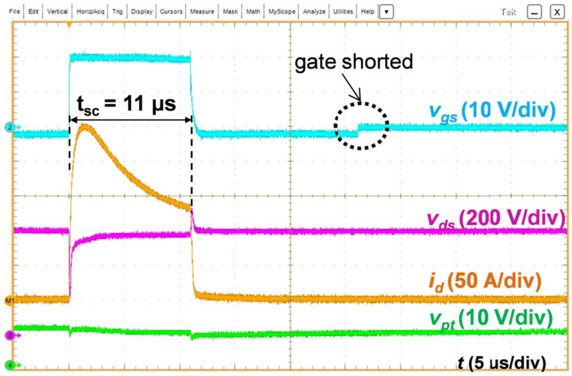


(b) 200 ºC

Fig. 6. Short circuit capability of ROHM SiC MOSFETs under different case temperatures when V_{dc} = 600 V.



(a) V_{dc} = 750 V and v_{gs} = + 18 / - 2 V



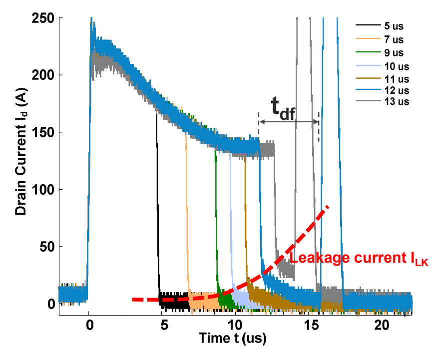
(b) V_{dc} = 600 V and v_{gs} = + 20 / - 2 V

Fig. 7. Short circuit capability of ROHM SiC MOSFETs with T_c = 200 ºC.

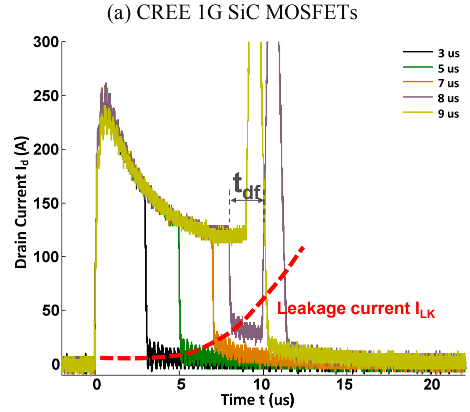
III. Behavior Comparison and Electro-Thermal Analysis

A. *Delayed Failure Mode*

According to the experimental results, both the CREE 1G and 2G devices present a delayed failure mode. In order to further investigate the evolution of the failure mode, the short circuit duration is gradually increased until the failure of the power device, as illustrated in Fig. 8. When the device is turned off, the initial leakage current I_{LK} gradually increases with the extension of short circuit duration. Once the leakage current is large enough, the internal thermal instability after device turn-off occurs following a delay time (depending on heat diffusion), which eventually leads to a thermal runaway. Moreover, the delay time to failure t_{df} is short circuit duration (i.e. energy) dependent. With the increase of short circuit duration (i.e. higher energy), the delay time to failure becomes shorter.



(a) CREE 1G SiC MOSFETs



(b) CREE 2G SiC MOSFETs

Fig. 8. Evolution of delayed failure mode with different short circuit durations.

After the destructive tests, the impedance between the three terminals of the DUT and the forward voltage of the body diode are measured using a digital multimeter. The typical measurement values are summarized in Table II. As can be observed, all three terminals are nearly shorted together for the CREE 1G and 2G SiC MOSFETs. The ROHM SiC MOSFETs only show a short circuit in gate-source junction. The gate-drain, drain-source junction, and body diode still appear to be normal. However, a detailed comparison with a new device reveals that the two junctions and the body diode are actually degraded. Both the impedance and forward voltage drop tend to decrease.

Table II. Summary of typical data of failed devices

Device Types / Parameters	CREE		ROHM
	1st Generation (1G)	2nd Generation (2G)	
R_{gs}/R_{sg} (Ω)	0.1 / 0.1	0.2 / 0.2	0.3 / 0.3
R_{gd}/R_{dg} (Ω)	10.4 / 10.4	17.2 / 17.2	800k / ∞
R_{ds}/R_{sd} (Ω)	10.5 / 10.5	17.4 / 17.4	∞ / 800k
V_F (V)	0.015	0.018	1.222

B. Short Circuit Withstand Time and Critical Energy

Based on the testing results under different case temperatures up to 200 °C, the temperature dependent short circuit withstand time and critical energy are summarized in Fig. 9, where the DC bus voltage is 600 V and the gate voltages are + 20 / - 2 V for the CREE devices and + 18 / - 2 V for the ROHM devices.

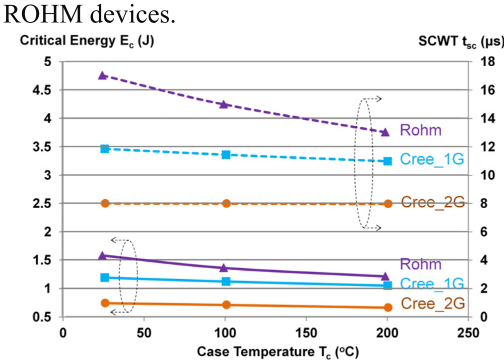


Fig. 9. Comparison of temperature dependent short circuit capability.

Under low temperature levels, more dissipated energy is required for the devices to reach the critical failure temperature point, and the corresponding SCWT is longer. The short circuit capability of the CREE 2G devices is nearly independent of temperature, and the short circuit critical energy and withstand time remain nearly constant. Similarly, the short circuit capability of the CREE 1G SiC MOSFETs show a slight dependence on temperature. In contrast to the CREE devices, both the short circuit critical energy and withstand time of the ROHM devices decrease linearly with the increase of case temperature.

The SCWT and critical energy under different DC bus voltage levels are also investigated, as shown in Fig. 10. The case temperature is kept at 200 ºC by a hot plate. The short circuit capability of the three SiC MOSFETs is strongly voltage dependent. With the increase of DC bus voltage, less dissipated energy is needed to cause a thermal destruction and the device can survive for shorter time duration.

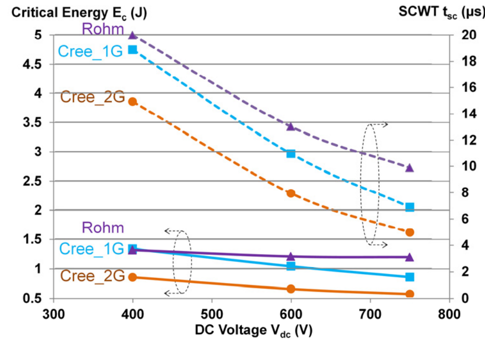


Fig. 10. Comparison of DC bus voltage dependent short circuit capability.

C. Electro-Thermal Model

In order to evaluate the temperature distribution across the device assembly and thus further investigate the failure mechanism of the tested power devices as well as other SiC MOSFETs, an electro-thermal model (including the power semiconductor die, die-attach material, and case) is built, as shown in Fig. 11.

During short circuit transient, the full DC bus voltage V_{dc} applies to the power device, leading to a depletion layer width of x_p in the P-well and x_n in the N- drift region

$$x_p = \frac{N_d}{N_d + N_a}\sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_d + N_a}{N_d N_a}\right)V_{dc}} \tag{2}$$

$$x_n = \frac{N_a}{N_d + N_a}\sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_d + N_a}{N_d N_a}\right)V_{dc}} \tag{3}$$

where, ε_s is the dielectric constant for the 4H-SiC material; q is the electron charge; N_a and N_d represent the doping density of P well and N- drift region respectively. For the three types of SiC MOSFETs, the breakdown voltage provides an estimated N- drift region thickness of 20 μm and doping density of 2×10^{15} cm^{-3}.

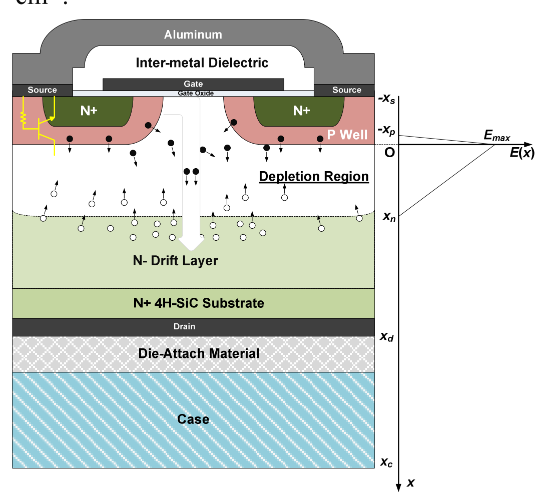


Fig. 11. Electro-thermal model of SiC MOSFET with TO-247 package.

The temperature distributions within the device T (x, y, z) under various short-circuit condition can be obtained by solving the heat diffusion equation in Cartesian coordinates

$$\frac{\partial}{\partial x}\left(k_p\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k_p\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k_p\frac{\partial T}{\partial z}\right)+Q = \rho c_p\frac{\partial T(x,y,z)}{\partial t} \quad (4)$$

where, k_p, ρ, and c_p are the thermal conductivity, material density, and specific heat; Q is the heat generation source due to the power dissipation during short circuit transient. Since the generated heat flux essentially flows in one dimension, from upper surface (i.e. source metallization layer) of the die to the case, (4) reduces to

$$\frac{\partial}{\partial x}\left(k_p\frac{\partial T}{\partial x}\right)+Q=\rho c_p\frac{\partial T(x)}{\partial t}. \quad (5)$$

The thermal properties of the die attach material and the case are assumed to be constant due to small temperature variation. However, the temperature dependence of thermal conductivity and specific heat of 4H-SiC material should be considered for SiC MOSFETs because of high internal temperature gradient [26]

$$k_p(T)=\frac{1}{-0.0003+1.05\times10^{-5}T} \quad (6)$$

$$c_p(T)=925.65+0.3772T-7.9259\times10^{-5}T^2-\frac{3.1946\times10^7}{T^2}. \quad (7)$$

The internal heat generation Q can be given as

$$Q=E(x)J(t)=\frac{E(x)I(t)}{S} \quad (8)$$

where J (t) is the short circuit current density; S is the power device active area; I (t) is the short circuit current in experiments; E (x) is the electric field distribution in the space charge region given by (9) and (10)

$$E(x)=-\frac{qN_d}{\varepsilon_s}(x-x_n) \qquad 0\le x\le x_n \quad (9)$$

$$E(x)=\frac{qN_a}{\varepsilon_s}(x+x_p) \qquad -x_p\le x\le 0. \quad (10)$$

Substituting (8) – (10) and (2) – (3) into (5) yields

$$\frac{\partial}{\partial x}\left(k_p\frac{\partial T}{\partial x}\right)+\frac{qN_d}{\varepsilon_s}\left[\frac{N_a}{N_d+N_a}\sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_d+N_a}{N_dN_a}\right)V_{dc}}-x\right]\frac{I(t)}{S} = \rho c_p\frac{\partial T(x)}{\partial t} \quad (11)$$

$$\frac{\partial}{\partial x}\left(k_p\frac{\partial T}{\partial x}\right)+\frac{qN_d}{\varepsilon_s}\left[\frac{N_d}{N_d+N_a}\sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_d+N_a}{N_dN_a}\right)V_{dc}}+x\right]\frac{I(t)}{S} = \rho c_p\frac{\partial T(x)}{\partial t}. \quad (12)$$

The above equations can be applied to all SiC MOSFETs to obtain their temperature distribution. According to (11) and (12), several qualitative conclusions can be drawn as follows: (a) The increase of DC bus voltage V_{dc} (thus the increase of short circuit saturation current I (t)), causes a fast junction temperature rise ($\partial T/\partial t$). For a given failure temperature, the short circuit withstand time will be reduced. (b) The increase of current density, by larger channel width to length ratio (W/L) and/or higher gate voltage levels, will be at the cost of lower short circuit capability. Currently, the low channel mobility of SiC MOSFETs requires higher positive gate bias (+18 V~ +20 V) than Si devices (+15 V). Under the same DC bus voltage, the temperature rising rate is actually proportional to the current density. (c) The device scaling through die paralleling should not affect the failure temperature and short circuit withstand time.

The derived heat equations can be solved by finite-difference methods. Since (11) and (12) are second order in spatial coordinates and first order in time, two boundary conditions and one initial condition must be specified. In this work, the case temperature is fixed (from 25 ºC to 200 ºC) at the bottom surface of the case. The generated heat flux is assumed to be unidirectional, and the top surface of the die is considered to be adiabatic. In addition, the device junction temperature before short circuit test equals to the case temperature. These boundary conditions and initial conditions are summarized as

$$T(x=x_c,t)=T_c \quad (13)$$

$$k_p\frac{\partial T}{\partial x}|_{x=-x_s}=0 \quad (14)$$

$$T(x,t=0)=T_c. \quad (15)$$

D. Leakage Current Model

Since the leakage current seems to be responsible for device failure in experiments, the temperature dependence of leakage current is also evaluated using the derived electro-thermal model. In this work, three essential leakage current mechanisms are taken into account, namely the thermal generation current, diffusion current, and avalanche multiplication current.

(1) Thermal Generation Current

The thermally activated carrier generation is described by Shockley-Read-Hall (SRH) theory, and the corresponding leakage current is given by (16) [27]

$$I_{g\_th}=\frac{qSn_i}{\tau_g}\sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_d+N_a}{N_dN_a}\right)V_{dc}} \quad (16)$$

where, n_i is intrinsic carrier concentration and τ_g is the SRH generation lifetime. As can be observed, the SRH generation current is actually both voltage and temperature dependent. With the increase of DC bus voltage (from 400 V to 750 V in this work), the thermal generation current will also increase. The temperature dependence of this leakage is mainly caused by the intrinsic charge carrier density of 4H-SiC material

$$n_i(T)=1.7\times10^{16}\times T^{\frac{3}{2}}\times e^{-\frac{2.08\times10^4}{T}}. \quad (17)$$

Although the intrinsic carrier concentration for SiC is far smaller than for Si due to the large difference in band gap energy, its impact on the leakage current of SiC MOSFETs at high junction temperatures cannot be neglected. The generation lifetime depends on not only temperature but also other factors, such as the material dislocation density, surface effects, the capture cross sections, and the trap energy [27]. Based on the previous measurement results in [28]–[30], the carrier generation lifetime in 4H-SiC epilayers ranges from less than 1 ns to approximately 1 μs. Due to its high uncertainty, several different lifetimes will be used in the later simulation to obtain a realistic value.

(2) Diffusion Current

As mentioned above, the intrinsic minority carriers in P well and N- drift layer will quickly increase due to the rise of junction temperature during short circuit transient. These minority carriers diffuse into the depletion region and drift across the PN- junction with the aid of electric field E (x), leading to a saturation current proportional to the doping concentration at the low doped side of the junction.

According to [31]–[35], the temperature dependence of the saturation current I_{g_diff} is given by the diffusion coefficient (D_p and D_n), minority diffusion length (L_p or L_n), and the intrinsic carrier concentration (n_i) as follows

$$I_{g\_diff} = qS\left(\frac{n_i^2 D_n}{L_n N_a} + \frac{n_i^2 D_p}{L_p N_d}\right) \tag{18}$$

$$L_p = \sqrt{D_p \tau_p} \qquad L_n = \sqrt{D_n \tau_n} \tag{19}$$

$$D_p = \frac{kT}{q}\mu_p \qquad D_n = \frac{kT}{q}\mu_n \tag{20}$$

$$\mu_p(T) = \mu_{p0}\left(\frac{T}{300}\right)^{-2.2} \qquad \mu_n(T) = \mu_{n0}\left(\frac{T}{300}\right)^{-2.6} \tag{21}$$

$$\tau_p(T) = \tau_{p0}\left(\frac{T}{300}\right)^{1.5} \qquad \tau_n(T) = \tau_{n0}\left(\frac{T}{300}\right)^{2.32} \tag{22}$$

where k is the Boltzmann constant; μ_p and μ_n are the temperature dependent hole and electron mobility of 4H-SiC epilayers; μ_{p0} and μ_{n0} are the hole and electron mobility at 300 K; τ_p and τ_n are the temperature dependent hole and electron lifetime in N- region and P well region respectively; τ_{p0} and τ_{n0} are the hole and electron lifetime at 300 K.

(3) Avalanche Generation Current

Under short circuit condition, both the majority electron charge and thermally induced minority charge carriers in the depletion region will be accelerated by the electric field E(x). Like the well-known avalanche breakdown mechanism, if the kinetic energy of the charge carriers is high enough to generate new electron hole pairs, an additional leakage current gradually forms based on the avalanche multiplication.

For a given DC bus voltage V_{dc}, the avalanche current is given as

$$I_{g\_av} = S\sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_d + N_a}{N_d N_a}\right)V_{dc}}\left(\alpha_n|J_n| + \alpha_p|J_p|\right) \tag{23}$$

In (23), J_n and J_p are the electron and hole current density, respectively. Since most of the short circuit current within SiC MOSFETs are composed by electrons, hole current density is neglected (i.e. $J_n = J$) in the following analysis. α_n and α_p represent the impact ionization coefficient for electrons and holes, which depend not only on electric field but also temperature. As reported in [36]–[37], the impact ionization rate of SiC material is much larger for holes than for electrons, which can be curve-fitted with the empirical law of impact ionization coefficient proposed by Chynoweth:

$$\alpha_p(T) = (6.3\times10^6 - T\times1.07\times10^4) \times exp\left[-\frac{1.75\times10^7}{E(x)}\right] \tag{24}$$

$$\alpha_n(T) = (1.6\times10^5 - T\times2.67\times10^2) \times exp\left[-\frac{1.72\times10^7}{E(x)}\right]. \tag{25}$$

E. Simulation Results

Using the experimental short circuit waveforms and derived electro-thermal model, the temperature distribution within the SiC MOSFETs can be evaluated and the temperature dependent leakage current is calculated numerically.

Fig. 12 shows the comparison of depletion region boundary (x = 0) temperature evolution for the three types of devices, under a DC bus voltage of 600 V and case temperature of 25 ºC. As can be seen, the failure temperatures of CREE SiC MOSFETs are close, while that of ROHM device is higher. Under the same short circuit condition, the device with higher current density presents faster temperature rising rate, as predicted by the electro-thermal model in (11) and (12). For example, the CREE 2G and ROHM SiC MOSFETs have the highest $\partial T/\partial t$ at the initial and end stage, respectively. For the CREE SiC MOSFETs, the higher current density or $\partial T/\partial t$ eventually leads to a lower SCWT. However, ROHM device has higher saturation current density, but also longer SCWT. Their different failure mechanisms will be discussed in detail later.

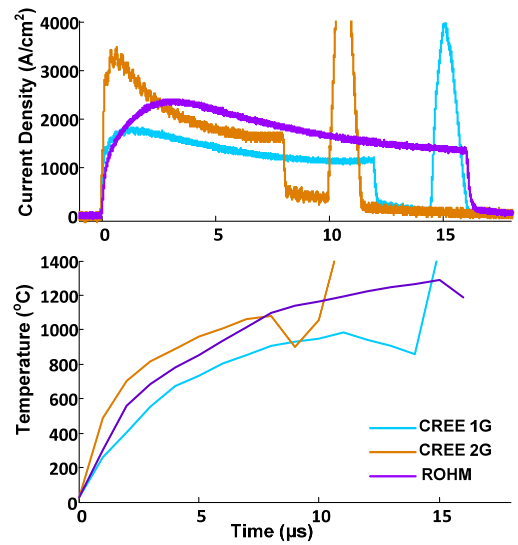


Fig. 12. Comparison of saturation current density and junction temperature.

The x-axis temperature distribution of the three devices at turn-off moment is plotted in Fig. 13. The maximum temperature is reached at the depletion region boundary (x = 0) due to the highest electric field. It is shown that the heat flux only diffuses less than 200 μm for the three types of devices. Compared with the other two devices, CREE 2G SiC MOSFETs tend to have a higher temperature gradient ($\partial T/\partial x$) and lower heat diffusion distance. This is probably because the current density of CREE 2G device is the highest at the turn-off moment. Such a low heat diffusion distance reveals that the short circuit capability of SiC MOSFETs can be independent of packaging technologies and external cooling conditions. Moreover, the concentrated heat generated within the depletion region could cause the degradation or even damage of the gate oxide and metallization layer [38].

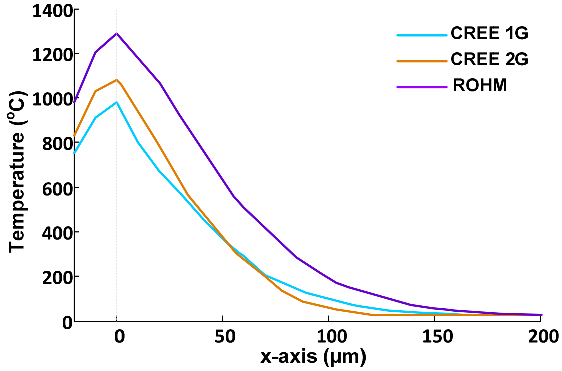
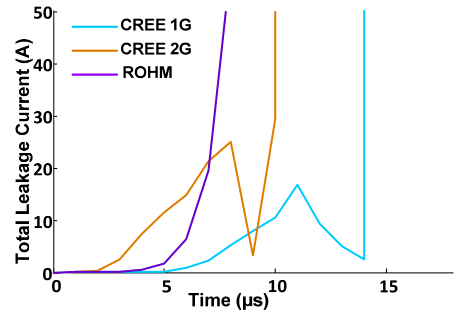


Fig. 13. Comparison of temperature distribution along vertical path.

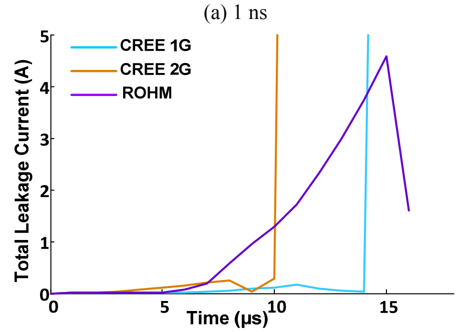
The leakage current of the three devices can be calculated from the junction temperature information. However, as discussed above, the thermal generation lifetime is not easy to be identified precisely for SiC MOSFETs from different device manufacturers. The simulation results will be tentatively obtained using different average generation lifetimes to match with experimental testing results. Based on the junction temperature and leakage current model, the total leakage current is shown in Fig. 14(a) and Fig. 14(b), with an average SRH generation lifetime of 1 ns and 100 ns, respectively. The simulated leakage currents decrease with the increase of generation lifetime. A comparison of the simulated leakage current with the previous experimental results reveals that CREE SiC MOSFETs tend to present a much lower thermal generation lifetime than ROHM SiC MOSFETs.

For CREE SiC MOSFETs, such a high additional bipolar leakage current flowing horizontally in the P well region may activate the parasitic BJT structure shown in Fig. 11. Moreover, high junction temperature will further contribute to the activation of the parasitic BJT, since the built-in voltage of the PN junction decreases with temperature (-2.3 to -3.5 mV / K for 4H-SiC [39]). If the parasitic BJT is on, short circuit current will increase quickly and eventually leads to a device failure due to typical second breakdown and associated thermal runaway issues. On the other hand, the small leakage current of ROHM SiC MOSFETs is difficult to initiate a thermal runaway phenomenon. They are more likely to be damaged because of the high local temperature close to the gate oxide.

Fig. 15 gives the calculated components of the total leakage current for the three devices. As can be observed, the thermal generation current (I_{g_th}) is dominant during the whole short circuit transient. The reason is that the heat wave within the depletion region creates a positive feedback on the intrinsic carrier density when flowing towards the substrate of the power devices. The thermal generation current, responsible for the thermal runaway issue, increases monotonously with temperature evolution and reaches around 20 A for CREE SiC MOSFETs before device turn-off. The avalanche generation current (I_{g_av}) is negligible, and decreases with temperature due to reduced impact ionization rate at higher temperatures. The diffusion generation current (I_{g_diff}) is also small before device turn-off, while it increases quickly at the end of short circuit the transient.



(a) 1 ns



(b) 100 ns

Fig. 14. Comparison of total leakage current with different generation lifetimes.

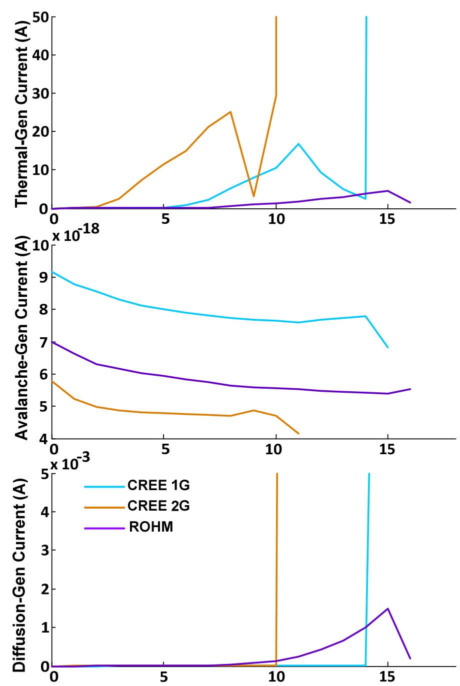


Fig. 15. Calculated leakage current components of the three SiC MOSFETs.

More numerical simulation studies have also been conducted for the CREE 1G SiC MOSFETs based on the previous testing results. Fig. 16 illustrates the comparison of depletion region boundary (x = 0) temperature evolution and total leakage current of the CREE 1G SiC MOSFETs with different combinations of DC bus voltage (600 V to 750 V) and case temperature (25 ºC to 200 ºC).

As can be observed, even though the short circuit critical energy and withstand time are different for the three cases, the leakage currents start to increase quickly when the temperature is higher than 700 ºC. The leakage currents continue increasing until the temperature reaches around 1000 ºC. With the assumption of the same device failure temperature, the short circuit withstand time can be predicted under given short circuit conditions. In addition, for the same die size (or current density), higher voltage stress (or electric field) results in a faster temperature rise, as revealed by the heat diffusion equation.

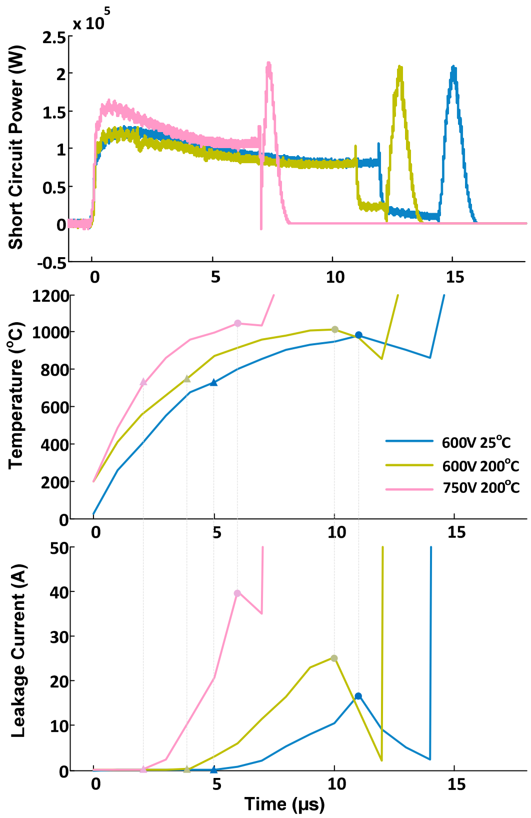


Fig. 16. Numerical simulation results with different combinations of DC bus voltage and case temperature.

IV. Conclusion

In this paper, the temperature dependent short circuit capability of three different types of commercial SiC MOSFETs has been evaluated experimentally. An electro-thermal model and a leakage current model, taking temperature dependent thermal properties of SiC material into account, have also been built to calculate the junction temperature distribution and leakage current components. The key points of this paper can be summarized as follows:

1) The short circuit withstand time and critical energy of SiC MOSFETs will be reduced with the increase of current density, case temperature, and DC bus voltage. However, these are nearly independent of device scaling (i.e. die paralleling) and fault types (i.e. HSF and FUL).

2) The junction temperature will increase quickly during a short circuit transient, which reaches a maximum point at the boundary of depletion region. The higher current density results in a faster temperature rise and larger temperature gradient.

3) The high temperature heat wave within depletion region creates a positive feedback on the intrinsic carrier density. The fast increase in intrinsic carrier density leads to a thermal generation current which dominates the total leakage current during the whole short circuit transient.

4) The short circuit failure mechanisms of SiC MOSFETs can be thermal generation current induced thermal runaway or high temperature related gate oxide damage.

5) The heat flux diffuses a limited distance toward the substrate before device failure, which indicates the short circuit capability of modern SiC MOSFETs can be independent of packaging materials and external cooling conditions.

The experimental results and numerical simulation results presented in this paper aim at helping designers to evaluate actual safety margins for SiC MOSFET based converters. Additionally, it may provide device manufacturers with some useful feedback to improve their future device technologies.

Acknowledgement

This work was partially funded by the II-VI Foundation and Oak Ridge National Laboratory under the U.S. Department of Energy's Vehicle Technologies Program. This work made use of Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation and the Department of Energy under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

References

[1] R. Wang, D. Boroyevich, P. Ning, Z. Wang, F. Wang, P. Mattavelli, K. Ngo, and K. Rajashekara, "A high-temperature SiC three-phase AC-DC converter design for > 100 °C ambient temperature," *IEEE Trans. Power Electron*., vol. 28, no. 1, pp. 555–572, Jan. 2013.

[2] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si evaluation of potentials for performance improvement of inverter and DC–DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron*., vol. 58, no. 7, pp. 2872–2882, Jul. 2011.

[3] J. Rabkowski, D. Peftitsis, and H.-P. Nee, "Silicon carbide power transistors—A new era in power electronics is initiated," *IEEE Ind. Electron. Mag*., vol. 6, no. 2, pp. 17–26, Jun. 2012.

[4] D. Peftitsis, G. Tolstoy, A. Antonopoulos, J. Rabkowski, J. -K. Lim, M. Bakowski, L. Ängquist, and H.-P. Nee, "High -power modular multilevel converters with SiC JFETs," *IEEE Trans. Power Electron*, vol.27, no. 1, pp. 28–36, Jan. 2012.

[5] I. Josifovic, J. Popovic-Gerber, and J. Ferreira, "Improving SiC JFET switching behavior under influence of circuit parasitics," *IEEE Trans. Power Electron*., vol. 27, no. 8, pp. 3843–3854, Aug. 2012.

[6] X. Wu, S. Cheng, Q. Xiao, and K. Sheng, "A 3600V/80A series-parallel connected silicon carbide MOSFETs module with single external gate driver," *IEEE Trans. Power Electron*., vol. 29, no. 5, pp. 2296–2306, May 2014.

[7] D. Aggeler, F. Canales, J. Biela, and J. W. Kolar, "D*v*/D*t*-control methods for the SiC JFET/Si MOSFET cascode," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4074–4082, Aug. 2013.

[8] Z. Wang, X. Shi, L. Tolbert, F. Wang, Z. Liang, D. Costinett, and B. Blalock, "A high temperature silicon carbide MOSFET power module with integrated silicon-on-insulator based gate drive," *IEEE Trans. Power Electron*., vol. 30, no. 3, pp. 1432–1445, Mar. 2015.

[9] K. Rajashekara, "Present status and future trends in electric vehicle propulsion technologies," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 1, pp. 3–10, Mar. 2013.

[10] W. Zhou, X. Zhong, and K. Sheng, "High temperature stability and the performance degradation of SiC MOSFETs," *IEEE Trans. Power Electron*., vol. 29, no. 5, pp. 2329–2337, May 2014.

[11] J. D. Scofield, J. N. Merrett, J. Richmond, A. Agarwal, and S. Leslie, "Performance and reliability characteristics of 1200 V, 100 A, 200 °C half-bridge SiC MOSFET-JBS diode power modules," in *Proc. IMAPS International Conference on High Temperature Electronics*, May 2010, pp. 1–8.

[12] S. DasGupta, R. J. Kaplar, M. J. Marinella, M. A. Smith, and S. Atcitty, "Analysis and prediction of stability in commercial, 1200 V, 33A, 4H-SiC MOSFETs," in *Proc. IEEE International Reliability Physics Symposium*, 2012, pp. 31–35.

[13] X. Huang, G. Wang, Y. Li, A. Q. Huang and B. Jayant Baliga, "Short-circuit capability of 1200 V SiC MOSFET and JFET for fault protection," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 197–200.

[14] A. Fayyaz, L. Yang, and A. Castellazzi, "Transient robustness testing of silicon carbide (SiC) power MOSFETs," in *Proc. European Conference on Power Electronics and Applications*, 2013, pp. 1–10.

[15] D. Othman, M. Berkani, S. Lefebvre, A. Ibrahim, Z. Khatir, and A. Bouzourene, "Comparison study on performances and robustness between SiC MOSFET & JFET devices–Abilities for aeronautics application," *Microelectronics Reliability*, vol. 52, no. 9, pp. 1859–1964, Sep. 2012.

[16] D. Othman, S. Lefebvre, M. Berkani, Z. Khatir, A. Ibrahim, and A. Bouzourene,, "Investigation of 1.2 kV investigation of SiC MOSFETs for aeronautics applications," in *Proc. European Conference on Power Electronics and Applications*, 2013, pp. 1–9.

[17] Z. Wang, X. Shi, Y. Xue, L. Tolbert, F. Wang, and B. Blalock, "Design and performance evaluation of overcurrent protection schemes for silicon carbide power MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5570–5581, Oct. 2014.

[18] R. S. Chokhawala, J. Catt, and L. Kiraly, "A discussion on IGBT short-circuit behavior and fault protection schemes," *IEEE Trans. Ind. Appl.*, vol. 31, no. 2, pp. 256–263, Mar. 1995.

[19] C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, and P. Mattavelli, "High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 3235–3242.

[20] Cree, CMF20120D-silicon carbide power MOSFET datasheet, 2012, available online at http://www.cree.com/.

[21] Cree, C2M0080120D-silicon carbide power MOSFET datasheet, 2014, available online at http://www.cree.com/.

[22] Rohm, SCT2080KE N-channel SiC power MOSFET datasheet, 2014, available online at http://www.rohm.com/.

[23] A. Pérez-Tomás, P. Brosselard, P. Godignon, J. Millán, N. Mestres, M. R. Jennings, J. A. Covington, and P. A. Mawby, "Field-effect mobility temperature modeling of 4H-SiC metal-oxide-semiconductor transistors," *Journal of Applied Physics*, vol. 100, no. 11, pp. 114508–114508–6, Dec. 2006.

[24] M. Otsuki, Y. Onozawa, H. Kanemaru, Y. Seki, T. Matsumoto, "A study on the short-circuit capability of field-stop IGBTs," *IEEE Trans. Electron Devices*, vol. 50, no. 6, pp. 1525–1531, Jun. 2003.

[25] Rohm, "SiC power devices and modules" *Application Note*, Jun. 2013, available online at http://rohmfs.rohm.com/en/products/databook/applinote/discrete/sic/common/sic_appli-e.pdf/.

[26] L. Snead, T. Nozawa, Y. Katoh, T. Byun, S. Kondo, and D. Petti, "Handbook of SiC properties for fuel performance modeling," *Journal of Nuclear Materials*, vol. 371, no. 1–3, pp. 329–377, Sep. 2007.

[27] Z. Khatir, S. Lefebvre, F. Saint-Eve, "Experimental and numerical investigations on delayed short-circuit failure mode of single chip IGBT devices," *Microelectronics Reliability*, vol. 47, no. 2–3, pp. 422–428, Mar. 2007.

[28] M. J. Marinella, D. K. Schroder, G. Chung, M. J. Loboda, T. Isaacs-Smith, and J. R. Williams, "Carrier generation lifetimes in 4H-SiC MOS capacitors," *IEEE Trans. Electron Devices*, vol. 57, no. 8, pp. 1910–1923, Aug. 2010.

[29] P. Neudeck, S. Kang, J. Petit, and M. Tabibazar, "Measurement of n-type dry thermally oxidized 6H-SiC metal–oxide–semiconductor diodes by quasi-static and high-frequency capacitance versus voltage and capacitance transient techniques," *Journal of Applied Physic*, vol. 75, no. 12, pp. 7949–7953, Jun. 1994.

[30] J. N. Pan, J. A. Cooper, and M. R. Melloch, "Extremely long capacitance transients in 6H-SiC metal–oxide–semiconductor capacitors," *Journal of Applied Physic*, vol. 78, no. 1, pp. 572–574, Jul. 1995.

[31] B. J. Baliga (2005), *Silicon Carbide Power Devices*. Singapore: World Scientific Press.

[32] T. T. Mnatsakanov, L. I. Pomortseva, and S. N. Yurkov, "Semiempirical model of carrier mobility in silicon carbide for analyzing its dependence on temperature and doping level," *Semiconductors*, vol. 35, no. 4, pp. 394–397, April 2001.

[33] S. Nigam, "Carrier lifetimes in silicon carbide," *Ph.D. Dissertation*, Carnegie Mellon University, Mar. 2008.

[34] O. Kordina, J. P. Bergman, C. Hallin, and E. Janzén, "The minority carrier lifetime of n type 4H and 6H SiC epitaxial layers," *Applied Physics Letters*, vol. 69, no. 5, pp. 679–681, Jul. 1996.

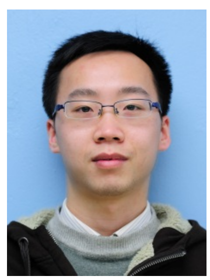
[35] T. Hayashi, K. Asano, J. Suda, and T. Kimoto, "Temperature and injection level dependencies and impact of thermal oxidation on carrier lifetimes in p-type and n-type 4H–SiC epilayers," *Journal of Applied Physics*, vol. 109, no. 1, pp. 0145051–0145055, 2011.

[36] R. Raghunathan and B. J. Baliga, "Temperature dependence of hole impact ionization coefficients in 4H and 6H-SiC," *Solid-State Electronics*, vol. 43, no. 2, pp. 199–211, Feb. 1999.

[37] D. M. Nguyen, C. Raynaud, N. Dheilly, M. Lazar, D. Tournier, P. Brosselard, and D. Planson, "Experimental determination of impact ionization coefficients in 4H-SiC," *Diamond & Related Materials*, vol. 20, no. 3, pp. 395–397, Mar. 2011.

[38] M. Bouarroudj-Berkani, D. Othman, S. Lefebvre, S. Moumen, Z. Khatir, and T. Ben Sallah, "Ageing of SiC JFET transistors under repetitive current limitation conditions," *Microelectronics Reliability*, vol. 50, no. 9–11, pp. 1532–1537, Sep. 2010.

[39] N. Zhang, "4H-Silicon carbide PN diode for harsh environment temperature sensing applications," *M.S. Thesis*, University of California, Berkeley, May. 2014.

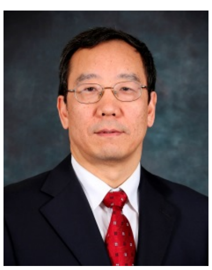


Zhiqiang Wang (S'11) received the B.S. degree from Hunan University, Changsha, China, in 2007 and M.S. degree from Zhejiang University, Hangzhou, China, in 2010, both in electrical engineering. He started Ph.D. study in 2010 at the Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, Blacksburg, and in 2011 he transferred to the Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT), The University of Tennessee, Knoxville, where he is currently working toward the Ph.D. degree. Since 2010, he has been a Graduate Research Assistant at CPES and CURENT. His research interests include high power grid-connected converters, high temperature high density power conversion, intelligent gate drivers, and packaging and integration of SiC power modules.

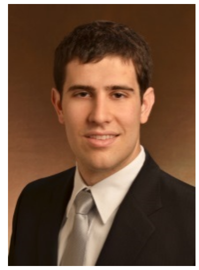
Xiaojie Shi (S'11) received the B.S. degree from Huaqiao University, Quanzhou, China, in 2008 and M.S. degree from Zhejiang University, Hangzhou, China, in 2011, both in electrical engineering. She started Ph.D. study in 2011 at the Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT), The University of Tennessee, Knoxville, where she is currently working toward the Ph.D. degree as a Graduate Research Assistant. Her research interests include high power grid-connected converters, HVDC transmission systems, and integration of distributed energy resources.

Leon M. Tolbert (S'88-M'91-SM'98-F'13) received the B.E.E., M.S., and Ph.D. degrees in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 1989, 1991, and 1999, respectively. He joined Oak Ridge National Laboratory (ORNL) in 1991 and joined the University of Tennessee, Knoxville, TN, USA, in 1999, and is currently the Min H. Kao Professor and Head of the Department of Electrical Engineering and Computer Science. He is also a part-time Senior Research Engineer at ORNL. Dr. Tolbert is a Registered Professional Engineer in the State of Tennessee. He was elected as a member-at-large to the IEEE Power Electronics Society Advisory Committee for 2010–2012, and he served as the Chair of the PELS Membership Committee from 2011 to 2012. He was an associate editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2007 to 2012 and the IEEE POWER ELECTRONICS LETTERS from 2003 to 2006.

Fei (Fred) Wang (S'85-M'91-SM'99-F'10) received his Ph.D. degree in electrical engineering from University of Southern California (USC). He was a Research Scientist in the USC Electric Power Lab from 1990 to 1992. He joined the GE Power Systems Engineering Department, Schenectady, NY, as an Application Engineer in 1992. From 1994 to 2000, he was a Senior Design Engineer with GE Industrial Systems, Salem, VA. During 2000 to 2001, he was the Manager of Electrical Systems Technologies Lab, GE Global Research Center, Niskayuna, NY and Shanghai, China. From 2001 to 2009, he was an Associate Professor at the Center for Power Electronics Systems (CPES), Virginia Tech. Since 2009, he has been with The University of Tennessee, Knoxville (UTK) and Oak Ridge National Lab as a Professor and Condra Chair of Excellence in Power Electronics. He is a founding member and Technical Director of the NSF/DOE Engineering Research Center CURENT at UTK.



Zhenxian Liang (SM'01) is a R&D staff member of the Power Electronics & Electric Power Systems Research Center at Oak Ridge National laboratory (ORNL). Prior to joining to ORNL, he worked with R&A division of Ford Motor Company, GE Global Research Center and CPES at Virginia Tech, Electrical Engineering School of Xi'an Jiaotong University. He has engaged in research to develop advanced electronics device/module technologies for highly functional, high power density and high temperature electronics systems. His expertise includes power semiconductors and devices physics; device/IC micro-fabrication technology; power module packaging, cooling and reliability assessment, as well as their applications in electric power conversion systems. He is currently involved in the development of power semiconductor packaging technology and integrated power electronics modules for advanced xEV applications. He has published more than 100 papers and holds four US patents and numerous technical disclosures. Zhenxian Liang received the B.Sc (Eng.) and the M. Sc (Eng.) degrees, both from Xi'an Jiaotong University, Xi'an, China, and the Ph. D degree from Chinese Academy of Sciences, China, all in electrical engineering in 1983, 1986 and 1993, respectively.



Daniel Costinett (S'10-M'13) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Colorado, Boulder, concluding in 2013. In 2012, he assisted with research and course development as an instructor at Utah State University. He is currently an Assistant Professor in the Department of Electrical Engineering and Computer Science at the University of Tennessee, Knoxville. His research interests include resonant and soft switching power converter design, high efficiency power supplies, mixed-signal integrated circuit design, implantable devices, and electric vehicles. Dr. Costinett is the Co-Director of Education and Diversity for the National Science Foundation/Department of Energy Research Center for Ultra-wide-area Resilient Electric Energy Transmission Networks (CURENT). He also has a joint appointment as a Research Engineer with the Power Electronics and Electric Machinery Group at Oak Ridge National Laboratory. He currently serves as Associate Editor for IEEE Transactions on Industry Applications.

Benjamin J. Blalock (SM'06) is a Professor in the Department of Electrical Engineering and Computer Science at The University of Tennessee where he directs the Integrated Circuits and Systems Laboratory (ICASL). He received his B.S. degree in electrical engineering from the University of Tennessee, Knoxville, in 1991 and the M.S. and Ph.D. degrees, also in electrical engineering, from the Georgia Institute of Technology, Atlanta, in 1993 and 1996 respectively. His research focus at UT includes analog/mixed-signal integrated circuit design for extreme environments (both wide temperature and radiation) across multiple semiconductor technologies, high-temperature/high-voltage gate drive circuits for silicon carbide (SiC) power electronics, multi-channel monolithic instrumentation systems, and mixed-signal/mixed-voltage circuit design for systems-on-a-chip. He has also worked as an analog IC design consultant for Cypress Semiconductor, Concorde Microsystems, and Global Power Electronics. Dr. Blalock is a senior member of the IEEE.