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SANDIA SYSTEMATIC DECLASSIFICATION REVIEW
[illegible] DECLASSIFICATION STAMP
Emilda Selph 9-11-97
AUTHORITY: R.B. Craner
PERSON CHANGING [illegible]
Carmela Gallegos 9/17/97
PERSON VERIFYING MARKING [illegible]
RECORD ID: 97SN3340
DATED: 9/3/97

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SC-TM-64-11

A CODED TRANSMISSION SYSTEM
(Title Unclassified)

[redacted]

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March 1964

SANDIA SYSTEMATIC DECLASSIFICATION REVIEW
1st Review Date: 8/19/97
Authority: ☐ADC ☒ADD
Name: W. Layne
2nd Review Date: 9/3/97
Authority: ADD
Name: R.B. Craner
Determination (Circle Numbers):
1. Classification Retained
2. Classification Changed to: U
3. Contains No DOE Classified Information
4. Coordinate With:
5. Contains UCAI?
6. Comments:
OK for Openmet

ABSTRACT

This report presents a cryptographic method of handling messages and attempts to show the feasibility of applying magnetics technology to this method.

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ACKNOWLEDGMENT

We sincerely thank J. L. Rogers, 2423, for his supervisory assistance, R. H. Braasch, 2423, for his suggestions and assistance in system design, and E. J. Bernard, 2423, for his design and development of the magnetic driver.

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A CODED TRANSMISSION SYSTEM

1. Summary

A method is described for encoding and subsequent decoding of a message. Message is defined as alpha or numeric characters in the form of groups of sentences or lists of numbers. Figure 1 illustrates a possible basic system configuration for a coded transmission system. This system is capable of making a message unintelligible except to a complementary decoding device.

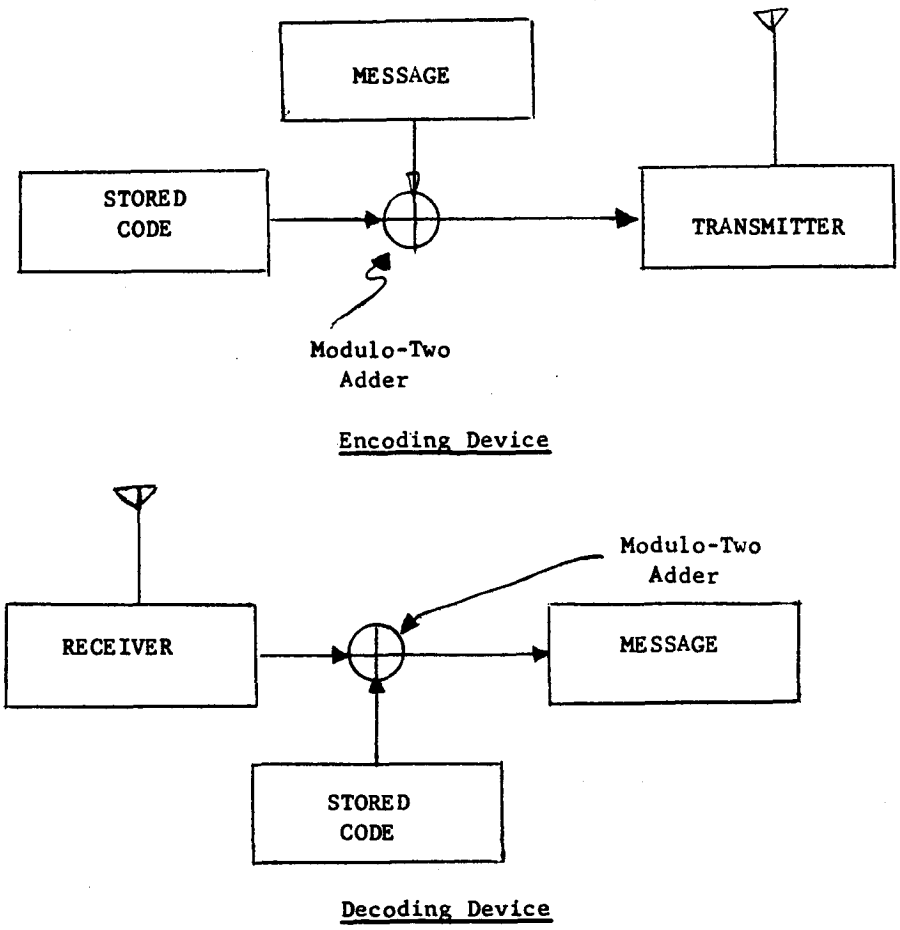

Figure 1. Encoding and decoding device

The coded transmission system consists of two distinctly separate units: the transmitter or encoding device and the receiver or decoding device. These units are centered around a stored code and a modulo-two adder.* In the encoding process, the modulo-two adder adds message information to the stored code; the output from the modulo-two adder contains the encoded message. The encoded message may be transmitted through some medium to the complementary decoding device. In the decoding process, the modulo-two adder adds the output from the receiver to the stored code. The output from the modulo-two adder will be the decoded message if the stored code in the decoding device is the same stored code which was used in the encoding device to encode the original message. Synchronizing the stored code input and the receiver input to the modulo-two adder in the decoding device is discussed in Section V of this report.

To illustrate the coding method, a demonstration model of a coded transmission system was implemented,** utilizing a hybrid configuration of magnetics and semiconductors. Magnetics were chosen to prove the feasibility of applying magnetic techniques to a complete system.

Topics discussed in this report are: terminology, the overall system, magnetic techniques, the transmitter or encoding device, the receiver or decoding device, input-output equipment, and circuitry.

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*Concept originated by J. L. Rogers, 2423, G. R. Bachand, 1421, and I. Browning, Panoramic Research, Palo Alto, Calif., formerly employed by Sandia.

**Method of implementation, idea of J. L. Rogers, 2423.

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II. Introduction

The coded transmission system was developed to demonstrate a principle. It is not intended as an operational device for use in the field. Figure 2 illustrates the basic configuration. One notes that both the transmitter and receiver utilize a paper-tape reader as the input device and a paper-tape punch as the output device. Any convenient input-output equipment can be utilized in this system. The demonstration model of the coded transmission system utilizes a switching network to eliminate redundancy in the input-output equipment. This eliminates one paper-tape reader and one paper-tape punch. In an operational device, the transmitter and receiver could be separated by a considerable distance. This would require each unit to have its own input-output equipment.

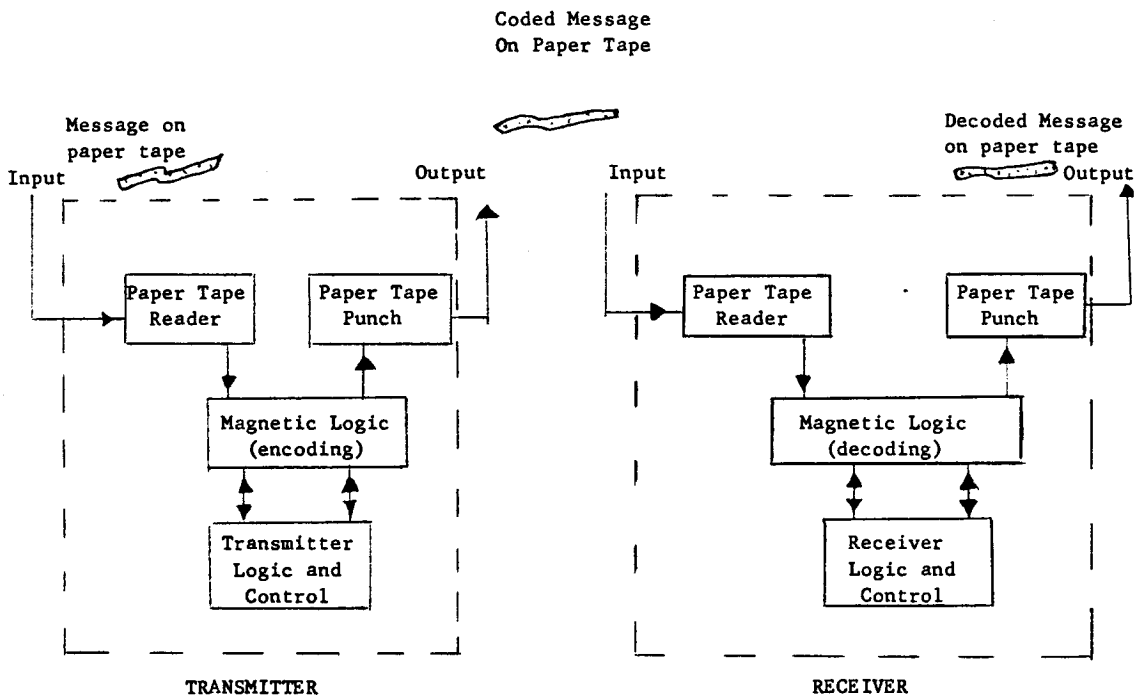

Figure 2. Block diagram of coded transmission system

In encoding a message, the first step is to punch the message onto a paper tape (standard 6-channel) using a Flexowriter. The second step is to read the message into the transmitter. The transmitter encodes the message and punches it out on paper tape.

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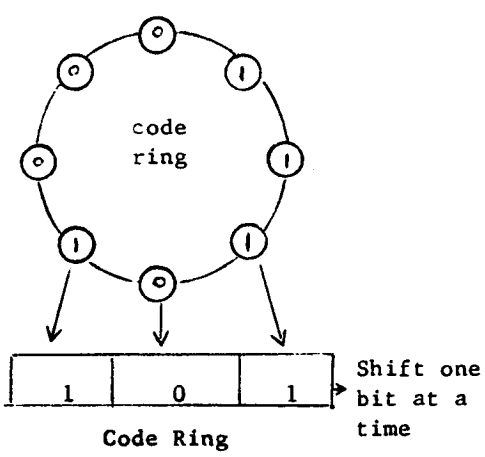
The encoded message can be transported or transmitted to its destination. An <u>important fact</u> to be kept in mind in the encoding process is that the same message can be encoded several times, and each time the encoded message can be made to take on a different configuration.

In decoding a message, the first step is to read the encoded message into the receiver. The second step is to make the receiver decode the message and punch it out on paper tape. The third step is to place the paper tape containing the decoded message on the Flexowriter and make it print out the message.

The following explanation of code rings is presented to provide an understanding of the encoding scheme. In a binary system of numbers, a <u>code ring</u> is a closed sequence of binary bits (0,1) which is 2^N bits long and contains all the combinations of N bit words once and only once as the sequence is shifted one bit at a time: N is any positive integer.

From this definition of a code ring, it can be seen that Figure 3 is a code ring of the Table of Elements where N=3, and $2^N=8$. It should be noted that the number of elements in the Table is equal to the number of bits in the code ring. The number of code rings available to express all combinations of N bit words is given by the expression

$$\text{Number of code rings} = 2^{(2^{N-1} - N)}$$



Decimal	N=3 Binary		
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

8 elements

Figure 3. Code ring and Table of Elements

In the case where N=3, the number of available code rings is two. An important feature of the code ring is that <u>no pattern is ever repeated until all other patterns have been represented</u>. This unique property of code rings suggested their application to cryptographic methods.

Modulo-two addition is used in the magnetic logic sections of both the transmitter and the receiver. It is the logic operation of EXCLUSIVE-OR term by term and is shown in Figure 4.

$$\begin{array}{r} 11001101011001 \\ \oplus\ \underline{10110011110101} \\ 01111110101100 \end{array}$$

Figure 4. Performing modulo-two addition

The Boolean expression for EXCLUSIVE-OR is

$$x \oplus y = X\overline{Y} + \overline{X}Y \ .$$

A simplification of the encoding process is given in Figure 5.

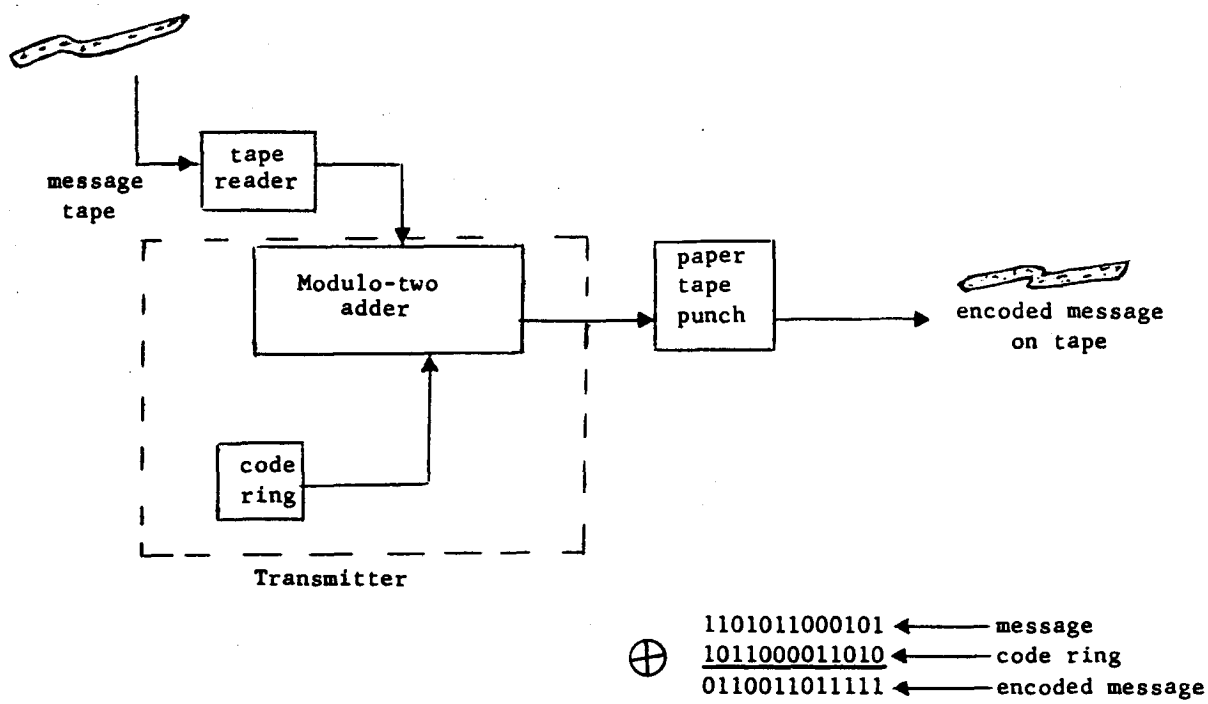
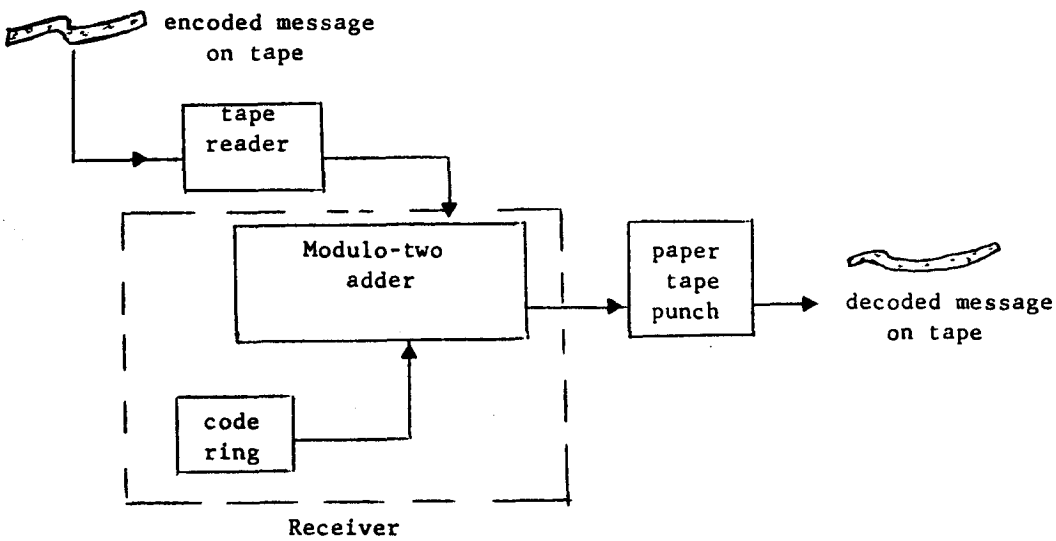


Figure 5. Encoding process

The binary bits on the message tape are modulo-two serially added to the binary bits of the code ring, and the results of this operation are punched on a paper tape. It can now be seen why a message can take on several different configurations when it is encoded. The configuration of the encoded message is wholly dependent upon the point in the code ring at which the encoding process is begun. That is to say, if the message and code ring are modulo-two added starting at one point in the code ring, the encoded message (on paper tape) will take on a unique configuration, but if the message and code ring are modulo-two added starting at any other point in the code ring, the encoded message (on paper tape) will take on another completely unique configuration.

A simplification of the decoding process is given in Figure 6.

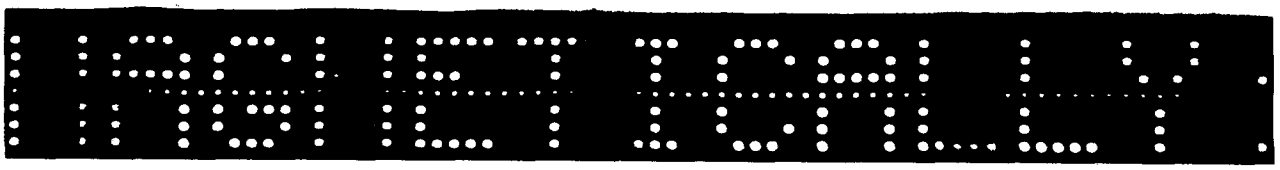


$$\begin{array}{rll} \oplus & 0110011011111 & \text{encoded message} \\ & \underline{1011000011010} & \text{code ring} \\ & 1101011000101 & \text{decoded message} \end{array}$$

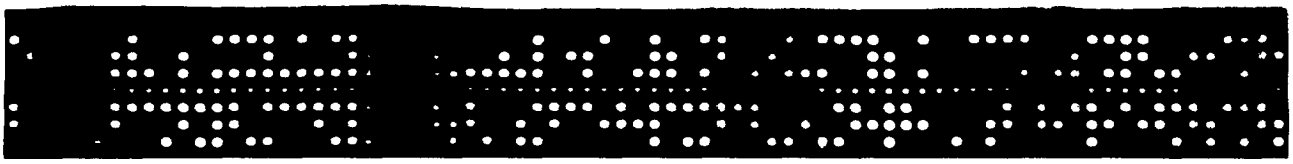
Figure 6. Decoding process

The binary bits on the encoded message tape are modulo-two serially added to the binary bits of the code ring, and the result of this operation (a decoded message) is punched on a paper tape. The question of where to start modulo-two adding of the code ring and the encoded message is answered in Section V of this report.

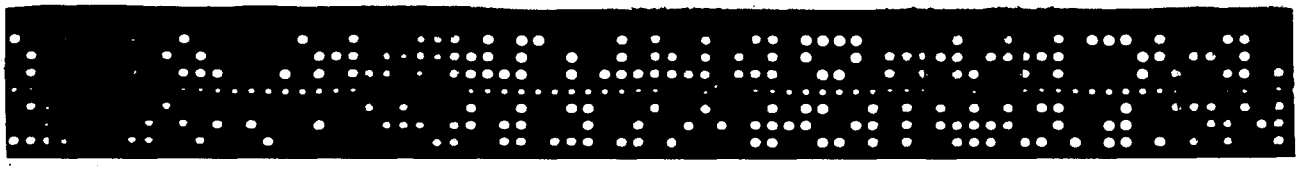
Figure 7 presents examples of message tapes. Figures 7b and 7c are encoded versions of Figure 7a. Figure 7d is the decoded version of either Figure 7b or Figure 7c. Note that Figure 7a and Figure 7d are identical.



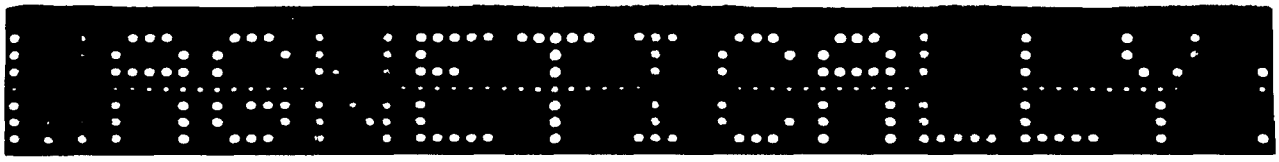
Message tape
(a)



Encoded message tape
(b)



Encoded message tape
(c)



Decoded message tape
(d)

Figure 7. Message tapes

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A large portion of the circuitry utilized in the coded transmission system was obtained from the Sandia AE-3100 series of printed-circuit cards. Most of the gates, flip-flops, Schmitt triggers, relay drivers, and flip-flop resets used in the device were obtained by making slight modifications to the cards. These ready-made logic circuits were used to save time in implementing the demonstration model. The circuitry is described in the Appendix.

Circuits built expressly for this device include delay amplifiers, buffers using silicon control rectifiers, pulse shapers, core drivers (to set bits), a comparator, and several four-layer semiconductor monostable multivibrators. These circuits are described in the Appendix. The comparator is explained in Section V. The logic circuitry used in the coded transmission system recognizes -12 volts as a logical one and ground as a logical zero.

III. Magnetics

The MAD (Multi-Aperture Device) is a specially shaped magnetic core which exhibits square hysteresis loop characteristics. The core is constructed of ferrite material in which a number of minor apertures are spaced around a major aperture (Figure 8).*

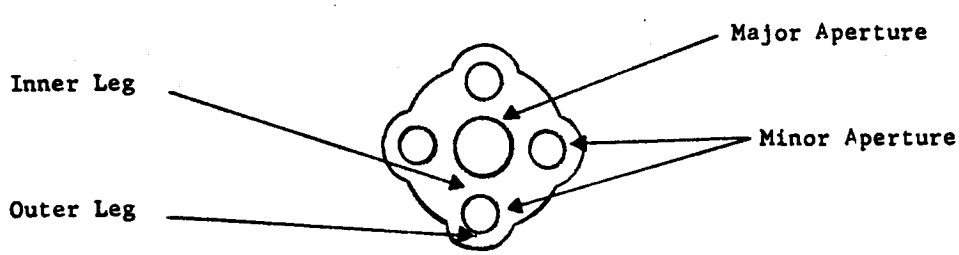

Figure 8. The MAD core

This device is capable of storing a bit of digital information for an indefinite amount of time. It consumes no power while the information is stored in it. Interrogation of the device may be either destructive or nondestructive. The output can be applied directly to a semiconductor, to another core for further utilization, or to a light bulb for visual readout.

*Amp. Inc. Bulletin "New Technique Amp-MAD."

Information and drive signals to cores, as well as interconnection between cores, are accomplished by wiring only. A unit consisting entirely of cores and wire is compact and reliable.

An explanation of how information is stepped through a MAD core and destructively read out is the following. Assume initially, that the core is in a "clear" state and all flux is in a clockwise direction (Figure 9). A logical one is placed in the core by passing through the set winding a current of sufficient amplitude to reverse the flux in the inner legs of all minor apertures. The core is now in a half flux set condition as illustrated in Figure 10.

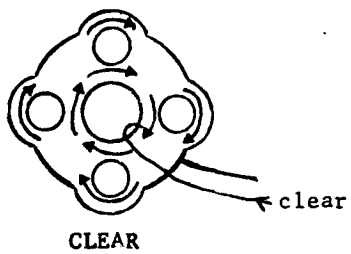

Figure 9. MAD core in clear state

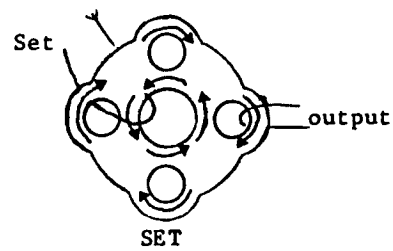

Figure 10. MAD core in set state

Note that there has been no flux reversal in the outer leg of the output aperture. It is now necessary to prepare the output aperture so that a clear signal applied to the core will clear it and generate a one signal in the output winding. The process of preparing the output aperture for readout is called "priming." Prime current serves to reverse the direction of flux around the output aperture of a set core after setting. The situation is depicted in Figure 11. DC prime current or a slowly rising pulse is used so that the flux around the output minor aperture switches slowly and little voltage is induced into the output winding. After priming, the flux linking the output winding is in the opposite direction to the normal "clear" state of the core. A clear pulse, delivered to a primed core, will reverse the flux around the output aperture rapidly and induce a voltage in the output winding as shown in Figure 12. Using this sequence of operation, a one is accepted, stored, and delivered either to another core or to external circuitry.

The coded transmission system uses MAD cores primarily in a magnetic shift register configuration. This configuration consists of two symmetrical rows of cores. The length of the rows is depend-

ent upon the number of stages required to perform the desired operations. The rows are referred to as the O (odd) line of cores and the E (even) line of cores.

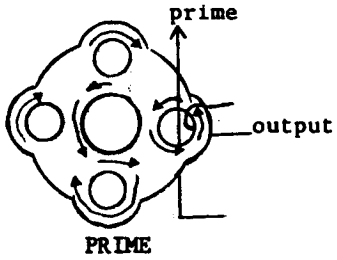

Figure 11. MAD core in prime state

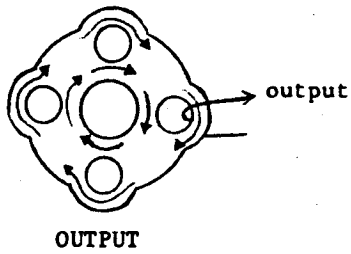

Figure 12. MAD core in output state

Information is inserted into and withdrawn from a shift register in two basic modes: serial and parallel. A serial-input register can accept bits of binary information, one bit at a time, into an input core. A parallel-input register can accept as many binary bits at a time as there are cores in the O line. When information is available from a register at one point only, usually the highest order E core, the register is a serial-output register. When information is available from all cores in the E line, the register is a parallel-output register.

A shift magnetic register can take on any of the following four configurations: serial-in serial-out, serial-in parallell-out, parallel-in serial-out, parallel-in parallel-out. Figure 13 illustrates a six-bit, serial-input, serial-output shift register.

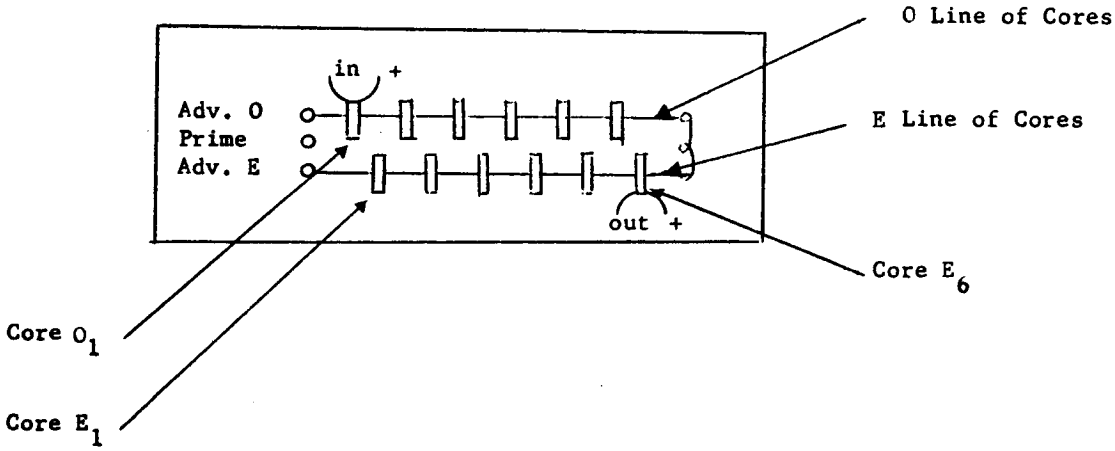

Figure 13. Shift register

Magnetic shift registers in the coded transmission system can accept information in parallel and process it serially, and they can accept information serially and process it in parallel. In addition, these registers can be used for timing and as storage mediums for fixed patterns.

In the following discussion of shift-register operation, the current performing the "clear" operation is referred to as "advance." In order to make a register propagate information, specific current waveforms must be applied to the register terminals with the correct relative polarity. These waveforms arrive in the following order: (1) set, (2) prime, (3) advance O (odd to even), (4) prime, (5) advance E (even to odd).

Utilizing the above waveform sequence, a bit is stepped along the register in the following manner. The bit is initially set into core O_1, and the output aperture of all O cores is primed. An advance O current is delivered to the O line, and the bit is transferred from core O_1 to core E_1. The output aperture of all E cores is then primed, and an advance E current is delivered to the E line. The bit moves from core E_1 to core O_2 and is stored in the O line until the sequence of current waveforms is initiated again. By the clocked arrival of the above-mentioned waveform sequence, it can be seen that the bit will eventually arrive at the output winding on core E_6. The bit may be recirculated from the output winding (going from core E_6 to core O_1) and also be utilized in external circuitry.

The circuitry which develops the current-waveform sequence for the register is called a "driver." A detailed explanation of the drivers contained in the coded transmission system may be found in SCTM 76-63(24).* The magnetic logic circuit which performs modulo-two addition is illustrated in Figure 14.

*E. J. Bernard, 2423, A Magnetic Pulse Generator as Driver for Magnetic Logic, May 1963.

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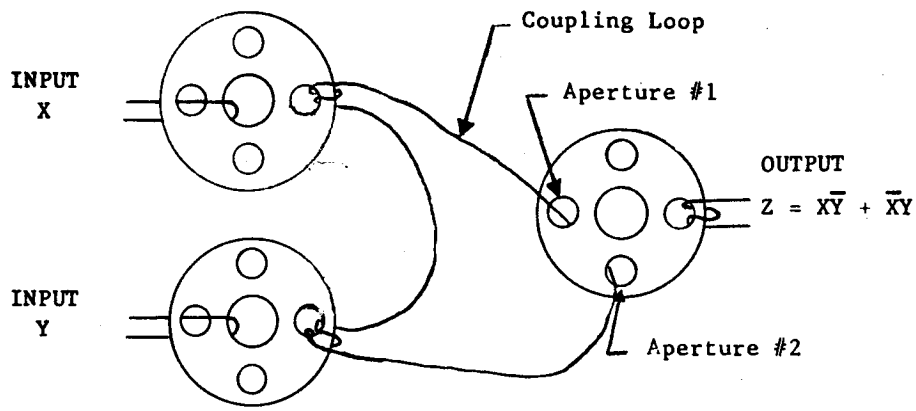

Figure 14. Modulo-two adder

It can be seen from Figure 14 that the output coupling loop windings on the X and Y cores are wound series-opposing. If a one were present in both the X and Y cores, then both cores would generate an equal amplitude but opposite-direction current in the coupling loop; therefore, two simultaneous ones are lost in the coupling loop.

If the X core had a one in it and the Y core did not, a current would be generated in the coupling loop in the proper direction so as to set a one into the Z core through minor aperture No. 2. If the Y core had a one in it and the X core did not, the resulting current in the coupling loop would set a one into the Z core through minor aperture No. 1. In essence, the modulo-two adder consists of three cores and a uniquely wound wire.

IV. Transmitter

The transmitter is used to encode the message tape prepared on the Flexowriter. Figure 15 is a simplified logic diagram to which the transmitter operation is referenced. Figure 16 is a complete logic diagram of the transmitter.

With power applied (±12 volts) and the reset button depressed, the logic levels of the solid-state circuitry are as illustrated in Figure 15. The sides of the flip-flops denoted by a letter, i.e. (M), are logical ones and the complementary sides, i.e. ($\overline{M}$),

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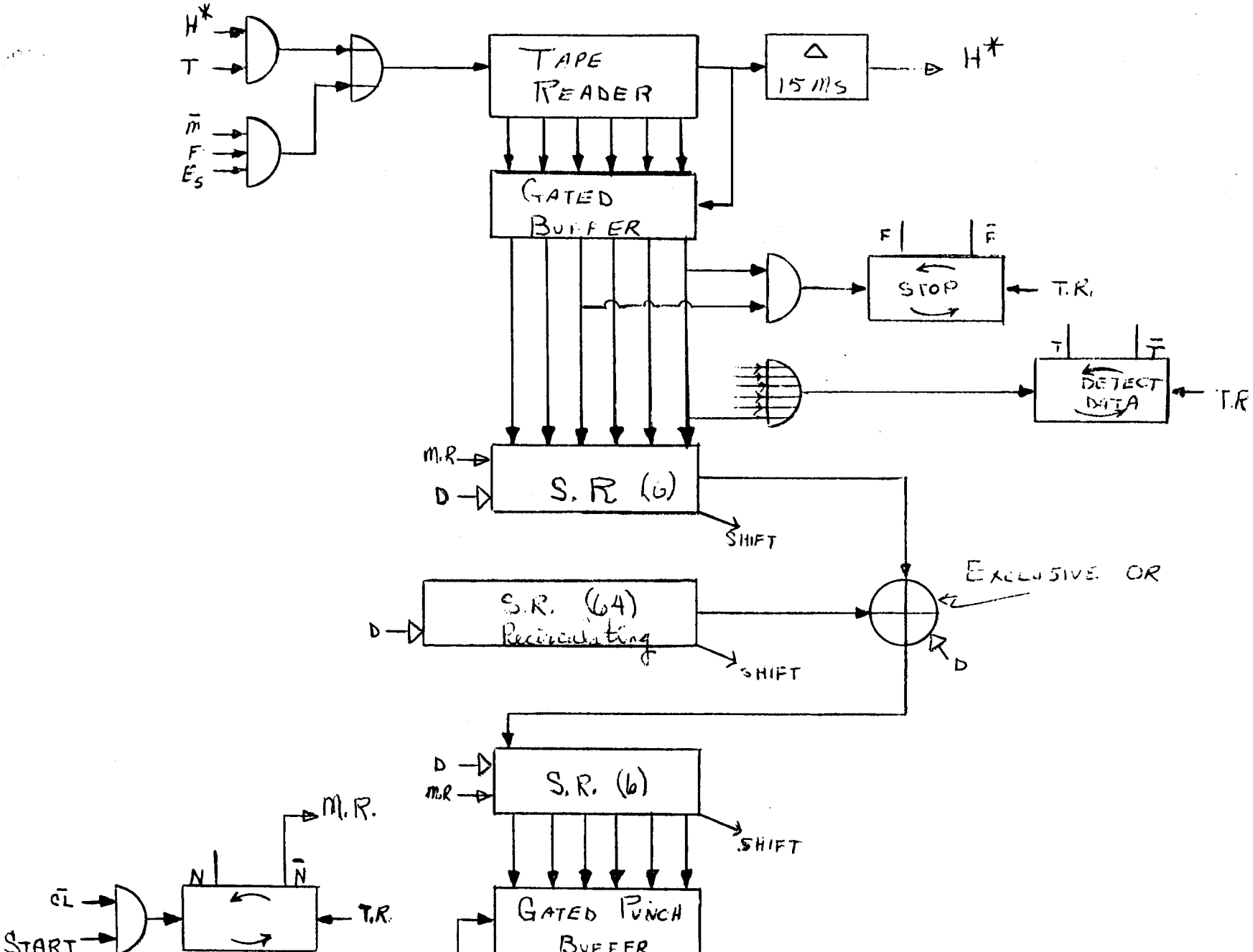

Figure 15. Simplified code

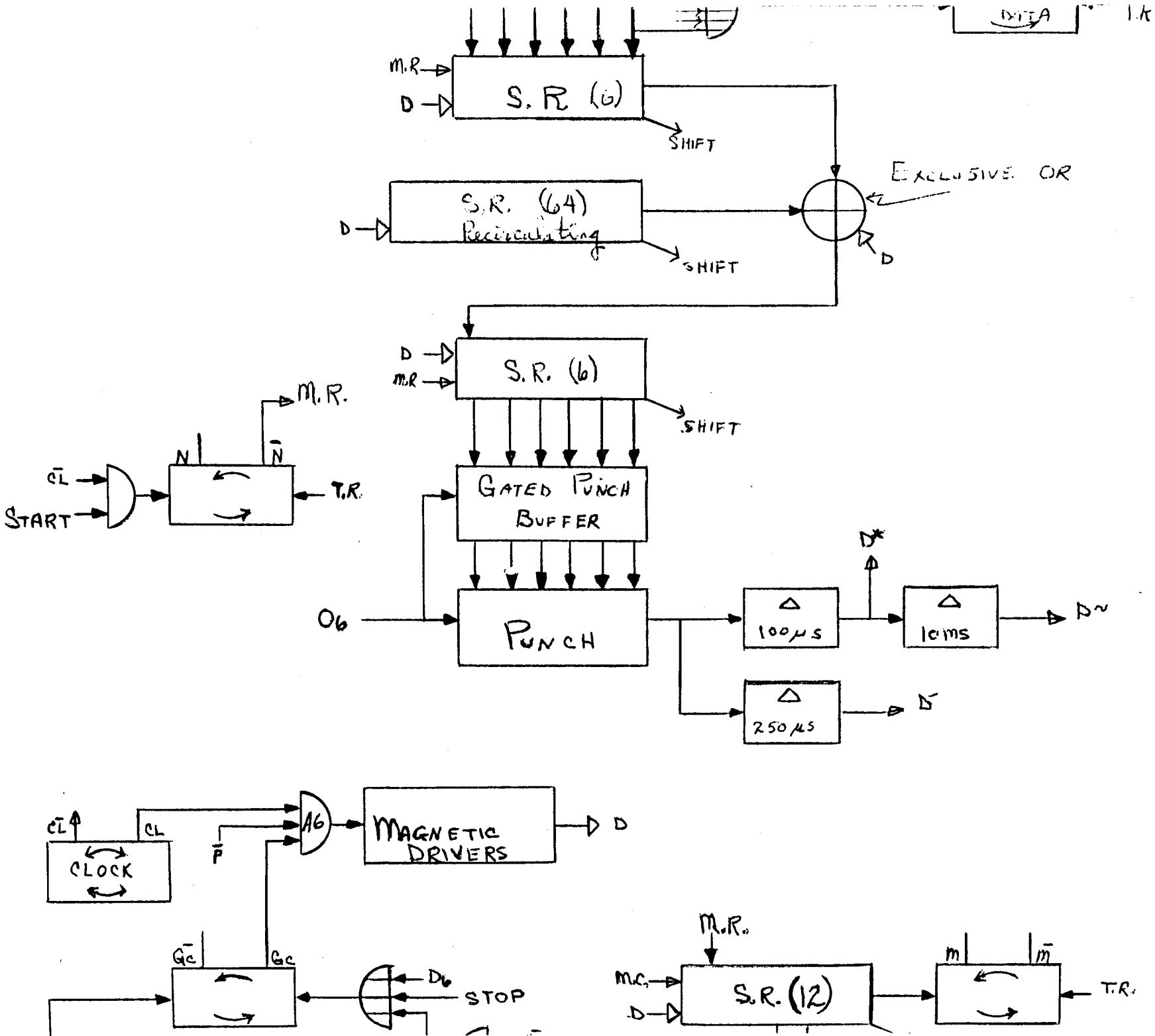

Figure 15. Simplified coded transmission system -- transmitter

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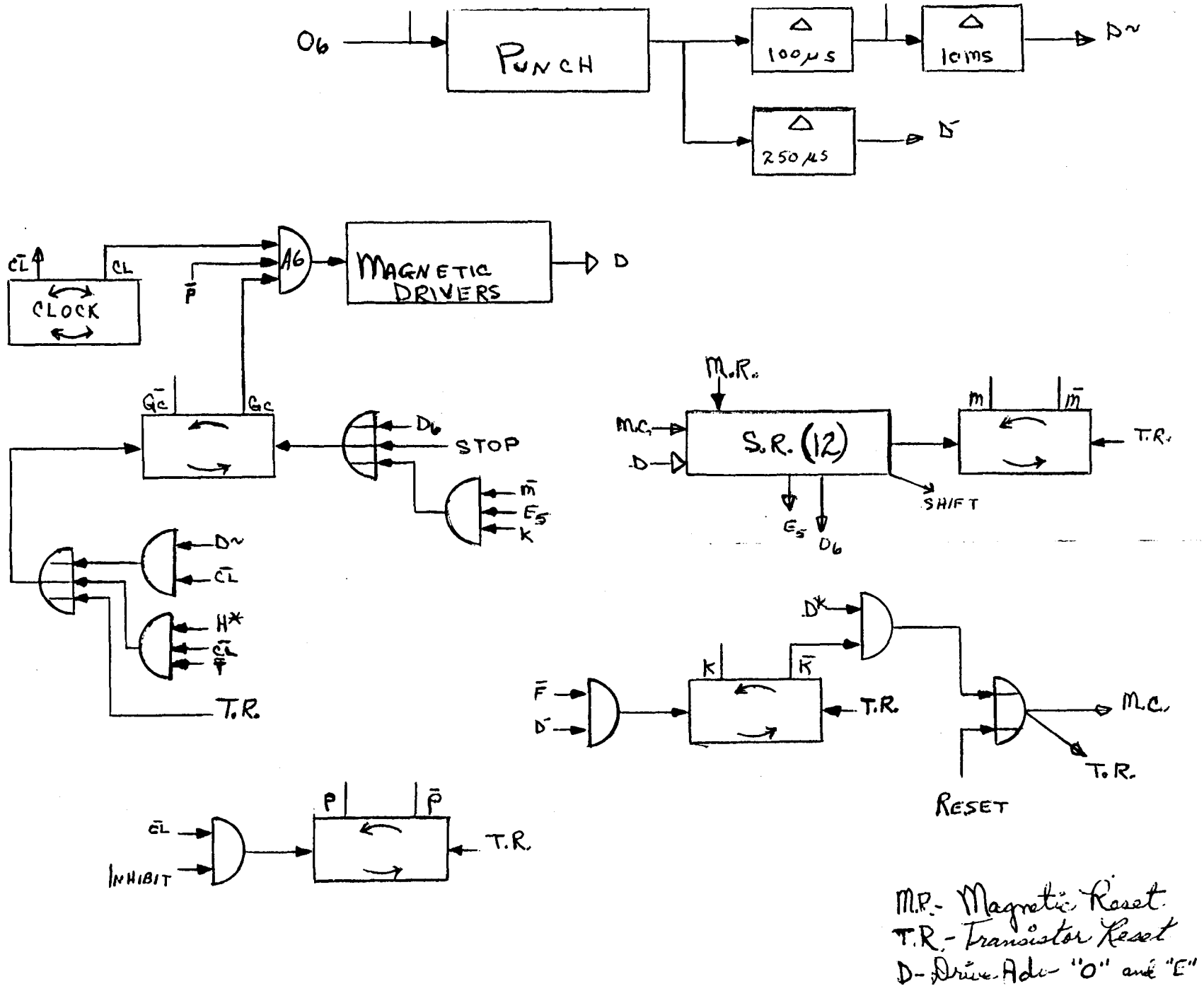

M.R.- Magnetic Reset
T.R.- Transistor Reset
D- Drive Adv "O" and "E"

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smission system -- transmitter

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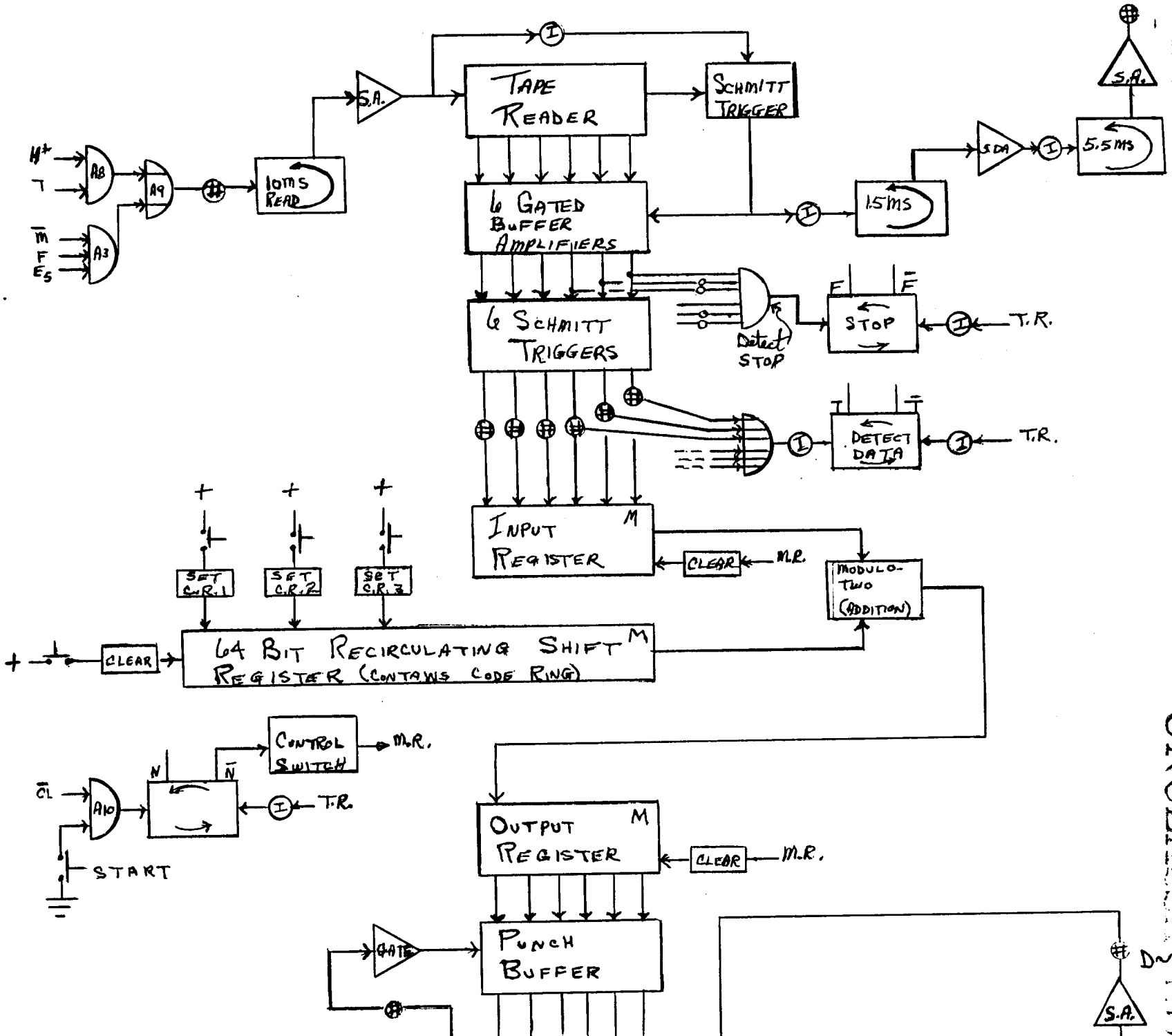

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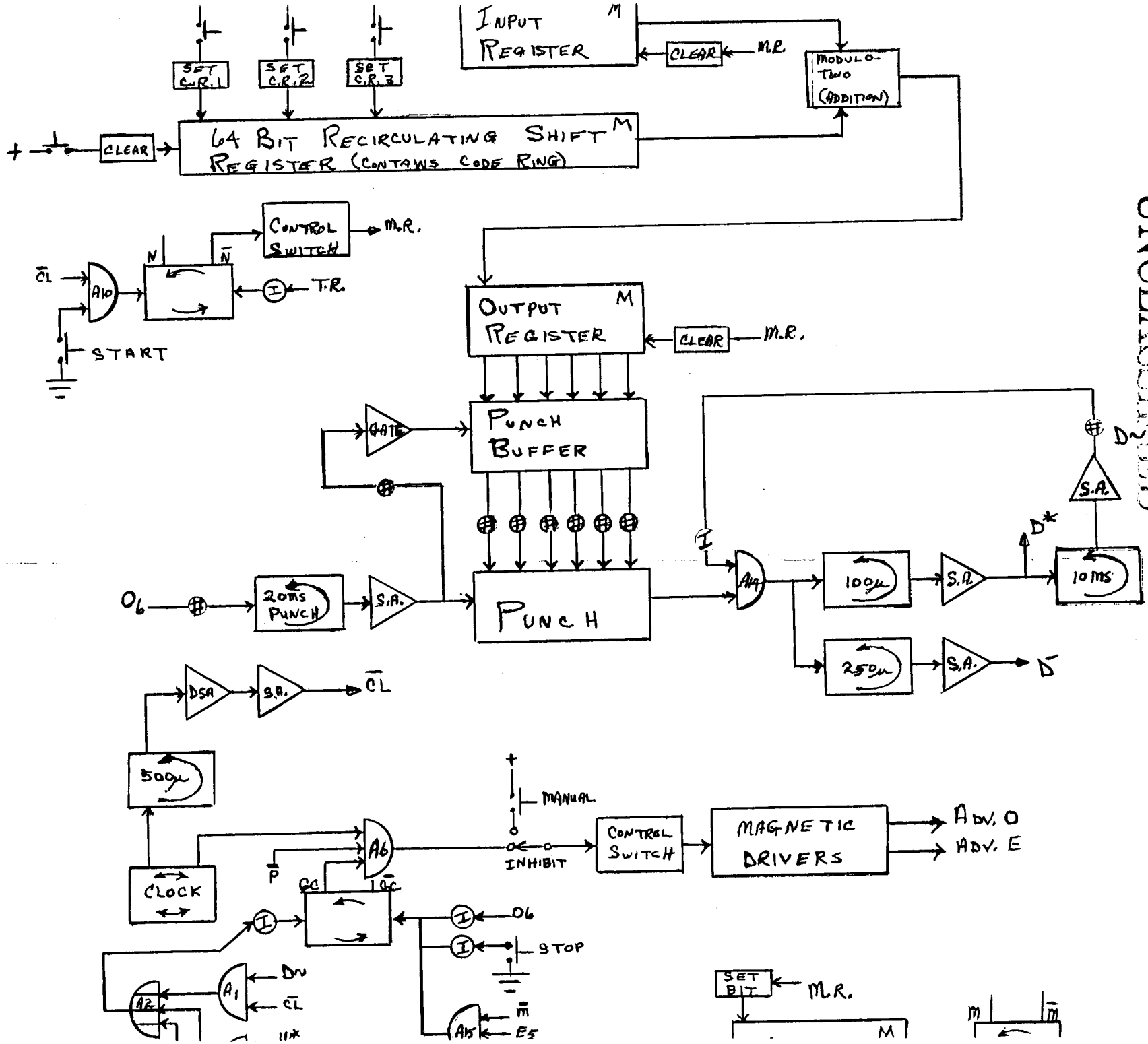

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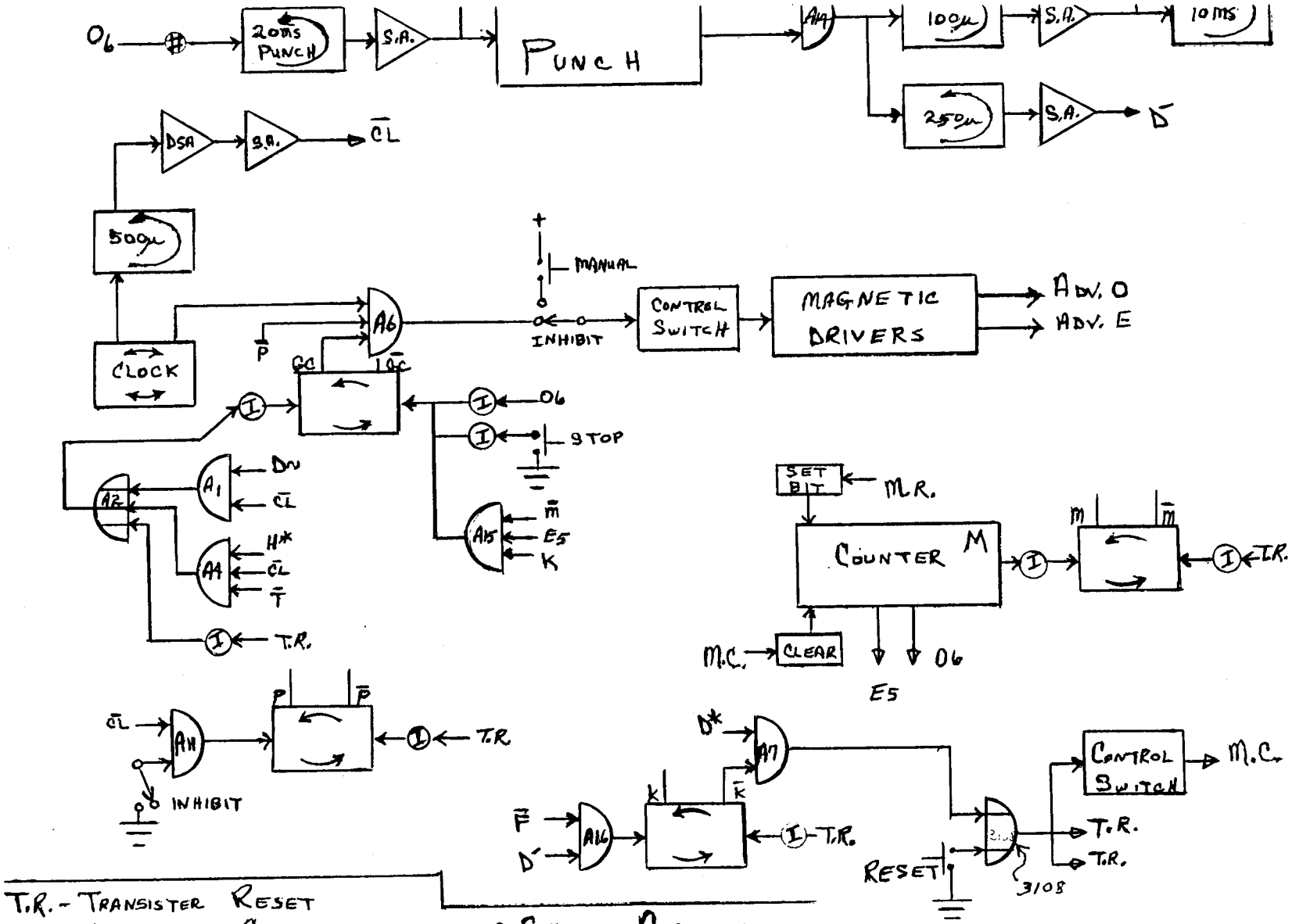

T.R. - TRANSISTER RESET
M.C - MAGNETIC CLEAR
M.R. - MAGNETIC RESET
M. - IMPLEMENTED W MAGNETICS
(R) - RELAY CONTACT

S.A - SPECIAL AMPLIFIER
SDA - SPECIAL DELAY AMPL.
(I) - INVERTER

are logical zeros. All magnetic shift registers are in the clear state, with the exception of the 64-bit register and the output register. The drivers are receiving signals from clock through gate A_6, and the preinstalled code ring is cycling in the 64-bit recirculating shift register and through the nonrecirculating output register.

The transmitter is timed by three timing marks per cycle which are in chronological order clock, advance O, and advance E. Logic can be performed at any one of these marks or at all three in a given cycle. The multimark timing adds flexibility to the system as well as complexity. In addition, the overall timing of the system is asynchronous.

The logic for the system is so arranged that clock signals are not received by the drivers when the reader or punch is operating. Upon the conclusion of the read or punch cycle, clock signals are reinstated to the drivers. Since most of the timing signals are generated dynamically by the magnetics for the transmitter, merely interrupting clock to the driver will halt the transmitter.

The first step in processing a message tape is to put some recognizable signal on the output encoded tape. This is done by preceding the encoded message with two characters (12 bits) of code ring.

It is necessary to put two characters of code ring on the tape, in lieu of one, because in a code ring where N=6, there is one character consisting of six zeros. If only one character were placed on the tape, the receiver could not distinguish between the unique character of the code ring (six zeros) and the many characters of tape leader (also all zeros); therefore, the receiver could not perform its specified function.

Actuating the start circuitry places a bit in the magnetic counting register and clears the input and output registers. A point to be noted at this time is that for every one-clock pulse received by the driver, it delivers the pair of pulses advance O and advance E.

The lone bit in the counter register is propagating through the register and uneventfully passes core E_5 because flip-flop M has not been set. Simultaneously, the serial output of the 64-bit register is being fed into one of the inputs of the modulo-two adder. The other input to the adder is being fed from the clear input register. Code ring modulo-two added to zeros yields code ring; therefore, straight code ring is being loaded into the output register.

The bit in the counter register enters core O_6 and triggers the following series of events. AND gate A_6 is inhibited; therefore, the driver receives no clock pulses and the bit in the counter register recirculates from core E_6 to core O_1 and comes to rest in core O_1, by virtue of the delivered pair of pulses from the driver. The punch buffer dumps six bits of code ring into the punch, and the punch cycle is actuated.

An end-of-punch signal reinstates clock to the drivers, and information is moving in all magnetic registers with the exception of the input register which is clear. On the ninth pair of drive pulses, after start, flip-flop M is set.

As the bit in the counter register arrives in core E_5 the following series of events takes place. AND gate A_6 is inhibited, and the driver receives no clock pulses. The reader circuit is actuated, and the reader takes in leader until the first character of message arrives. This character of message is placed into the input register. An end-of-read signal reinstates clock to the driver, and the bit in the counter enters core O_6. The O_6 signal initiates the series of events previously described. At this time, 12 bits of code ring have been placed on the output tape. The logically controlled process of reading in message and punching out encoded tape continues until a stop code is detected by the transmitter. The stop code is encoded, placed on the output tape, and the entire transmitter is reset.

V. Receiver

The receiver is used to decode the message that was encoded by the transmitter. A detailed description of the decoding process will be undertaken with the aid of the logic diagram of Figure 17. Figure 18 is a simplified logic diagram of the receiver. The decoding of a message will be followed chronologically through the device.

The first step in the decoding process is to read the first character (six binary bits) of data on the encoded message tape. As was explained previously, the first two characters of data on the encoded message tape are code ring. The first character (six bits) of code ring is read into a six each one-bit magnetic shift register.* This is a parallel operation; therefore, all six bits of code ring are read into the six one-bit shift registers simultaneously. This first character (six bits) of code ring is also read into a magnetic six-bit data register (nonrecirculating). It was previously noted that the code transmission system uses a 64-bit code ring. This code ring is placed in a 64-bit magnetic shift register (recirculating). The 64-bit magnetic shift register has a six-bit parallel output which feeds into a magnetic comparator register (six-bit magnetic EXCLUSIVE-OR) and also a serial output which feeds into a magnetic modulo-two adder. The magnetic comparator register has 12 inputs and 1 output. Six of the inputs to the magnetic comparator register come from the six each one-bit shift registers, and the other six inputs come from the outputs of the 64-bit magnetic shift register (recirculating).

The decoding of the encoded message does not begin until the magnetic comparator register signals the comparator logic. It was previously noted that the key to decoding a message is to lock onto the code ring at the proper location before performing the modulo-two addition between the code ring and the encoded data. Another important fact that should be noted is that both the transmitter and the receiver contain the same code rings. To lock onto the code

*A six each one-bit shift register is six one-bit recirculating shift registers.

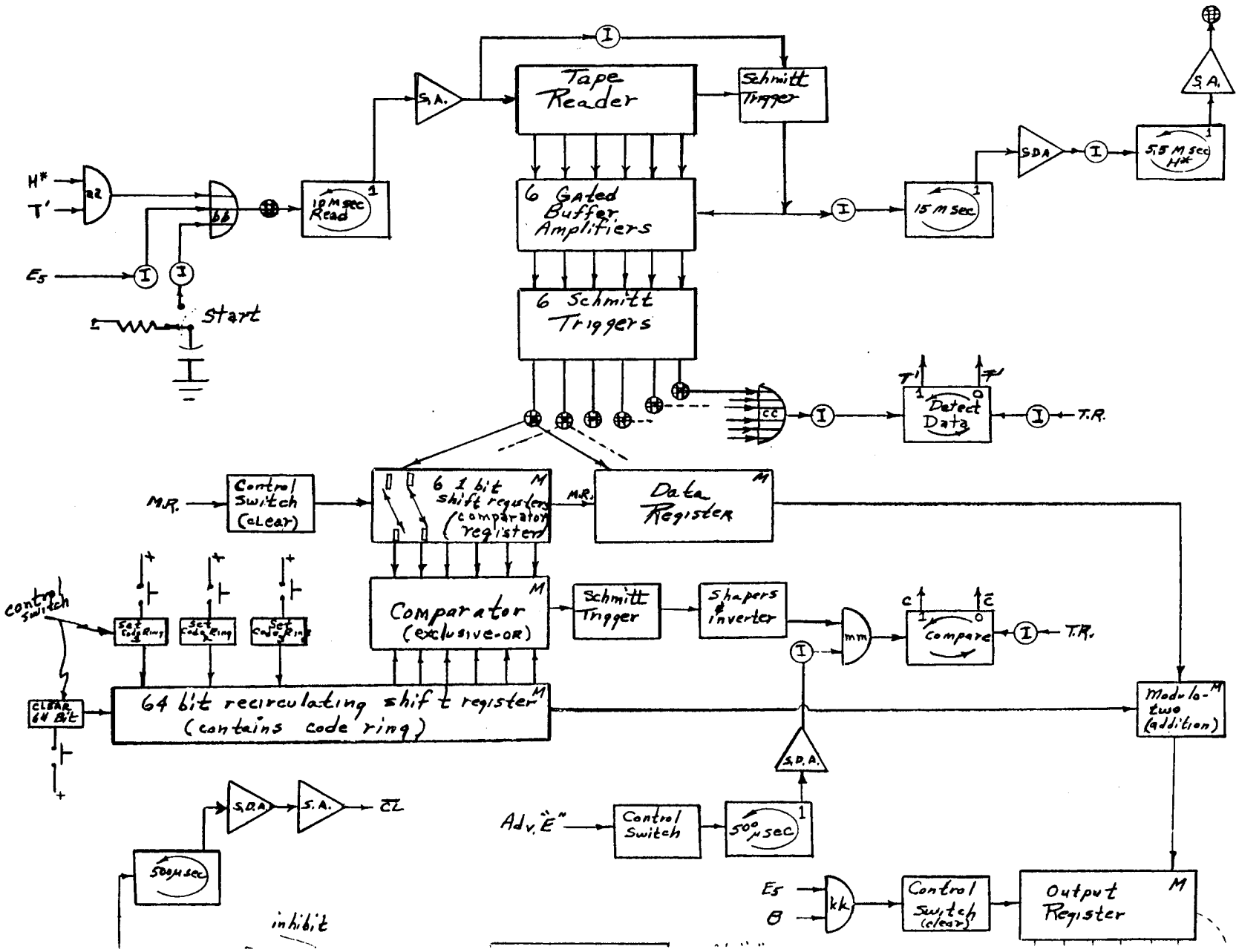

Figure 17. Coded tra

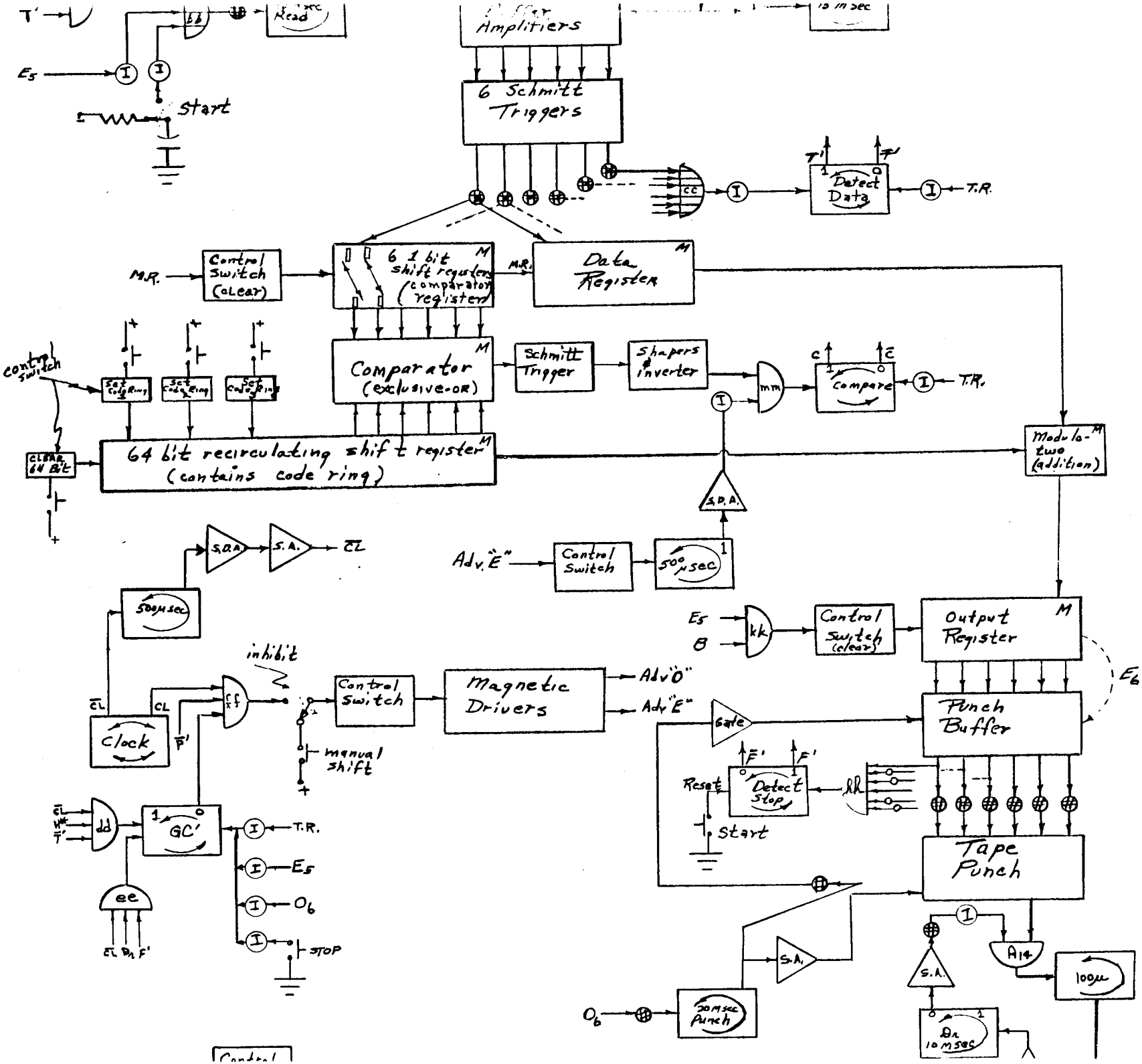

Figure 17. Coded transmission system -- (receiver)

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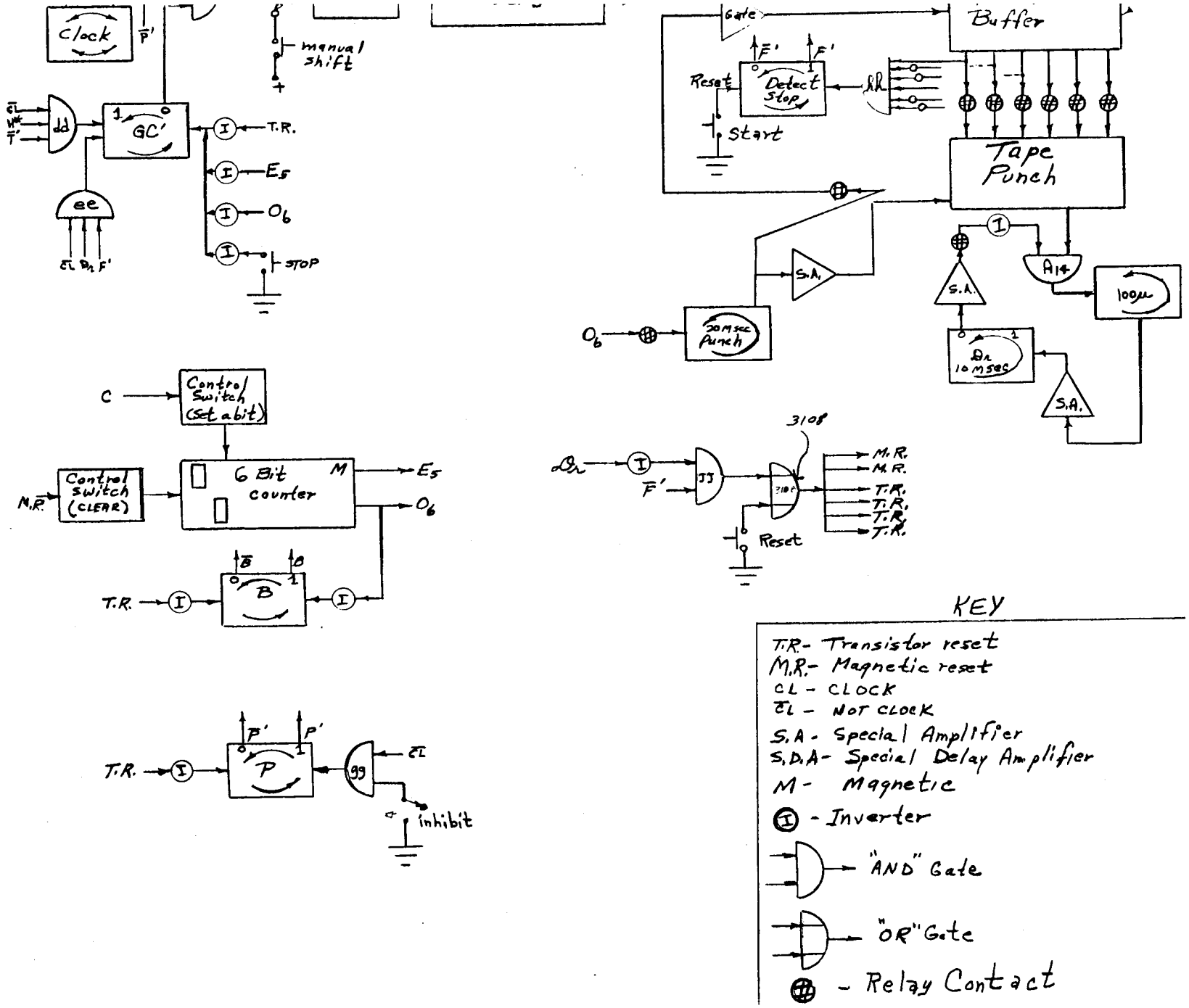

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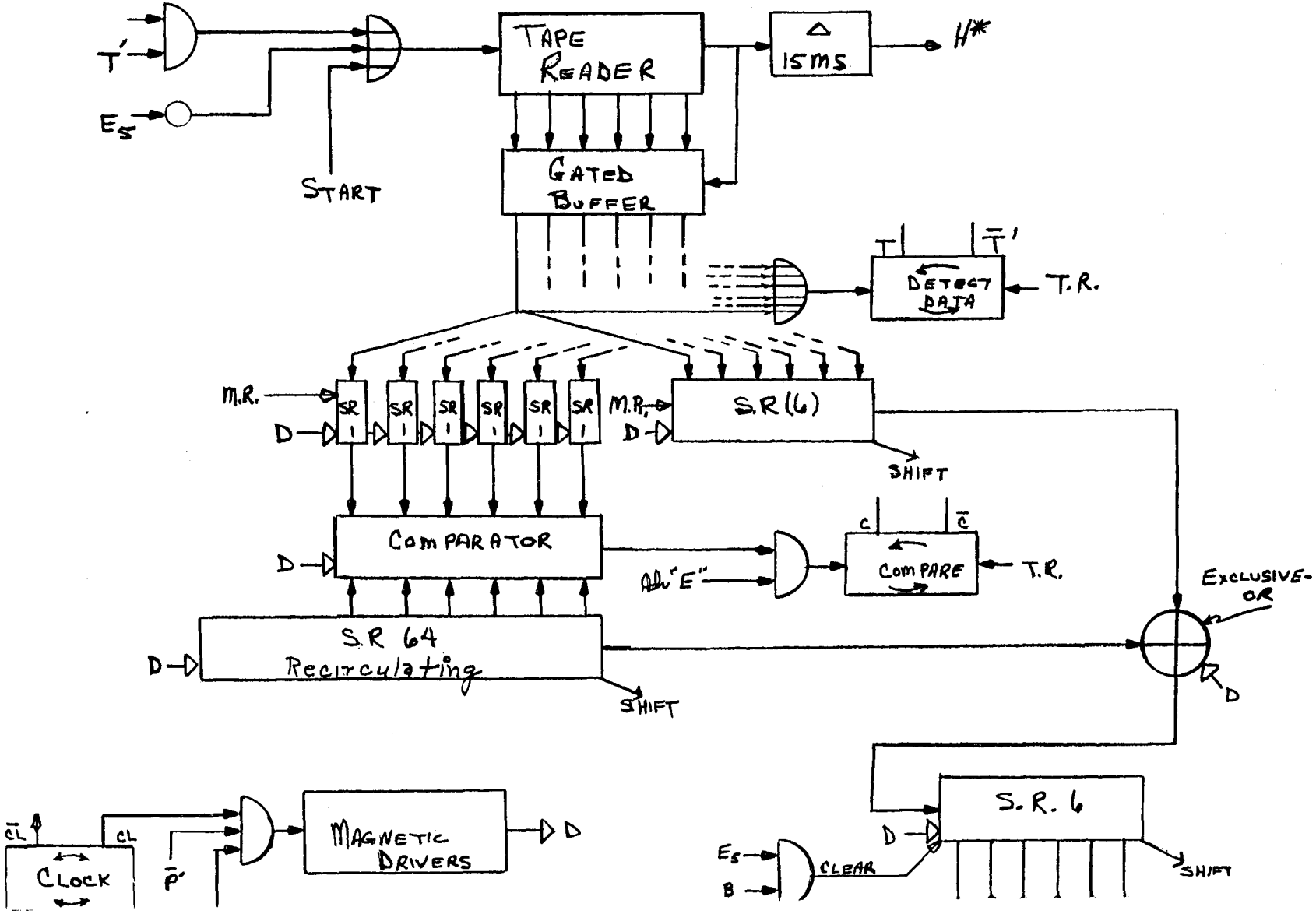


Figure 18. Simplified coded tra

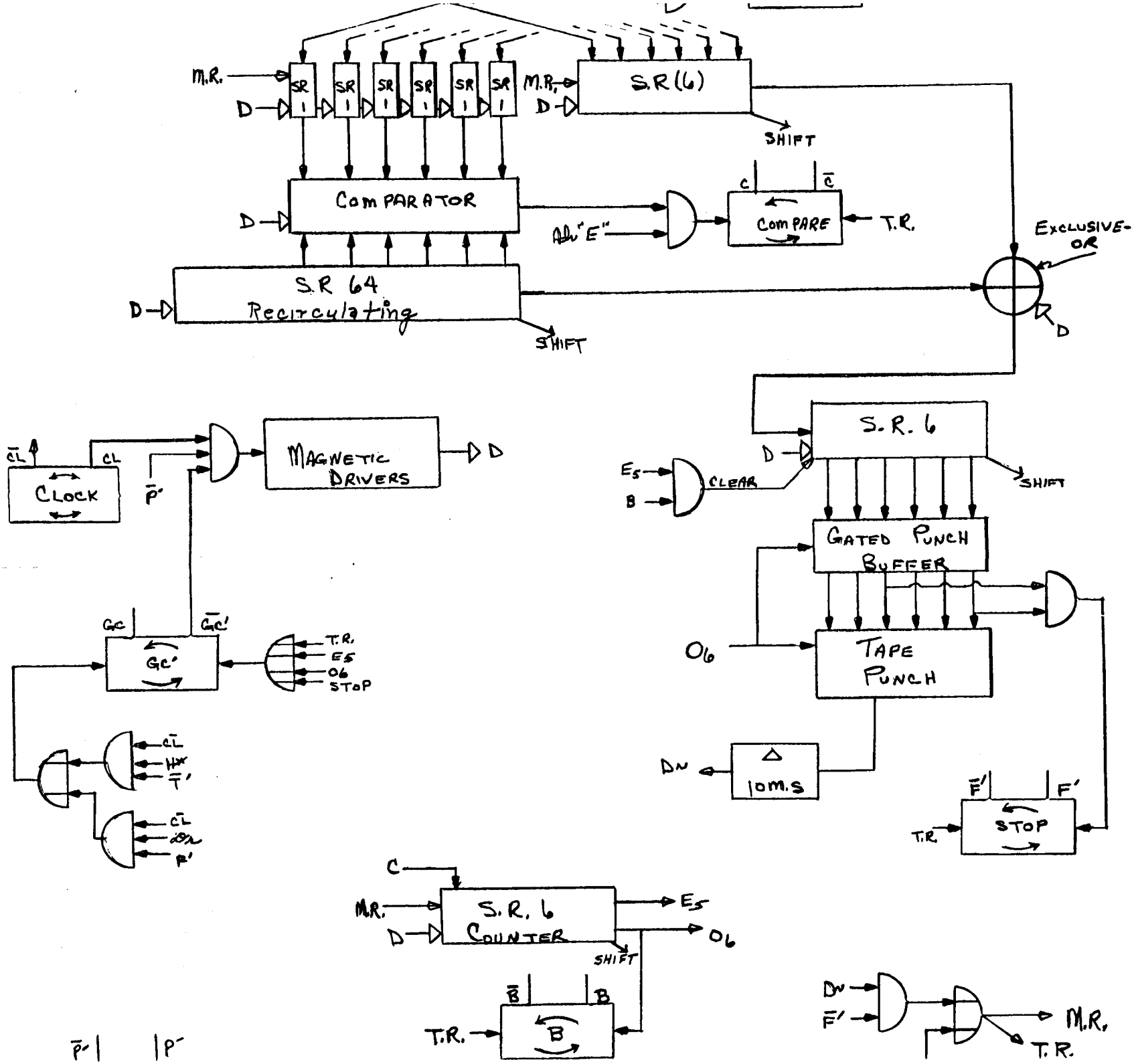
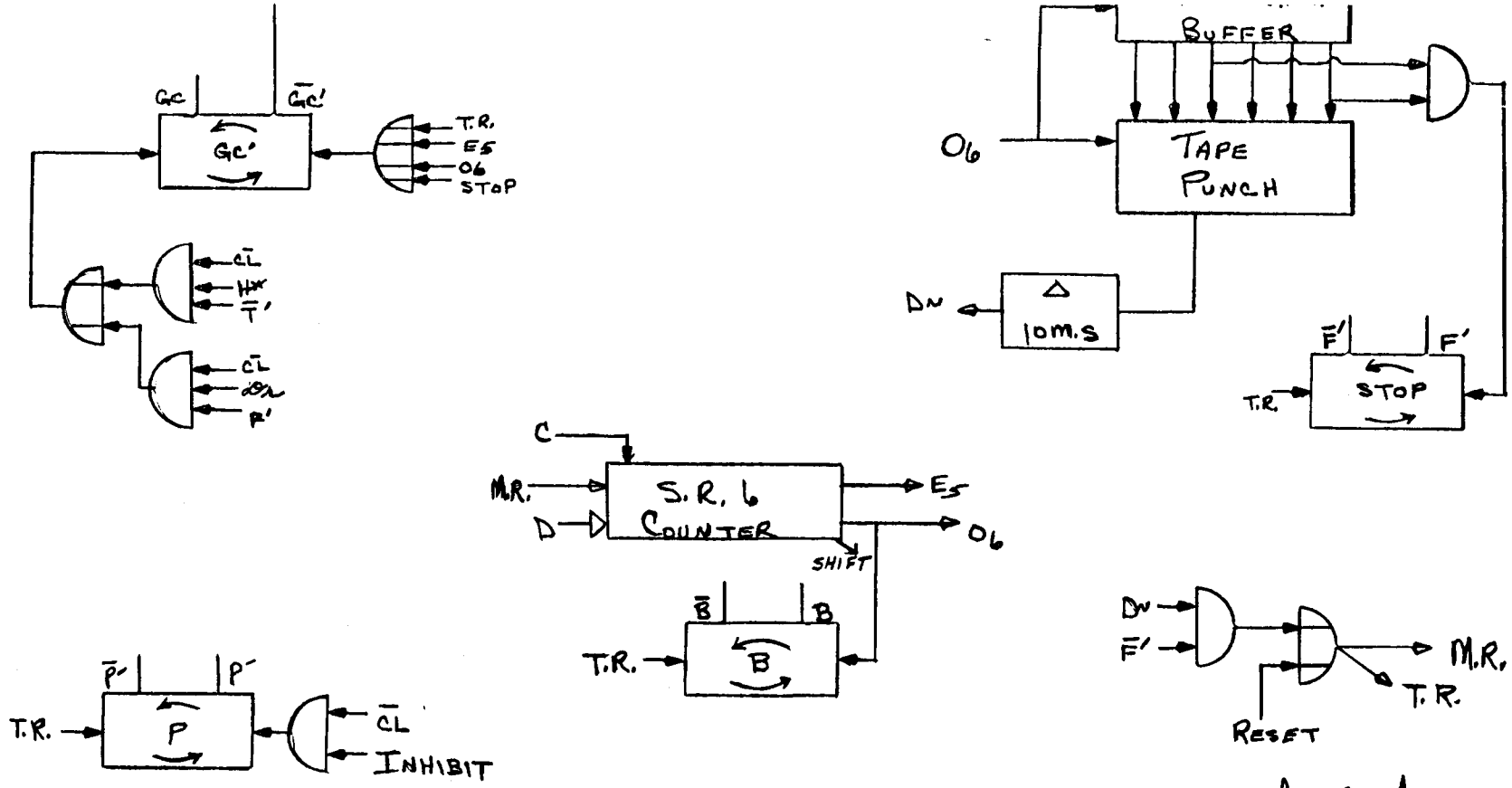


Figure 18. Simplified coded transmission system -- reader

ission system -- reader



M.R.- Magnetic Reset
T.R.- Transistor Reset
D- Drive Adv "O" and "E"

ring at the proper location, the 64-bit shift register is shifted one bit at a time. Each time a shift occurs, the comparator register looks at the six-bit pattern in the six each one-bit shift registers, compares it to the six-bit pattern in the 64-bit shift register, and then produces a single output pulse which is fed into the comparator logic circuitry. The output of the comparator register has a 2.5:1 discrimination ratio between compare and no compare. That is to say, the amplitude of the output pulse during no compare is 2.5 times the amplitude of the output pulse during compare.

A Schmitt trigger is connected directly to the output of the comparator register and is adjusted in such a manner as to give an output for all no-compare signals. The output of the Schmitt trigger is connected to an inverter, and therefore the proper signal occurs only when a comparison takes place. The output from the comparator logic is fed into an AND gate, and a slightly delayed advance E pulse is also fed into the AND gate. An output from the AND gate occurs only when a comparison occurs, and this output sets a flip-flop which in turn sets a bit into a six-bit magnetic counter (recirculating). Five advance E times later, an output pulse occurs from the E_5 core in the six-bit magnetic counter. This E_5 pulse serves to trigger a control switch which in turn dumps a capacitor whose current is fed through the clear windings of the six-bit magnetic output register. At this point, it should be mentioned that the serial input of the output register comes from the output of the modulo-two adder. The modulo-two adder has two serial inputs. One input comes from the serial output of the 64-bit register which contains the code ring, and the other input comes from the serial output of the magnetic data register. It can be seen from the logic diagram of Figure 17 that the output of the modulo-two adder is serially fed into the input of the output register. The pulse from the E_5 core of the six-bit counter serves to clear the output register and prepare it for receiving decoded data from the modulo-two adder.

At O_6 time, a pulse occurs from the O_6 core in the six-bit counter, and this pulse actuates a monostable multivibrator which in turn initiates the punching cycle. It can be seen from the logic diagram of Figure 17 that the E_5 and O_6 pulses perform other functions beside those which have been mentioned.

The receiver uses an asynchronous timing system, as careful study of the logic diagram of Figure 17 will indicate.

VI. Input-Output Equipment

The peripheral equipment of the coded transmission system consists of one Photocircuit Model 100 photoelectric tape reader and one Friden Model M-1095-CA mechanical punch.

The transmitter and receiver perform separate and unique operations, and each subsystem requires its own input-output equipment. Rather than go to the expense of dual readers and punches for the subsystems, switching circuitry was incorporated in the demonstration model which allowed time sharing of the peripheral equipment and eliminated redundancy in the system.

VII. Application

A possible application of the coded transmission system could be the following. Assume that there is an omnidirectional transmitting station and this station desires to send messages to three receiving stations designated Stations A, B, and C. The transmitting station does not necessarily want messages which are sent to Station A to be decoded at Stations B or C. And likewise the same condition holds for messages sent to Station B or Station C. The transmitting station also wants to be able to send decodable messages to any combination of receiving stations, including all stations.

Using the coded transmission system described in this report, the problem is easily solved. Each receiving station can be supplied with a selected set of code rings. The transmitting station will have all the code rings that the individual stations possess. When the transmitting station desires to send a message to Station A alone, it encodes the message with the code ring that Station A possesses. Therefore, although all stations will receive the encoded message, only Station A will be able to decode the message. When

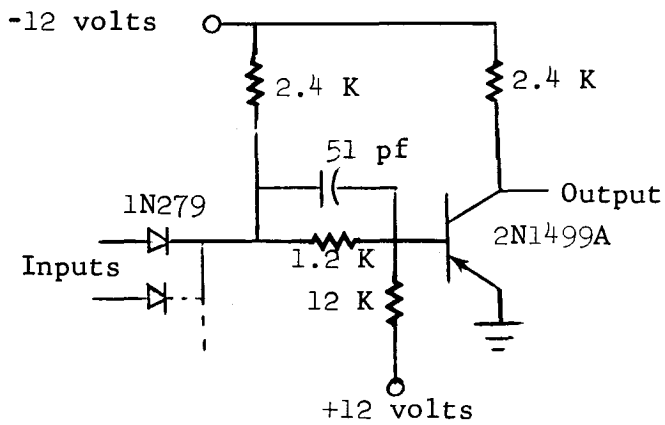
the transmitting station desires to send an all-stations message, it merely encodes the message with a code ring which all receiving stations possess. It can be seen that by utilizing different sets of code rings any desired combination may be obtained.

VIII. Conclusion

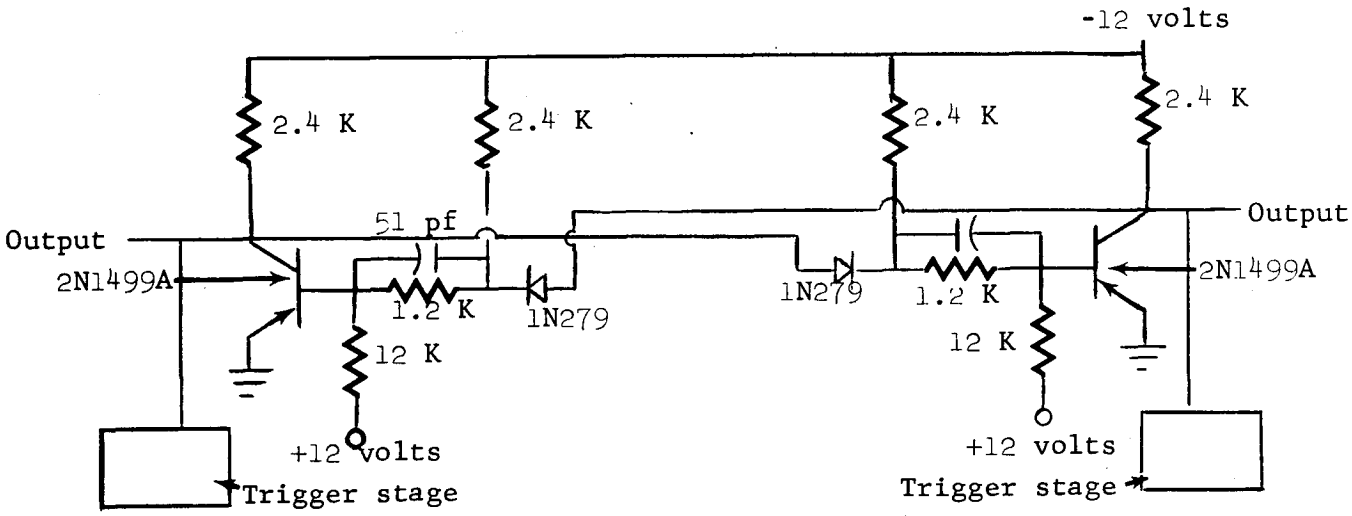
In this report, a method for encoding and subsequent decoding of a message has been presented, and a particular coded transmission system built to demonstrate the coding principle has been described.

APPENDIX

Figure A-1 illustrates the gate and flip-flop circuitry utilized in the coded transmission system.



AE 3101, 2, 3, 5 gate



AE 3104 flip-flop (modified)

Figure A-1. Gate and flip-flop circuitry

The circuitry illustrated in Figure A-1 recognizes -12 volts as logical one and ground as logical zero. With logical one applied to the input of the gate circuit, the input diode is back-biased and decouples the gate circuit from the prior stage. At this point, the voltage divider (2.4 K, 1.2 K, 12 K) establishes a negative potential on the base with respect to the emitter, and the transistor turns on. The output of the stage with a one applied is logical zero.

A logical zero applied to the input forward biases the diode and places a nominal ground at the junction of the 2.4 and 1.2 K resistors. The voltage divider, consisting of the 1.2 and 12 K resistors to +12 volts, establishes a positive potential on the base with respect to the emitter and turns the transistor off. At this time, the output of the stage is a nominal -12 volts.

The flip-flop (AE 3104) is basically two gate circuits DC-coupled, and its operation is the same as previously explained. The stages of the flip-flop are AE 3101 gate circuits with their collector resistors removed. Collector triggering was selected because of its positive-action and noise-rejection characteristics.

The Schmitt trigger circuit utilized in the transmission system is illustrated in Figure A-2.

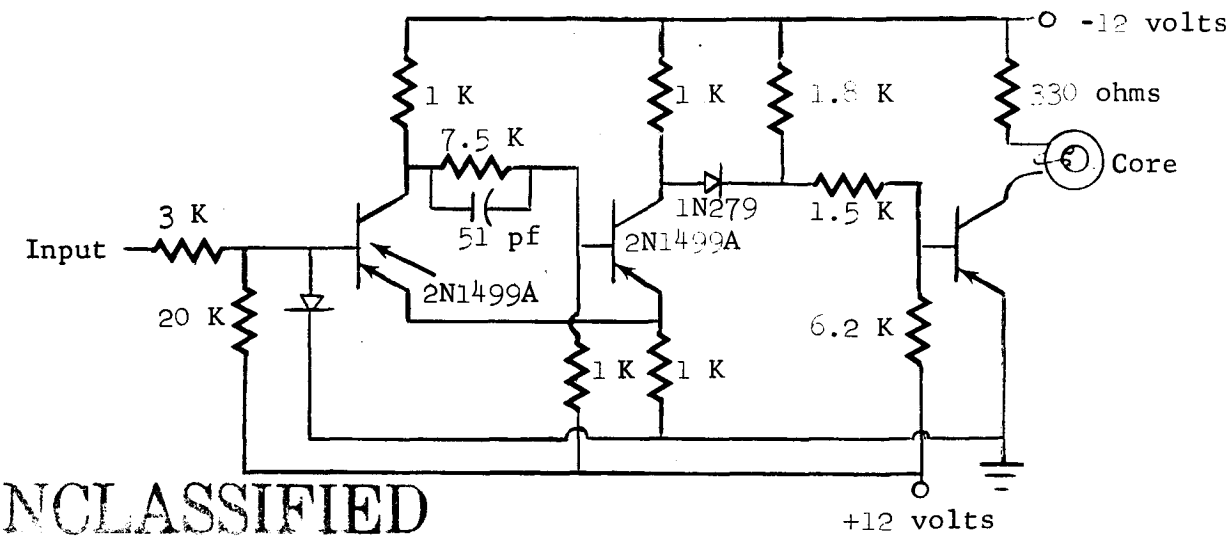


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Figure A-2. AE 3165 Schmitt trigger

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The circuit components have been so selected that the circuit will actuate when a nominal -6 volts is applied to the input. The collector circuit of the output buffer stage has been modified to include a core. When the input voltage exceeds the selected threshold potential, a logical one is placed in the previously mentioned core. By this method, information travels from the reader to the input magnetic shift register. In addition, Schmitt triggers perform threshold detection in the comparator circuit of the receiver and punch output circuits.

The relay-driver circuit (Figure A-3) is used to actuate the solenoids in the mechanical punch. The driver-circuit operation is similar to the gate-circuit operation in that -12 volts input will actuate the relay and a grounded input will keep the transistor off and the relay de-energized.

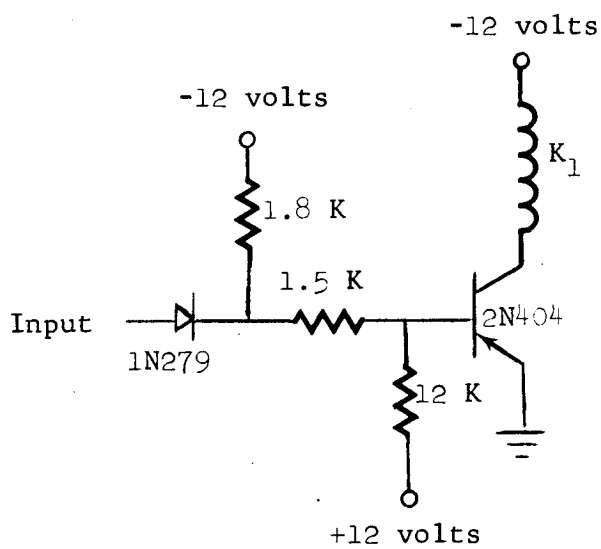

Figure A-3. AE 3112 relay driver

The flip-flop reset circuit is illustrated in Figure A-4. By placing a logical one at the input, the transistor is turned on thereby pulling one side of the flip-flop to ground and causing it to be reset.

Figure A-5 depicts the controlled-switch monostable multivibrator and its delay amplifier and buffer stage as used in the transmission system. The four-element device in the monostable is

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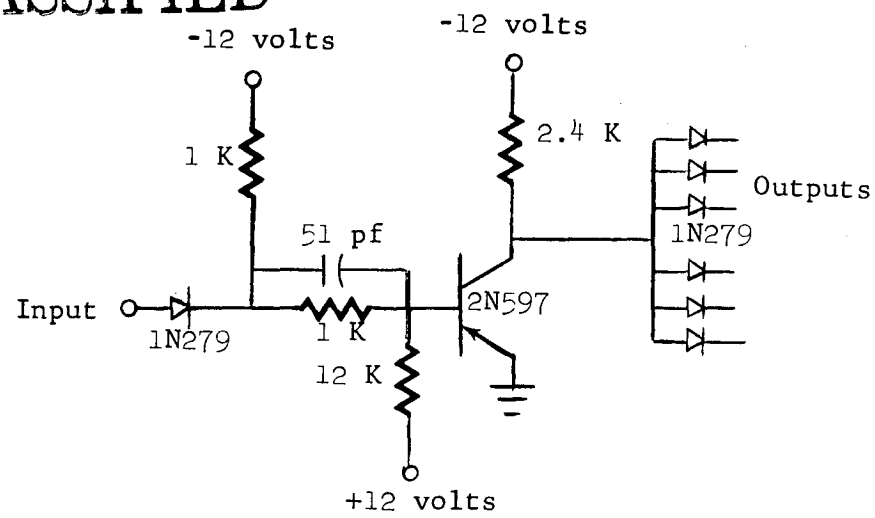
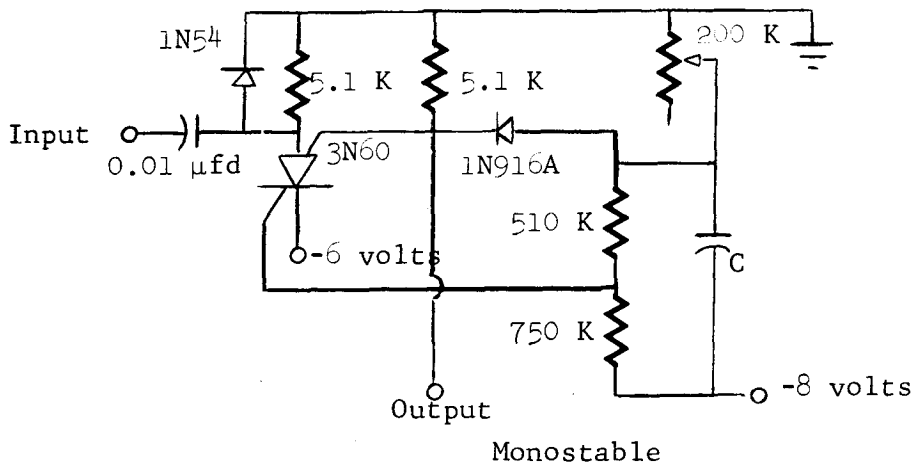


Figure A-4. AE 3108 flip-flop reset



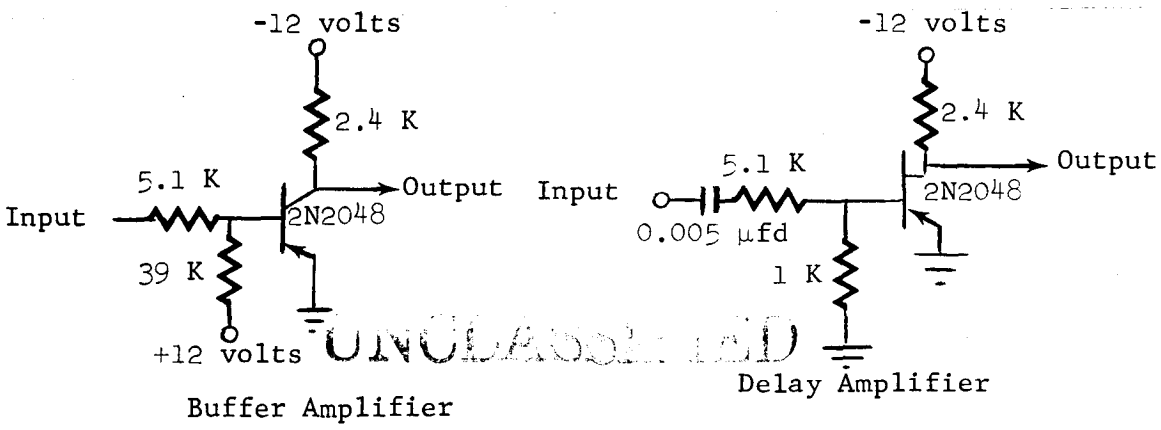


Figure A-5. Controlled-switch monostable and buffer

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a GE 3N60 controlled switch. The prime advantage of this monostable circuit over conventional circuits is its noise-rejecting ability. An internal biasing network keeps the switch on, and therefore noise pulses leave the circuit unaffected. To actuate the monostable action, a negative pulse with a minimum-time duration of 10 microseconds and a minimum amplitude of -5 volts must be applied. This pulse turns off the switch and starts the delay action. The disadvantages of the monostable circuit are its poor temperature characteristics and its special voltage requirements. The special voltages utilized in the monostable circuit were generated from Zener-diode references.

Control rectifiers perform several functions in the transmission system. The rectifiers act as memory elements in buffers (Figure A-6) and as current-switching elements for magnetics (Figure A-7).

Figures A-8 through A-14 illustrate the complete system and component breakdown.

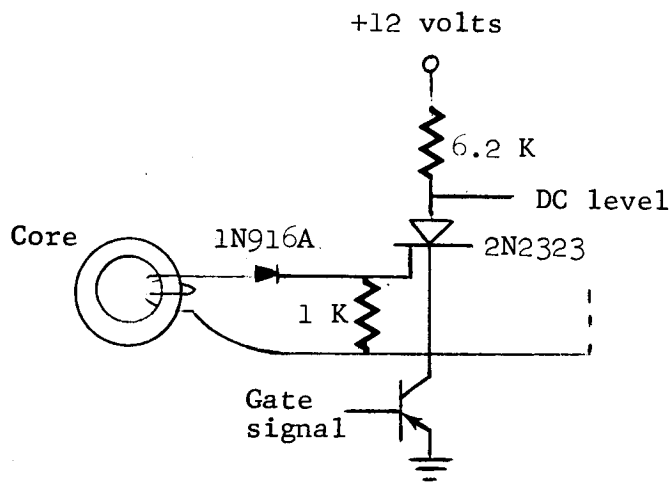

Figure A-6. Buffer storage

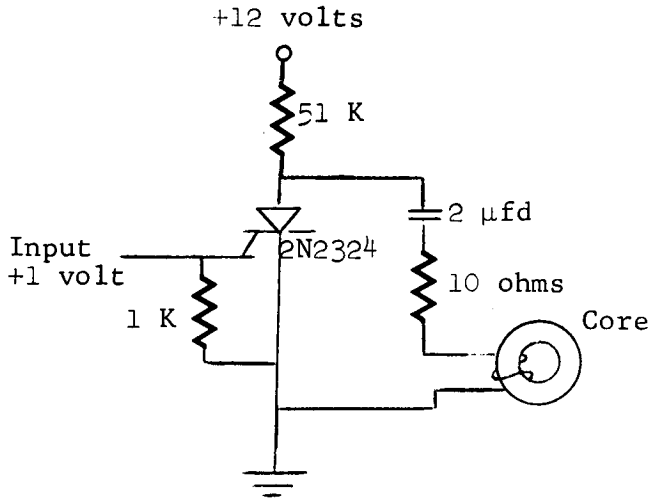

Figure A-7. Current-switching circuit

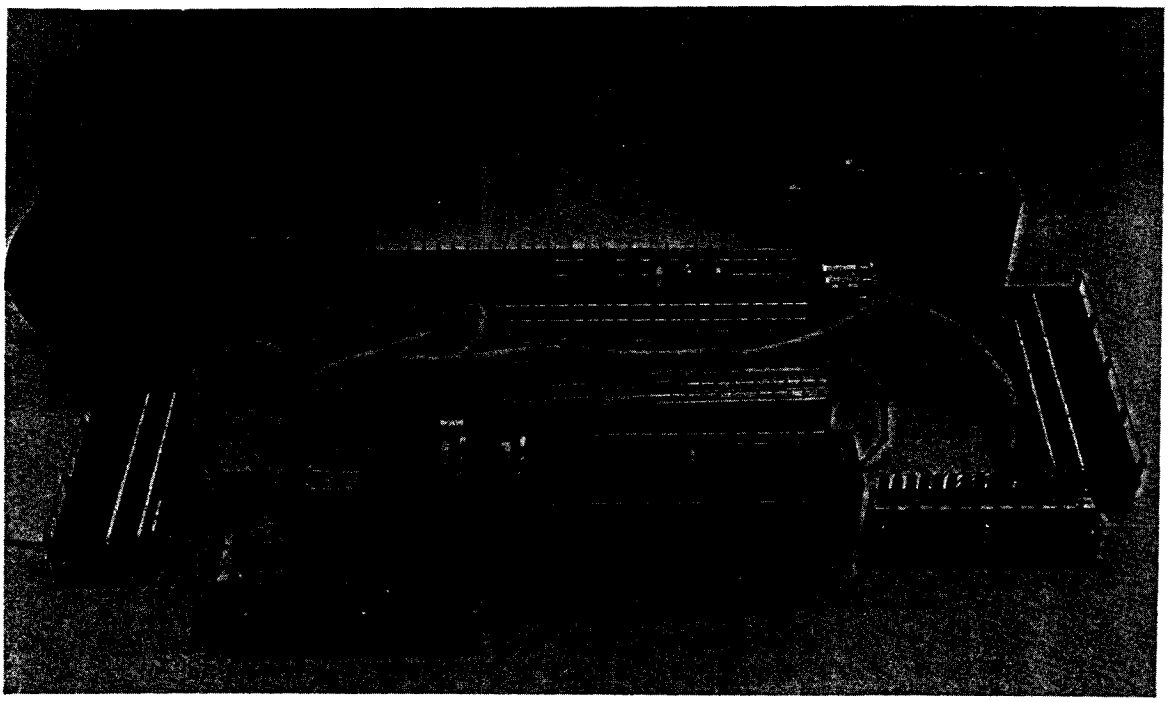

Figure A-8. Complete coded transmission system

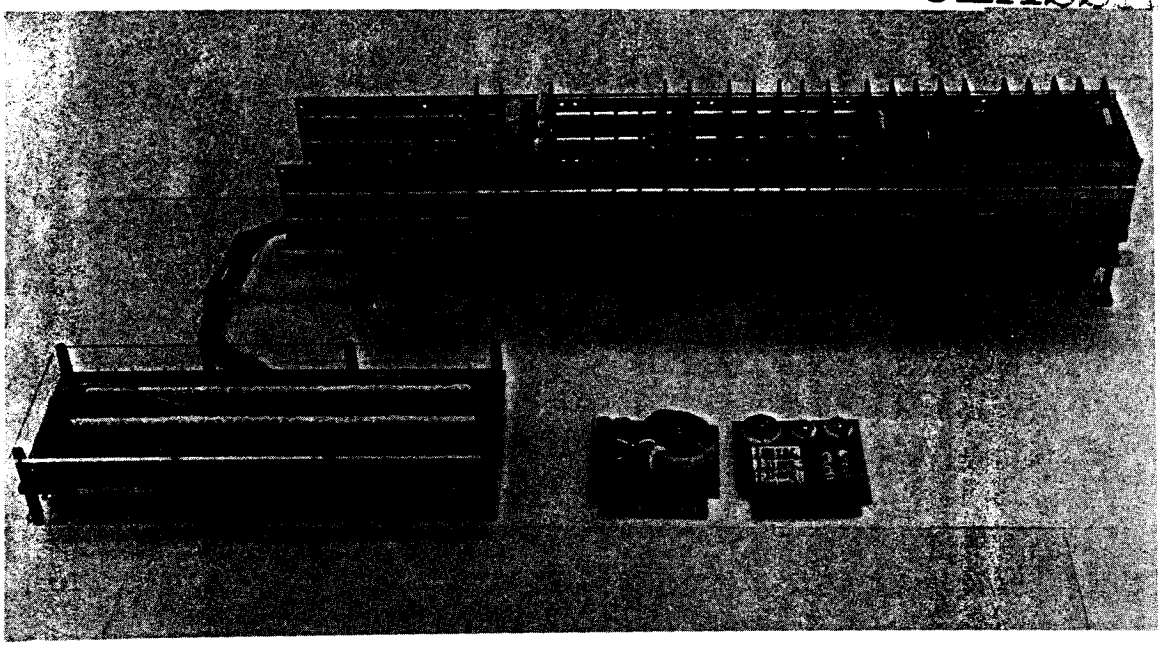

Figure A-9. Transmitter and driver

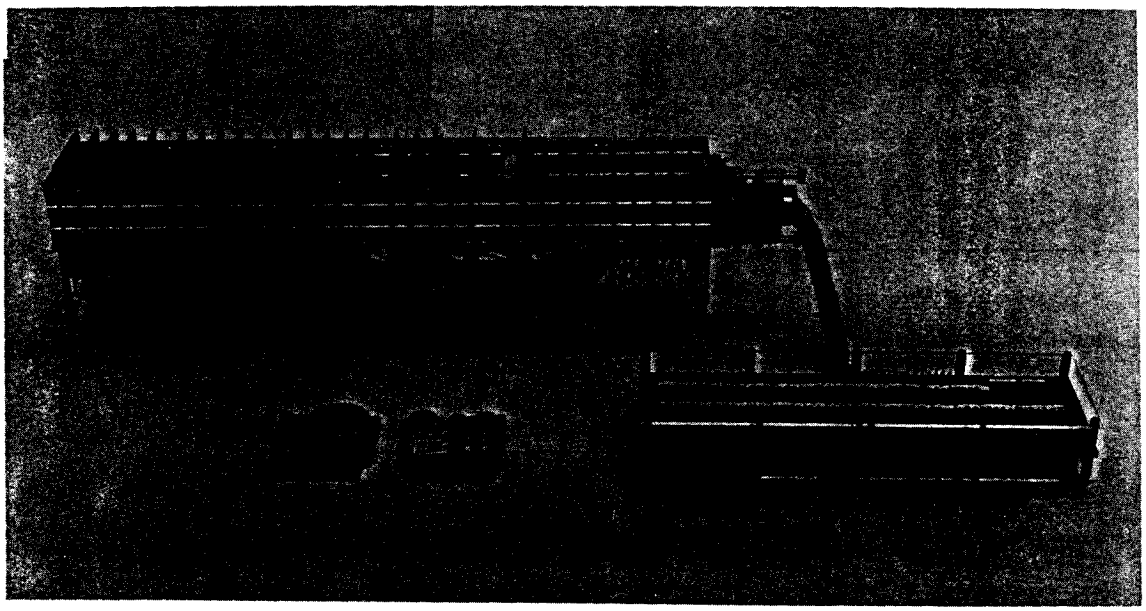

Figure A-10. Receiver and driver

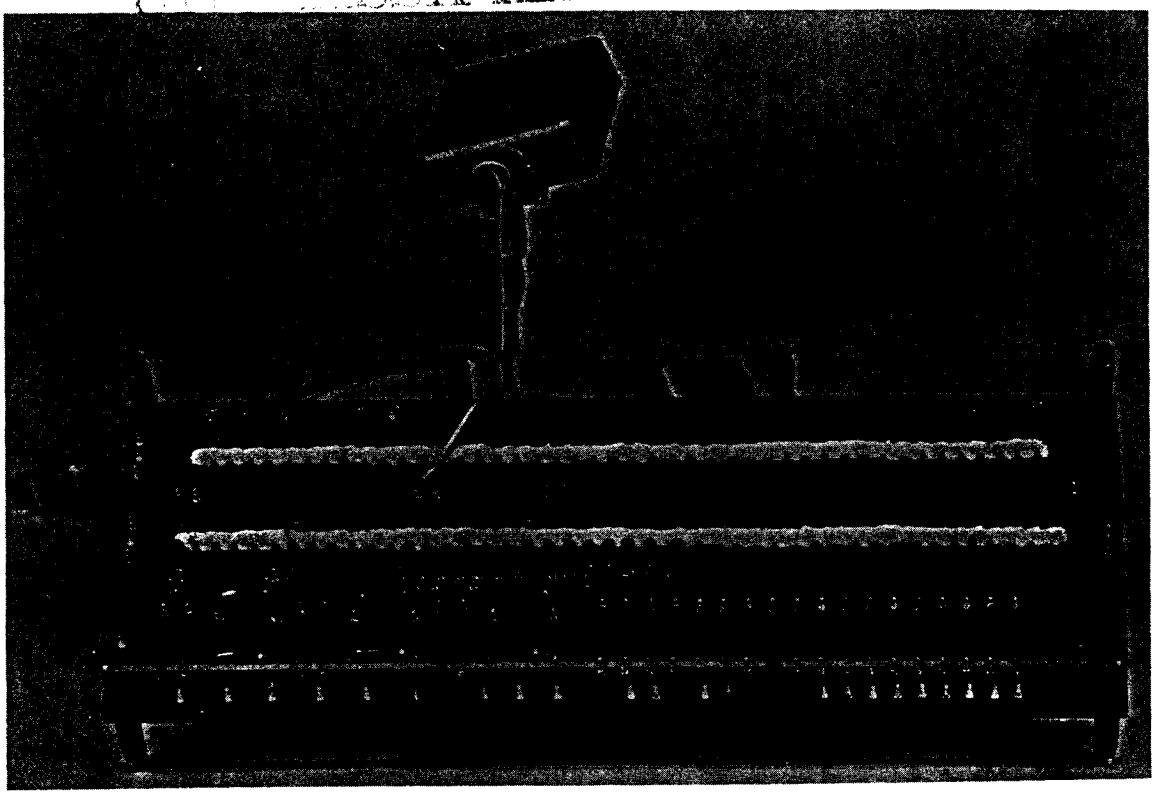

Figure A-11. Transmitter magnetics (top view)

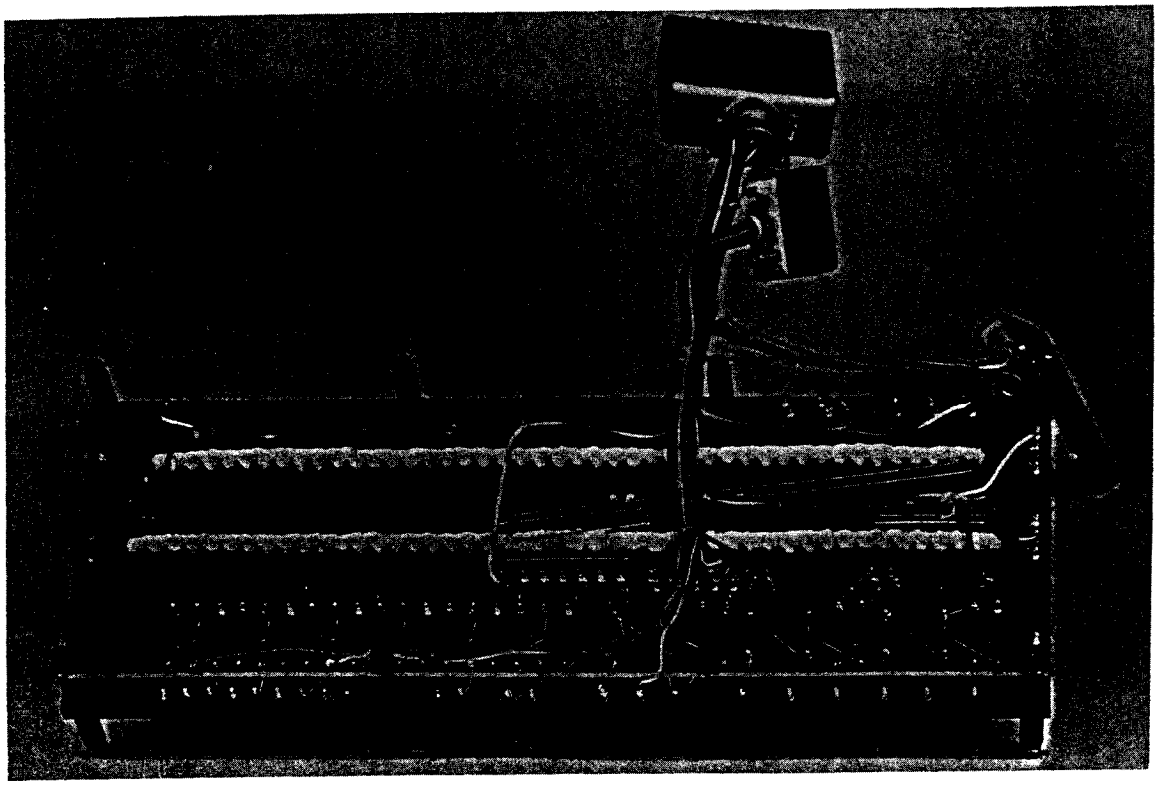

Figure A-12. Transmitter magnetics (bottom view)

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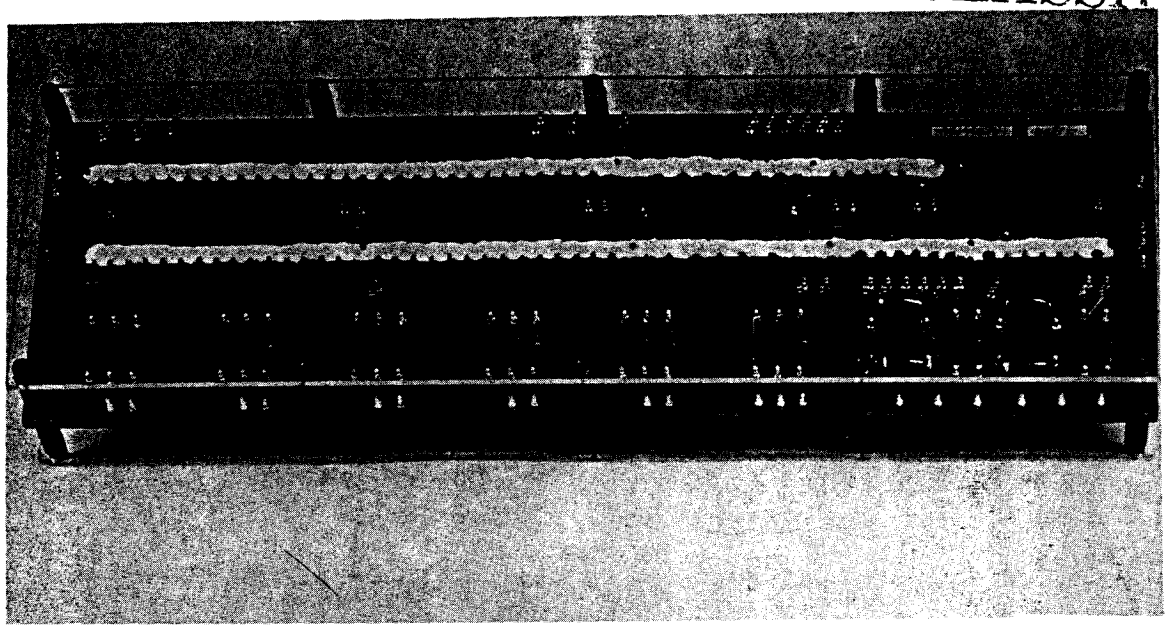

Figure A-13. Receiver magnetics (top view)

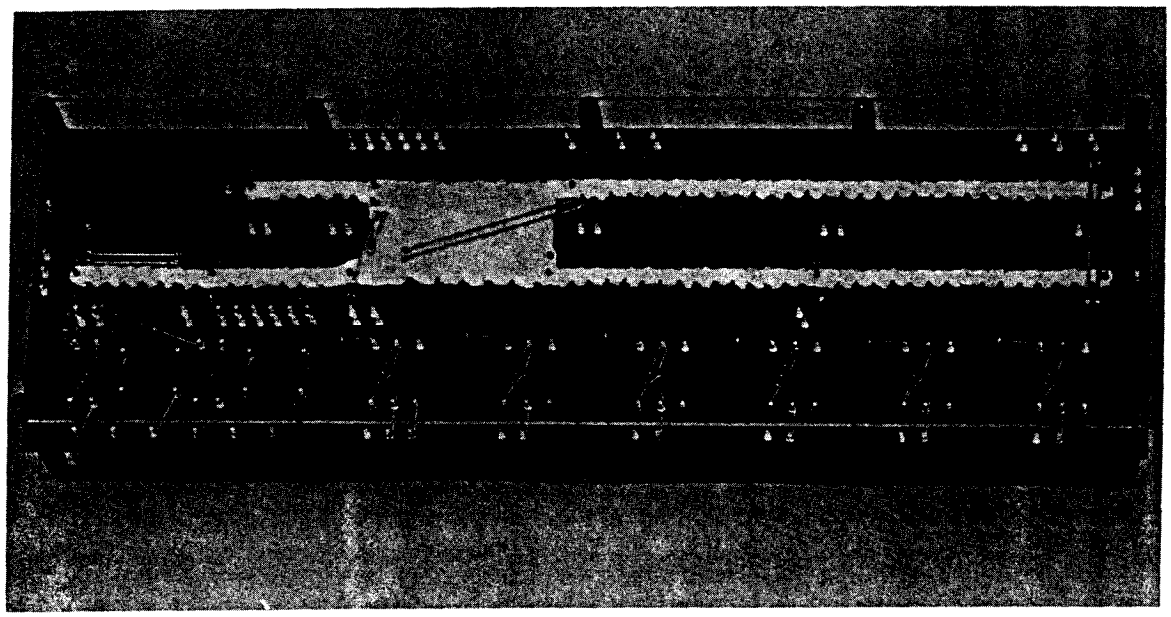

Figure A-14. Receiver magnetics (bottom view)

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