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The Transistor as Low Level Switch

Anders Lydén

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A Lydén

Summary:

The common collector transistor switch has in the on state with open emitter a certain offset voltage $U_{EK} \approx -\frac{kT}{q\,B_N}$. This expression is derived in a new, more physical way. It is further shown at which emitter current the current amplification factor B_N should be measured to get a correct value for the above expression. The collector current I_K at zero collector voltage follows the equation $I_K = I_o\left[\exp\left(\frac{q\,U_E}{kT}\right) - 1\right]$ extremely well. Substitution of I_{EBO} and I_{KBO} by I_o in Eber's and Moll's relations consequently improves these equations and the characteristics of the transistor switch can be better determined. At switching on and off transients appear across the switch. The influence of the "spike" at switching off can be described by an current I_{SPIKE}, which is easy to calculate. I_{SPIKE} is approximately dependent only on the base - emitter depletion layer capacitance and the chopper frequency f_o.

Some compensated switches have lower drift than the drift in U_{EK}. They may, for example, have a temperature drift < 0.2 $\mu V/^{o}C$ and a long time drift <2 μV/week. Some compensated switches also have $I_{SPIKE} < 10^{-12} \cdot f_o$ A. The static offset current in the off state can easily be made $< 10^{-12}$ A.

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1. Introduction

In chopper amplifiers and commutators there is a need for elements which can switch small signals. The transistor is useful for this purpose.

The theory of the transistor as a low level switch has been imperfect. A more complete theory is presented in this paper. Several compensated low level switches have earlier been described. Only those which give the switch better characteristics will be analyzed here.

Bright [1, 3] and Kruper [2, 3] showed the suitability of the transistor as a low level switch and found that the offset voltage U_{EK} in the on state is smallest in the inverted or common collector connection shown in fig. 2.1. Chaplin [4] pointed out that it is possible to get sufficiently high off resistance with the drive voltage zero in the off state. This reduces the offset current to a high degree. In this paper it will be shown that the low level transistor switch can be described by an equivalent circuit as shown in fig. 2.2. Here

S = ideal switch controlled by the drive voltage
U_{EK} = the offset voltage in the on state
R_S = the on resistance
I = the offset current in the off state
R_o = the off resistance
I_{SPIKE} = this current describes the influence of the discharge of the base-emitter capacitance at switching off.

2. Physical derivation of the offset voltage

Several authors have by means of Eber's and Moll's relations [5] derived the following expression for the offset voltage U_{EK} in the inverted connection:

$$U_{EK} \approx -\frac{1}{\Omega B_N} \quad \text{for pnp} \tag{2.1}$$

and

$$U_{EK} \approx \frac{1}{\Omega B_N} \quad \text{for npn} \tag{2.2}$$

where

$$\Omega = \frac{q}{kT}$$

q = magnitude of electron charge
k = Boltzmann constant
T = absolute temperature
B_N = large signal current gain in common emitter connection

This derivation has two serious lacks. Firstly it affords no physical understanding of why the offset voltage becomes so small and seems to depend only on B_N. Secondly it does not tell at which emitter current B_N should be measured in order to get a correct value for (2.1) or (2.2).

Eq. (2.1) will in the sequel be derived in a more directly physical way, which gives a better understanding of the offset voltage.

Assume we have a pnp transistor. Positive currents and voltages are defined in fig. 2.1. A positive voltage U_K is suddenly impressed between the collector and the base. The emitter is open. This reduces the electrostatic potential in the pn-junction and the excess hole density p_{BK} in the base at the edge of the depletion layer at the collector junction increases.

$$p_{BK} = P_o \left(e^{\Omega U_K} - 1\right) \tag{2.3}$$

where

P_o = the equilibrium hole density in the uniform n-type base.

For the excess hole density in the base at the emitter side p_{BE} a similar expression holds:

$$p_{BE} = P_o \left(e^{\Omega U_E} - 1\right) \tag{2.4}$$

At the outset $U_E = 0$ and $p_{BE} = 0$. This gives a very heavy gradient in the excess hole density as shown in fig. 2.3, and a large hole diffusion current flows from the collector to the emitter. This current charges the emitter and U_E and p_{BE} will be > 0, since the emitter is open. As soon as U_E becomes > 0 there will be an electron current from the base to the emitter. Equilibrium occurs when this electron current equals the hole current from the collector, because then the total current to the emitter is zero (Curve a, fig. 2.3). Now if we want $U_E - U_K$ to be small, we see from (2.3) and (2.4) that we shall have $p_{BK} - p_{BE}$ small. This means that the hole current from the collector to the emitter shall be as small as possible, but also that the electron current from the base to the emitter shall be as small as possible.

An expression for U_{EK} can now be obtained by simple reasoning. Say that we make $U_K = 0$, but do not change U_E. This does not change the base - emitter electron current, because this current is dependent only on U_E and not on U_K. The base - collector electron current on the other hand changes and becomes 0. Curve b in fig. 2.3. shows the excess hole distribution in the base. A hole diffusion current flows from the emitter to the collector. This current is B_N times as large (by definition of B_N) as the base - emitter electron current, i.e. B_N times as large as the hole current we earlier had from the collector to the emitter when $I_E = 0$. We can describe this by the following expression:

$$\frac{p_{BK} - p_{BE}}{p_{BE}} = \frac{1}{B_N} \qquad 2.5$$

Provided that the linear diffusion equation holds.

Eq. (2.3), (2.4) and (2.5) gives:

$$\frac{p_{BE}}{p_{BK}} = A_N = \frac{e^{\Omega U_E} - 1}{e^{\Omega U_K} - 1} \approx e^{\Omega(U_E - U_K)} = e^{\Omega U_{EK}}$$

$$U_{EK} \approx \frac{1}{\Omega} \cdot \ln A_N \qquad 2.6$$

Expanding (2.6) in series gives for larger B_N:

$$U_{EK} \approx - \frac{1}{\Omega B_N} \qquad 2.7$$

The hole density in the base P_o was above assumed to be the same everywhere in the base. In a drift transistor this is not the case. In the latter the base is doped much more heavily at the emitter junction than at the collector junction. Appendix A shows that even in this case the base - emitter electron current should be as small as possible in order to get a small offset voltage.

Determination of the I_E at which B_N should be measured

B_N is not a constant and therefore we must determine how it should be measured. The determination above of U_{EK} shows directly that B_N should be measured at $U_K = 0$ and U_E unchanged at the value it acquired with $I_E = 0$ and U_K at a given value. Now as a rule we do not know this U_E, but we know the base current I_B which brings the transistor into the on state. The question to answer is therefore: At which I_E should we measure B_N, when I_B is known, to get a correct value for the equation $U_{EK} = -\frac{1}{\Omega B_N}$?

To answer this question we shall use the double-diode equivalent circuit shown in fig. 2.4. This means that the total excess hole density distribution is obtained by superposing two excess hole density distributions shown by curves b and c in fig. 2.4. These distributions cause diffusion currents to flow, and $A_N I_N$ reaches the collector and $A_I I_I$ reaches the emitter. Now, if there is negligible "built in" field in the base, $I_K (U_E, O) = I_E (O, U_K)$ when $U_E = U_K$, as shown by Ebers and Moll [5], and we can write:

$$A_N I_N = - I_o (e^{\Omega U_E} - 1) \qquad 2.8$$

$$A_I I_I = - I_o (e^{\Omega U_K} - 1) \qquad 2.9$$

Fig. 2.4. gives:

$$I_E = I_N - A_I I_I \qquad 2.10$$

$$I_K = I_I - A_N I_N \qquad 2.11$$

Assuming $I_E = 0$ gives:

$$I_N = A_I I_I \qquad 2.12$$

$$I_K = - I_B \qquad 2.13$$

and

$$I_N = - \frac{A_I}{1 - A_N A_I} \, I_B \qquad 2.14$$

If we now make $U_K = 0$ but do not change U_E we see from (2. 8) that $A_N I_N$ does not change, nor I_N either if we assume that A_N is dependent only on U_E but not on U_K · $I_I = 0$ because $U_K = 0$. The emitter current I_E becomes:

$$I_E' = - \frac{A_I}{1 - A_N A_I} \, I_B \qquad 2.15$$

Normally this equation can be written approximately:

$$I_E' \approx - B_I I_B \qquad 2.16$$

Eq. (2. 16) tells us at which emitter current B_N should be measured when I_B is known. Since B_I is included in (2. 16) we must determine at which collector current B_I should be measured. Then we must instead make $U_E = 0$ but keep U_K unchanged. This gives $I_N = 0$ and the collector current I_K' becomes:

$$I_K' = - \frac{1}{1 - A_N A_I} \, I_B \qquad 2.17$$

Normally this equation can be written approximately:

$$I_K' \approx - (1 + B_I) \, I_B \qquad 2.18$$

Eq. (2. 18) tells us at which collector current B_I should be measured. The equation contains the quantity to be measured and therefore a trial calculation is necessary.

3. Modification of Ebers's and Moll's relations

For further calculations we need equations describing the DC signal behaviour of the transistor. Ebers's and Moll's relations contain four constants which vary with the working point, namely I_{KBO}, I_{EBO}, A_N and A_I. However, it will be shown in this section that the relations can be modified to include only two variable constants, namely A_N and A_I.

Sah et al. [6] have explained why A_N and A_I vary. Part of the current in a silicon pn junction is due to generation and recombination of carriers in centers in the space charge region. In a forward bias junction this space charge recombination current I_{rg} has a voltage dependence which is:

$$I_{rg} \cdot \text{constant} = e^{\frac{\Omega U}{m}} - 1 \qquad 3.1$$

where $1 \leq m \leq 2$ (m varies with U).

While the voltage dependence of the hole diffusion current I_d and the electron diffusion current I_d' through the junction is

$$I_d \cdot \text{constant} = I_d' \cdot \text{constant} = e^{\Omega U} - 1 \qquad 3.2$$

A_N can be written

$$A_N = \vartheta_N \cdot \gamma_n \qquad 3.3$$

where

ϑ_N = the forward transport efficiency

γ_N = the emitter efficiency

γ_N can be calculated from the following expression:

$$\gamma_N = \frac{I_d \coth \frac{W_B}{L_B}}{I_d \coth \frac{W_B}{L_B} + I_d' + I_{rg}} \qquad 3.4$$

where I_d and I_d' are the injected currents into the base and the emitter region, respectively, when these regions are thought to extend toward infinity. The base is thin, however, and the collector functions as a diffusion sink and increases the diffusion current component to $I_d'' = I_d \cdot \coth \frac{W_B}{L_B}$. W_B is the base layer width and L_B the minority carrier diffusion length in the base. At small forward bias $I_d' << I_{rg}$ and 3.3 can be written:

$$A_N = \vartheta_N \frac{\frac{I_d''}{I_{rg}}}{1 + \frac{I_d''}{I_{rg}}}$$

If we assume $\vartheta_N = 1$ we get:

$$B_N = \frac{I_d''}{I_{rg}} \qquad 3.5$$

Eq. (3.1), (3.2) and (3.5) give:

$$B_N \cdot \text{constant} = \frac{e^{\Omega U}}{e^{\frac{U}{m}}} = e^{\Omega U (1 - \frac{1}{m})}$$

$$B_N = \text{constant} \cdot I_d''^{(1 - \frac{1}{m})}$$

But $I_d'' = I_k$ because $\vartheta_N = 1$

This gives:

$$B_N = \text{constant} \cdot I_k^a \qquad 3.6$$

where $a = 1 - \frac{1}{m}$ $\qquad 0 \leq a \leq 0.5$

Alloy and Mesa silicon transistors have at small forward bias $I_{rg} >> I_d''$. Sah [7] has pointed out that for these transistors the space charge recombination is mainly localized to the surface. This gives low B_N at low I_E. Planar and planar epitaxial silicon transistors have oxide-protected pn junctions and therefore much lower I_{rg} which gives fairly high B_N at low I_E. This is illustrated by diagrams 3.1 and 3.2 which show I_E and $I_K = f\ (U_E)$ at $U_K = 0$ for the alloy silicon transistor 2N1676 and the planar silicon transistor 2N1613. $I_K = \vartheta_N \cdot I_d''$ and $I_E = I_d'' + I_d' + I_{rg}$. At $U_E = 430$ mV in diagram 3.1 $A_N \approx 0.5$, that is $I_{rg} \approx I_d''$ since $\vartheta_N \approx 1$. When $U_E < 430$ mV, I_{rg} is largest and proportional to $\exp\left(\frac{\Omega U_E}{m}\right)$ where $m \approx 1,7$. 2N1613 has a much lower space charge recombination and already at $U_E = 200$ mV $A_N \approx 0.5$. In this case $m \approx 1.3$.

I_K is proportional to $\exp\ (\Omega\ U_E)$ both for 2N1676 and 2N1613. Sah [7] has pointed out that this relation holds very well. The slope of the curve is exactly given by Ω. This means that (2.8), (2.9) holds very well. All types of transistor give this result. At negative U_E, I_o also is a constant. I_o and Ω are consequently constants which do not vary with U_E and U_K. It is evidently desirable to modify Ebers's and Moll's relations to include I_o. These relations can be written in explicit form (pnp):

$$I_E = -\frac{I_{EBO}}{1 - A_N A_I}\left(e^{\Omega U_E} - 1\right) + \frac{A_I\ I_{KBO}}{1 - A_N A_I}\left(e^{\Omega U_K} - 1\right) \qquad 3.7$$

$$I_K = \frac{A_N\ I_{EBO}}{1 - A_N A_I}\left(e^{\Omega U_E} - 1\right) - \frac{I_{KBO}}{1 - A_N A_I}\left(e^{\Omega U_K} - 1\right) \qquad 3.8$$

$$A_N\ I_{EBO} = A_I\ I_{KBO} \qquad 3.9$$

When $U_K = 0$, I_K becomes:

$$I_K = \frac{A_N \, I_{EBO}}{1 - A_N A_I} \left(e^{\Omega U_E} - 1\right) \qquad 3.10$$

Eq. (2.8) and (2.11) give:

$$I_K = I_o \left(e^{\Omega U_E} - 1\right) \qquad 3.11$$

Eq. (3.10) and (3.11) give:

$$I_o = \frac{A_N}{1 - A_N A_I} \; I_{EBO} \qquad 3.12$$

$U_E = 0$ gives correspondingly:

$$I_o = \frac{A_I}{1 - A_N A_I} \cdot I_{KBO} \qquad 3.13$$

Eq. (3.7) and (3.8) can be written:

$$\frac{I_E}{I_o} = - \frac{1}{A_N} \left(e^{\Omega U_E} - 1\right) + e^{\Omega U_K} - 1 \qquad 3.14$$

$$\frac{I_K}{I_o} = e^{\Omega U_E} - 1 - \frac{1}{A_I} \left(e^{\Omega U_K} - 1\right) \qquad 3.15$$

In (3.14) and (3.15) A_N and A_I are the only constants which vary with I_E and I_K.

Also at negative U_E and U_K the generation of carriers from the centers in the space charge region has a great influence. In silicon transistors most of I_{EBO} and I_{KBO} is due to this generation. The generation current is proportional to the width of the transition region. This width is voltage-dependent and therefore I_{EBO} and I_{KBO} will vary also at negative U_E and U_K respectively. A_N at $U_E \leq 0$ and A_I at $U_K \leq 0$ is normally ≤ 0.1 for silicon transistors. This means that

$$I_{EBO} \approx \frac{I_o}{A_N} \quad \text{when } U_E \leq 0$$

$$I_{KBO} \approx \frac{I_o}{A_I} \quad \text{when } U_K \leq 0$$

These equations show how directly I_{EBO} and I_{KBO} depend on A_N and A_I respectively.

Sah [7] has shown that I_o can be calculated from the following expression:

$$I_o = A_E \, q \, n_i^2 \, \frac{D_B}{N_B \, W_B}$$

where A_E = the emitter area

n_i = density of electron or hole in an intrisic specimen

D_B = the diffusion constant for minority carriers in the base

N_B = the density of doping impurities in the base

W_B = the base layer width

This expression shows that I_o depends on quantities which have fairly little spread, particularly for diffused transistors. The spread in I_o is therefore little and much less than that in I_{EBO} and I_{KBO}.

4. The static characteristics of the low level switch

In this section the static characteristics of the switch will be determined by means of Ebers's and Moll's modified relations (3.14) (3.15). Formulas for the quantities in the equivalent circuit of fig. 2.2 will be given.

Determination of the offset voltage and the on resistance

Assume the transistor is in the inverted connection as shown by fig. 2.1. In the on state U_E and U_K are $\gg \frac{1}{\Omega}$. Eq. (3.14) and (3.15) can in this case be written approximately:

$$\frac{I_E}{I_o} = -\frac{1}{A_N} e^{\Omega U_E} + e^{\Omega U_K}$$

$$\frac{I_K}{I_o} = e^{\Omega U_E} - \frac{1}{A_I} e^{\Omega U_K}$$

These equations give

$$\Omega(U_E - U_K) = \ln A_N \frac{I_K + \frac{1}{A_I} \cdot I_E}{I_K + A_N I_E} \qquad 4.1$$

and

$$U_E - U_K = \frac{1}{\Omega} \ln A_N + \frac{1}{\Omega} \ln \frac{1 - \frac{I_E}{I_B} \cdot \frac{1}{B_I}}{1 + \frac{I_E}{I_B} \cdot \frac{1}{1 + B_N}}$$

$I_E = 0$ gives

$$(U_E - U_K)_{I_E = 0} = U_{EK} = \frac{1}{\Omega} \ln A_N \qquad 4.2$$

When $I_E \ll I_B$ we get by expansion of (4.2):

$$U_E - U_K = U_{EK} - \frac{I_E}{\Omega\, I_B} \left(\frac{1}{B_I} + \frac{1}{1 + B_N} \right)$$

This can be written:

$$U_E - U_K \approx U_{EK} + R_S \cdot I_E \qquad 4.3$$

where R_S is the on resistance.

$$R_S = \frac{1}{\Omega\, |I_B|} \left(\frac{1}{B_I} + \frac{1}{1 + B_N} \right) \qquad 4.4$$

Eq. (4.3) is in accordance with the equivalent circuit given in fig. 2.2. In (4.4) B_N and B_I should be measured at I_E and I_K given by (2.16) and (2.18) respectively.

Experimental measurements

Several measurements were made to test the above formulas for the offset voltage U_{EK} and the on resistance R_S. The offset voltage of seventeen OC 44 was measured at $U_K = 0.15$ V. B_N was measured at $U_E = 0.15$ V and $U_K = 0$, in accordance with the conclusions in section 2. In diagram 4.1 the different values of U_{EK} are plotted against the respective values of $\frac{1}{B_N}$. A mean straight line is drawn through the points. The inclination of the line is in perfect agreement with the theoretical value $\frac{1}{\Omega}$ = 25.6 mV given by (2.7).

U_{EK} was also measured as a function of I_B for some different types of transistors. These measurements are presented in diagrams 4.2 and 4.3. B_N and B_I for these transistors were measured, respectively, at U_K and $U_E = 0$, and at different values of I_E and I_K. See diagrams 4.4 and 4.5. By means of these diagrams and (2.6), (2.15) and (2.17), $U_{EK} = f(I_B)$ was determined. These calculated curves are plotted for comparison in diagrams 4.2 and 4.3. There is good agreement except for higher values of I_B. U_{EK} increases strongly with decreasing I_B for the alloy transistors OC 202 and 2N 1676 on account of the rapid fall off of B_N and B_I at low I_E and I_K respectively. These decreases are much less for the planar transistors 2N 1613 and 2N 2432 and therefore U_{EK} in these cases does not increase so much at decreasing I_B.

Calculated and measured values of R_S are presented in diagrams 4.6 and 4.7. The agreement is good. The relative deviation is approximately constant. It is probably due to space charge layer widening, which causes B_I to be a little higher at $U_E = 0$ than at $U_E > 0$. For 2N 1676 the difference is so great that it has displaced the calculated U_{EK} to the left. This is because too high values of B_I have been used in the calculation of U_{EK}.

The offset voltage at larger I_B

When $I_B > 0.1$ - I mA the measured value of U_{EK} becomes greater than the calculated value. This is partly due to the collector bulk resistance r_c which gives a contribution to U_{EK} which is $= r_c \cdot I_B$. Therefore r_c ought to be small. Furthermore B_I ought to be > 1. High frequency diffused transistors very often have very low B_I due to carrier lifetime reduction in the base (0.01 at 1 mA for example). This gives indirectly a rather high U_{EK}, since (2.16) shows that - if I_B is of normal magnitude - B_N should be measured at a very low I_E, which gives rather low B_N. If I_B is increased to get a higher B_N the voltage $r_c\ I_B$ will not be negligible.

There are other causes of the deviation. For example when p_{BE} is not $\ll N_B$, the linear diffusion equation is not valid; hence (2.5) is not valid, nor consequently (2.6) either. Webster [8] has shown that when $p_{BE} \approx N_B$ and $p_{BK} = 0$ a field is created in the base which helps the holes to flow towards the collector. This gives a rise in B_N which is not present when $p_{BK} \approx p_{BE} \approx N_B$. The measured B_N will be too high and (2.7) will give too low values of U_{EK}.

The variation in U_{EK} --

In a chopper amplifier the drift is mainly due to the variation of U_{EK}. Variations which are caused by fluctuations of the temperature can be determined by differentiation of (2. 7).

$$\frac{d\,U_{EK}}{d\,T} = U_{EK}\left[\frac{1}{T} - \frac{1}{B_N} \cdot \frac{d\,B_N}{d\,T}\right] \qquad 4.5$$

$d\,B_N$ must be determined with a certain change in I'_E. This we get by differentiation of (2. 16).

$$d\,I'_E = -\,I_B \cdot d\,B_I$$

$d\,B_I$ must be determined with a certain change in I'_K. This we get by differentiation of (2. 18).

$$d\,I'_K = I_B \cdot d\,B_I$$

This equation contains the quantity to be measured and a trial calculation is necessary. For 2N 1613, 2N 2432 and 2N 1676, $\frac{d\,B_N}{B_N dT} \approx 5 \cdot 10^{-3}/^{o}K$ at $I_E = 1$ mA according to data sheets. This gives:

$$\frac{d\,U_{EK}}{d\,T} \approx -\,U_{EK} \cdot 2 \cdot 10^{-3}\,V/^{o}K \qquad 4.6$$

Sometimes it is possible to find an I_B which gives $\frac{d\,U_{EK}}{d\,T} = 0$. As a rule this I_B is so high that (2. 7) is not valid.

Even if the temperature is constant there will be a drift in U_{EK} due to the variation of B_N with time. This variation seems to be less for transistors with getter in the case than for transistors with silicon grease-filled cases [11]. Planar transistors probably have better long time stability of B_N than other types of transistors. For example 2N 1613 [12] seems to have $\frac{d\,B_N}{B_N} < 2\,\%$ during 3000 hours.

Determination of the offset current and the off resistance

In the off state the transistor is equal to an off resistance R_o in parallel with a current generator I (the leakage current) as shown in fig. 2.2.

Normally a transistor is brought into the off state by large reverse bias on the junctions. When the signal to be switched is small (< 0.3 V), this is not necessary. Silicon transistors have sufficiently large R_o even when the reverse voltage is 0. This gives no offset current and the smallest possible spike at switching off and on.

The offset current at large reverse voltage

The circuit assumed is shown in fig. 4.1. Here $U_K = -E$, $E \gg \frac{1}{\Omega}$ and $R_L \; |I_E| \ll |U_K|$. (3.14) gives:

$$\frac{I_E}{I_o} = \frac{1}{A_N} - 1 = \frac{1}{B_N}$$

$$I_E = -I = \frac{I_o}{B_N} \qquad 4.7$$

The offset current at small reverse voltage

A typical circuit for this case is shown in fig. 4.2. Here $|U_K| \ll \frac{1}{\Omega}$ and $|U_K - U_E| \ll |U_K|$.

Expansion of (3. 14) gives:

$$\frac{I_E}{I_o} = -\frac{1}{A_N} \cdot \Omega U_E + \Omega U_K = -\Omega U_K \cdot \frac{1}{B_N}$$

$$I_E = - I = -\Omega U_K \cdot \frac{I_o}{B_N} \qquad 4.8$$

The leakage current I is hence reduced by the factor $|\Omega U_K|$. If, for example, the leakage current of D_1 is 10^{-9} A and $R_1 = 25\,K\Omega$ we get $|\Omega U_K| = 10^{-3}$.

The off resistance

This is lowest when the reverse voltage is 0. Here $|U_K|$ and $|U_E| \ll \frac{1}{\Omega}$. (3. 14), (3. 15) and fig. 4. 2 give:

$$\frac{I_E}{I_o} = -\frac{1}{A_N} \cdot \Omega U_E + \Omega U_K \qquad 4.9$$

$$\frac{I_K}{I_o} = \Omega U_E - \frac{1}{A_I} \Omega U_K$$

$$R_1 \cdot I_B = U_K$$

These equations give:

$$R_o = \frac{U_E - U_K}{I_E} = \frac{1}{\Omega |I_o|} \cdot \frac{1 + B_N\left(\frac{1}{R_1 \Omega |I_o|} + \frac{1}{B_I}\right)}{1 + \frac{B_N}{A_N}\left(\frac{1}{R_1 \Omega |I_o|} + \frac{1}{B_I}\right)}$$

As a rule $B_N\left(\frac{1}{R_1 \Omega |I_o|} + \frac{1}{B_I}\right) \gg 1$, which gives:

$$R_o = \frac{A_N}{\Omega \left| I_o \right|} \qquad 4.10$$

This result is given directly by (4.9) if we assume $U_K = 0$.

Measurements

Table 4.1 shows some measured values of I at the reverse voltage = - 1 V for some different transistors. The product $\left| R_L \; I \right|$ shows that only 2N 1613 is suitable for switching off in this way when $R_L \geq 100$ KΩ.

Table 4.1. Leakage current at large reverse voltage

No	2N 1613	2N 1676	OC 44
Type	Planar silicon	Alloy silicon	Alloy germanium
I A	$-2 \cdot 10^{-12}$	$6 \cdot 10^{-10}$	10^{-7}
$R_L I$ µV $R_L = 100$ kΩ	-0.2	60	10000

Table 4.2 shows some calculated and measured values of R_o for the same transistors as in table 4.1. B_N and I_o for 2N 1676 and 2N 1613 were estimated from diagrams 3.1 and 3.2 (at U_E = 30 mV). B_N and I_o for OC 44 were directly measured.

Table 4.2. Measured and calculated values of R_o

No	2N 1613	2N 1676	OC 44
I_o A	$6 \cdot 10^{-14}$	$-1.2 \cdot 10^{-13}$	-10^{-6}
B_N	0.15	$1.5 \cdot 10^{-3}$	10
R_o calculated	63 kMΩ	310 MΩ	25 kΩ
R_o measured	50 kMΩ	330 MΩ	25 kΩ

5. The behaviour of the switch at switching on and off

The shape of the spikes

Fig. 5.1 shows the circuit assumed and the voltage response U over R_L. The spikes are mainly due to the base-emitter depletion-layer capacitance C_{TE}. (Silicon alloy transistors have high U_{EK} at low I_B. This gives a contribution to the spikes. However, these spikes are very short if the drive voltage has a good square form.) If R_B is very small the amplitude of the spike U_1 at switching off becomes:

$$U_1 \approx \frac{C_{TE}}{C_{TE} + C_L} \cdot U_E$$

The spike then decreases with a time constant τ_1 which is:

$$\tau_1 \approx R_L \left(C_{TE} + C_L\right)$$

If R_B is not small, the amplitude and the time constant also depend on the base-collector depletion-layer capacitance C_{TK} and R_B/R_L. Generally the spike becomes lower but broader. The spike at switching on is very short, especially if f_α is high. Diagram 5.1 shows the shape of the spikes for 2N 1613 with different values of R_B and R_L. The diagram shows that the spike at switching on is almost independent of R_L.

However, an analysis of the shape of the spikes is as a rule of minor interest. In most applications it is, instead, the area of the spikes which is of interest. This can be easily calculated by examining how the different charges in the transistor are supplied and removed.

Calculation of the area of the spikes

Switching off

The switch is assumed to be in the on state. In the base there is an excess hole charge Q_B. Further the charge Q_C of C_{TE} is:

$$Q_C = U_E \cdot C_{TE} \tag{5.1}$$

At switching off the holes begin to diffuse out of the base. During the first part of the process the pn junctions are low resistive, and the currents are mainly determined by outer resistances. Q_B passes mainly out through the collector junction. A negligibly small part of Q_B passes through the emitter junction because R_L makes this a high resistive path. C_{TE} discharges mainly through the emitter junction. This is illustrated in diagram 5.2 where u_E and u for 2N 2432 are shown as function of time at switching off. When time $t \leq 3\ \mu$ s, u_E decreases approximately linearly with time from 630 mV to about 500 mV. The excess hole density in the base hence decreases about 2 decades during this time, and therefore when $t = 3\ \mu$s only a very small part of Q_B is left in the base. How this little part discharges is of no importance. Further, for $t \leq 3\ \mu$s, $u \approx 0$, i.e. the current through $R_L \approx 0$. C_{TE} on the other hand at $t = 3\ \mu$s, has most of its charge left. When $t > 3\ \mu$s the junctions are high resistive and C_{TE} discharges mainly through $R_L + R_B$. This is also shown in diagram 5.2.

Now to simplify the problem we may imagine that, when the base - emitter resistance $R_{EB} < R_B + R_L$, C_{TE} discharges entirely through R_{EB} and, when $R_{EB} > R_L + R_B$, C_{TE} discharges entirely through $R_L + R_B$. $R_{EB} = R_L + R_B$ occurs at a certain emitter voltage U_E' and the charge Q which passes through R_L is consequently approximately given by:

$$Q \approx U_E' \cdot C_{TE} \tag{5.2}$$

In appendix B it is shown that when $\frac{1}{\Omega I_K} < R_B$:

$$R_{EB} \approx \frac{1}{\Omega I_K A_I} \tag{5.3}$$

and when $\frac{1}{\Omega I_K} > R_B$:

$$R_{EB} \approx \frac{1}{\Omega\, I_K} \left(\frac{1}{B_I} + \frac{1}{1 + B_N} \right) \qquad 5.4$$

Eq. (5.4) is the same expression as that for R_S. R_{EB} will vary with I_K as shown by fig. 5.2.

The only thing we want to know is when $R_{EB} = R_B + R_L$ and for the sake of simplicity we may imagine that (5.4) holds for all values of R_{EB}. This means that we consider R_{EB} to be linearly dependent on $\frac{1}{I_K}$. In appendix C eq. (8) shows that:

$$I_K = \text{constant}\ e^{\Omega U_E}$$

Hence

$$R_{EB} = \text{constant}\ e^{-\Omega U_E}$$

To change R_{EB} from R_S to $R_B + R_L$ there must be a change in U_E which is:

$$\Delta U_E = \frac{1}{\Omega} \ln \frac{R_B + R_L}{R_S} \qquad 5.5$$

This gives U_E':

$$U_E' = U_E - \frac{1}{\Omega} \ln \frac{R_B + R_L}{R_S} \qquad 5.6$$

In a chopper amplifier Q will cause a current which has the same effect as the offset current I. Therefore it is convenient to define a spike current at switching off, I_{SPIKE} (fig. 2.2):

$$I_{SPIKE} = \frac{Q}{\frac{T}{2}} = 2\, f_o \cdot Q \qquad 5.7$$

where $f_o = \frac{1}{T}$ = the chopper frequency

Hence

$$I_{SPIKE} \approx 2 f_o \cdot C_{TE} \cdot U_E' \qquad 5.8$$

I_{SPIKE} flows through R_L and causes a voltage U_{SPOFF}.

$$U_{SPOFF} = R_L \cdot I_{SPIKE} \qquad 5.9$$

U_{SPOFF} and U_{EK} have different signs. However, in a chopper-amplifier they appear in different phases and therefore they causes voltages of the same sign at the output of the amplifier.

Switching on

The voltage spike at switching on has an area ϕ_{SPON} which as a rule is much smaller than the area of the spike at switching off. ϕ_{SPON} depends on both f_α and C_{TE} but is almost independent of R_L. It is therefore approximately equivalent to a certain increase in U_{EK}. High C_{TE} and low f_α give high ϕ_{SPON}. It is convenient to define a voltage U_{SPON} which is:

$$U_{SPON} = 2 f_o \cdot \phi_{SPON}$$

As a rule $U_{SPON} << U_{EK}$ for $f_o \leq 1$ kc/s.

Measurements

The theory above contains several approximations. Some different measurements were made to check the theory. The circuit employed is shown in fig. 5.3. U_{EK} (at I_B = 0.15 mA) was measured with S in position 1. In position 2 a voltage U_M was measured which is:

$$U_M = \frac{U_{EK}}{2} + \frac{U_{SPOFF}}{2} + \frac{U_{SPON}}{2}$$

U_{EK} and U_{SPON} are negative and U_{SPOFF} positive with pnp transistors. If U_{SPON} is assumed to be negligible we get:

$$U_{SPOFF} = 2\ U_M - U_{EK} \qquad 5.10$$

Measurement No. 1

A capacitance C was connected between the base and the emitter of a 2N 2432. R_L was 100 kΩ. U_M was measured and U_{SPOFF} calculated from (5.10). Diagram 5.3 shows $U_{SPOFF} = f\ (C)$. The curve is a straight line, which is in accordance with (5.8). The curve cuts the C-axis approximately at - 2.5 pF, which gives $C_{TE} \approx 2.5$ pF.

Measurement No. 2

U_{SPOFF} was measured for some transistors with and without a C connected. R_L was 100 kΩ. Eq. (5.8) and (5.9) give:

$$\frac{\Delta U_{SPOFF}}{U_{SPOFF}} = \frac{C}{C_{TE}} \qquad 5.11$$

where ΔU_{SPOFF} is the increase in U_{SPOFF} owing to C.

C_{TE} was calculated by means of (5.11). Direct measurement of C_{TE} in a capacitor bridge was also done. Table 5.1 shows that good agreement was obtained between these two determinations of C_{TE}.

Table 5.1. Determination of C_{TE} –

Transistor	C pF	U_{SPOFF} mV	ΔU_{SPOFF} mV	C_{TE} pF calculated from (5.11)	C_{TE} pF measured in bridge
2N 2432	10	- 0.22	- 0.78	2.8	2.6
2N 1613	51	- 5.4	- 4.0	69	64
OC202	51	2.0	3.3	31	31
2N 1676	51	1.8	3.8	24	24

Measurement No. 3

U_{SPOFF} was measured for the same transistors as in measurement No. 2, but with different values of R_L. By means of (5.6), (5.8) and (5.9), U_{SPOFF} was calculated for corresponding cases. The result is presented in table 5.2. The deviation between measured and calculated values of U_{SPOFF} is small with the exception of the values for $R_L = 10\ k\Omega$. The reason is that in this case U_{SPON} is not negligibly small. For the sake of comparison the table includes a column for f_α which is a measure of $\frac{1}{Q_B}$. This shows that high f_α does not in itself give small U_{SPOFF}. 2N 1613 has the highest f_α but still the highest value of U_{SPOFF}. The fast 2N 1676 does not give lower U_{SPOFF} than the slower OC202.

Table 5.2. Determination of U_{SPOFF} with different R_L

Transistor	U_E mV	R_L k	R_S	U_E' mV	C_{TE} measured in bridge pF	U_{SPOFF} calculated mV	U_{SPOFF} measured mV	f_α Mc/s
2N 2432	640	10	45	455	2.6	-0.024	-0.01	20 (min)
		100		435		-0.23	-0.22	
		900		385		-1.8	-1.6	
2N 1613	530	10	400	400	64	-0.51	-0.34	100 (typ)
		100		380		-4.9	-5.4	
		1000		330		-42	-50	
OC202	550	10	180	400	31	0.25	0.08	3 (typ)
		100		380		2.3	2.0	
		900		330		19	18	
2N 1676	620	10	40	430	24	0.21	0.15	40 (typ)
		100		410		2.0	1.8	
		900		360		16	15	

The drift of I_{SPIKE} ---

The temperature drift of I_{SPIKE} is made up of the variations both in U_E and in C_{TE}. The latter is smallest and a fairly good estimate of the temperature drift can be obtained by assuming:

$$\frac{dU_E}{U_E\ dt} \approx \frac{dI_{SPIKE}}{I_{SPIKE} \cdot dt}$$

This assumption gives:

$$\frac{dI_{SPIKE}}{dt} \approx - I_{SPIKE} \cdot 5 \cdot 10^{-3}\ \ A/{}^{o}C \qquad 5.12$$

Comparison with (4.6) shows that the relative temperature drift in I_{SPIKE} and U_{EK} is of the same order of magnitude. dI_{SPIKE} and dU_{EK} have different signs, but in a chopper amplifier they cause drift voltages of the same sign at the output of the amplifier.

The above analysis shows that the spikes have a great influence at higher R_L. Amplitude cutting can, however, reduce I_{SPIKE} to a high degree. Most appropriate is to choose a transistor with low C_{TE}.

6. Compensated switches

The imperfections of the low level switch can partly be eliminated in different ways. It is desirable to decrease especially U_{EK} and Q. Compensated switches have earlier been presented which cancel U_{EK} by creating a voltage $- U_{EK}$ in series with the switch in the on state. This does not decrease the drift (dU_{EK}), but is only a zero displacement and this can be done in a simpler way. Here only such switches as have smaller drift than the variation in U_{EK} will be described and analyzed.

The influence of the capacitances of the transformer

Compensated switches sometimes contain a transformer. This as a rule gives rise to a certain problem, which will be treated separately here. The transformer is in general included in a drive circuit as shown in fig. 6.1 a. If the transformer had no capacitances the voltage u_3 would be zero. Now this is not the case and therefore $u_3 \neq 0$. Capacitive transmission directly between the windings can mainly be eliminated by a screen between the windings as shown in fig. 6.1.a. However, this is not sufficient to get $u_3 = 0$. The secondary winding has a certain distributed capacity to earth. This is illustrated by C_f in fig. 6.1.b. C_f can be replaced by an equivalent capacitor $C_e < C_f$ connected between earth and one end of the secondary winding as shown in fig. 6.1.c.

Assume now that the drive voltage is a square wave like u_1 in fig. 6.2. The secondary voltage u_2 has a certain tilt of the top and certain rise and fall times. Mostly C_eR_3 > rise and fall times of u_2. The spikes in u_3 therefore are almost of the same size as the steps in u_2. Between the steps C_eR_3 functions as a differentiator and the tilt of the top of u_2 causes a constant current I_3 to flow through R_3.

$$I_3 = C_e \cdot \frac{du_2}{dt} \approx C_e \cdot \frac{s \cdot U_2}{T} \cdot 2 \qquad 6.1$$

where s is the percentage tilt of the top of u_2.

Suppose that $C_e = 20$ pF. T = 1 ms. p = 0.05 and $U_2 = 5$ V. This gives $I_3 = 10^{-8}$ A and there will be a voltage $U_3 = 1$ mV across R_3 if $R_3 = 100$ kΩ. R_3 is often equal to R_L. U_3 will therefore appear across the switch in the off state and 1 mV will be much to great to be tolerated. The spikes in u_3 might also be intolerably large. The term $\frac{s \cdot C_e}{T}$ is hard to make $< 10^{-9}$ without special arrangements and U_2 must be > 0.5 V. Therefore it is difficult to get $I_3 < 10^{-9}$ A.

One-transistor switch with switching-on current to both junctions[9)]

By supplying drive current to both base and emitter in the on state as shown in fig. 6.3 a, it is possible to get the compensated offset voltage $U_s = 0$. The currents can be calculated from (4.1):

$$1 = A_N \frac{1 + \frac{1}{A_I} \cdot \frac{I_E}{I_K}}{1 + A_N \cdot \frac{I_E}{I_K}} \qquad 6.2$$

which gives:

$$\frac{I_E}{I_K} = \frac{B_I}{B_N} = k \qquad 6.3$$

By expansion of (4.1) we get:

$$\Omega U_s = A_N \frac{1 + \frac{k}{A_I}}{1 + A_N \cdot k} - 1 \qquad 6.4$$

Analyzing how U_s changes when A_N and A_I change gives a good picture of how great the drift will be. Differentiation of 6.4 gives:

$$d(\Omega U_s) = \frac{k \cdot d\frac{1}{A_I}}{\frac{1}{A_N} + k} - \frac{(1 + \frac{k}{A_I})\ d\frac{1}{A_N}}{(\frac{1}{A_N} + k)^2} \qquad 6.5$$

Eq. (6.2) and (6.5) give:

$$d(\Omega U_s) = \frac{A_N}{1 + k \cdot A_N} \left(k\, d\frac{1}{B_I} - d\frac{1}{B_N}\right) \qquad 6.6$$

because $d\frac{1}{A_N} = d\frac{1}{B_N}$ and $d\frac{1}{A_I} = d\frac{1}{B_I}$

$A_N \approx 1$. For symmetrical transistors $k \approx 1$. Eq. (6.3) and (6.6) give:

$$d\,U_s \approx -\frac{U_{EK}}{2}\left(\frac{dB_N}{B_N} - \frac{dB_I}{B_I}\right) \qquad 6.7$$

where $U_{EK} = -\frac{1}{\Omega\, B_N}$

Symmetrical transistors have as a rule

$$\frac{d\,B_N}{B_N \cdot d_t} \approx \frac{d\,B_I}{B_I \cdot d_t}$$

and therefore they are very suitable to switch in this way. If only B_N but not B_I changes, $d\,U_s$ will be:

$$d\,U_s \approx -\frac{U_{EK}}{2} \cdot \frac{d\,B_N}{B_N} \qquad 6.8$$

For unsymmetrical transistors $k \ll 1$. Eq. (6.6) becomes:

$$d\,U_s \approx -U_{EK}\left(\frac{d\,B_N}{B_N} - \frac{d\,B_I}{B_I}\right) \qquad 6.9$$

In this case it generally happens that

$$\frac{d\,B_N}{B_N\,dt} > \frac{d\,B_I}{B_I\,dt}$$

2N 2432 have for example:

$$\frac{dB_N}{B_N\ dt} \approx 3 \cdot \frac{dB_I}{B_I \cdot dt}$$

Unsymmetrical transistors are therefore not suitable to switch in this way.

If only B_N but not B_I changes, dU_s will be:

$$dU_s \approx - U_{EK} \cdot \frac{dB_N}{B_N} \qquad 6.10$$

This expression is also valid for the uncompensated switch.

The circuit in fig. 6.3 gives no elimination of the spikes. The capacity of the secondary winding causes a voltage across R_L as described above.

Two transistors in series[2)]

Fig. 6.4 shows some examples of how this switch can be realized. (All quantities will in the sequel be indexed 1 or 2 showing that they belong to transistor No. 1 or No. 2). If $B_{N1} \approx B_{N2}$ and they change, a certain dU_s will arise, which is:

$$dU_s = - U_{EK} \left(\frac{dB_{N1}}{B_{N1}} - \frac{dB_{N2}}{B_{N2}}\right) \qquad 6.11$$

$$dU_s = 0 \ \text{ if } \ \frac{dB_{N1}}{B_{N1}} = \frac{dB_{N2}}{B_{N2}}$$

Circuit a is the one usually described. The bases are directly connected in circuit b. This gives $U_{K1} = U_{K2}$, but not necessarily $I_{B1} = I_{B2}$. As a rule $I_{01} = I_{02}$ and then the excess hole densities in the bases are equal. This gives the best chances of B_{N1} being equal to B_{N2}, and hence the best matching. Circuit b can be realized very conveniently with a newly presented transistor which has two emitters. This is shown in circuit c. In circuit d there is no transformer, but the switch must be followed by a A. C. differential amplifier. The switch drives a current $\frac{U_{EK1}}{R_{L1}}$ through the source in the on state. This has in general no significance. The spikes are subtracted in the differential amplifier if $C_{TE1} = C_{TE2}$ and $R_{L1} = R_{L2}$.

If terminal No. 2 in circuits a, b or c is earthed, a certain charge current to C_f goes through R_{L2}. Furthermore the spikes will not eliminate each other owing to the capacitances of the transformer.

Two transistors in parallel [10]

This switch can be realized in two ways as shown in fig. 6.5. In this case the transistors in the on state drive a current through each other, so $U_s = 0$. If one terminal of the switch in fig. 6.5.a is earthed, charge current to C_f will give a certain voltage across R_L. The circuit with complementary transistors in fig. 6.5.b contains no transformer, which is a great advantage. In this circuit the spikes, too, are eliminated if $C_{TE1} = C_{TE2}$.

In appendix C it is shown that $U_s = 0$ when:

$$\frac{I_{B2}}{I_{B1}} = \frac{1 + \frac{B_{N2}}{B_{I2}}}{1 + \frac{B_{N1}}{B_{I1}}} \qquad 6.12$$

It is further shown that:

$$dU_s \approx \frac{-U_{EK}}{2\left(1+\frac{B_I}{B_N}\right)} \left(\frac{dB_{N1}}{B_{N1}} - \frac{dB_{I1}}{B_{I1}} + \frac{dB_{I2}}{B_{I2}} - \frac{dB_{N2}}{B_{N2}}\right) \qquad 6.13$$

if $\quad B_{N1} = B_{N2},\ B_{I1} = B_{I2}$ and $\frac{I_{B2}}{I_{B1}} = 1.$

$dU_s = 0$ if $\frac{dB_{N1}}{B_{N1}} = \frac{dB_{N2}}{B_{N2}}$, which also was the case in the circuit in fig. 6.4, but $dU_s = 0$ also if $\frac{dB_N}{B_N} = \frac{dB_I}{B_I}$, which often happens in symmetrical transistors. The factor $2\left(1+\frac{B_I}{B_N}\right) \approx 2$ for unsymmetrical transistors and ≈ 4 for symmetrical. Consequently this circuit ought to have, at the most, only half as great a drift as the circuit in fig. 6.4. To test this the drift of 5 pairs of OC44 (unsymmetrical alloy germanium) during 7 days was measured. The transistors in each pair were in the on state and connected in series or parallel depending on the position of a switch. (Between the measurements the transistors were always connected in series.) $dU_s = f$ (time) is presented in diagram 6.1, which shows that dU_s for all pairs is smallest in parallel connection.

For chopper applications suitable complementary planar transistors are now available (for example 2N 2466 and 2N 2593). Perfect complementary transistors are in principle impossible to obtain. (Holes and electrons have different mobilities.) In this case, however, only B_N, B_I and C_{TE} need to be similar. Unfortunately there does not yet seems to be any suitable complementary symmetrical silicon transistors on the market. However, symmetrical epitaxial transistors will probably be available in the future.

Switch transistor with emitter current from the base of another transistor

In section 2 it was shown that the base - emitter electron current demands a hole current from the collector to the emitter of the same magnitude in order to get $I_E = 0$. This caused $U_{EK} \neq 0$. Therefore if the current from the base of another transistor is supplied to the emitter it is possible to get $U_s = 0$. This can be done as shown in fig. 6.6.a. If the transistors have the same I_o and B_N, $U_s = 0$ if $U_{E1} = U_{E2}$, i.e. $U_{K1} = U_{E2} = E$. If B_{N1} and B_{N2} change, dU_s will be:

$$dU_s = - U_{EK} \left(\frac{dB_{N1}}{B_{N1}} - \frac{dB_{N2}}{B_{N2}} \right) \qquad 6.14$$

The spikes will eliminate each other if $C_{TE1} = C_{TE2}$.

The voltages E demand a relatively complicated drive circuit. The circuit in fig. 6.6.b is a more simple solution, which is useful for unsymmetrical transistors. It is shown in appendix D that dU_s in this case will be:

$$dU_s \approx - U_{EK} \left(\frac{dB_{N1}}{B_{N1}} - \frac{dB_{N2}}{B_{N2}} - \frac{dB_{I1}}{B_{I1}} \right) \qquad 6.15$$

The change in B_{I1} consequently gives a certain increase of the drift. However, $\frac{dB_{I1}}{B_{I1}}$ is as a rule relatively small. The temperature change in B_{I1} can be cancelled out if I_{E2} increases a little with temperature. Such an increase can be achieved by making use of the decrease of U_{E2} with temperature. This is about 2.5 mV/°C. If $\frac{dB_{I1}}{B_{I1}} = 2 \cdot 10^{-3}/°C$ (typical value for 2N 2432 at $I_K = 1$ mA) the drift will be cancelled out if $E_2 \approx 1.8$ V and $E_1 >> U_{K1}$.

The switch in fig. 6.6.b is attractive because it includes no transformer, and does not require B_N-matched transistors. Only

$$\frac{dB_{N1}}{B_{N1}} = \frac{dB_{N2}}{B_{N2}}$$ is desirable.

A chopper amplifier with this circuit as input chopper was constructed. The drift of this amplifier is $< 2\mu$ V/week at room temperature.

7. Thermoelectric effects in the switch

Thermoelectric voltages may appear in the switch. Temperature differences within the transistor are not so easily created. Therefore the thermoelectric voltages in the junctions cancel each other to a high degree. Temperature differences between the transistor leads arise far more easily, and therefore the thermoelectric power between the leads and copper is of great importance. The leads consist of a copper alloy which in some cases has a rather high thermoelectric power in relation to copper. Fig. 7.1 gives $U_L = 0$ in the off state and $U_L = U_{EK} + e_1 - e_2$ in the on state, where e_1 and e_2 are the thermoelectric voltages in the soldered joints. A temperature difference between the emitter and collector leads is hence equivalent to a change in U_{EK}.

The thermoelectric power between copper and the leads was measured for some different transistors. The result is presented in table 7.1, which shows that transistors with metal case have leads with rather high thermoelectric power. Obviously it is very important to have a uniform temperature around the switch.

Table 7.1. Magnitude of thermoelectric power between copper and some different transistor leads

Transistor	OC 45	2N 1308	OC 202	2N 1613	2N 1676	2N 2432
Magnitude of thermoelectric power $\mu V/^{\circ}C$	4.4	18	3.1	14	14	15

8. Conclusions

A switch transistor for small signals ought to have the following properties:

1. High B_N (also at low I_E)
2. B_I ought to be > 1
3. Small r_c
4. Small I_o
5. Small C_{TE}
6. In general f_α only needs to be > a few Mc/s

Planar epitaxial silicon transistors with small emitter area meet these requirements best.

The static and dynamic characteristics of the transistor switch can well be calculated by the theory given in this paper.

Some compensated switches have lower drift than the uncompensated switch. The two-transistor-in-parallel connection (fig. 6.5) has the lowest drift.

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Appendix A

The offset voltage at variable doping in the base

At variable doping in the base P_o will be a function of position. The one-dimensional case, i.e. $P_o = P_o$ (x) (x is defined in fig. 2.3), will be treated here. The hole density in the base at the emitter junction P_{BE} is:

$$P_{BE} = P_{oE}\ e^{\Omega U_E} \qquad 1$$

where P_{oE} is the equilibrium hole density in the base at the emitter junction.

The hole density in the base at the collector junction P_{BK} is:

$$P_{BK} = P_{oK}\ e^{\Omega U_K} \qquad 2$$

where P_{oK} is the equilibrium hole density in the base at the collector junction.

The electrostatic potential ψ in the base will vary with x, and $P_o(x)$ can be written:

$$P_o(x) = n_i \cdot e^{\Omega [\varphi - \psi (x)]} \qquad 3$$

where the Fermi level φ is independent of x. When excess holes appear, the hole density P(x) can be written:

$$P(x) = n_i \cdot e^{\Omega [\varphi_p - \psi (X)]} \qquad 4$$

where φ_p is the quasi-Fermi level for the holes.

An electrostatic field E is created in the base. The hole current density J_p is:

$$J_p = q \cdot \mu_p \cdot P \cdot E - q \cdot D_p \cdot \frac{dP}{dx} \qquad 5$$

where

μ_p = the mobility of the holes

D_p = the diffusion constant for holes

It is convenient to assume $J_p = 0$ and then examine which value U_{EK} acquires.

Eq. (5) gives:

$$\mu_p \cdot P \cdot E - D_p \cdot \frac{dP}{dx} = 0 \qquad 6$$

Further:

$$E = - \frac{d\psi}{dx} \qquad 7$$

$$D_p = \frac{\mu_p}{\Omega} \qquad 8$$

Eq. (6), (7) and (8) give:

$$- \mu_p \cdot P \cdot \frac{d\psi}{dx} - \frac{\mu_p}{\Omega} \cdot P \cdot \Omega \cdot \frac{d}{dx} (\varphi_p - \psi) = 0$$

$$\frac{d\varphi_p}{dx} = 0$$

$$\therefore \varphi_p = \text{constant} \qquad 9$$

Eq. (3), (4) and (9) give:

$$\frac{P(x)}{P_o(x)} = n_i \quad e^{\Omega(\varphi_p - \varphi)} = \text{constant}$$

Hence the relative increase in P is the same everywhere in the base. From (1) and (2) it follows that $U_E = U_K$, i.e. $U_{EK} = 0$.

Therefore when I_p is small, U_{EK} will also be small, and consequently the base - emitter electron current should be small in order to get a small U_{EK}.

Appendix B

Derivation of R_{EB} --

It is assumed that the following expression holds for the collector current:

$$E = U_K + I_K \cdot R_B \qquad 1$$

Further, (3.14) and (3.15) can be written approximately:

$$\frac{I_E}{I_o} = -\frac{1}{A_N} \cdot e^{\Omega U_E} + e^{\Omega U_K} \qquad 2$$

$$\frac{I_K}{I_o} = e^{\Omega U_E} - \frac{1}{A_I} \quad e^{\Omega U_K} \qquad 3$$

Differentiation of (2) and (3) gives:

$$\frac{dI_E}{I_o} = -\frac{1}{A_N} \Omega \cdot e^{\Omega U_E} dU_E + \Omega \; e^{\Omega U_K} dU_K \qquad 4$$

$$\frac{dI_K}{I_o} = \Omega \cdot e^{\Omega U_E} \, dU_E - \frac{1}{A_I} \, \Omega \cdot e^{\Omega U_K} \cdot dU_K \qquad 5$$

Eq. (4) and (5) give:

$$\frac{dI_E}{I_o} + A_I \frac{dI_K}{I_o} = \Omega \, e^{\Omega U_E} \left(A_I - \frac{1}{A_N}\right) \, dU_E \qquad 6$$

Assuming $I_E = 0$, (2) gives:

$$\frac{1}{A_N} \, e^{\Omega U_E} = e^{\Omega U_K} \qquad 7$$

Eq. (3) and (7) give:

$$\frac{I_K}{I_o} = \frac{1}{A_I} \cdot e^{\Omega U_E} \left(A_I - \frac{1}{A_N}\right) \qquad 8$$

Eq. (6) and (8) give:

$$dI_E + A_I \, dI_K = \Omega \, A_I \, I_K \, dU_E \qquad 9$$

Differentiation of (1) gives:

$$0 = dU_K + R_B \cdot dI_K \qquad 10$$

Eq. (4), (5), (7) and (8) also give:

$$A_N \, dI_E + dI_K = \Omega \, I_K \, dU_K \qquad 11$$

Eq. (10) and (11) give:

$$0 = A_N\, dI_E + dI_K + R_B\, \Omega\, I_K\, dI_K \qquad 12$$

Eq. (9) and (12) give:

$$1 - \frac{A_N\, A_I}{1 + R_B\, \Omega\, I_K} = \Omega\, A_I\, I_K\, \frac{dU_E}{dI_E} \qquad 13$$

When $\frac{1}{\Omega\, I_K} << R_B$, (13) gives:

$$\frac{dU_E}{dI_E} = R_{EB} = \frac{1}{\Omega\, A_I\, I_K} \qquad 14$$

When $\frac{1}{\Omega\, I_K} >> R_B$, (13) gives:

$$\frac{dU_E}{dI_E} = R_{EB} = \frac{1}{\Omega\, I_K} \left(\frac{1}{A_I} - A_N\right) \qquad 15$$

Appendix C

Derivation of dU_s for the switch in fig. 6.5

From (4.1) we have for transistor No. 1: ($U_s << \frac{1}{\Omega}$):

$$\Omega U_s = \frac{1 - \frac{1}{B_{I1}} \cdot \frac{I_{E1}}{I_{B1}}}{\frac{1}{A_{N1}} + \frac{1}{B_{N1}} \cdot \frac{I_{E1}}{I_{B1}}} - 1 \qquad 1$$

And for transistor No. 2:

$$- \Omega U_s = \frac{1 - \frac{1}{B_{I2}} \cdot \frac{I_{E2}}{I_{B2}}}{\frac{1}{A_{N2}} + \frac{1}{B_{N2}} \cdot \frac{I_{E2}}{I_{B2}}} - 1 \qquad 2$$

Fig. 6.5 shows that:

$$I_{E1} = I_{E2} \qquad 3$$

I_{B1} and I_{B2} are presumed to be constant.

Combining (1) and (2) gives:

$$\frac{I_{B2}}{I_{B1}} = \frac{\left(\frac{\Omega U_s}{A_{N1}} + \frac{1}{B_{N1}}\right)\left(\frac{1}{B_{N2}} + \frac{1}{B_{I2}} - \frac{\Omega U_s}{B_{N2}}\right)}{\left(\frac{-\Omega U_s}{A_{N2}} + \frac{1}{B_{N2}}\right)\left(\frac{1}{B_{N1}} + \frac{1}{B_{I1}} + \frac{\Omega U_s}{B_{N1}}\right)} \qquad 4$$

Neglecting terms with U_s^2 (4) gives:

$$\frac{I_{B2}}{I_{B1}} = \frac{\Omega U_s \left(\frac{1}{A_{N1}\, B_{N2}} + \frac{1}{A_{N1}\, B_{I2}} - \frac{1}{B_{N1}\, B_{N2}}\right) + \frac{1}{B_{N1}\, B_{N2}} - \frac{1}{B_{N1}\, B_{I2}}}{-\Omega U_s \left(\frac{1}{A_{N2}\, B_{N1}} + \frac{1}{A_{N2}\, B_{I1}} - \frac{1}{B_{N1}\, B_{N2}}\right) + \frac{1}{B_{N1}\, B_{N2}} - \frac{1}{B_{N2}\, B_{I1}}} \qquad 5$$

When $U_s = 0$ we have:

$$\frac{I_{B2}}{I_{B1}} = \frac{1 + \frac{B_{N2}}{B_{I2}}}{1 + \frac{B_{N1}}{B_{I1}}} \qquad 6$$

For the sake of simplicity it is here assumed that $\frac{I_{B2}}{I_{B1}} = 1$. Differentiation of (5) gives, if $U_s = 0$:

$$d\Omega\, U_s = - \frac{\frac{1}{B_{N1}}\, d\, \frac{1}{B_{I2}} + \frac{1}{B_{I2}}\, d\, \frac{1}{B_{N1}} - \frac{1}{B_{N2}} \cdot d\, \frac{1}{B_{I1}} - \frac{1}{B_{I1}}\, d\, \frac{1}{B_{N2}}}{\frac{1}{A_{N2}\, B_{N1}} \left(1 + \frac{B_{N1}}{B_{I1}}\right) + \frac{1}{B_{N2}\, A_{N1}} \left(1 + \frac{B_{N2}}{B_{I2}}\right) - \frac{2}{B_{N1}\, B_{N2}}} \qquad 7$$

Eq. (6) and (7) give the approximate expression:

$$d\Omega\, U_s = \frac{\frac{1}{B_{N1}\, B_{I2}} \left(\frac{dB_{I2}}{B_{I2}} + \frac{dB_{N1}}{B_{N1}}\right) - \frac{1}{B_{N2}\, B_{I1}} \left(\frac{dB_{I1}}{B_{I1}} + \frac{dB_{N2}}{B_{N2}}\right)}{\left(1 + \frac{B_{N1}}{B_{I1}}\right) \left(\frac{1}{B_{N1}} + \frac{1}{B_{N2}}\right)}$$

Assuming $B_{N1} = B_N$, $B_{I1} = B_{I2} = B_I$ we have:

$$dU_s = - \frac{U_{EK}}{2\left(1 + \frac{B_I}{B_N}\right)} \left(\frac{dB_{N1}}{B_{N1}} - \frac{dB_{I1}}{B_{I1}} + \frac{dB_{I2}}{B_{I2}} - \frac{dB_{N2}}{B_{N2}}\right)$$

Appendix D

Derivation of dU_s for the switch in fig. 6.6.b

Eq. (4.1) gives for transistor No. 1 ($U_s \ll \frac{1}{\Omega}$):

$$\Omega U_s = \frac{1 - \frac{1}{B_{I1}} \cdot \frac{I_{E1}}{I_{B1}}}{\frac{1}{A_{N1}} + \frac{1}{B_{N1}} \cdot \frac{I_{E1}}{I_{B1}}} - 1 \qquad 1$$

From fig. 6.6.b we have:

$$I_{E1} = - I_{B2} = (1 - A_{N2})\, I_{E2} \qquad 2$$

Combining (1) and (2):

$$\Omega U_s = \frac{1 - \frac{1}{B_{I1}} \cdot \frac{a}{1 + B_{N2}}}{\frac{1}{A_{N1}} + \frac{1}{B_{N1}} \cdot \frac{a}{1 + B_{N2}}} - 1 \qquad 3$$

where $a = \frac{I_{E2}}{I_{B1}}$ is presumed to be constant.

When $U_s = 0$ we have:

$$\frac{I_{E2}}{I_{B1}} = - \frac{1 + B_{N2}}{1 + \frac{B_{N1}}{B_{I1}}} \qquad 4$$

Differentiating (3) and assuming $U_s = 0$ gives:

$$d\Omega\, U_s = \frac{-\left(1 + \frac{B_{I1}}{B_{N1}}\right) \frac{dB_{N2}}{1 + B_{N2}} + \frac{dB_{N1}}{B_{N1}} - \frac{dB_{I1}}{B_{I1}}}{B_{N1} + B_{I1} + 1} \qquad 5$$

For unsymmetrical transistors (5) can be written approximately:

$$dU_s \approx - U_{EK} \left[\frac{dB_{N1}}{B_{N1}} - \frac{dB_{N2}}{B_{N2}} - \frac{dB_{I1}}{B_{I1}} \right] \qquad 6$$

AL/EL

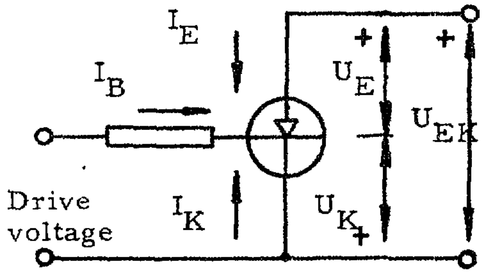


Fig. 2.1. The common collector transistor switch.

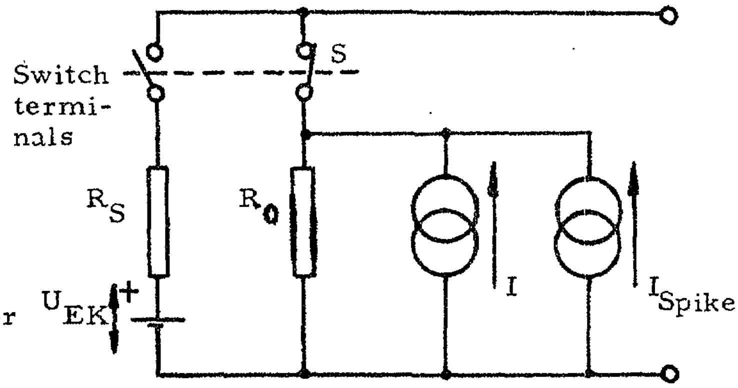


Fig. 2.2. The equivalent circuit of the low level switch.

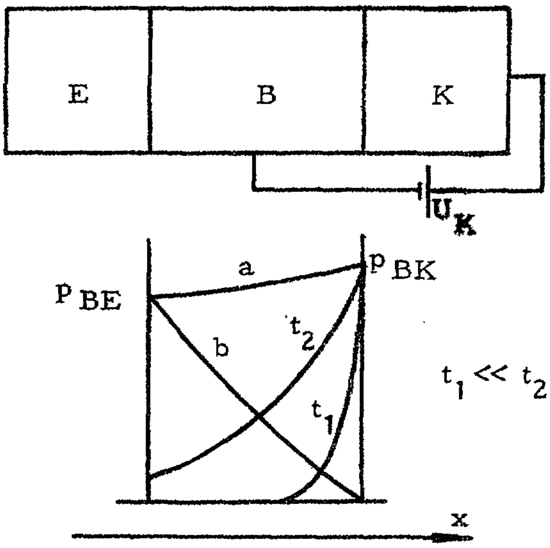


Fig. 2.3. The excess hole density distribution in the base with open emitter after a positive voltage U_K has been impressed between the collector and the base.

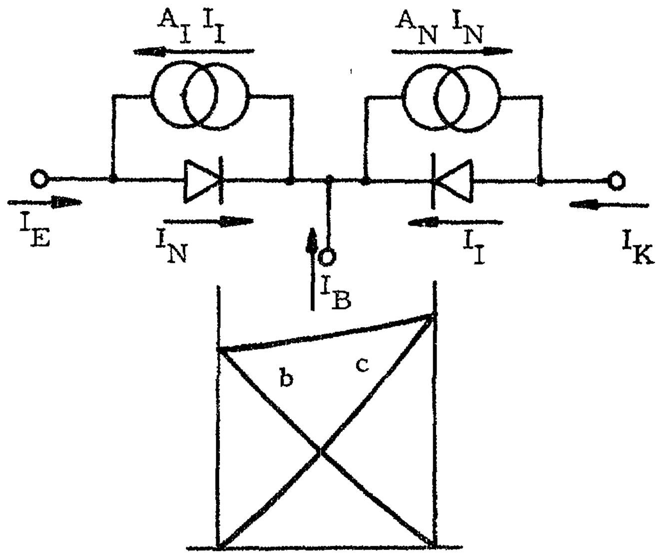


Fig. 2.4. The double diode equivalent circuit. This is derived by superposing two excess hole density distributions shown by curves b and c.

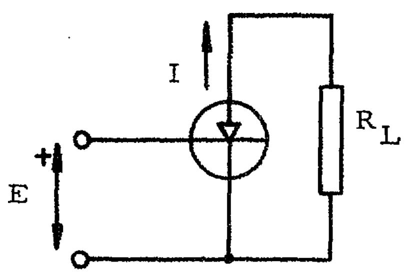


Fig. 4.1. The switch in the off state with large reverse voltage.

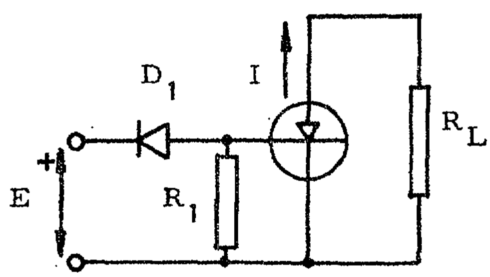


Fig. 4.2. The switch in the off state with small reverse voltage.

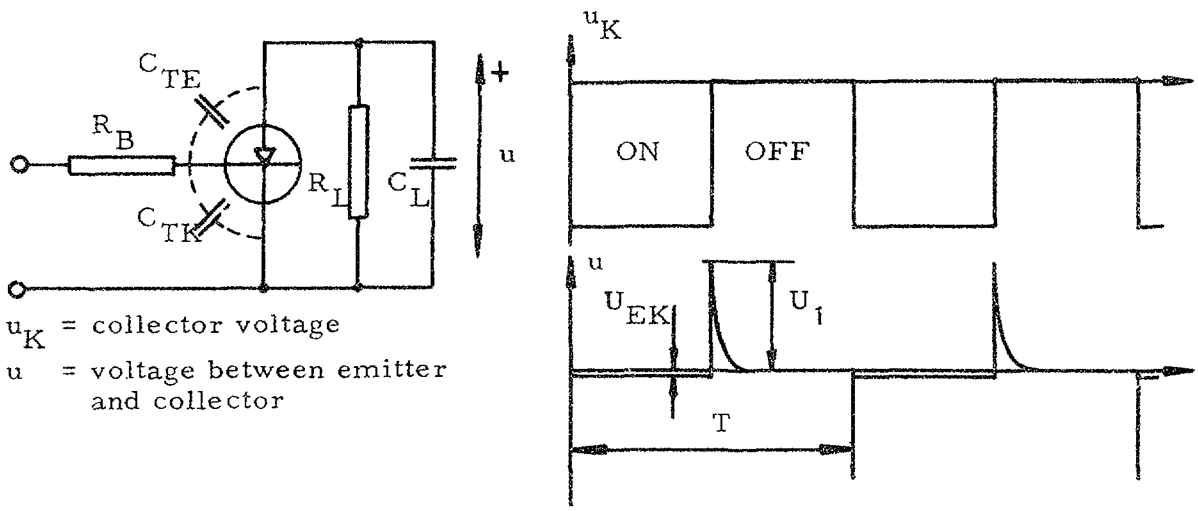


Fig. 5.1. Spikes appear over the switch at switching on and off.

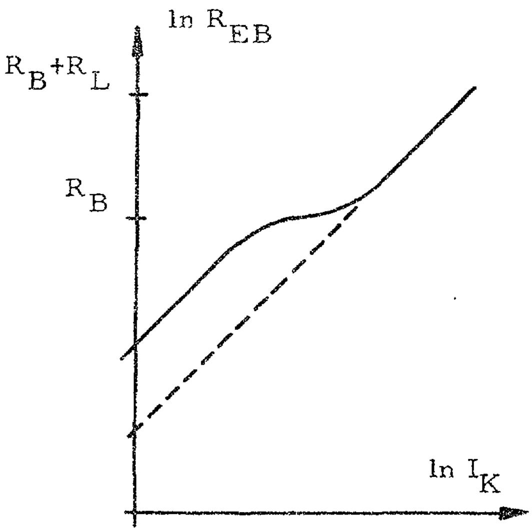


Fig. 5.2. $R_{EB} = f(I_K)$

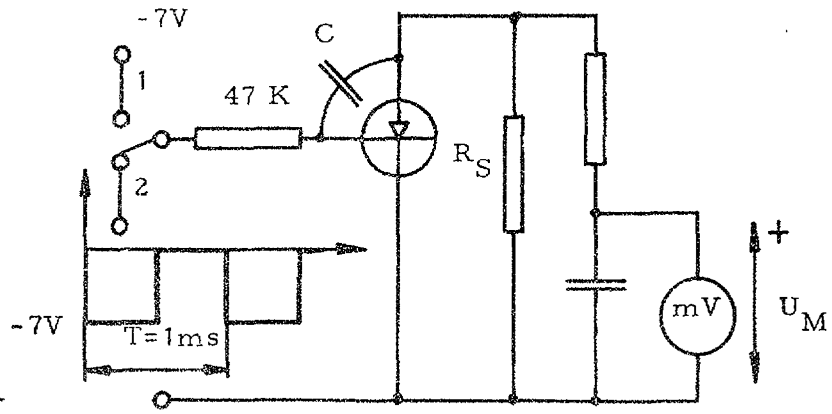


Fig. 5.3. Circuit for the measurement of U_{SPOFF}

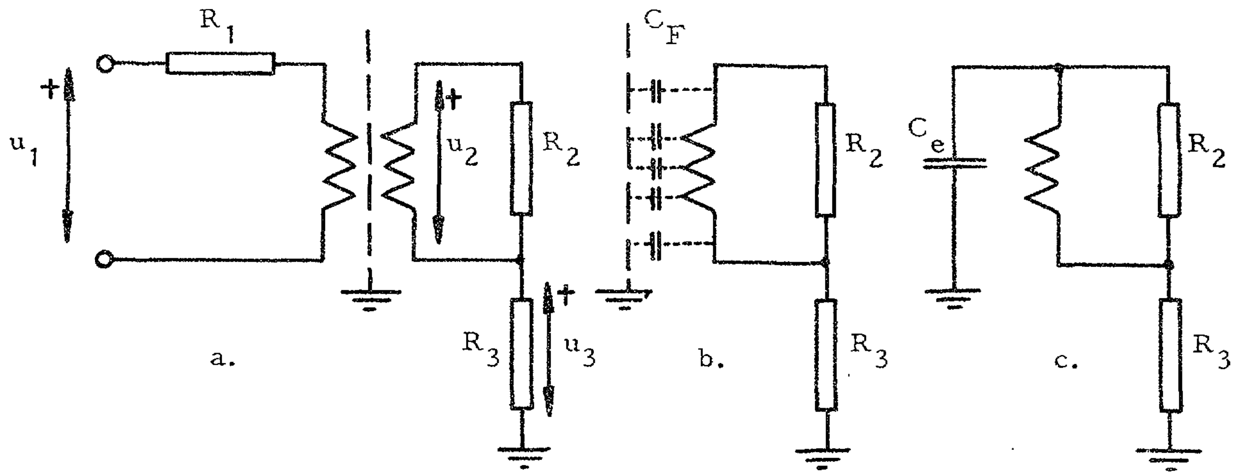


Fig. 6.1. a. Drive circuit with a transformer.
b. There is a distributed capacity C_F between the screen and the secondary winding.
c. C_F replaced by an equivalent capacitance C_e.

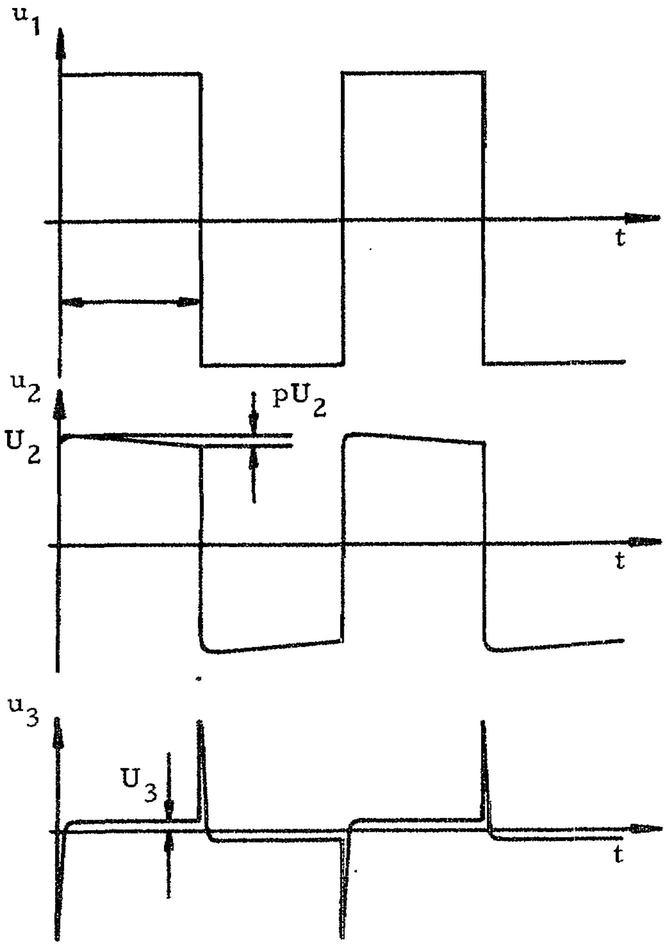
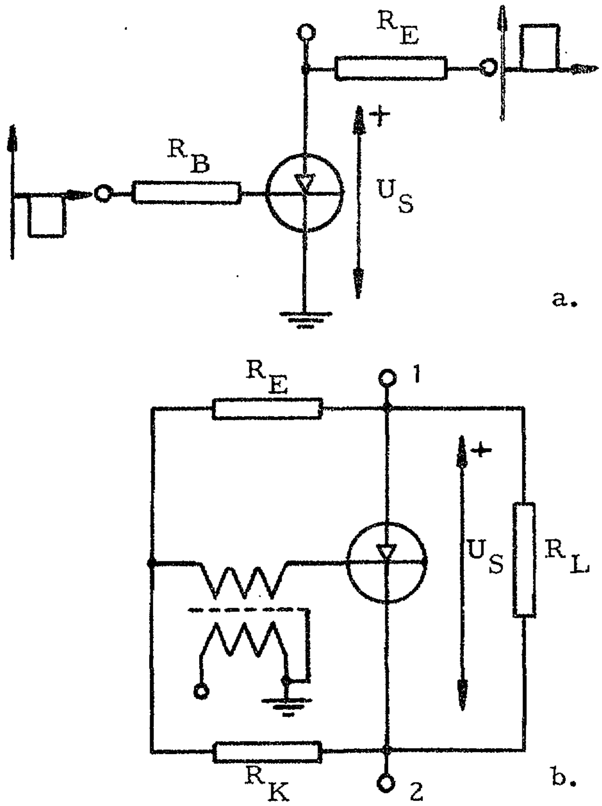


Fig. 6.2. Waveformes in the drive circuit fig. 6.1.a.



6.3. One-transistor switches with switching-on current to both junctions.

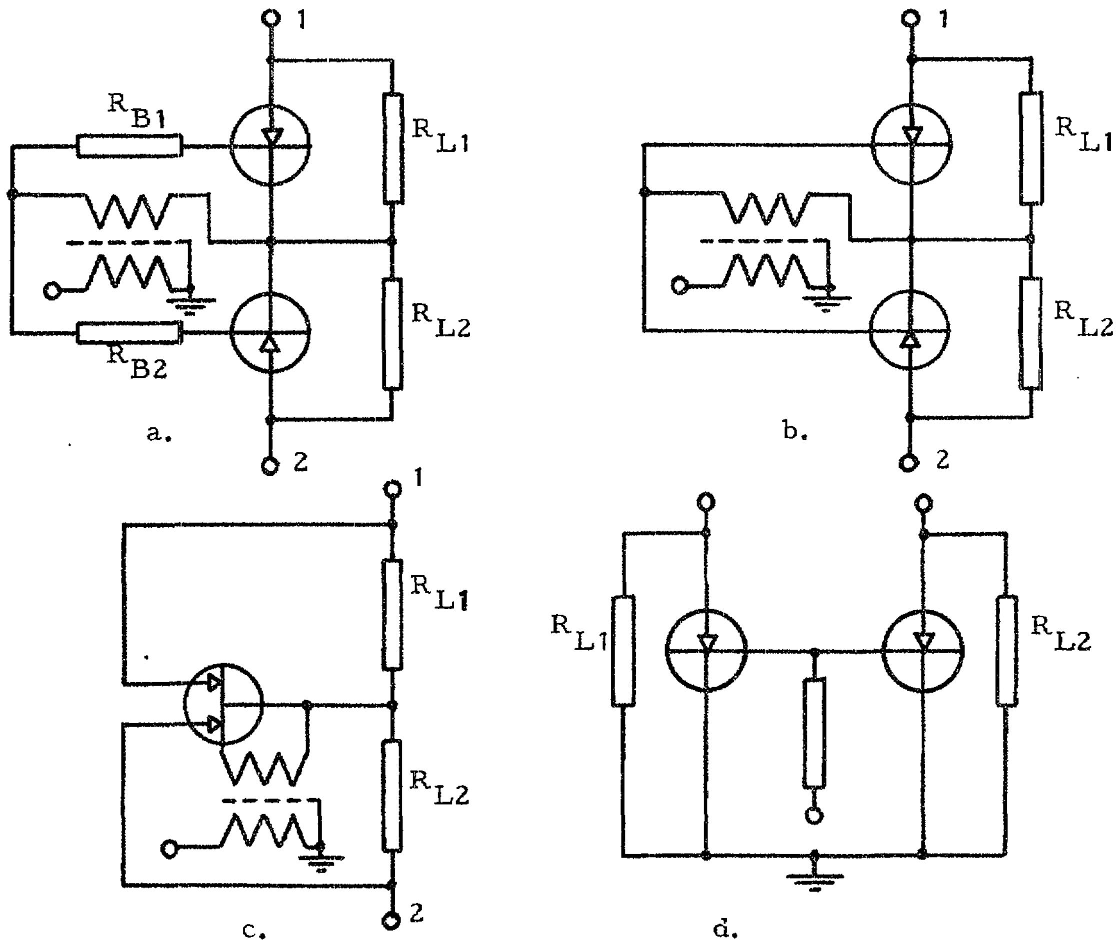


Fig. 6.4. Two transistors in series switches.

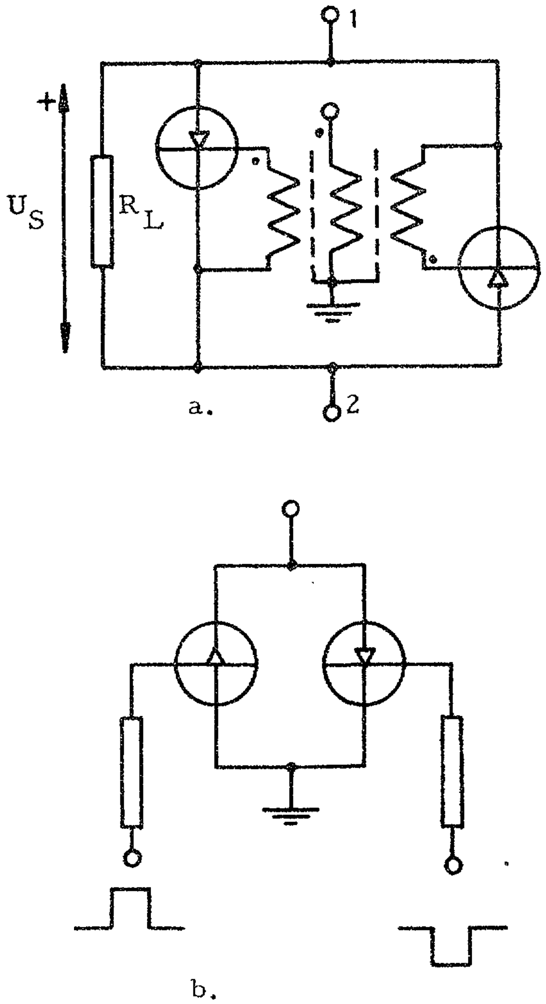


Fig. 6.5. Two transistors in parallel switches.

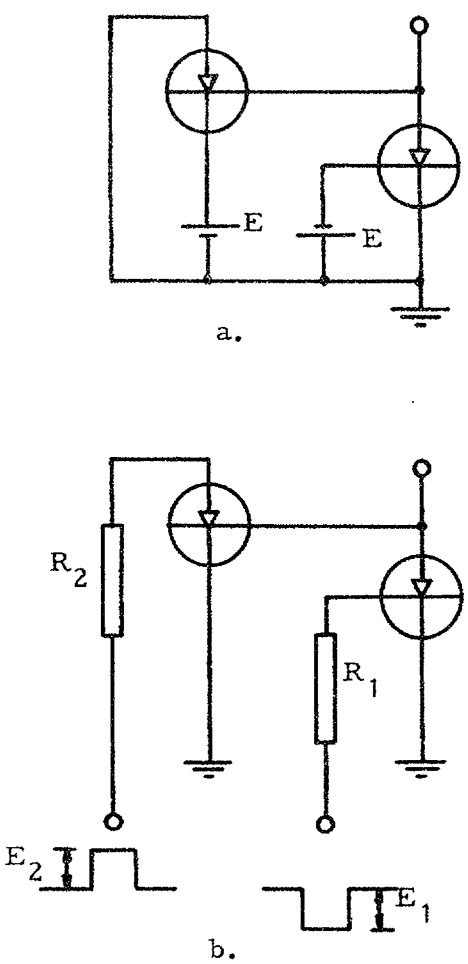


Fig. 6.6. Switch transistor with emitter current from the base of another transistor.

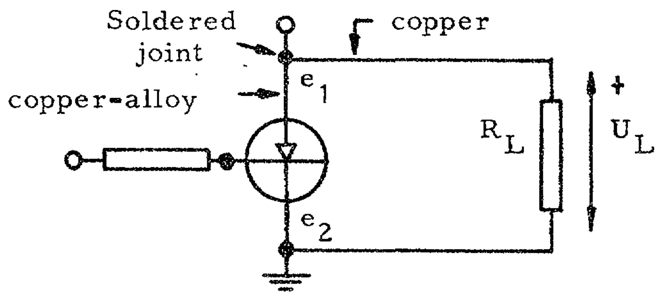


Fig. 7.1. Thermoelectric voltages in the switch.

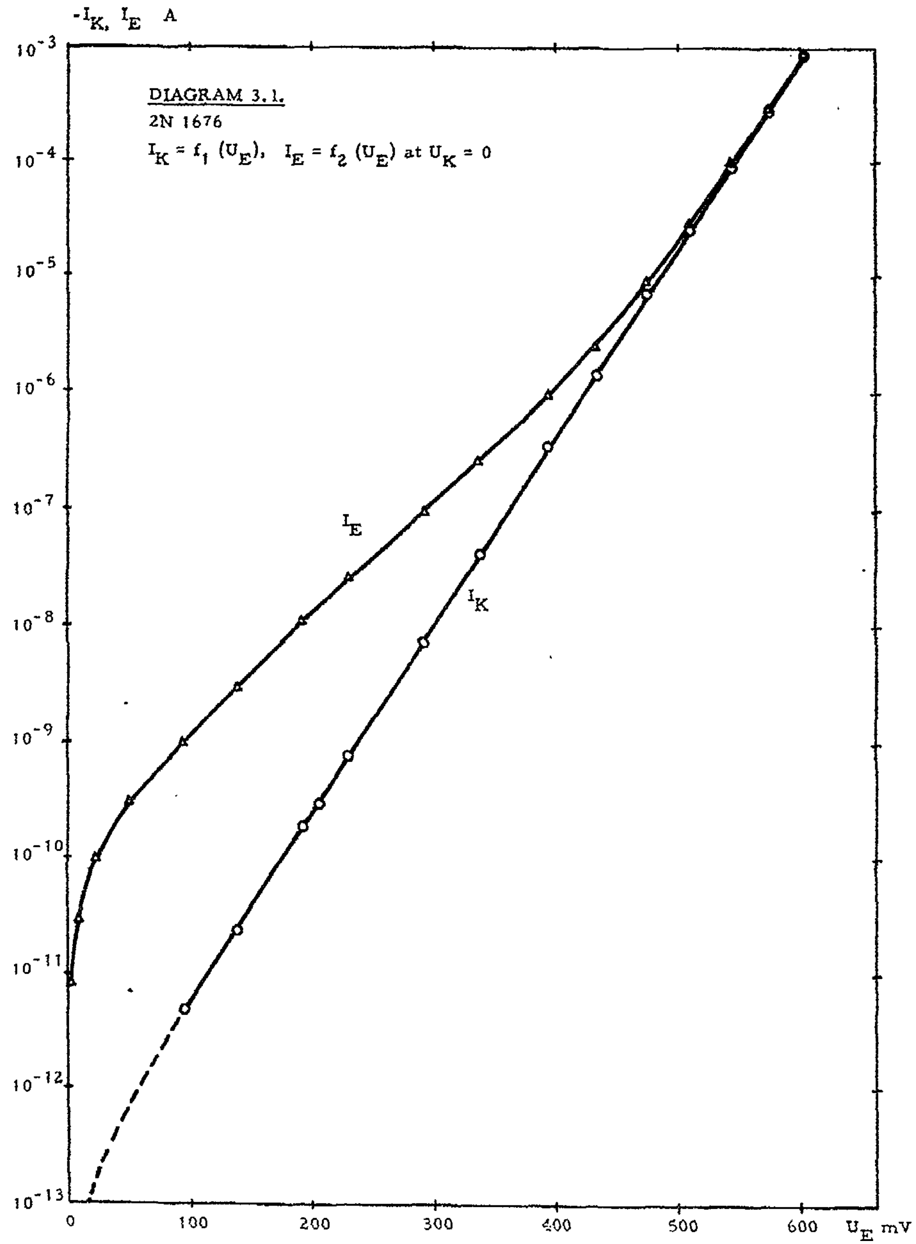


DIAGRAM 3.1.
2N 1676
$I_K = f_1\,(U_E)$, $I_E = f_2\,(U_E)$ at $U_K = 0$
$-I_K$, I_E A
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
I_E
I_K
0
100
200
300
400
500
600
U_E mV

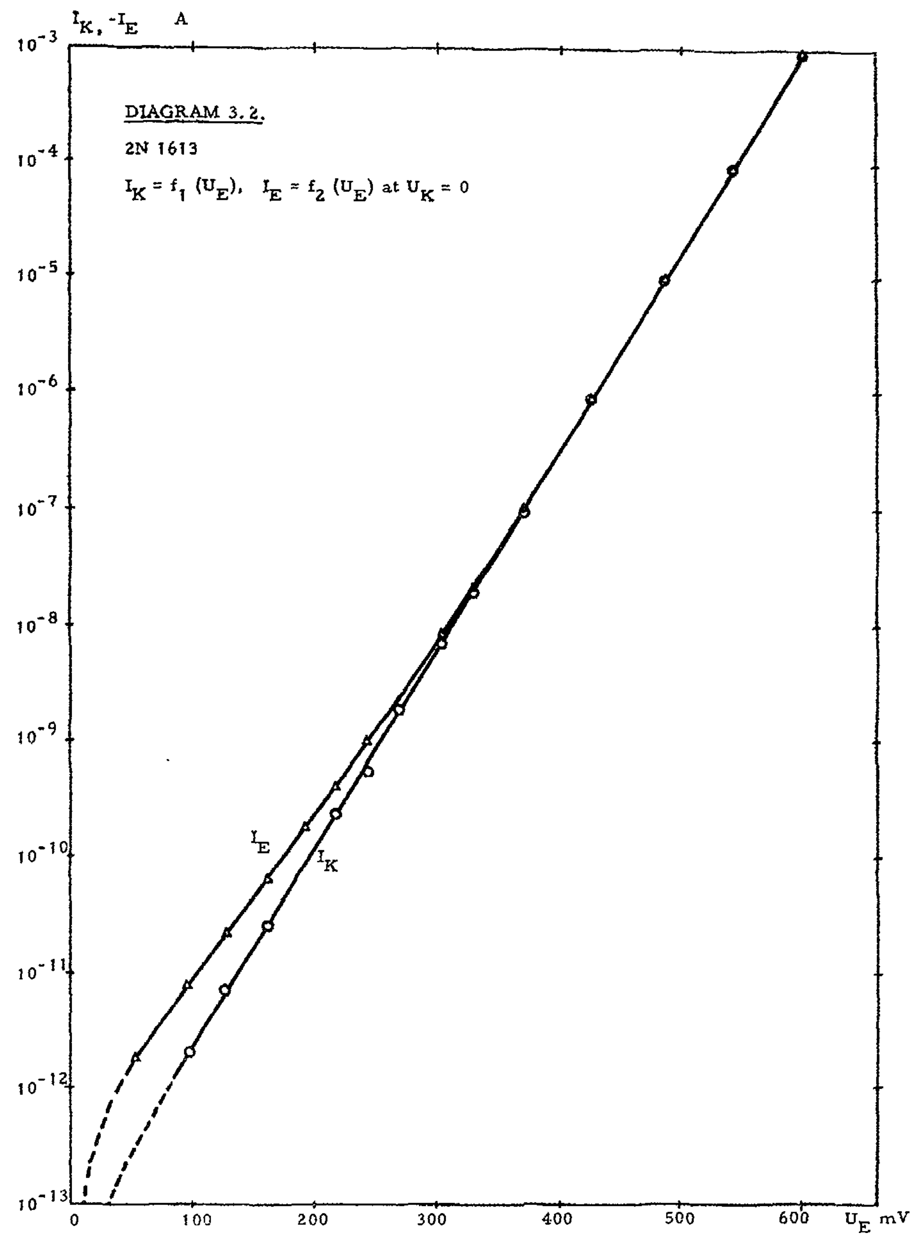


DIAGRAM 3.2.
2N 1613
$I_K = f_1\,(U_E)$, $I_E = f_2\,(U_E)$ at $U_K = 0$
I_K, $-I_E$ A
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
I_E
I_K
0
100
200
300
400
500
600
U_E mV

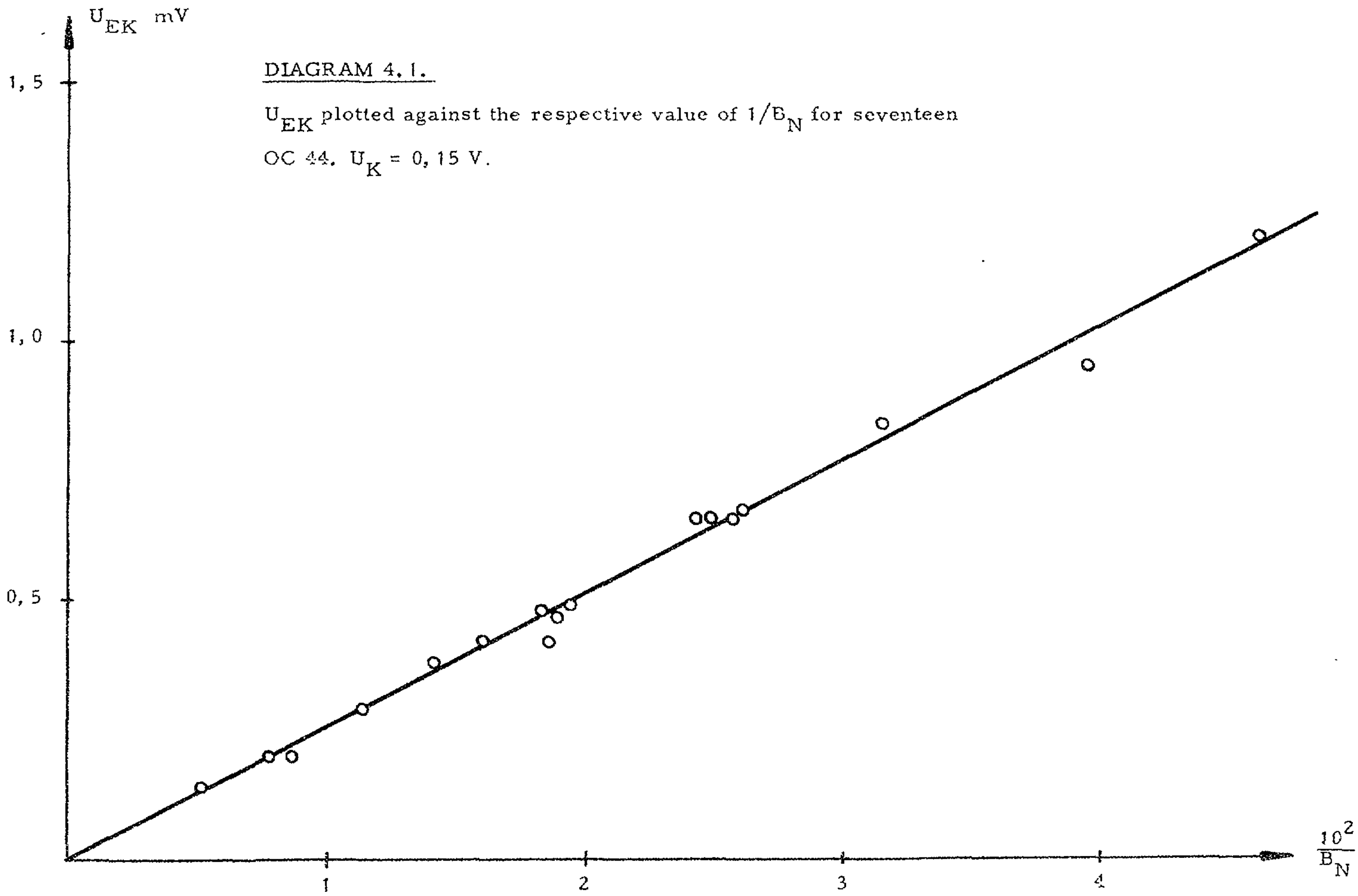


DIAGRAM 4.1.

U_{EK} plotted against the respective value of $1/B_N$ for seventeen OC 44. U_K = 0,15 V.

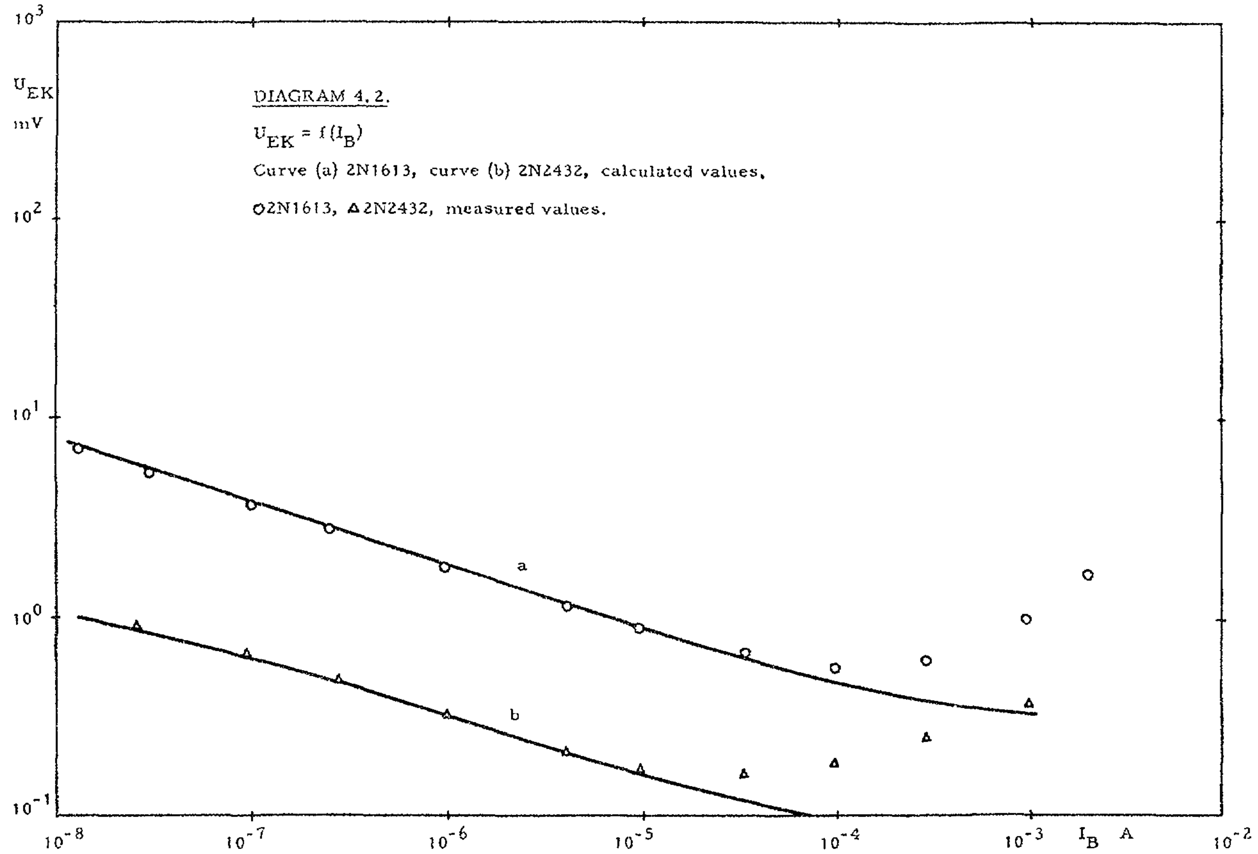


DIAGRAM 4.2.

$U_{EK} = f(I_B)$

Curve (a) 2N1613, curve (b) 2N2432, calculated values.

○2N1613, △2N2432, measured values.

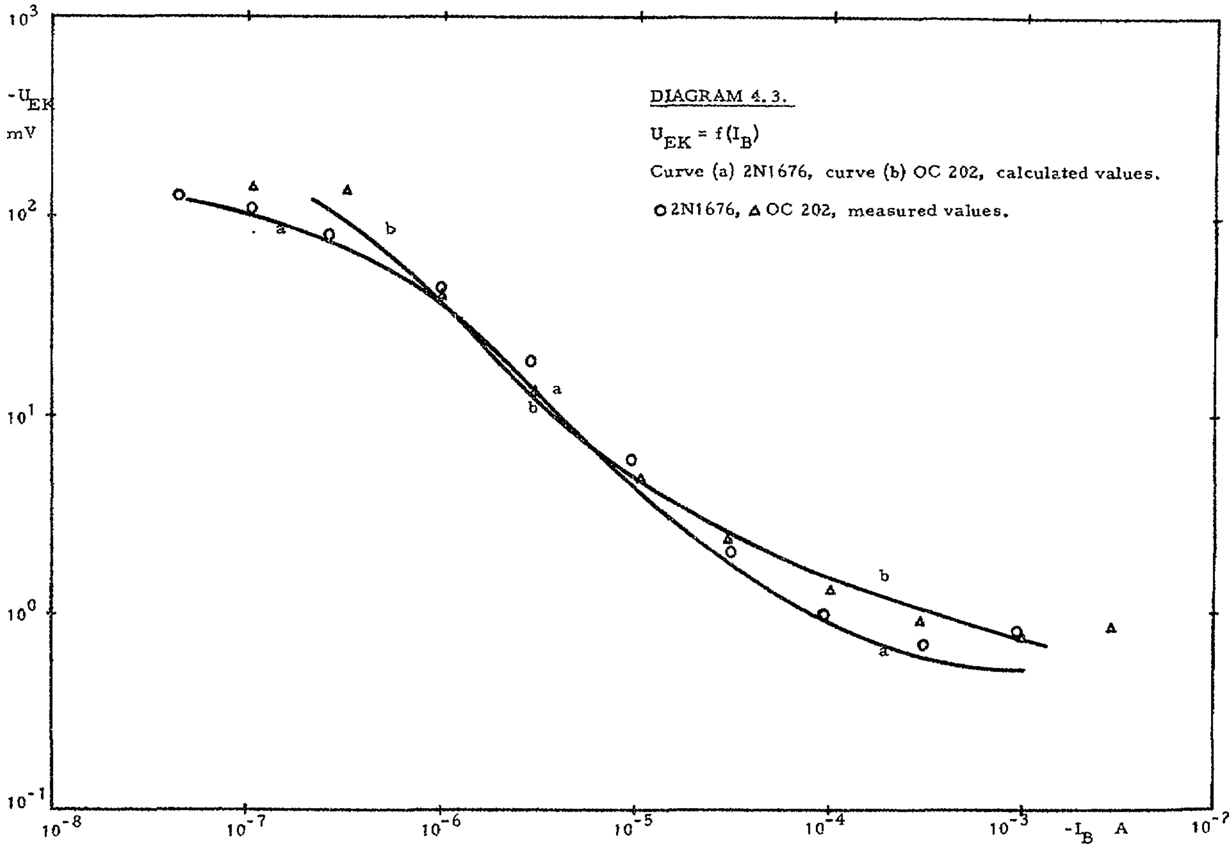


DIAGRAM 4.3.
$U_{EK} = f(I_B)$
Curve (a) 2N1676, curve (b) OC 202, calculated values.
○ 2N1676, △ OC 202, measured values.
$-U_{EK}$
mV
10^3
10^2
10^1
10^0
10^{-1}
10^{-8}
10^{-7}
10^{-6}
10^{-5}
10^{-4}
10^{-3}
$-I_B$ A
10^{-2}
a
b

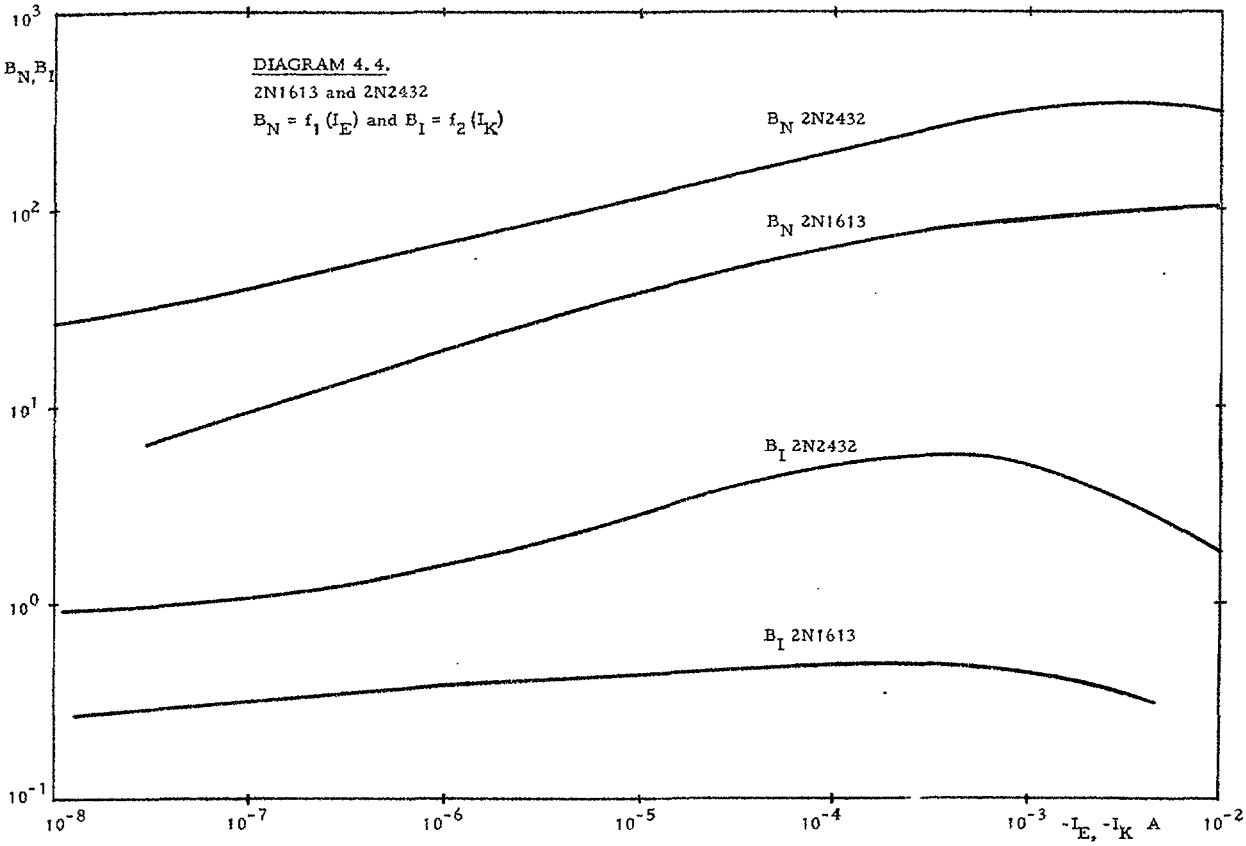
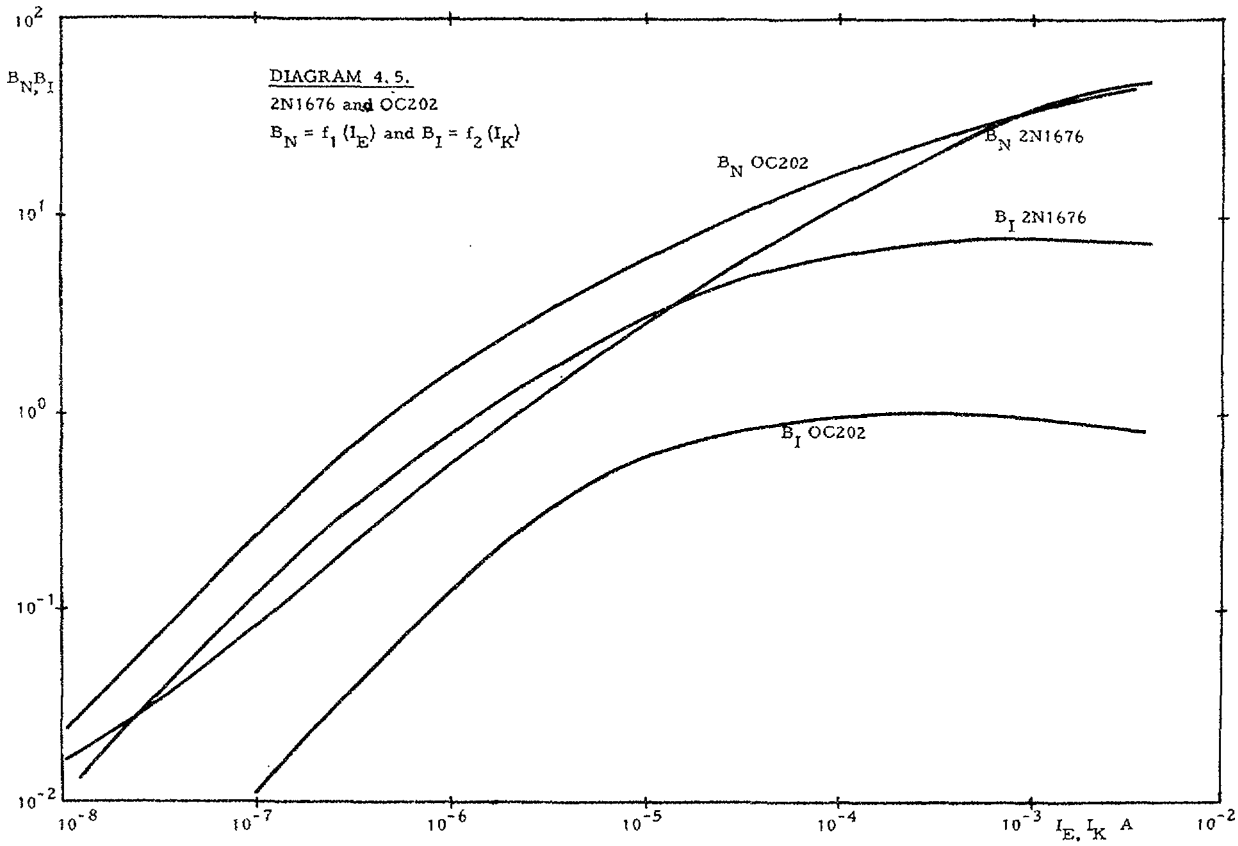
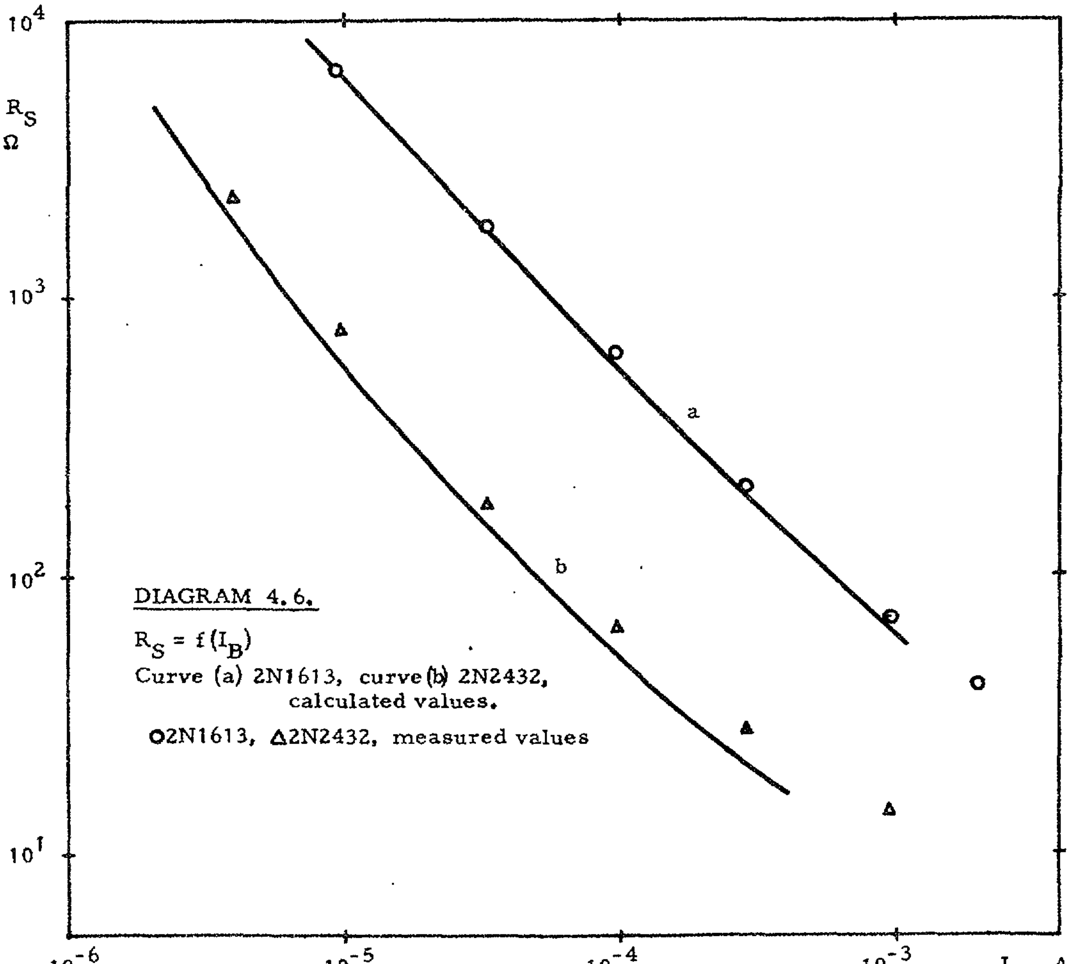


DIAGRAM 4.4.
2N1613 and 2N2432
$B_N = f_1(I_E)$ and $B_I = f_2(I_K)$
B_N, B_I
B_N 2N2432
B_N 2N1613
B_I 2N2432
B_I 2N1613
10^3
10^2
10^1
10^0
10^{-1}
10^{-8}
10^{-7}
10^{-6}
10^{-5}
10^{-4}
10^{-3}
$-I_E, -I_K$ A
10^{-2}



10^2
B_N, B_I
DIAGRAM 4.5.
2N1676 and OC202
$B_N = f_1(I_E)$ and $B_I = f_2(I_K)$
B_N OC202
B_N 2N1676
B_I 2N1676
B_I OC202
10^1
10^0
10^{-1}
10^{-2}
10^{-8}
10^{-7}
10^{-6}
10^{-5}
10^{-4}
10^{-3}
I_E, I_K A
10^{-2}



10^4
R_S
Ω
10^3
10^2
10^1
a
b
DIAGRAM 4.6.
$R_S = f(I_B)$
Curve (a) 2N1613, curve (b) 2N2432,
calculated values.
o2N1613, Δ2N2432, measured values
10^{-6}
10^{-5}
10^{-4}
10^{-3}
I_B A

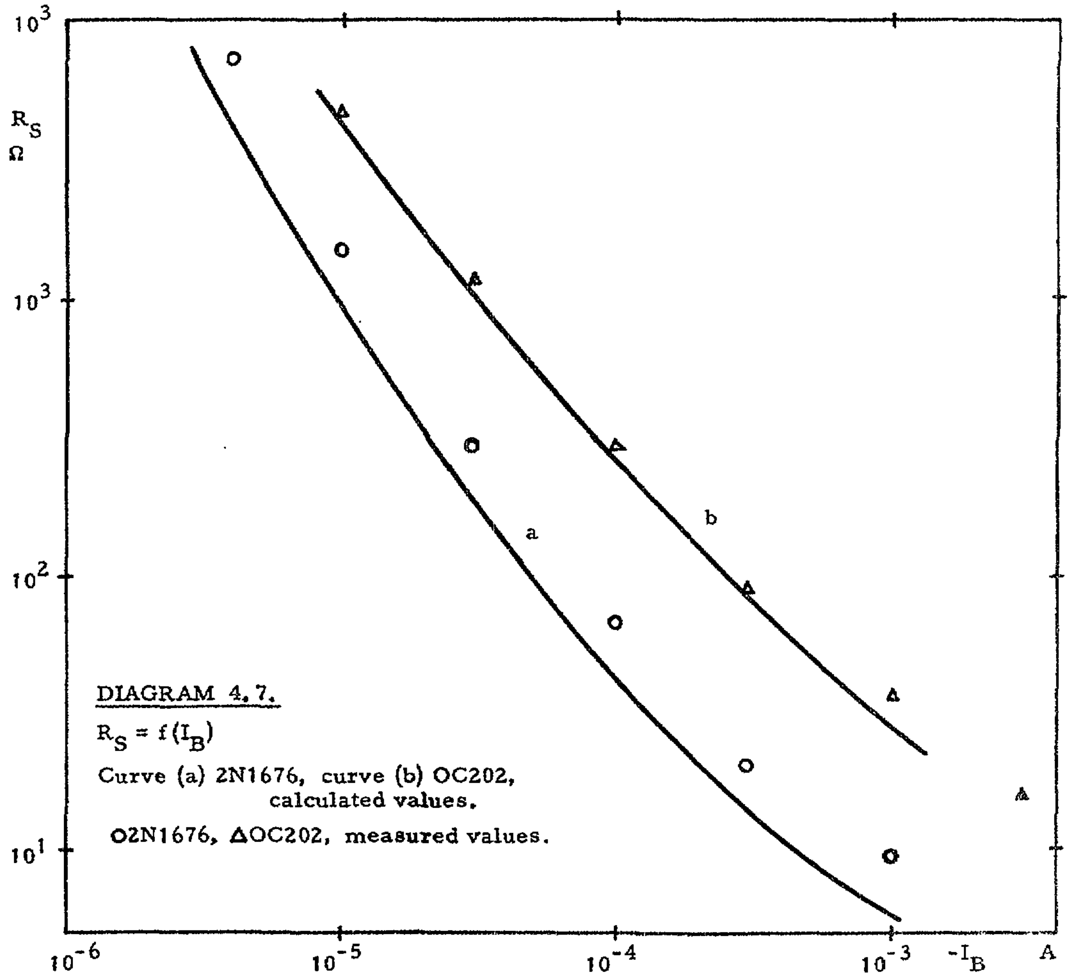


DIAGRAM 4.7.

$R_S = f(I_B)$

Curve (a) 2N1676, curve (b) OC202, calculated values.

O2N1676, ΔOC202, measured values.

DIAGRAM 5.1.

Switching spikes.

2N1613. I_B = 0,15 A. C_L = 60 pF.

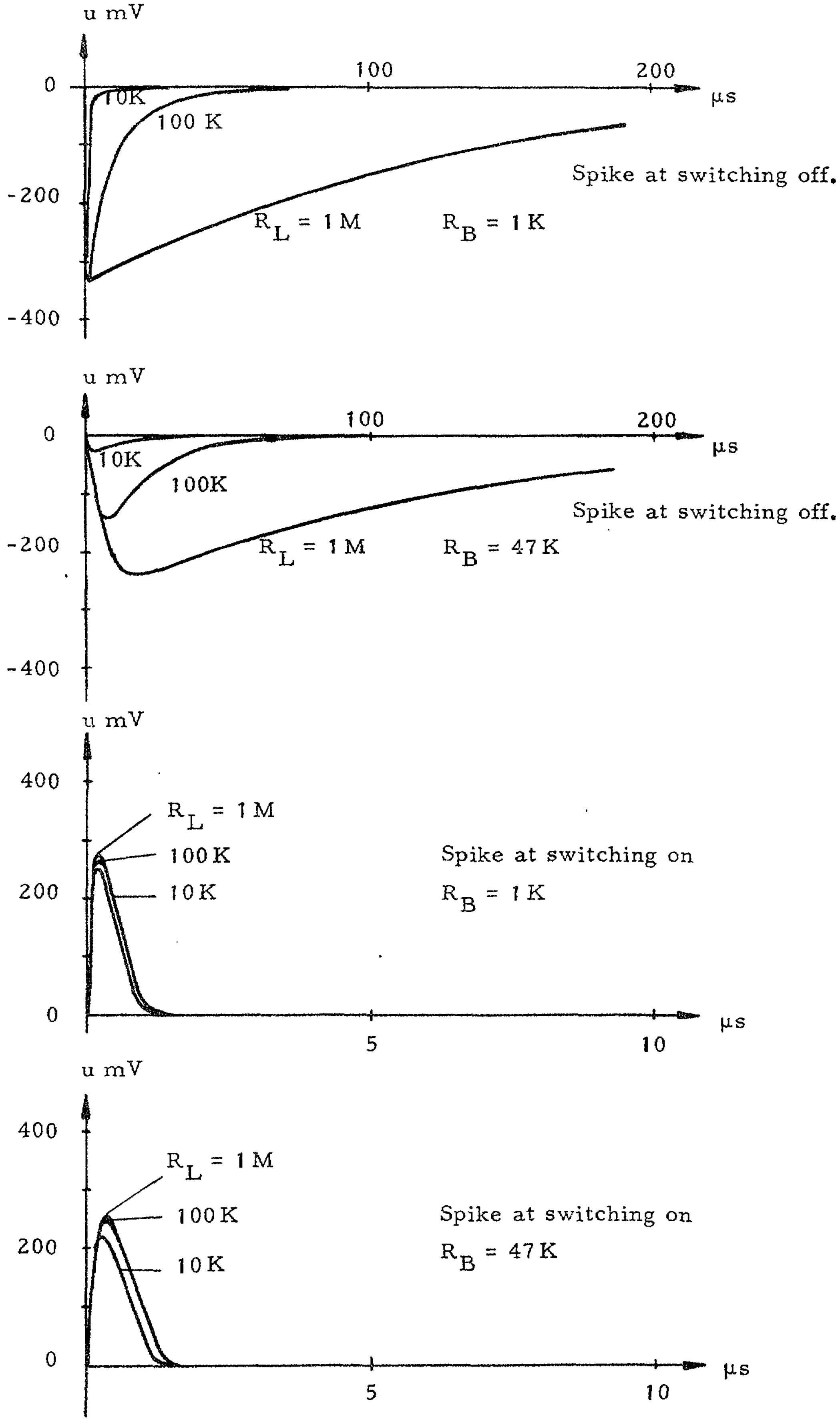


DIAGRAM 5.2.

2N2432

$u_E = f_1$ (time), $u = f_2$ (time)

R_L = 100 K, R_B = 47 K, C_L = 60 pF

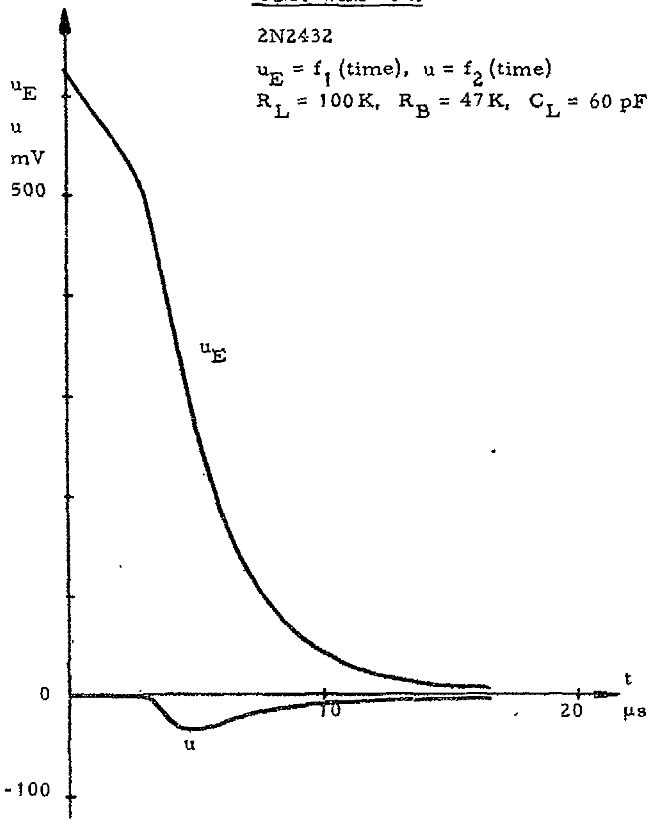


DIAGRAM 5.3.

2N2432

$U_{SPOFF} = f(C)$

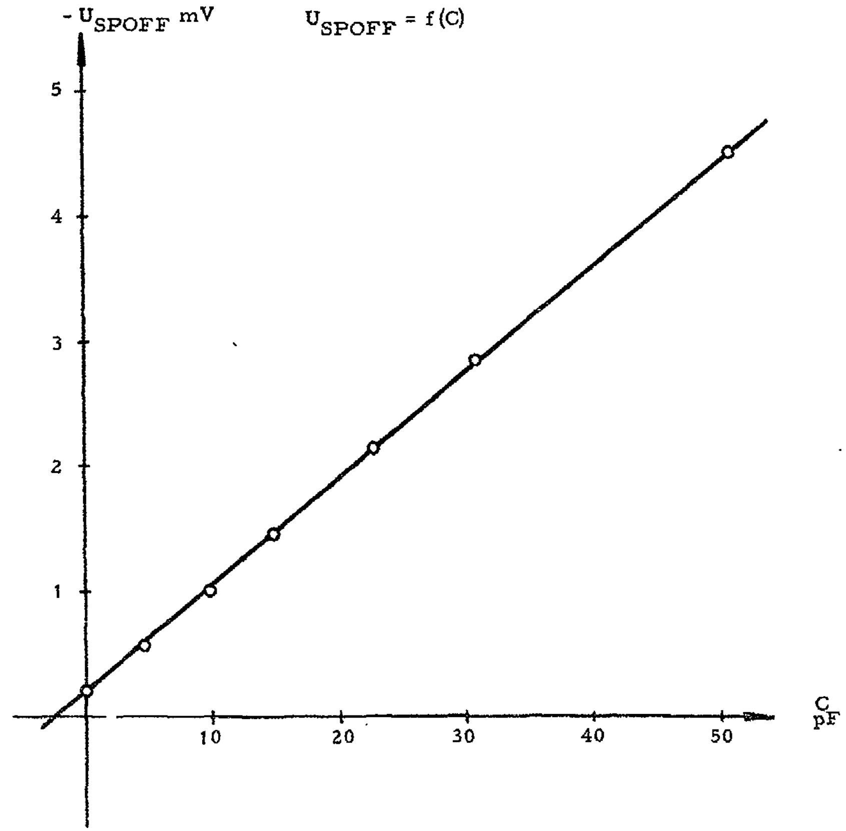
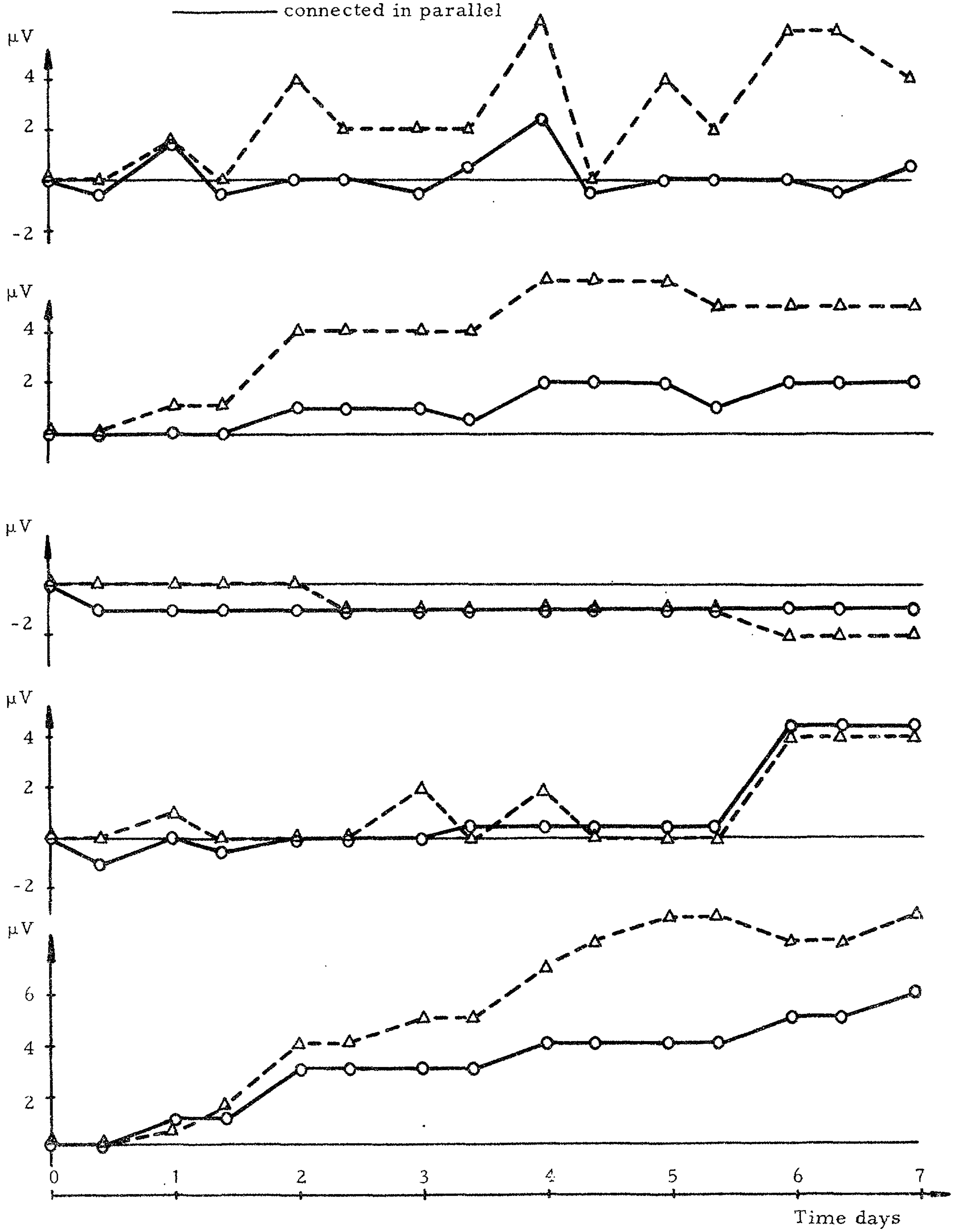


DIAGRAM 6.1.

The drift of 5 pairs of OC44 during 7 days.

- - - - - - connected in series

———— connected in parallel



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