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Institute of Energy Technology
Department of Electrical Energy Conversion

Bang & Olufsen A/S
CTV Technology
Research & Development

Minimization of the Power Losses in Televisions

Report No. 1

Leo Østergaard, Aalborg University/Bang & Olufsen A/S

March 1996

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Preface

This note describes the main results obtained in the first 7 months of the project "Minimization of the Power Losses in Televisions":

Title:	Minimization of the Power Losses in Televisions.
Period:	1/8, 1995 - 31/1, 1997.
Financing:	The Energy Ministry, Denmark, Bang & Olufsen A/S, and The Institute of Energy Technology, Aalborg University.
Management:	CETEC E/F.
Author:	Leo Østergaard.

According to the purpose, the project will contain the following subjects handled chronologically:

1. Initial phase	- get and read relevant literature, participate in SABER course.
2. Preliminary analysis	- construct, measure and simulate the simplified deflection/e.h.t. circuit.
3. Power losses	- measure the power losses and select critical components for analysis.
4. Modelling	- model the selected components and determine the model parameters.
5. Simulation/calculation	- simulate/calculate the power losses and the efficiency.
6. Final analysis	- compare simulations and measurements, propose improvements.
7. Final documentation	- complete the documentation of the project.

The first three subjects of the project have been carried out by the author while the rest of the project will be made by the person who takes over the project. This note, that covers the period 1/8, 1995 - 29/2, 1996, is then primarily minded for this person in order to give him the information necessary for a successful take-over of the project. Besides, the note is relevant for the constructors at Bang & Olufsen A/S and for other persons with interest in simulation of power electronics.

The initial phase will not be treated in a separate section due to its function as a kind of background to the other phases. It shall only be noted here that the information retrieval has been focused on the following subjects:

- Deflection/EHT circuits in general.
- Modelling power electronic components.
- Modelling transformers (high frequency/high voltage).
- Modelling magnetic materials.
- Modelling windings at high frequencies.

A reference list is given at the back of the note along with other supplements supporting the chapters.

I want to thank the employees working in the power electronic group at Bang & Olufsen A/S for their always positive attitude and willingness to answer questions in relation to the project and the production of televisions in general. This has also been the case at the Institute of Energy Technology, Aalborg University, where the knowledge of measuring, modelling, and simulating power electronic components has been a great help.

March 1996, Aalborg University

Leo Østergaard

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Content

1 Introduction

Since the first commercial TV-broadcasting in the late twenties the technology of televisions has developed rapidly. In recent years this has resulted in a growing use of digital technology in many parts of the television, but in relation to the control of the cathode ray tube (CRT) analog electronics and power components are still needed. This is due to the necessity of a high voltage supply (EHT) to the CRT and to the use of magnetic deflection and thereby the need of a high deflection current. The demands to this deflection/EHT circuit are increasing mainly because of a higher scan rate in the "future" television sets, where the newly developed television characterized as "the 100 Hz television" is an example. The higher scan rate results in increased power losses in the deflection/EHT circuit and thus an increased heating which is a serious problem in the construction of reliable products. In addition, the efficiency of the entire television sets is perceptibly increased by reducing the power losses in the deflection/EHT circuit.

To be able to deal with the above problems it is necessary to understand the factors affecting the power losses in the deflection/EHT circuit. This project will contribute to this understanding by analysing, calculating, and simulating the characteristic of the deflection/EHT circuit in use at B&O. The present knowledge of the issue at B&O is limited because the work in developing new televisions has never focused directly on the power losses. However, the power losses have always been a problem due to the heating of the components and solder points and in consequence the validity of the individual components and the entire deflection/EHT circuit. The constructors at B&O use their experience in the field to solve these problems more than systematically analysing the problem by calculations and simulations. In this way the used solutions are not necessarily the most optimal, and it is unknown whether other components or circuit topologies could be profitable in the minimization of the power losses. Because of this, the purpose of the project is to:

- ☞ *form the basis of a reduction of the power consumption in televisions by means of an increased level of knowledge.*
- ☞ *be able to increase the efficiency of the deflection/EHT circuit by no less than 10 percent of the overall power losses in the circuit.*
- ☞ *initiate the modelling of the components, carry out calculations/simulations, and evaluate the possibilities of creating new design tools for the constructors of televisions.*

1.1 The content of the report

This note covers the first part of the project whose purpose in general is to collect knowledge and information on the area and to map the power losses in the deflection/EHT circuit. In this way, the work documented in this note will make the basic for the future work in the project and point out where to concentrate the work in the minimization of the power losses.The note is divided into six chapters and the content of these is as follows:

Chapter 2, The basic deflection/EHT circuit

The overall mode of operation of the deflection/EHT circuit in use at B&O is described. According to the purpose of the project the deflection circuit is simplified and the resultant circuit is presented along with assumptions and arguments. In addition, the basic mode of operation of the simplified circuit is explained together with idealized equations.

Chapter 3, Measurements on the horizontal deflection/EHT circuit

A laboratory model of the simplified circuit is built and measurements of voltage and current waveforms are performed at different loads of the diode split transformer. The measurements are presented and comments are made on the shape of the waveforms.

Chapter 4, Simulation in SABER™

The simulation program SABER™ from Analogy® is used and the procedure of simulating the deflection/EHT circuit is explained. The most important facilities in SABER™ are highlighted and the used models of the individual components are shortly explained. The results of the simulations are presented and compared with the measurements.

Chapter 5, Mapping the power losses by measurements

The power losses in the simplified deflection/EHT circuit are measured for the individual components at different loads of the diode split transformer. From the measurements it is concluded which components to focus on when minimizing the overall power losses in the deflection/EHT circuit.

Chapter 6, Conclusion

Finally, some conclusions are made, and proposals and modifications for the future work are discussed.

2 The deflection/EHT circuit

A television set is a very complex device containing a large variety of engineering subjects from digital signal processing to power electronics and high voltage engineering. In Fig. 2.1 a very simplified diagram of a television set is shown where some of the main functions are illustrated by boxes.

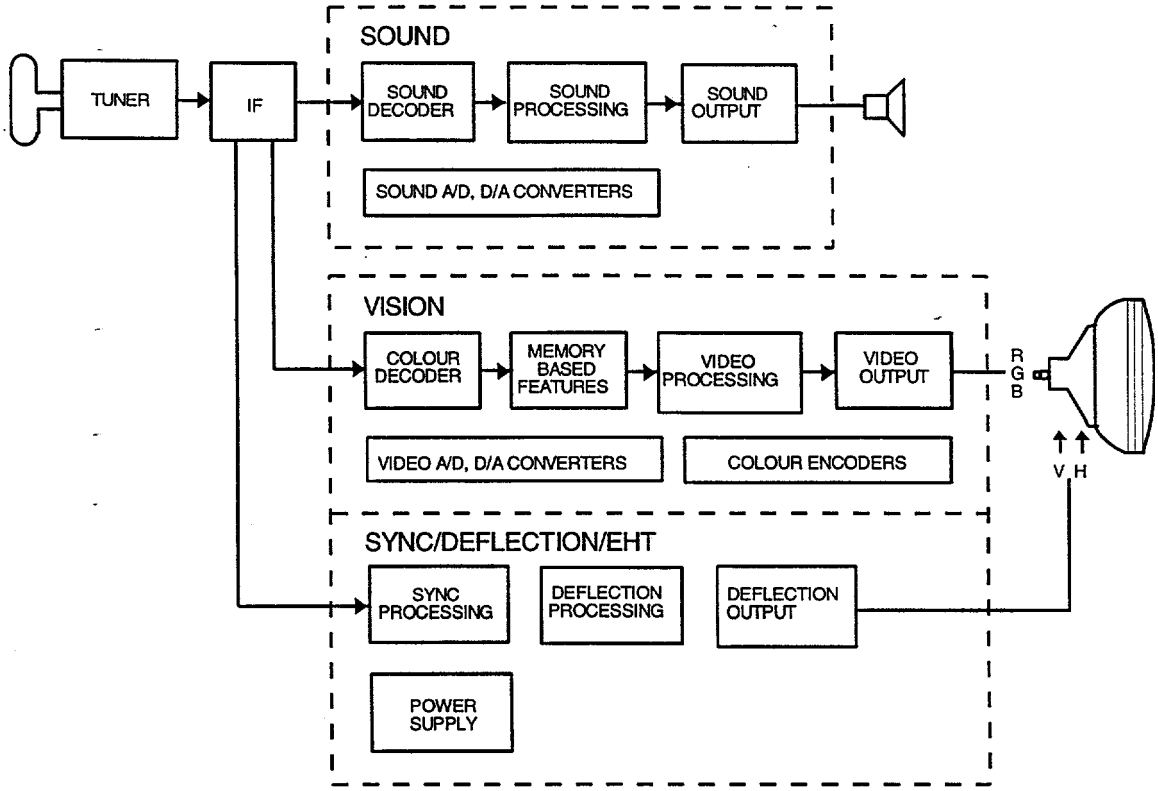


Fig. 2.1: *Partitioning of a television set where only the basic functions are shown /8/.*

It is not the scope of this report to explain the function of the entire television set, but it is to focus on the deflection/EHT circuit and the possibilities of minimizing the power consumption in this circuit. The deflection/EHT circuit is illustrated in the bottom part of Fig. 2.1 as the boxes "deflection output" and "power supply". The box "power supply" involves other supplies than the ones generated by the EHT generator, but these supplies will not be treated in this report.

This chapter introduces the deflection/EHT circuit in the television sets from B&O and it explains shortly its function in the television. Futher, a demarcation to a simplified deflection/EHT circuit is performed and the mode of operation of this circuit is explained.

2.1 The deflection/EHT circuit from B&O

The deflection/EHT circuit consists of the following parts:

- The horizontal deflection
- The vertical deflection
- The EHT generator
- Other supplies

The vertical deflection is of no particular importance as regards the overall power consumption due to the fact that the power losses are concentrated in the horizontal deflection circuit and the EHT generator. The vertical deflection circuit is therefore not treated in this report.

The circuit of interest is in this way the horizontal deflection circuit and the EHT generator that have to deliver the following properties:

- Horizontal deflection
- S-correction
- East/west modulation
- EHT
- Focus voltage
- Screen grid voltage
- Information for beam current limitation
- Flyback pulses
- Filament voltage for the picture tube
- Other TV supply voltages

A principal diagram of the horizontal deflection circuit and the EHT generator in use at B&O is shown in Fig. 2.2. A detailed circuit diagram of the deflection/EHT circuit in the 100 Hz television is shown in supplement 3.

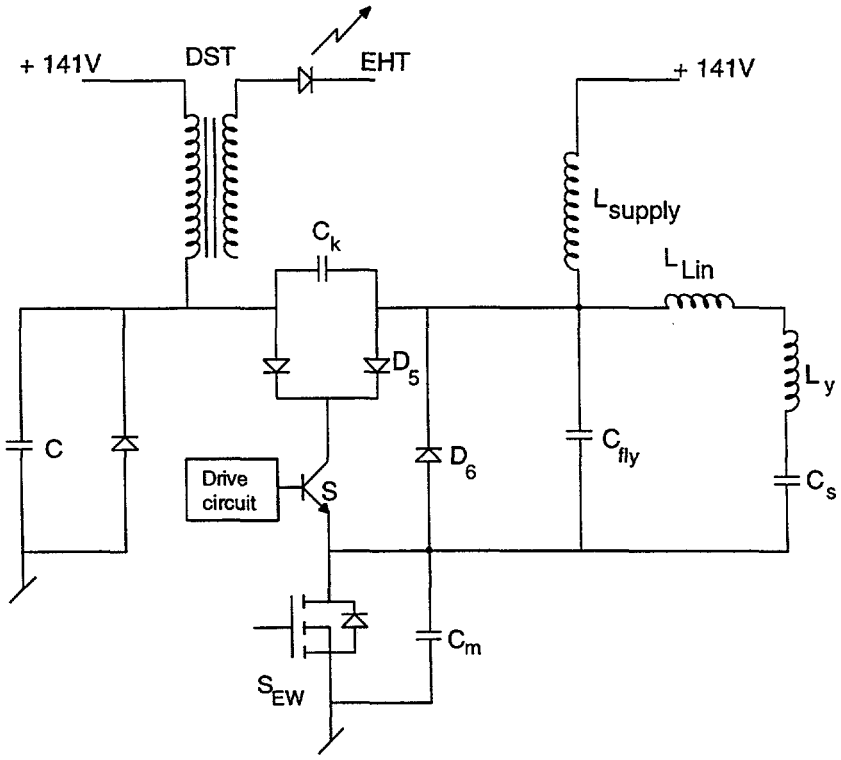


Fig. 2.2: *Principal diagram of the horizontal deflection circuit and the EHT generator in use at B&O.*

A detailed explanation of the mode of operation of the circuit in Fig. 2.2 is found in [5] so it shall only be stressed here that the circuit topology is used in order to partly separate the deflection circuit and the EHT generator. The two circuits are only connected by the capacitor C_k that has the function to transfer reactive power from the deflection circuit to the EHT generator. In this way the deflection circuit is affected by the generation of the EHT. The value of C_k is therefore mainly a compromise between the performance and the power losses, volume and price of the components in the EHT generator.

2.2 Demarcation to the simplified deflection/EHT circuit

In order to achieve a simple and a manageable circuit to analyse, the deflection/EHT circuit in Fig. 2.2 is simplified. The analysed circuit must be as simple as possible in order to be able to verify the models of the individual components and to investigate the interaction between the individual components. In the simplified deflection/EHT circuit the EHT generator and the horizontal deflection are fully coupled, and the east/west modulation and the linearity coil are among other facilities ignored. The result is the simplified deflection/EHT circuit shown in Fig. 2.3 with the current pump and the drive circuit shown in Fig. 2.4.

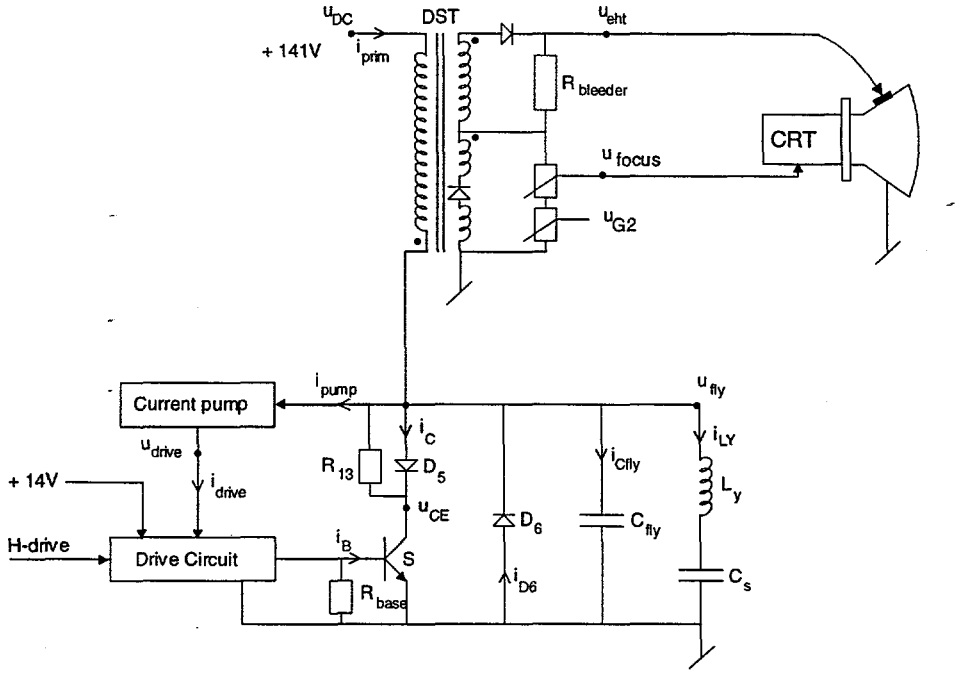


Fig. 2.3: *The simplified deflection/EHT circuit.*

The fact that the horizontal deflection and the EHT generator are fully coupled does not influence the basic mode of operation of the circuit. The EHT generator works as in the original circuit whereas the horizontal deflection is slightly changed concerning the amount of components. This results in a more significant interaction between the deflection circuit and the EHT generator and influences the performance of the picture on the CRT. The change in the deflection circuit is of no particular importance when the basic mode of operation is analysed and the power losses are measured. The overall power losses are of course not the same, but the critical components are still included in the simplified circuit, and it results in the characteristic shapes of the currents and the voltages.

2.2.1 The deflection circuit

By neglecting the east/west modulation, S_{EW} and C_m in Fig. 2.2, the deflection circuit always operates at the maximum supply voltage and therefore with the maximal width on the picture. This changes the power losses in the resulting deflection circuit and of course no power is consumed in the east/west modulation circuit. The influence on the power losses in the deflection/EHT circuit is not investigated, but as a simplification it is decided not to include the east/west circuit in the simplified circuit.

Another simplification is to neglect the linearity coil connected in series with the deflection coil. This coil corrects the picture distortion due to the voltage drop across the series resistance of the deflection coil: The voltage across the coil decreases as the beam scans the screen from left to right. Therefore, the beam travels more slowly towards the right side of the screen, and "equidistant vertical lines" are drawn closer together resulting in an asymmetric picture distortion. The function of the linearity coil is to correct for this distortion, as shown graphically in [9, pp. 4-7].

Since the linearity coil has a much lower inductance than the deflection coil, it does not have any influence of importance on the other current and the voltage waveforms in the circuit - except for the wanted corrections of the deflection current. The power losses in the linearity coil are obviously not included in the measurements of the power losses, but these can with some approximations be measured separately, if required.

The diode D_5 is inserted in series with the transistor as in the original circuit shown in Fig. 2.2. The only function of the diode in the simplified circuit is to prevent a negative current immediately after the flyback pulse caused by the forward recovery voltage of the power diode D_6. The forward recovery voltage results in a negative collector-emitter blocking voltage on the transistor with a value of approximately 40 V. A BJT cannot block this voltage because the B-E junction has a very low breakdown voltage due to the very heavy emitter doping used to increase the amplification of the transistor. The diode D_5 prevents the transistor to break down by blocking for any current. The resistor R_{13} is inserted in order to ensure that the collector-emitter voltage drops to zero between the flyback period and the turn-on of the transistor. If the resistor is not applied, the collector-emitter voltage remains high due to the internal collector-emitter capacitor C_{CE} in the transistor. Even though the energy in this capacitor is low, the resistor is inserted and results in a time constant of $R_{13} \cdot C_{CE}$. Besides, the resistor R_{13} ensures that the reverse voltage of the diode D_5 never exceeds its maximum rating, here 600 V.

2.2.2 The current pump and the drive circuit

The control of the transistor is very important in relation to the overall performance and especially the reliability of the deflection circuit, and the circuit used in the televisions from B&O is designed with special reference to minimize the power losses which is also called the current pump principle, see Fig. 2.4.

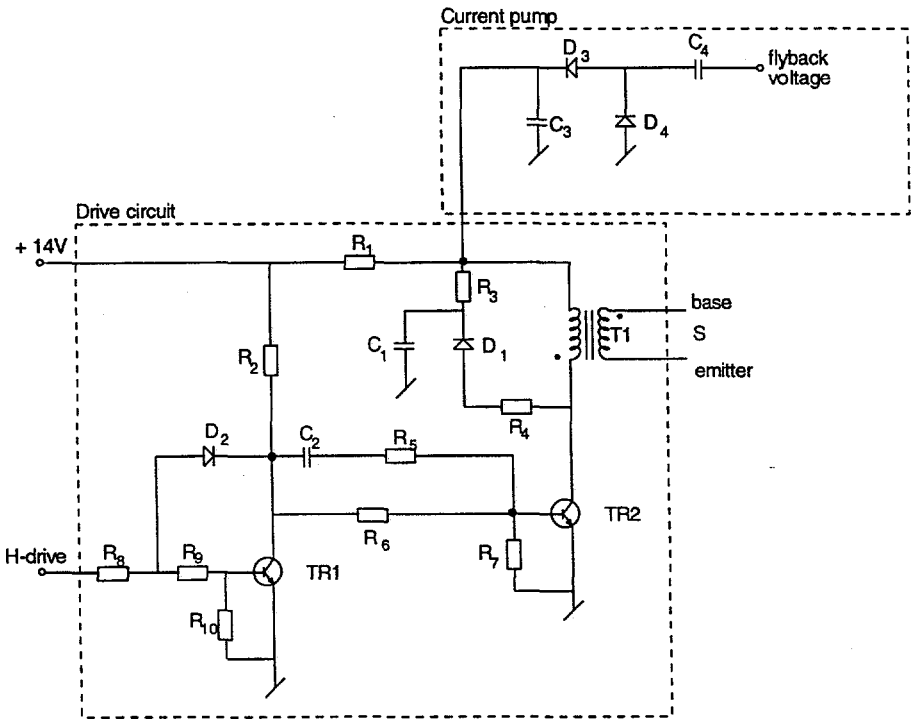


Fig. 2.4: *The current pump and the drive circuit used in the simplified deflection/EHT circuit.*

The drive circuit in Fig. 2.4 is less complex than the one in the television sets from B&O, but it still uses the same basic principle which results in a similar control of the transistor. The difference is that the facilities as slow start, slow turn-off, etc., are ignored. The control of these facilities is handled by

the control circuits in the chassis connected in parallel with the simplified deflection/EHT circuit which will be explained in chapter 3.

2.2.3 The EHT generator

The EHT generator consists of a flyback transformer with built-in diodes at the secondary as shown in Fig. 2.3. This kind of transformer is called a Diode Split Transformer, DST. Only two diodes are shown in Fig. 2.3 but the actual DST is divided into 10 sections separated by 8 diodes. This is done in order to split up the necessary blocking voltage of the diodes and to minimize the energy in the undesirable ringing that exists in the EHT winding due to the stray capacitances [7]. The DST in the simplified circuit has the same construction as the DST in the original circuit that is constructed with slot windings. The main function of the DST is to generate the EHT and the voltage to the focus on the CRT, as shown in Fig. 2.3. Besides, the DST works as a voltage supply to other circuits when the television works in the TV mode. Anyway, the DST in the simplified circuit generates only the EHT and the focus voltage because the other supplies are without importance in relation to the overall power delivered from the DST.

2.3 The fundamentals of the deflection/EHT circuit

This section explains the fundamentals of the simplified deflection/EHT circuit. This is done by a discussion of the operation of the circuit and by explaining how the circuit produces the characteristic deflection waveforms and the waveforms at the EHT generator. The discussion is based on idealized considerations whereas a discussion of measurements is placed in chapter 3.

2.3.1 The current pump and the drive circuit

A detailed explanation of the mode of operation of the current pump and the drive circuit exists in [6]. For that reason this section describes only the basic principle of the circuits in Fig. 2.4.

The current pump is supplied by the flyback voltage in the deflection circuit through the capacitor C_4 and the diodes D_3 and D_4. The achieved current I_{drive} is determined by the peak value of the flyback voltage $\hat{u}_{fly}$, the capacitor C_4 and the periodic time T in the deflection circuit:

$$I_{drive} = C_4 \frac{\hat{u}_{fly}}{T} \tag{2.1}$$

The capacitor C_3 retains the supply voltage to the drive circuit during a switching period without any ripple voltage of importance.

The drive circuit operates in a nonsimultaneous mode meaning that when the transistor TR2 turns on, the transistor in the deflection circuit turns off and vice versa. The transistor TR2 forces the base current through the transformer T1 that transforms the voltage down and the current up with a ratio of n_{T1}. The value of the base current is determined by the current from the current pump I_{drive}, the number of windings on the transformer n_{T1}, and the duty cycle δ of the transistor TR2:

$$I_B = n_{T1} \frac{I_{drive} - \frac{Q_s}{T}}{1 - \delta} \tag{2.2}$$

where Q_s is the charge, transformed to the primary of the transformer, that accounts for the negative base current during turn-off.

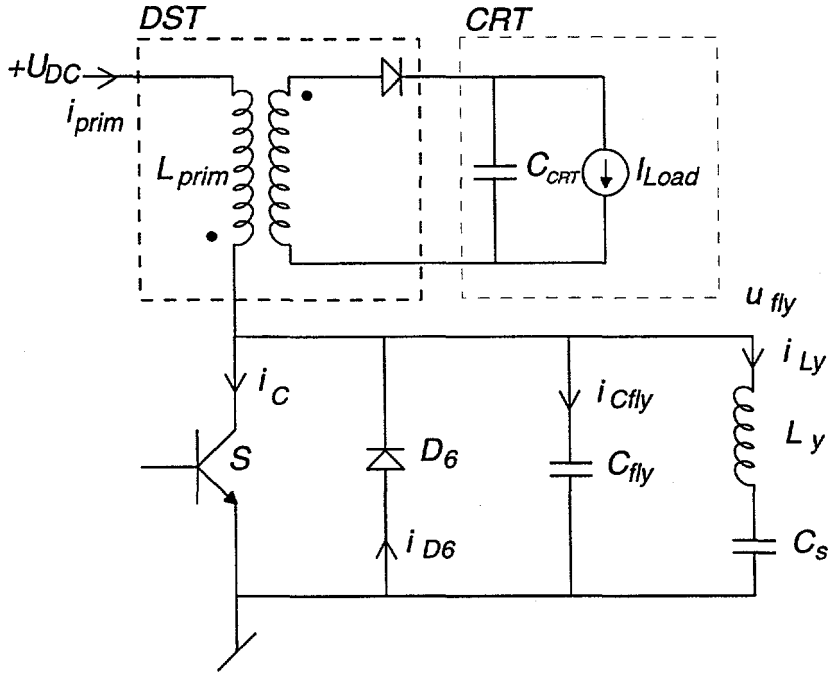
The transformer T1 is constructed with a stray inductance that gives the wanted slope of the base current when the transistor in the deflection circuit is turned off. In on-state the base current decreases only very little due to the large magnetization inductance in the transformer T1.

During the start-up of the circuit the voltage supply +14 V and the resistor R_1 supply a small current through the transformer T1 and the corresponding base current forces the transistor in the deflection circuit to turn-on. In this way flyback pulses are created and they start to supply the current pump. The power to the drive circuit is after the start-up no longer supplied through R_1 but only from the current pump.

It shall be stressed that the current pump influences especially the current in the flyback capacitor C_{fly} in the deflection circuit. This property will be treated in chapter 3 where measurements on the circuit are presented.

2.3.2 The deflection/EHT circuit

The simplified circuit in Fig. 2.5 is used to explain how the circuit produces the characteristic deflection waveform and the waveforms at the EHT generator, see Fig. 2.6 to Fig. 2.10. The operation of the circuit is explained by assuming ideal components etc. The values in the right of Fig. 2.5 are approximated values for the 100 Hz television from B&O.



U_{DC}	= 141 V
L_{prim}	= 1.1 mH
L_Y	= 307 µH
C_{fly}	= 10 nF
C_S	= 470 nF
C_{CRT}	= 2.9 nF
T	= 32 µs

Fig. 2.5: *A simplified diagram of the deflection/EHT circuit.*

It is seen that the diode D_5 and the resistor R_{13} are not included because they do not influence the basic mode of operation of the circuit. The cathode ray tube is illustrated as a parallel connection of a capacitor and a current generator. This is a simple and widely used model of the CRT where the capacitor C_{CRT} is the capacitor from the cathode to the aquadag coating of the CRT and the current generator symbolizes the mean value of the beam current, I_{Load}.

The transistor is turned on by applying a positive current to the base and the collector-emitter is held at ground potential. The voltage across the primary of the transformer is therefore constant at U_{DC} causing i_{prim} to rise linearly, see Fig. 2.9. The voltage across the deflection coil is not constant because the voltage on the capacitor C_s is modulated by the deflection current. When the transistor conducts and the current in L_Y is "negative", the voltage on C_s will drop as C_s discharges. This causes approximately a parabolic shape of the voltage on C_s due to the saw-toothed deflection current. The rise of the deflection current is therefore not linear but follows the wanted shape in order to compensate for picture distortions. This is shown in Fig. 2.7 and Fig. 2.8, respectively. Because of the S-capacitor, C_S, the deflection current i_{LY} has no DC component.

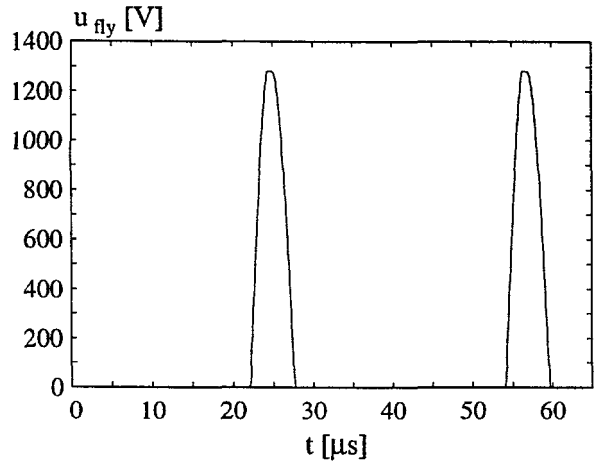


Fig. 2.6: *The flyback voltage u_{fly} at I_{Load} = 1 mA.*

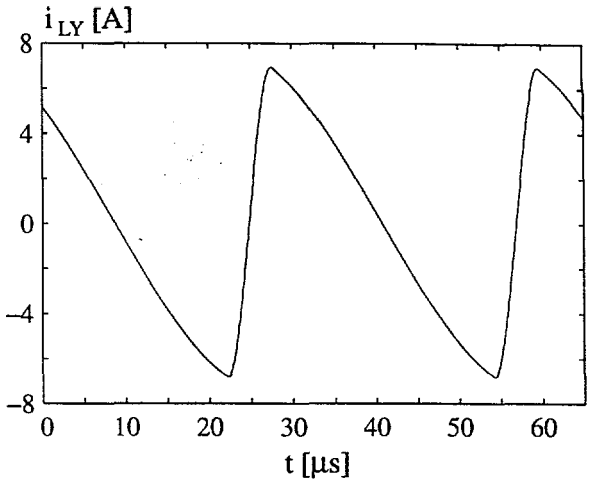


Fig. 2.7: *The deflection current i_{LY} at I_{Load} = 1 mA.*

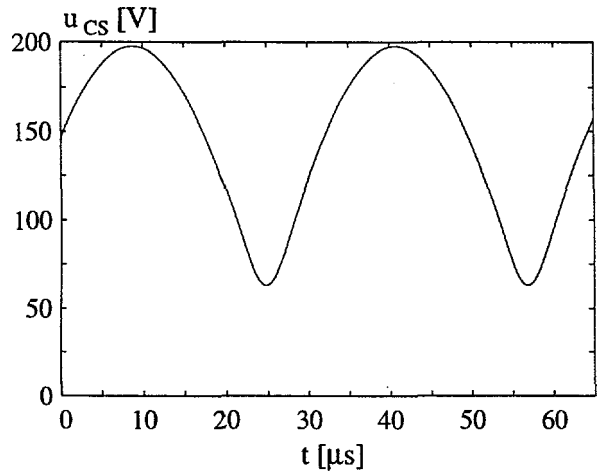


Fig. 2.8: *The voltage across the S-capacitor, u_{CS} at I_{Load} = 1 mA.*

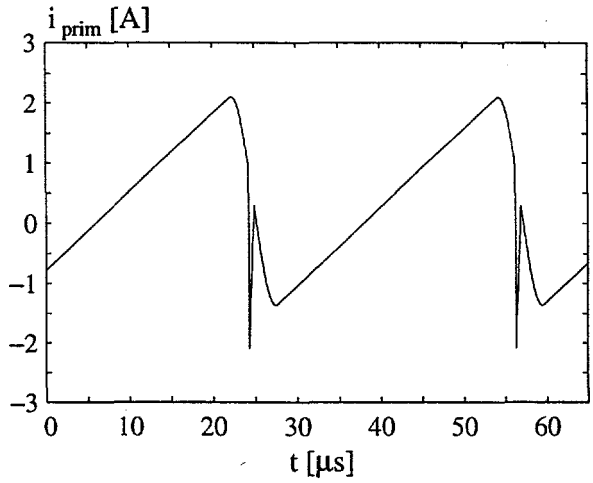


Fig. 2.9: *The primary current of the DST, i_{prim} at I_{Load} = 1 mA.*

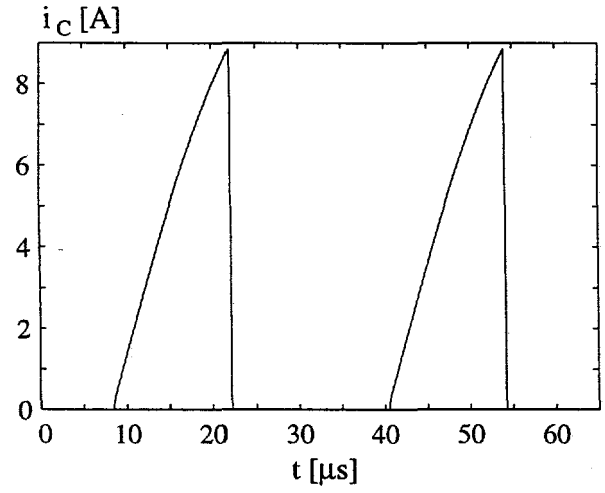


Fig. 2.10: *The collector current in the transistor, i_C at I_{Load} = 1 mA.*

By applying a negative current to the base, the transistor is turned off. Following the storage time of the transistor, the collector current will drop to zero. This is the initiation of the flyback. The turn-off of the transistor causes i_{prim} and i_{Ly} to flow into the flyback capacitor C_{fly}, and so the capacitor voltage

rises following a sine curve as i_{prim} falls and i_{Ly} rises, see Fig. 2.6. The time period of this sine curve is determined from the wellknown equation for a LC resonant circuit which results in a flyback time T_{fly} that is one half of the period time:

$$T_{fly} = \pi \sqrt{L_{yp} C_{sf}} ; \qquad L_{yp} = L_{prim} \| L_Y ; \qquad C_{sf} = \frac{C_s C_{fly}}{C_s + C_{fly}} \tag{2.3}$$

By assuming ideal components and that all the energy in the primary inductance and the deflection circuit is transferred to the capacitor, the peak value of the flyback voltage can be determined as:

$$\hat{u}_{fly} = U_{DC} \left(\frac{T - T_{fly}}{2} \right) \sqrt{\frac{1}{L_{yp} C_{sf}}} \tag{2.4}$$

When the voltage has risen sufficiently, the diode on the secondary of the DST conducts for a short period, and the current flows into the CRT. Because the DST is considered as an ideal transformer without any ringing, the secondary current is seen as a single spike in the primary current, Fig. 2.9. In addition the flyback voltage is flat at the top where the secondary diode conducts, Fig. 2.6. Power is in this way only delivered to the secondary at the top of the flyback voltage.

When all the energy in the primary of the DST and in the deflection coil has been transferred to the flyback capacitor C_{fly} and the secondary of the DST, the energy in C_{fly} will flow back to L_{prim} and L_Y. This resonance would continue, with the currents and voltages following sinusoidal parts, were it not for the diode, D_6. When the capacitor voltage starts to go negative, the diode D_6 becomes forward biased and clamps the capacitor voltage. This also clamps the voltage across the deflection coil L_Y to approximately the same value as it was when the transistor was conducting; the line voltage U_{DC} modulated by the capacitor C_s. This represents the end of flyback and the initiation of a new scan. The deflection current i_{LY} is now positive and decreasing and the current in the primary of the DST i_{prim} is negative and increasing, see Fig. 2.7 and Fig. 2.9, respectively. Before the sum of these currents passes through zero, the transistor is turned on, maintaining the path for the currents. They continue to flow until the transistor is turned off again to initiate a new flyback.

3 Measurements on the deflection/EHT circuit

In order to gain some experience in the field of horizontal deflection and the generation of EHT and to obtain measurements for later comparison with simulations, a laboratory model of the simplified circuit is built and measurements are made. The measurements are focused on the quasi stationary shape of the voltages and currents at a circuit level whereas more detailed measurements on the individual components in relation to the power losses are treated in chapter 5.

The chapter introduces the construction of the measuring system, the used instruments, and the methods of measuring the different signals. Afterwards measurements at three different loads of the diode split transformer are presented and comments are made on the shape of the waveforms.

3.1 The measuring system

The laboratory model of the simplified deflection/EHT circuit is connected in parallel to a 100 Hz television set from B&O. This connection is illustrated in Fig. 3.1.

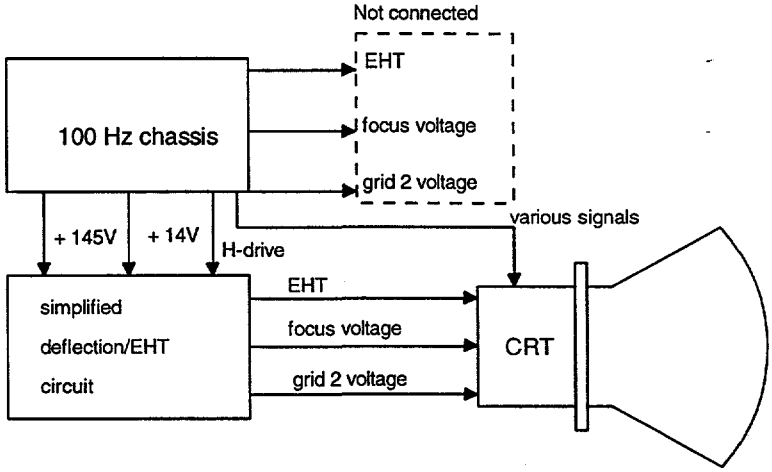


Fig. 3.1: *Diagram showing the parallel connection of the 100 Hz chassis and the simplified deflection/EHT circuit.*

The chassis supplies the simplified circuit with +145 V and +14 V and also the drive signal, H-drive, to the horizontal deflection transistor. The H-drive signal is controlled by a phase-locked loop, PLL, in the chassis. Thus, no control circuit is needed in the simplified deflection/EHT circuit. The output from the simplified circuit is the screen grid 2 voltage, the focus voltage, and the EHT to the CRT. These supplies are disconnected in the chassis and in that way the DST in the chassis is loaded only by the low voltage supplies that are used when the television is in the TV mode.

The above procedure demands two identical deflection coils: one placed on the CRT in order to deflect the beam, and one used in the simplified horizontal deflection circuit. The deflection coil on the CRT is supplied by the deflection circuit in the chassis while the simplified deflection circuit uses a seperate deflection coil.

3.1.1 The circuit diagram

The laboratory model of the simplified circuit is dimensioned in order to achieve shapes of the current and the voltage waveforms that are equivalent to the ones in the original deflection/EHT circuit. The components in the circuit are therefore, in so far as it is possible, identical to the ones used in the original circuit. The simplified circuit is shown in Fig. 3.2 where the signals to be measured are indicated.

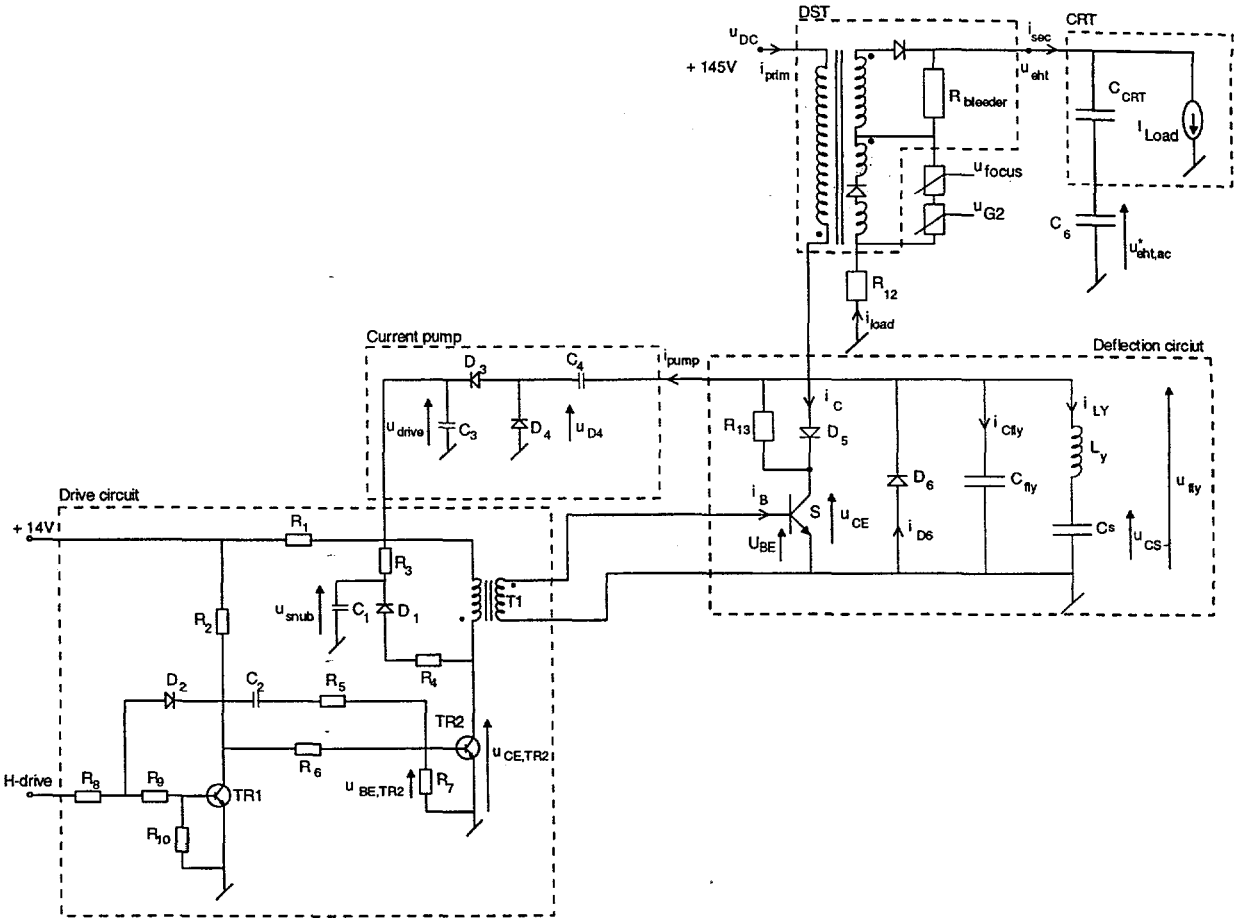


Fig. 3.2: *Diagram of the built laboratory model of the simplified deflection/EHT circuit. A diagram with the values of the components is given in supplement 4.*

A diagram of the circuit is also shown in supplement 4 where the values of the components are shown. The diagrams in Fig. 3.2 and in supplement 4 are used as references in the rest of the chapter.

3.1.2 The measuring instruments

The measurements of the voltage and the current waveforms are carried out by the following instruments:

Instrument	Type
Oscilloscope	Tektronix, TDS 744A (500 MHz, 2 GS/s)
Current probe amplifier	Tektronix, AM 503
Current probe	Tektronix, A6302
Voltage probe	Tektronix, P6139A (10x)
Voltage probe	Tektronix, P5100 (100x)
EHT probe (d.c.)	B&O (1000x)
Multimeter	Fluke, 8020B (connected to the EHT probe)
Multimeter	Fluke, 8060A (True RMS)
LF Impedance Analyzer	Hewlett Packard, HP 4192A (5 Hz - 13 MHz)

The purpose of the measurements is to obtain the voltage and the current waveforms in the deflection/EHT circuit. The measurements of these signals are primarily based on the digital storage oscilloscope and the current probe connected to the current probe amplifier. The oscilloscope has a horizontal resolution of 8 bit which may give waveforms where the resolution is visible. The only exception from this procedure is the measurement of the beam current I_{Load} which is measured as the voltage across the resistance R_{12}. The resistor $R_{12} = 1016\ \Omega$ is connected in parallel to a capacitor with a value of 2 µF resulting in a time constant of 2 ms. The voltage is measured with the multimeter Fluke 8060A.

Special attention should be paid to the voltage probe used to measure the EHT voltage. The probe has an internal impedance of approximately 1 GΩ and a maximum voltage of 30 kV_{DC}. The calibration of this "home-made" probe is very difficult for which reason the accuracy is unknown. A further discussion of the EHT probe is made in chapter 5, section 5.1.1.

3.2 Results

The measurements on the simplified deflection/EHT circuit are carried out at three different loads of the DST:

1) The beam current to the picture tube, $I_{Load} = 0$ mA
2) The beam current to the picture tube, $I_{Load} = 1$ mA
3) The beam current to the picture tube, $I_{Load} = 2$ mA

It shall be pointed out that I_{Load} is the mean values of the beam current and that a current limiter in the chassis is set to 1.8 mA. This current limiter is not installed in the simplified deflection/EHT circuit for which reason it is possible to overload the circuit at $I_{Load} = 2$ mA.

All the different waveforms are not measured silmultaneously due to the limitations in the amount of channels in the used digital storage oscilloscope. In consequence of this, one of the four channels in the oscilloscope has been used to measure a reference signal in order to be able to make the same time scale for all the measurements. The reference signal is the H-drive signal. By use of this method it is possible to compare the measured voltage and the current waveforms.

The presentation of the measurements is divided into four categories where the first is related to the drive circuit, the next to the horizontal deflection transistor, the third to the horizontal deflection circuit, and the last to the generation of the EHT. The most relevant current and voltage waveforms in relation to these categories are presentated at a load current of $I_{Load} = 1$ mA, and a comparison of the waveforms at the three different load currents is presented with the exception of the waveforms in the drive circuit.

3.2.1 Measurements on the drive circuit and the current pump

The drive circuit and the current pump consist of a lot of components, and it does not serve the purpose of the project to measure the current and the voltage waveforms for each of these components. The most important waveforms for showing the mode of operation of the circuits are picked out and the result of the measurements is shown in Fig. 3.3.

The first time in Fig. 3.3 where the transistor, TR2, turns on is at approximately 20 µs. The transistor in the deflection circuit begins subsequently to turn off and the charge is forced out of the base of the transistor. This is seen as a voltage overshot in the base-emitter voltage of the transistor TR2, Fig. 3.3 (a). The voltage overshoot in $u_{BE.TR2}$ results consequently from the negative base current in the deflection transistor that is transformed to the primary of the transformer T1 and is added to the magnetizing current in the transformer. This extra current in the transformer T1 leads to a drop in the voltage to the drive circuit, Fig. 3.3 (d).

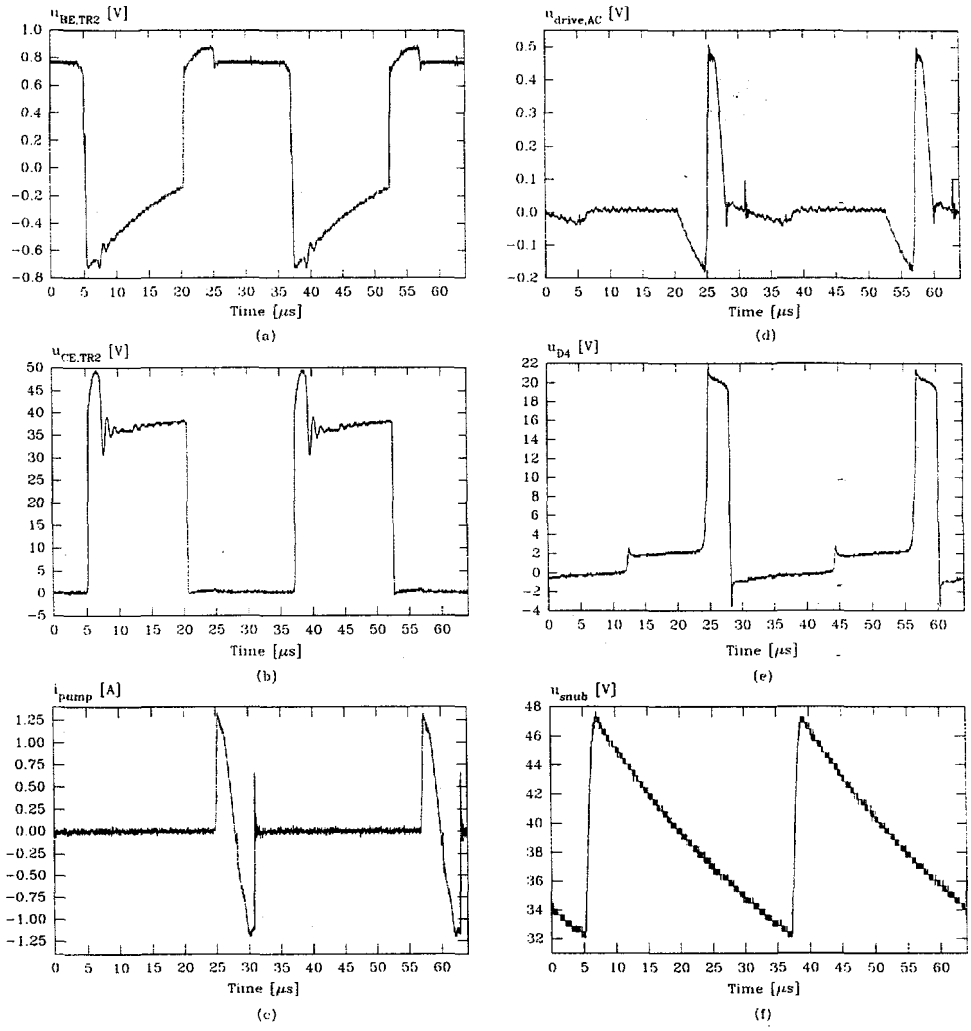


Fig. 3.3: *The voltage and the current waveforms in the drive circuit at I_{Load} = 1 mA. (a) the base-emitter voltage for the transistor, TR2, (b) the collector-emitter voltage for the transistor, TR2, (c) the current to the current pump, (d) the a.c. content of the voltage to the drive circuit where the d.c. content is approximately 19.7 V, (e) the voltage across the diode, D_4, (f) the voltage across the snubber capacitor, C_1.*

When the charge in the base of the deflection transistor is removed, the transistor is turned off and the flyback pulse in the deflection circuit arises. Current is then fed into the capacitor C_4 in the current pump as seen in Fig. 3.3 (c). The voltage across D_4 rises to the d.c. level of the voltage to the drive circuit U_{drive} plus the voltage drop of the diode D_3, and as the current to the current pump decreases the voltage drop of D_3 decreases similarly, see Fig. 3.3 (e). In this interval the voltage to the drive circuit increases due to the energy supplied to the capacitor C_3.

When the flyback pulse has reached its peak value, the current to the current pump changes polarity, Fig. 3.3 (c), and the voltage across D_4 is negative because D_4 conducts instead of D_3. In order to turn on the deflection transistor, the transistor TR2 is turned off at approximately 37 μs. This causes an overshoot in $u_{CE,TR2}$ because of the stray inductance in the transformer T1, Fig. 3.3 (b). This overshoot is controlled by the snubber configuration and the voltage across the snubber capacitor C_1 rises as seen in Fig. 3.3 (f). The deflection transistor does not conduct before the sum of the deflection current and the primary current in the DST is zero which is at approximately 45 μs, see Fig. 3.3 (e).

3.2.2 Measurements on the deflection transistor

The switching process that takes place within the transistor shows itself indirectly in the measurements shown in Fig. 3.4. Anyway, it is not the scope to explain the switching process in details, so in order to achieve the fundamental knowledge of the high voltage bipolar transistor, it is recommended to study the detailed treatment of the subject given in [10].

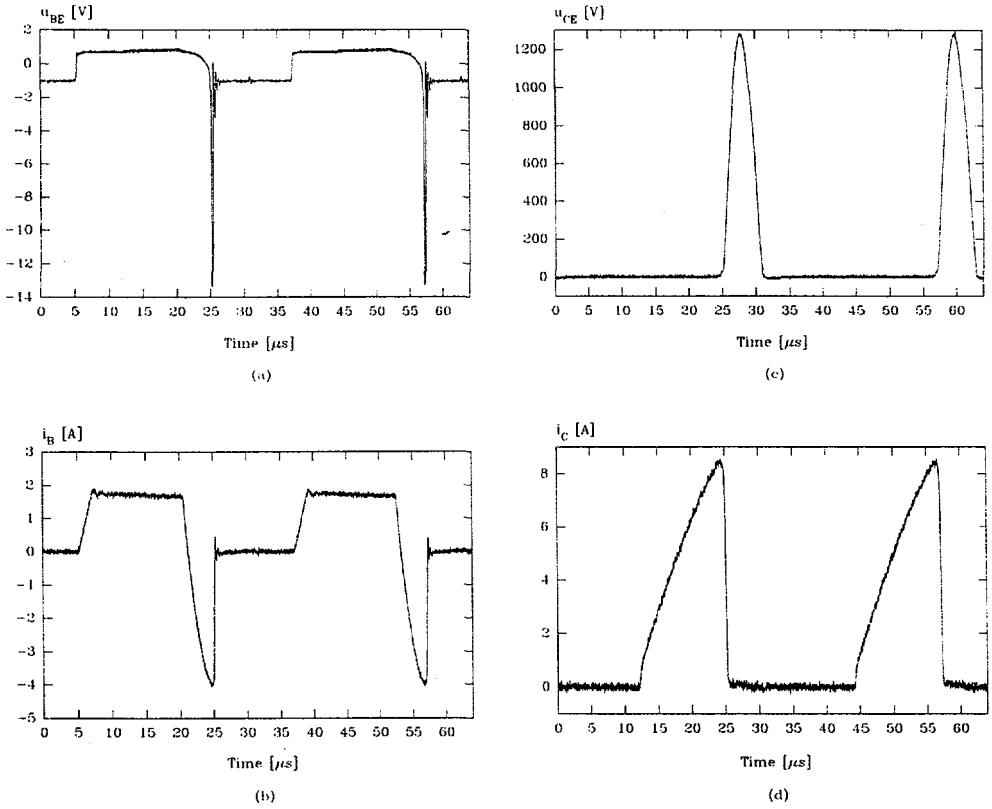


Fig. 3.4: *The voltage and the current waveforms of the deflection transistor at I_{Load} = 1 mA. (a) the base-emitter voltage, (b) The base current, (c) the collector-emitter voltage, (d) the collector current.*

The turn-on signal to the transistor is the first time, in Fig. 3.4, applied at approximately 5 μs. The base-emitter voltage rises to the on-state voltage, Fig. 3.4 (a), and charge is supplied to the base resulting in a base current, Fig. 3.4 (b). The transistor is in the on-state, but no collector current is present due to the fact that the diode D_6 conducts the deflection current i_{LY}. The collector-emitter voltage, shown in Fig. 3.4 (c), is therefore negative according to the on-state voltage drop of the diode D_6. The power losses during turn-on can in this way be neglected which is a very good quality of the deflection circuit.

At approximately 12 μs the transistor starts to conduct the deflection current and the primary current in the DST. The first part of the collector current has a bigger slope than the rest of the time until the turn-off of the transistor, Fig. 3.4 (d). This increased slope is mainly due to the reverse recovery phenomena in the diode D_6. The explanation of the phenomena is as follows: When the sum of the primary current in the DST and the deflection current becomes zero, the diode D_6 turns off and the current i_{D6} starts to go negative due to the removal of the charge in the power diode D_6. The collector

current in the transistor is still zero and remains zero until the peak negative value of i_{D6} where the reverse recovery begins. Because the current in D_6 during the reverse recovery decreases rather fast and because the sum of the primary current in the DST and the deflection current still increases, the collector current has a bigger slope until the reverse recovery is finished. During the on-state of the transistor the base current decreases a little due to the demagnetization of the magnetization inductance in the driver transformer T1.

The turn-off of the transistor starts at approximately 20 µs. At turn-off the charges in the transistor are removed in an active way by applying a negative base current which pulls the charges out of the transistor. The slope of the negative base current, Fig. 3.4 (b), is determined by the stray inductance in the drive transformer T1 and is a very important factor when designing the drive circuit in order to minimize the turn-off power losses. The first decrease in the base-emitter voltage is due to the increase in the internal base resistance during the extraction of the charge. The second decrease, that results in a negative peak value of - 13 V, is primarily caused by the stray inductance in the drive transformer T1.

The stray inductance in T1 and the wiring inductances in the base and the emitter leads cause ringing on the base-emitter voltage, see Fig. 3.4 (a). In order to have a greater safety margin and to avoid spurious turn-on, the ringing could be reduced by a base-emitter damping resistor.

The voltage and the current waveforms of the deflection transistor at I_{Load} = 0 mA, I_{Load} = 1 mA, and I_{Load} = 2 mA are shown in Fig. 3.5.

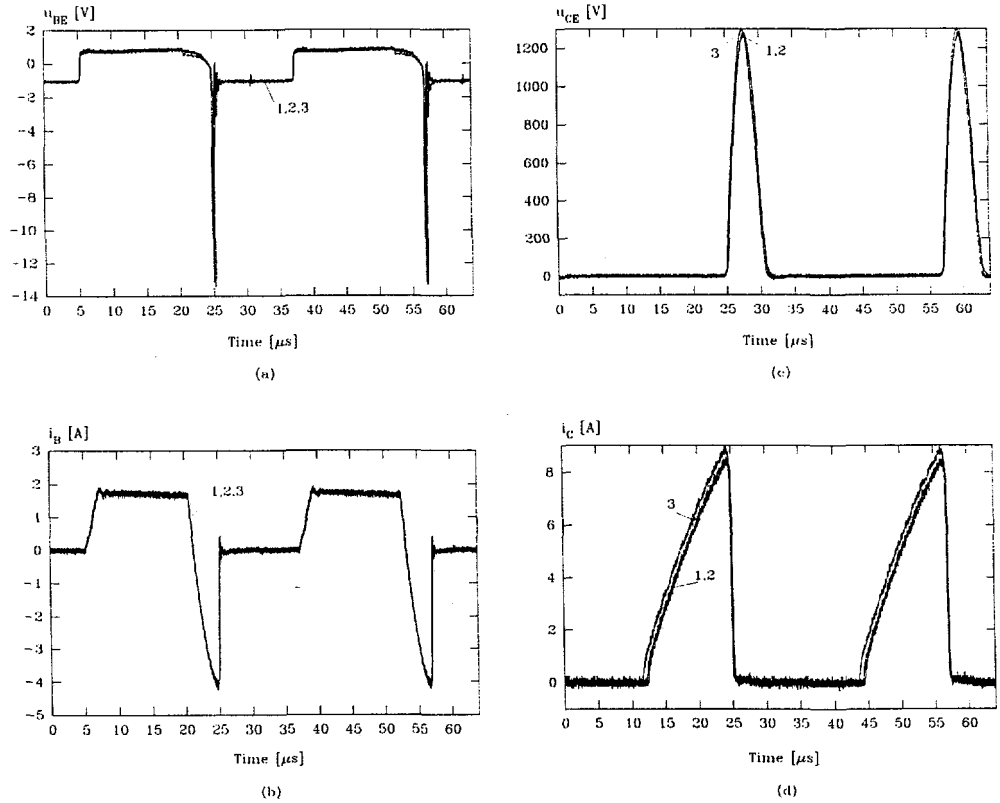


Fig. 3.5: *The voltage and the current waveforms of the deflection transistor at 1: I_{Load} = 0 mA, 2: I_{Load} = 1 mA, and 3: I_{Load} = 2 mA. (a) the base-emitter voltages, (b) the base currents, (c) the collector-emitter voltages, (d) the collector currents.*

At a higher load of the DST the DC component of the current in the primary of the DST increases and is fed through the transistor because the S-capacitor C_S blocks for any DC component. This is clearly seen in Fig. 3.5 (d) even though no significant difference is visible for $I_{Load} = 0$ mA and $I_{Load} = 1$ mA. It is further seen that the collector current starts to flow earlier, the higher the load current. The explanation is that the sum of the primary current in the DST and the deflection current becomes zero earlier, the higher the load current, and thus, the transistor has to conduct earlier. No significant difference is visible in the three waveforms for the base-emitter voltage and the base current.

The high current in the DST results in a higher energy in the primary inductance of the DST. During the flyback this energy is transferred to the flyback capacitor C_{fly} resulting in a higher flyback voltage, Fig. 3.5 (c).

3.2.3 Measurements on the deflection circuit

The deflection circuit has two functions; to deliver the deflection current and to generate the flyback voltage to the DST. In Fig. 3.6 some of the waveforms in the deflection circuit are shown.

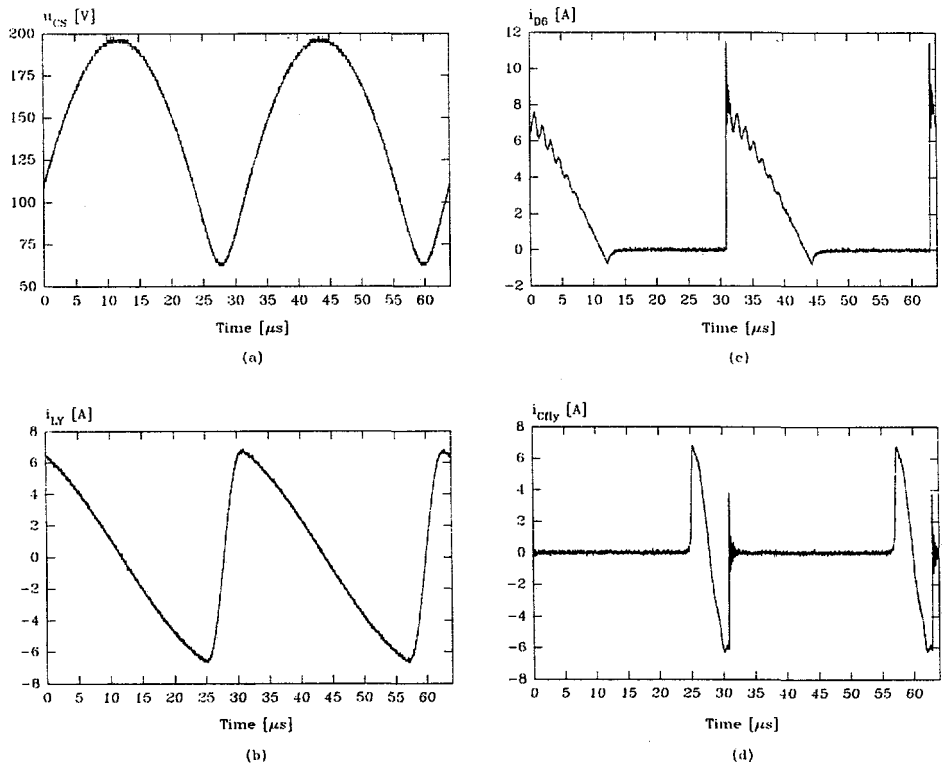


Fig. 3.6*: The voltage and the current waveforms in the deflection circit at I_{Load} = 1 mA. (a) the voltage across the S-capacitor, C_S, (b) the deflection current, (c) the current through the diode, D_6, (d) the current through the flyback capacitor C_{fly}.*

The voltage across the S-capacitor in Fig. 3.6 (a) has the characteristic shape like a parabola and the deflection current in Fig. 3.6 (b) has the S-shape as mentioned in chapter 2. Thus, the waveforms are the result of a mutual influence of the deflection coil and the S-capacitor.

The current through the diode D_6 is shown in Fig. 3.6 (c). At approximately 12 µs the reverse recovery current is visible and reaches a minimum value of -0.8 A. The diode conducts again after the flyback at approximately 31 µs where the diode shall begin to conduct the peak value of the positive deflection current. At the end of the flyback high frequency ringing exists between the flyback capacitor C_{fly} and the diode D_6. The frequency of the ringing is approximately 5 MHz and it might be a problem due to electromagnetic interference (EMI). The ringing, that follows these high frequency ringing within the MHz range, has a frequency of approximately 770 kHz. This ringing is caused by the stray capacitance and inductance of the DST. During the construction of the DST the frequency of the ringing is controlled in order to achieve a frequency of the 9th or 11th harmonic of the flyback pulse. The advantage of doing this is that the top of the transferred flyback pulse to the secondary of the DST is more flat. This results in a smaller secondary peak current and thus, less power loss and a smaller internal resistance in the DST.

At the beginning of the flyback the current through the flyback capacitor shall take over the current in the transistor with the exception of the current to the current pump. The current through the flyback capacitor in Fig. 3.6 (d) has a peak value of approximately 7 A while the current through the transistor is approximately 8.3 A at the beginning of the flyback. Thus, the remaining current is supplied to the current pump, see Fig. 3.3 (c).

In Fig. 3.7 the voltage and the current waveforms in the deflection circuit at the three load currents are shown.

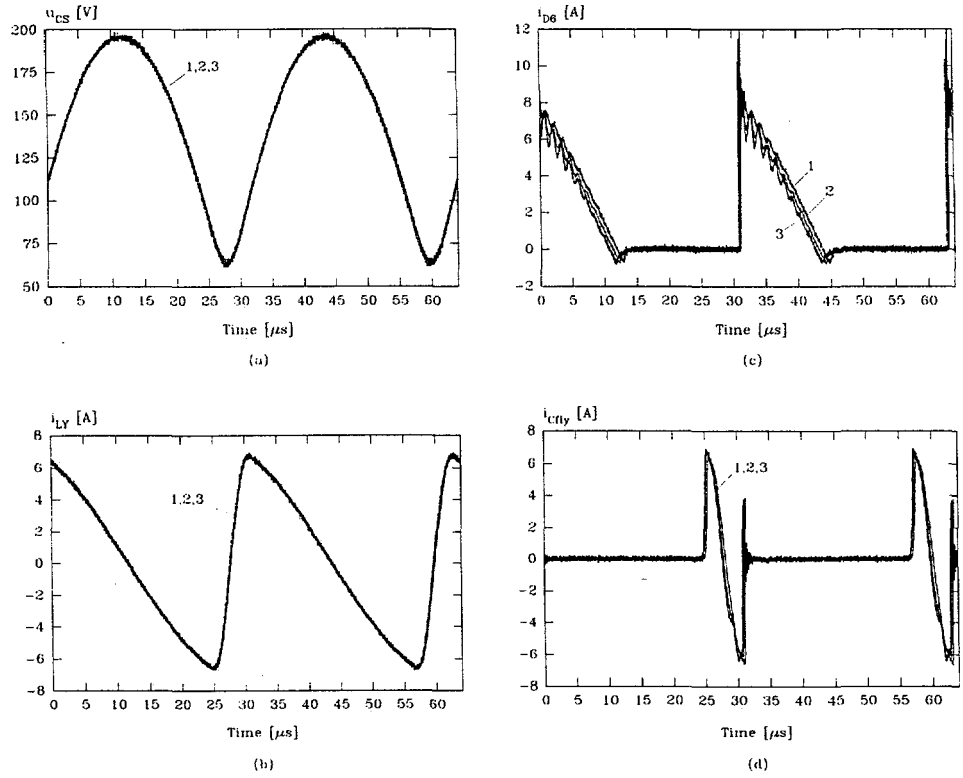


Fig. 3.7: *The voltage and the current waveforms in the deflection circuit at 1: I_{Load} = 0 mA, 2: I_{Load} = 1 mA, and 3: I_{Load} = 2 mA. (a) the voltage across the S-capacitor, C_S, (b) the deflection current, (c) the current through the diode, D_6, (d) the current through the flyback capacitor C_{fly}.*

It is only in Fig. 3.7 (c) that a distinct change in the waveforms is seen as a function of the load current, I_{Load}. At a first glance it seems remarkable that the current through the diode D_6 is smaller at a higher I_{Load}, but the explanation is very simple: At a higher load current the d.c. component of the primary current in the DST increases. Because the current through D_6 is given as the difference between the primary current and the deflection current, the current through D_6 decreases as the load current increases.

3.2.4 Measurements on the diode split transformer

The DST transforms the flyback voltage to the secondary in order to deliver power to the CRT. The most relevant waveforms are shown in Fig. 3.8.

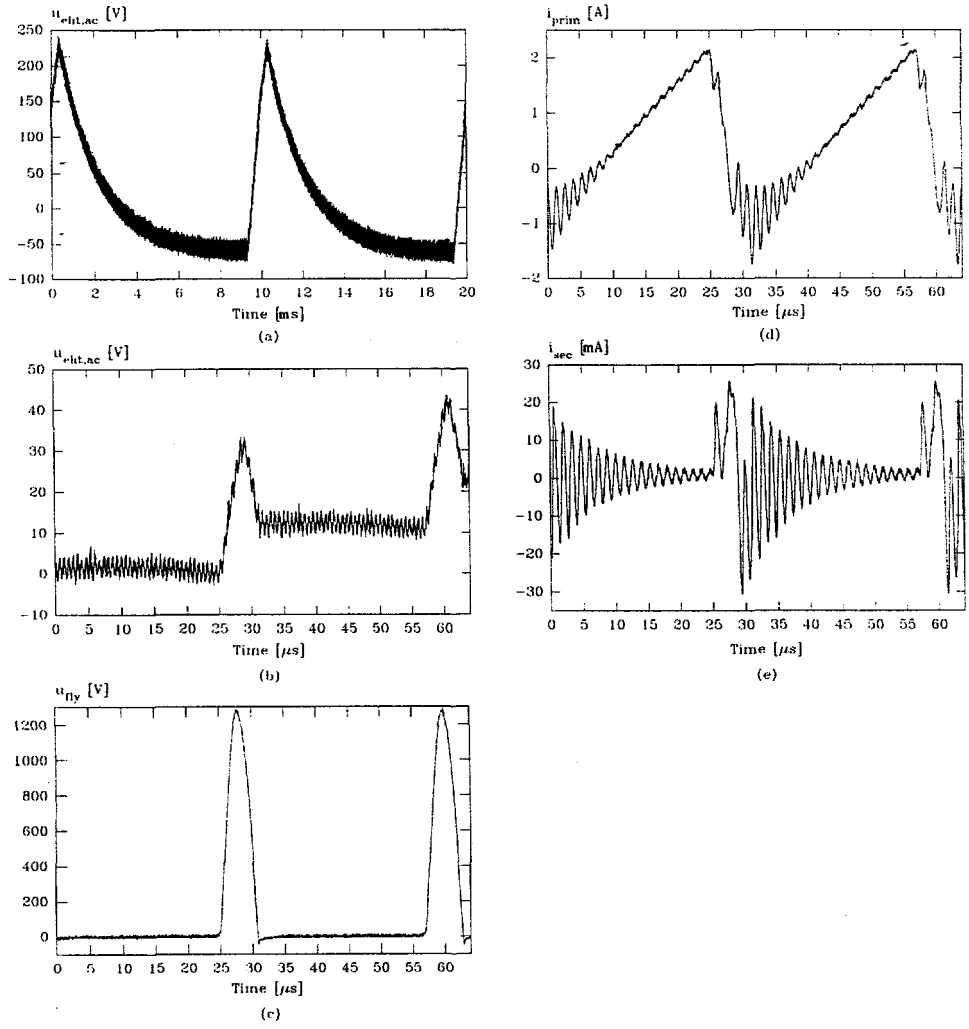


Fig. 3.8: *The voltage and the current waveforms in the diode split transformer, DST, at I_{Load} = 1 mA. (a) the a.c. content of the EHT, (b) the a.c. content of the EHT, (c) the flyback voltage, (d) the primary current, (e) the secondary current.*

The flyback voltage in Fig. 3.8 (c) is almost identical to the collector-emitter voltage of the transistor with the exception of the voltage drop across the diode D_5. At the end of the flyback the flyback voltage goes negative due to the forward recovery voltage of the diode D_6. This voltage is not seen on the collector-emitter voltage because the voltage is placed across the diode, D_5.

The d.c. value of the EHT is measured to U_{EHT} = 28.6 kV and the a.c. content is shown in Fig. 3.8 (a) and in Fig. 3.8 (b). The a.c. content of the EHT is measured by the capacitive voltage divider consisting of the capacitor from the cathode to the aquadag coating of the CRT, C_{CRT}, and the capacitor C_6. The waveform in Fig. 3.8 (a) is measured in a time interval of 20 ms corresponding to two half images on the CRT (in the ABAB system it is the A and the B frame. In a 100 Hz television both the A and the B frame are sent twice to the screen in every 40 ms). Immediately after the EHT has reached its peak value at approximately 0.5 ms, the creation of a new half image is started, here called the A frame. The EHT decreases during the vertical scan and increases during the vertical flyback. At 10.5 ms the creation of the B frame is started and the shape of the EHT is identical to the one during the creation of the A frame.

During the vertical scan the voltage across the capacitor C_{CRT} decreased according to the load current I_{Load} even though the DST supplies the secondary in every horizontal flyback period, see Fig. 3.8 (b). The duration of the vertical flyback is 0.8 ms and is determined by the number of active line scans and the number of lines during the vertical flyback. The total number of lines is 625 of which 575 are used as active lines. The result is that 8 percent of the total vertical scan period is spend on the vertical flyback corresponding to 0.8 ms.

The primary current in Fig. 3.8 (d) is maximum at approximately 25 μs where the flyback pulse begins. The energy in the primary of the DST is then transferred to the flyback capacitor C_{fly} resulting in the high negative slope on the primary current. During the flyback the DST delivers power to the secondary. This is seen in the secondary as two positive pulses, Fig. 3.8 (e), and as notches in the primary current, Fig. 3.8 (d). If the DST was ideal, the current to the secondary would be delivered as a single pulse at the top of the flyback voltage, but due to the tuning of the DST this is not the case. The primary current goes negative during the last part of the flyback, and the energy in the primary inductance L_{prim}, resulting from this negative current is moved before the primary current becomes positive after the flyback. The ringing in the DST is large immediately after the flyback due to the energy that where built up during the transfer of energy to the secondary, in the stray capacitances and inductances in the DST. When the transistor conducts again, the ringing is reduced considerably and the primary current increases in relation to the primary inductance and the supply voltage.

In Fig. 3.9 the voltage and current waveforms are shown for the three load currents. The ripple in the EHT is of course higher, the higher the load current, and at no load only the a.c. content due to the flyback voltage is present. The d.c. content of the primary current increases as the load current increases which is also the case for the secondary current pulses during the flyback period. The amplitude of the ringing increases too because more energy is present due to the higher energy that is transferred through the DST.

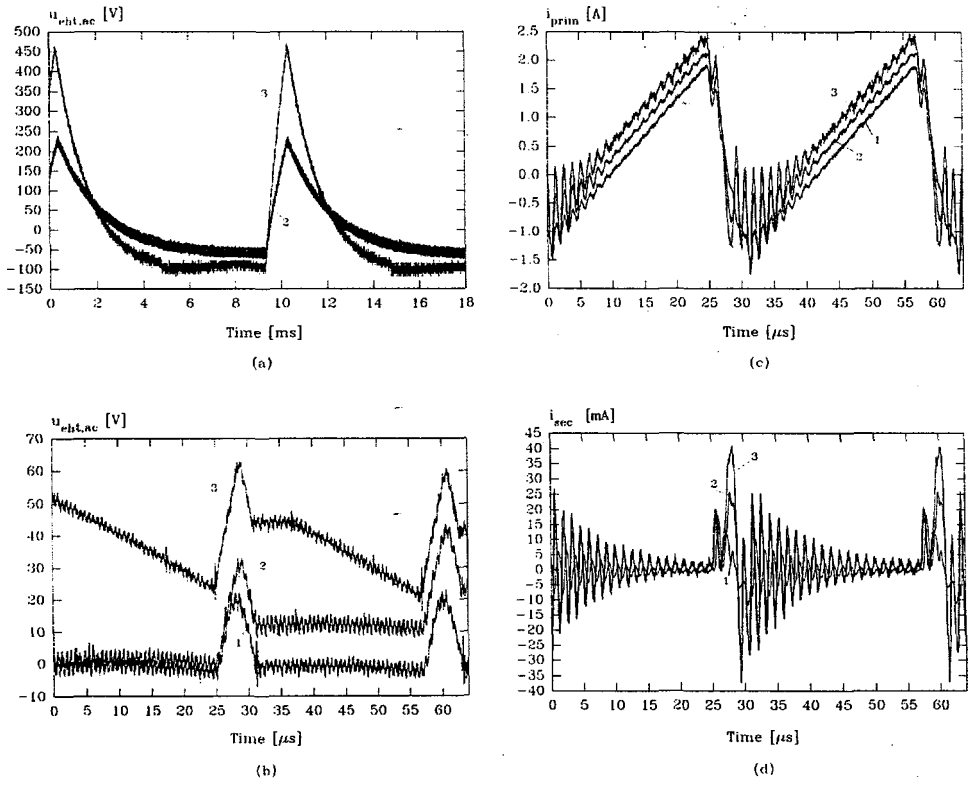


Fig. 3.9: *The voltage and the current waveforms in the diode split transformer, DST, at 1: I_{Load} = 0 mA, 2: I_{Load} = 1 mA, 3: I_{Load} = 2 mA. (a) the a.c. content of the EHT, (b) the a.c. content of the EHT, (c) the primary current, (d) the secondary current.*

4 Simulation in Saber™

The general object of the project is to form a basis of the reduction of the power consumption in the deflection/EHT circuit in televisions. To fulfil this purpose a calculation/simulation tool is necessary as expressed in the introduction:

initiate the modelling of the components, carry out calculations/simulations, and evaluate the possibilities of creating new design tools for the constructors of televisions.

To serve this purpose it will be investigated whether some of the calculations/simulations can be executed in the circuit-simulator Saber™ from Analogy®. This would be desirable because of the built-in libraries with models of the power electronic components in Saber™. If these models are accurate enough to be used only with a few corrections of the models and their parameters, it will be a strong tool because the program will be able to simulate on both a system and a component level. However, the intension of this chapter is not to perform any detailed investigations of the applicability of Saber™ on a component level, but to focus on the system level.

The chapter introduces some of the facilities in Saber according to which the procedure of simulating the simplified deflection/EHT circuit is explained. The used models of the components are shortly introduced and the performed simulations are compared to the measured waveforms obtained in chapter 3.

4.1 The simulation program Saber™

Saber™, from Analogy®, is a general purpose simulator which is developed to serve a broad scope of applications. It is often compared to the SPICE simulator even though SPICE was only intended to simulate microelectronic integrated circuits. Saber is on the other hand capable of simulating many different applications as it is as applicable to mechanical systems as it is to electrical ones. The simulations documented in this chapter are of course focused on the simulation of power electronics.

The Saber concept of separating the models from the simulator is the fundamental difference between SPICE and Saber. In Saber the simulator core is Saber and the modelling language is called MAST. Since simulation and modelling in this way are completely separate processes, the primary description of a physical system is contained in an input file that is accessed by the Saber simulator during the simulation process. The input file is either extracted from a schematic circuit created by a CAE system or directly from an ascii word processor, see Fig. 4.1. The input file contains a netlist that describes the interconnections of the components of the system and contains the names of library files in where the models of these components are stored. A library file is called a generic template because it describes the general behaviour of a component category such as transistors, diodes, signal sources, etc., but when the parameter values of a component are inserted, the generic template becomes a specific model.

Saber is superior to SPICE in modelling efficiency because the Saber simulator allows the creation of new models in the MAST language. However, the MAST language will not be discussed here as only the standard component library of analog component models created by Analogy is used in the performed simulations. The simulations are therefore restricted to modelling at the netlist level, selecting existing component models from component libraries. The benefits of this kind of modelling is the fast implementation of the deflection/EHT circuit in the Saber simulator. Besides, a concept known as graphical modelling, where the available building blocks are simply connected, is used in the implementation of the circuit. Graphical modelling is in this way the development of the deflection/EHT circuit using a graphic front-end, called DesignStar, rather than programming directly in the MAST language. However, the underlying model is represented in MAST.

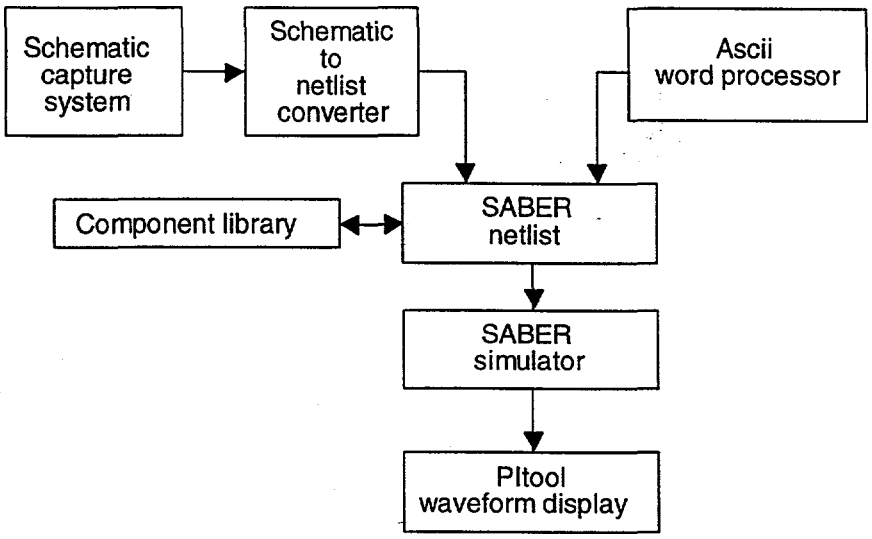


Fig. 4.1: *A simple representation of the Saber environment.*

The Saber netlist is the input to the Saber simulator as shown in Fig. 4.1. It is not the intension to explain the architecture of the Saber simulator, but only to mention some of its advantages compared to SPICE. The following information is taken directly from [11].

Saber employs numerical integration techniques to transform the system of ordinary differential equations to a series of nonlinear algebraic equations. An iterative technique is used to transform these nonlinear algebraic equations into a series of linear algebraic equations. These linear equations are solved using direct matrix techniques. A major difference between Saber and SPICE is the manner in which the iterative solution is achieved. SPICE utilizes tolerances (e.g. ABSTOL, RELTOL, and CHGTOL) with the Newton-Raphson algorithm to determine convergence to a valid solution. Thus, the exact system of equations is solved to within a prespecified tolerance. In Saber, there are no tolerances on the algorithm to determine convergence. The exact system of equations is piecewise linearly evaluated (based on a concept known as sample points) and the resulting linearized system of equations is solved exactly. The piecewise linear evaluation of the models actually provides the user with more straightforward control of the accuracy of the solution. The control is decentralized to each model so that the accuracy can be increased or decreased on a local basis. In SPICE the tolerances apply to the entire system of equations and the accuracy control is global.

Another advance of Saber is that Saber can extract an initial point from the results of a previous analysis. This is used in the simulation of the deflection/EHT as explained in the next section.

4.2 The simulation procedure

A secondary objective of the simulations is to obtain a general knowledge of the facilities in Saber, because neither the author or the staff at B&O are familiar with the Saber program. The simulations are therefore not carried out with the chief aim of obtaining accurate simulation results but rather to obtain some experience in the general technique of simulation in Saber. The simulations are therefore performed with considerable limitations of which the following are the most significant:

- The existing models of the components in the library in Saber are used. This is especially a demarcation in relation to the DST because the used model in this way is an ordinary ideal transformer with no parasitic components.
- The CRT is modelled as a capacitor in parallel with an ideal current generator.

- The models of the inductors and the transformers do not include models for the iron losses and the a.c. resistance of the windings.
- The passive components are considered as ideal with the exception of the inductances and transformers where the d.c. resistance is included.
- The wires between the individual components are considered to be ideal.
- The control circuit, PLL, used to synchronize the sync signal and the front of the flyback pulse is omitted. Thus, only stationary conditions can be simulated and the time until the circuit is stabilized is rather long.
- There are no limitations of the signals in the circuit, as an example the current limiter for the beam current is omitted.

The simulation of the deflection/EHT circuit is performed at two different levels of simplification:

I) Simulation with idealized components.
II) Simulation with existing models of the components in Saber.

where both I) and II) are compared to the measurements at I_{Load} = 1 mA.

The simulation with idealized components is done as an introduction to the Saber simulator. The implementation of I) is straightforward, and due to the idealized components no interaction between the individual components is introduced. Thus, the result of the simulation shows the basic mode of operation of the deflection/EHT circuit. Besides, when the simulation with the idealized components is compared to the simulation with the nonidealized components, it is expected that the influence of the nonidealized components on the waveforms in the circuit is more visible.

In order to overcome the fact that the time until the circuit is stabilized is rather long, the initial points for the simulations are extracted from a single transient simulation in which the circuit has been stable. The measured value of the passive components is implemented in Saber rather than using the value specified by the manufacture of the components. The measured values of the passive components together with the used models in the simulations are shortly presented in the next sections.

4.2.1 The passive components

The passive components in the deflection/EHT circuit have been measured with a LCR meter (Escot, ELC-130) and the measured values are as shown in the table below.

Resistors	Capacitors	Inductances
R_1 = 1.49 kΩ	C_1 = 4.87 nF	L_Y = 307 μH
R_2 = 2.16 kΩ	C_2 = 5.11 nF	
R_3 = 8.19 kΩ	C_3 = 22.1 μF	
R_4 = 68.5 Ω	C_4 = 1.90 nF	
R_5 = 2.16 kΩ	C_5 = 2.9 nF	
R_6 = 2.19 kΩ	C_8 = 9.97 nF	
R_7 = 996 Ω	C_9 = 470 nF	
R_8 = 9.88 kΩ		
R_9 = 2.19 kΩ		
R_{10} = 4.70 kΩ		
R_{13} = 4.68 kΩ		

The above components are all implemented as ideal components by use of the standard models in

Saber. Please note that the implementation of the components R_{11}, R_{12}, C_6, and C_7 is not necessary due to the possibility of measuring the voltage and current directly at any node in the Saber simulator.

A few remarks on the implementation of the deflection coil and the transformer in the driver circuit are given while the implementation of the DST is explained in the next section: The deflection coil is considered as an air coil, thus, the ferrite shield is disregarded. The deflection coil is therefore implemented as an ideal inductance, L_{LY}, in series to a resistance of 0.5 Ω which is measured at a frequency of 31.25 kHz. The transformer in the driver circuit has a primary inductance with the value $L_{T1,prim}$ = 39.8 mH at a frequency of 31.25 kHz. The transformer has 437 turns on the primary and 26 turns on the secondary resulting in a ratio of n_{T1} = 16.8. The ideal transformer model in Saber requires both a primary and a secondary inductance, thus, the secondary inductance is implemented as 141 µH. The stray inductance of the transformer seen from the secondary is implemented as a separate inductance in series to the base of the transistor with a value of $L_{T1,stray}$ = 1.45 µH.

4.2.2 The diode split transformer

The transformer is considered as it consists of only one primary and one secondary winding. Moreover the diodes in the secondary are represented as a single diode. The primary of the DST has an inductance of L_{prim} = 1.11 mH as specified in the data sheet, and the resistance of the primary winding is measured to be approximately 0.6 Ω. The data sheet states that the DST has 70 turns on the primary and 1883 turns on the secondary resulting in a ratio of n_{DST} = 26.9. As explained above the ideal transformer model requires a secondary inductance, here with the calculated value of 803 mH. The diode in the secondary is implemented as an ideal diode.

The bleeder and the focus resistance in the DST are implemented as a single ideal resistor R_{eq} with the value

$$R_{eq} = \frac{R_{focus} R_{bleeder}}{r R_{bleeder} + (1 - r) R_{focus}} \; ; \qquad r = \frac{N_{focus}}{N_{sec}} \tag{4.1}$$

where r is the ratio of the number of windings on the focus tab, N_{focus}, and the total number of the secondary windings, N_{sec}. In the data sheet for the DST the approximate values of the bleeder and the focus resistance are given as $R_{bleeder}$ = 580 MΩ and R_{focus} = 130 MΩ, while the number of windings are given as N_{focus} = 754 and N_{sec} = 1883. This results in an equivalent resistor of R_{eq} = 243 MΩ.

4.2.3 The diodes

In the simulations with the idealized components the current pump and the drive circuit are not implemented. Thus, the only diodes to be implemented are D_5, D_6, and D_{EHT}. The diode D_{EHT} in the DST is in reality not a single diode but a series connection of 8 diodes as explained in chapter 2. Anyway, only a single diode is implemented in the simulation program as indicated in the following table where the implemented diodes in both simulation 1 and simulation 2 are shown.

The implementation of simulation 1 is straightforward due to the use of ideal diodes which are implemented with all the parameters kept at their default value in the template. The current in the ideal diode model is an exponential function of the voltage across it. Because the diode is ideal no reverse and forward recovery phenomena are modelled as well as the capacitance and the temperature effects are disregarded. Further information on the diode model is found in the manuals covering the model fundamentals for the MAST models in Saber.

			Simulation 1	Simulation 2
Diode	Type	Saber model	Implementation	Implementation
D_1	1n4148	yes	-	Saber model
D_2	1n4148	yes	-	Saber model
D_3	BA157	no	-	ideal model
D_4	BA157	no	-	ideal model
D_5	BYW95C	yes	ideal model	Saber model
D_6	BY359F	no	ideal model	modified ideal model
D_{EHT}	BY8406	no	ideal model	ideal model
D_{EHT}	BY8410	no		

The implementation is not as simple for simulation 2 as the libraries in Saber only contain models of three of the used diodes. These three models are directly implemented while the model for D_3, D_4, D_6, and D_{EHT} is the ideal diode model.

The model of the DST is very simplified because the ringing is totally disregarded. Thus, it does not serve any purpose to implement a detailed model of the diodes in the secondary of the DST and the ideal diode model is therefore sufficient. Further, from the author's point of view, it is not critical that the diodes D_3 and D_4 in the current pump are implemented as ideal diodes when an analysis on a system level is wanted. On the other hand, a detailed model for the flyback diode D_6 is more important due to especially the reverse recovery phenomena in the diode as explained in chapter 3.

To model the reverse recovery the template dp (Power Diode) is used with all the parameters kept at the default values as explained in the Saber manual. The only exception is the three parameters describing the storage phenomenon and the reverse recovery of the diode: the carrier life time, tt, the transit time of the base, tm, and the charge sweep-out time, tsw.

The model of the reverse recovery is treated in [12], [13] where the following equation is used to determine the carrier life time, tt:

$$I_{RM} = a(tt - \tau_{rr})\left[1 - \exp\left(-\frac{T_1}{tt}\right)\right] \qquad (4.2)$$

where a is the slope of the decreasing diode current, T_1 is the time from the current starts to decrease until it is at the minimum value I_{RM}, and τ_{rr} is the reverse recovery time constant. The transit time of the base and the charge sweep-out time are considered as identical and can therefore be replaced by the value of the reverse recovery time constant τ_{rr}.

The reverse recovery time constant τ_{rr} is measured directly from the current waveform of the diode D_6 which is also the case for the time T_1, the minimum value of the current I_{RM}, and the slope a. The measured values are approximately $\tau_{rr} = 400$ ns, $T_1 = 13$ µs, $I_{RM} = 0.79$ A, and $a = 0.85$ A/µs. From (4.2) the carrier life time is calculated to approximately $tt = 1.3$ µs. Thus, the implemented values are $tt = 1.3$ µs, $tm = 400$ ns, and $tsw = 400$ ns.

4.2.4 The transistors

The implemented models of the transistors for both simulation 1 and simulation 2 are shown in the following table.

			Simulation 1	Simulation 2
Transistor	Type	Saber model	Implementation	Implementation
TR1	BC547B	yes	-	Saber model
TR2	BC337	yes	-	Saber model
TR3	BU2525AX	no	ideal model	BU2508AX

The ideal model of the transistor in simulation 1 is a simple contact with a resistance of 100 MΩ in the open position and with no resistance in the closed position. The duty cycle is 0.52 at a switching period of 32 µs and both the turn-on and the turn-off times are 200 ns. The turn-off time is the same as the one specified in the data sheet for the actual transistor BU2525AX. The turn-on time is unimportant due to the soft turn-on of the transistor.

No model of the transistor BU2525AX exists in Saber, so the model for the transistor BU2508AX is used instead. The influence of this will be seen in the simulation results from simulation 2.

4.3 Simulation with idealized component models

The simplified deflection/EHT circuit is implemented as shown in the schematic diagram, printed directly from DesignStar, in Fig. 4.2.

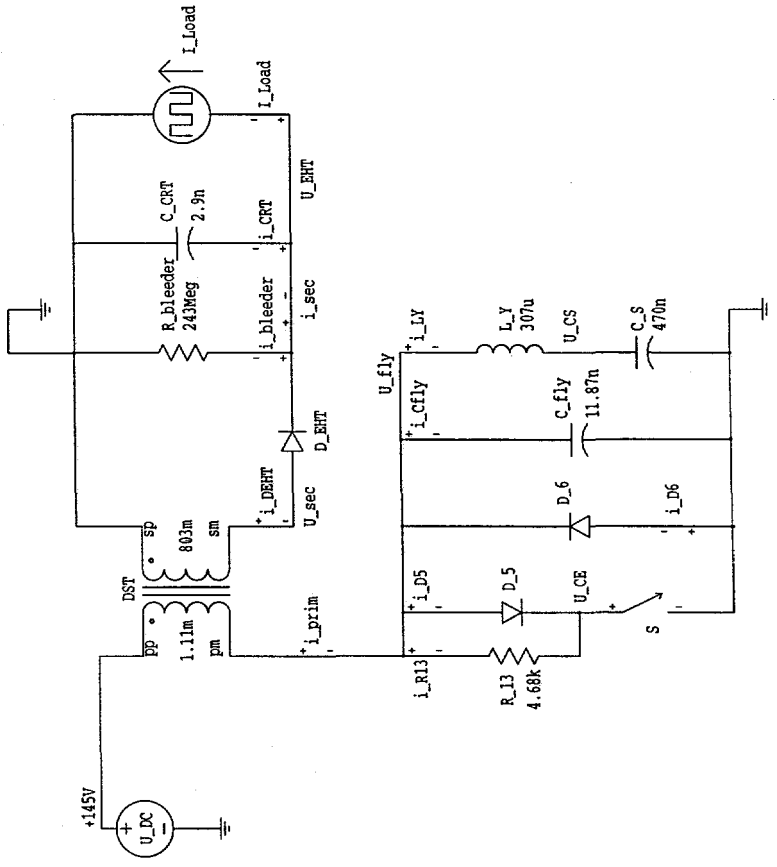


Fig. 4.2: *The created schematic circuit of the simplified deflection/ EHT circuit in DesignStar. The circuit is used in simulation 1.*

The simulation results from the simulation of the circuit in Fig. 4.2 is shown in Fig. 4.3 to Fig. 4.14.

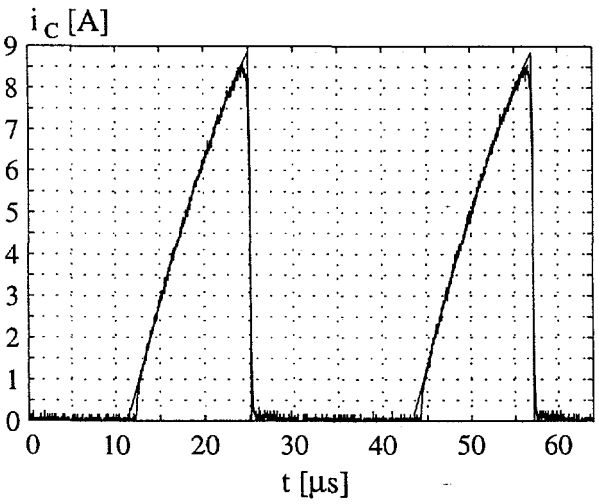


Fig. 4.3: *The measured and the simulated collector current at I_{Load} = 1 mA.*

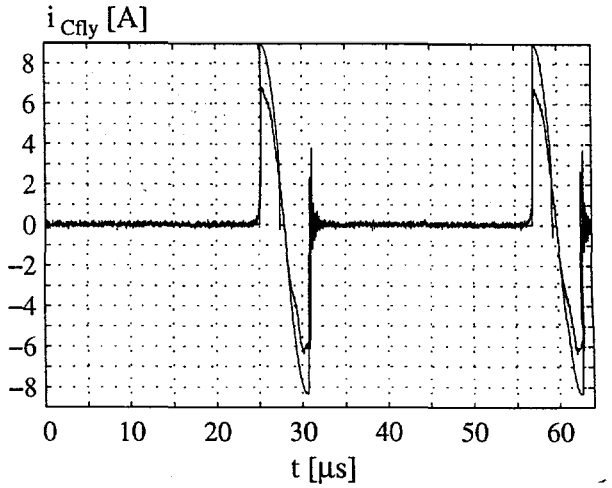


Fig. 4.4: *The measured and the simulated current through the flyback capacitor at I_{Load} = 1 mA.*

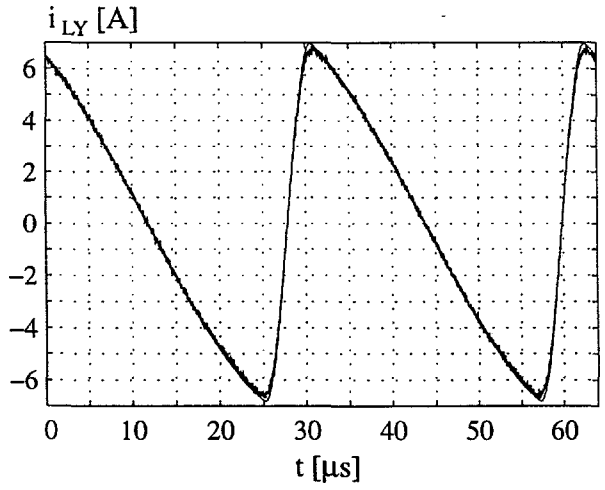


Fig. 4.5: *The measured and the simulated deflection current at I_{Load} = 1 mA.*

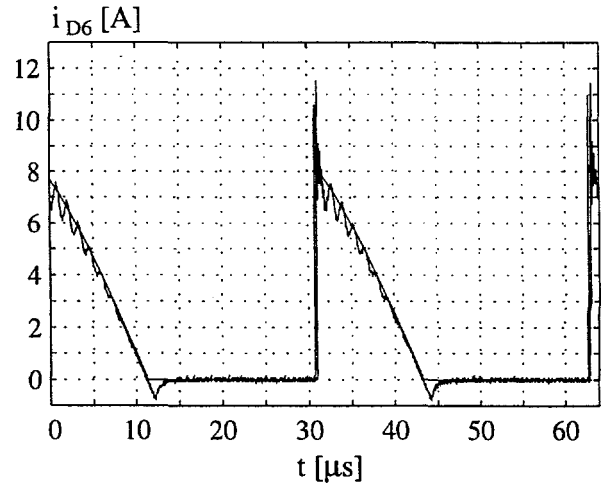


Fig. 4.6: *The measured and the simulated current through the diode D_6 at I_{Load} = 1 mA.*

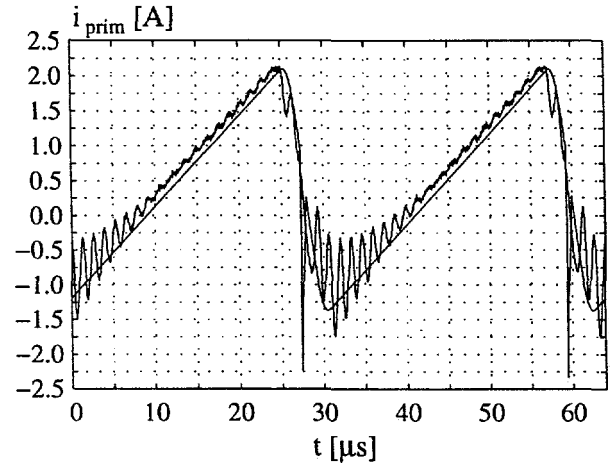


Fig. 4.7: *The measured and the simulated primary current at I_{Load} = 1 mA.*

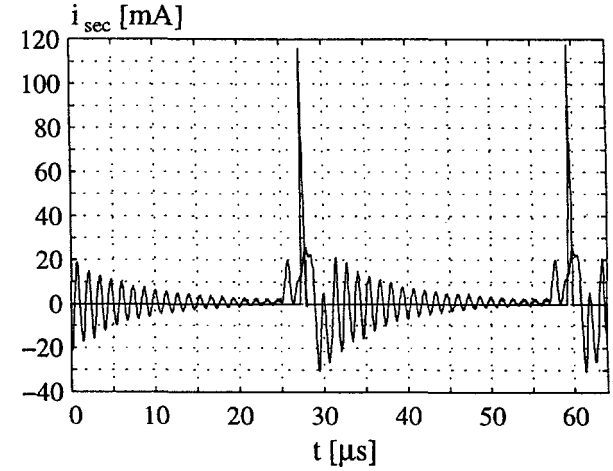


Fig. 4.8: *The measured and the simulated secondary current at I_{Load} = 1 mA.*

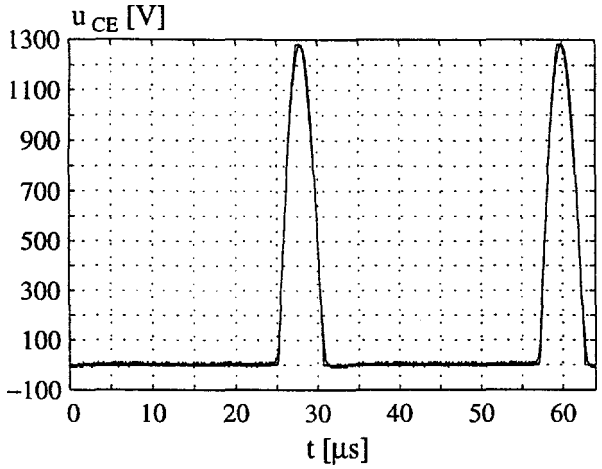


Fig. 4.9: *The measured and the simulated collector-emitter voltage at I_{Load} = 1 mA.*

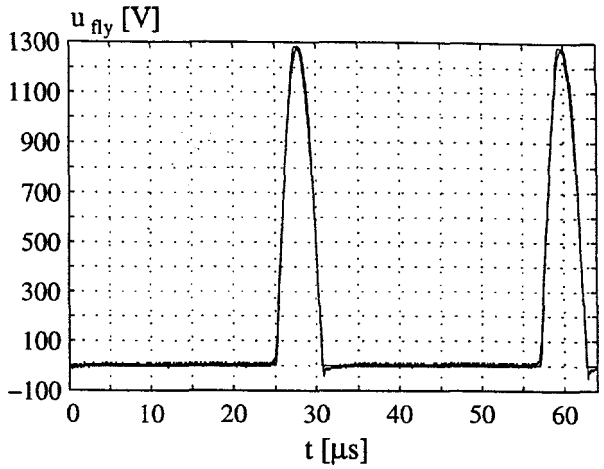


Fig. 4.10: *The measured and the simulated flyback voltage at I_{Load} = 1 mA.*

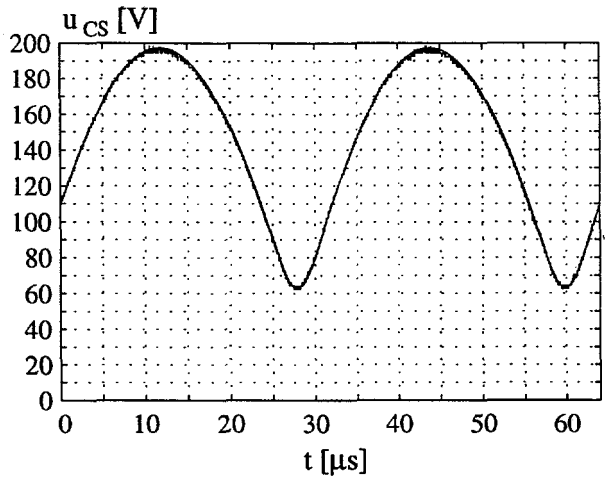


Fig. 4.11: *The measured and the simulated voltage across the S-capacitor at I_{Load} = 1 mA.*

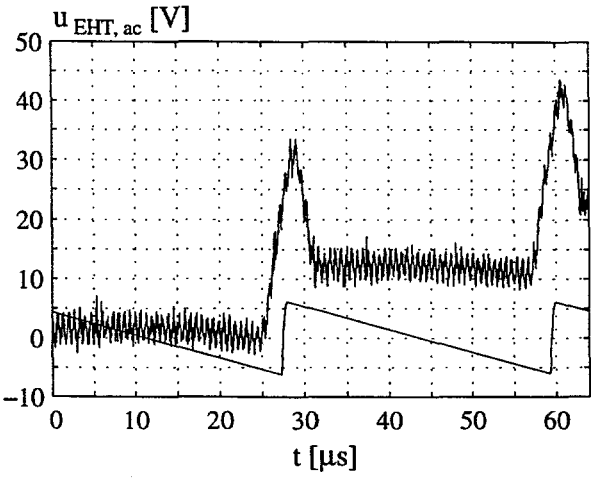


Fig. 4.12: *The measured and the simulated a.c. content of the EHT at I_{Load} = 1 mA.*

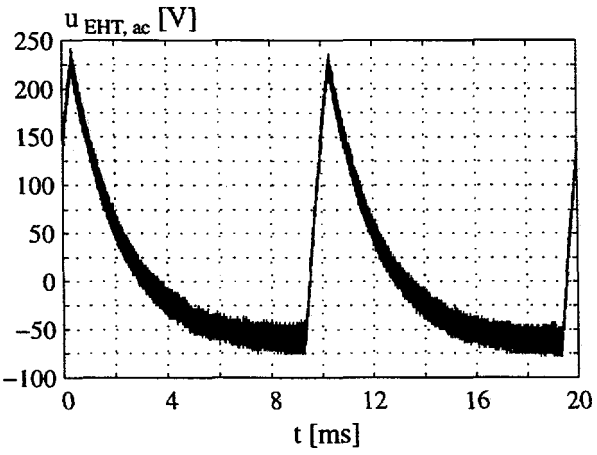


Fig. 4.13: *The measured a.c. content of the EHT at I_{Load} = 1 mA.*

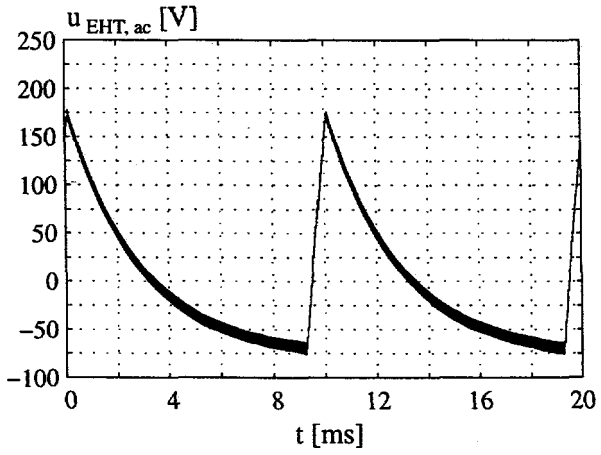


Fig. 4.14: *The simulated a.c. content of the EHT at I_{Load} = 1 mA.*

The simulated collector current in Fig. 4.3 is almost identical to the measured one with the exception of the initial part of the waveform and the maximum value of the current. The deviation at the initial part is due to the lack of the reverse recovery current in D_6 as explained in chapter 3 while the bigger value of the simulated current is probably caused by the idealized model of the transistor.

The simulated current through the flyback capacitor is much bigger than the measured one. This is because no current flows into the current pump simply as the current pump is not implemented in the simulation circuit. In order to achieve the same flyback time the implemented flyback capacitor C_{fly} has a value calculated as the parallel connection of the original flyback capacitor and the capacitor to the current pump, $C_{fly} = C_4 + C_8 = 11.87$ nF. The simulated flyback voltage is then nearly as the measured one, and the simulated current in the flyback capacitor is therefore bigger than the measured one.

The simulated deflection current is almost identical to the measured one which is very important because the deflection current is one of the outputs from the deflection circuit to the CRT. The simulated current in the diode D_6 has the same shape as the measured current with the exception of the ringing from the DST and the reverse recovery current, see Fig. 4.6. The lack of the ringing is clearly seen in the primary and the secondary current of the DST in Fig. 4.7 and Fig. 4.8, respectively. Thus, power is only transferred to the secondary in a single current spike in the simulation. This is also seen in the collector-emitter voltage and the flyback voltage as a flat top, see Fig. 4.9 and Fig. 4.10. The measured flyback voltage has a negative value immediately after the flyback period due to the forward recovery of the diode D_6. This is of course not modelled in the ideal diode model, and the phenomenon is not important when simulating on a circuit level, but if the power losses in D_6 are important, the forward recovery is of major importance.

The d.c. value of the simulated EHT is 30.5 kV while the measured value is 28.6 kV. This deviation is primarily caused by the fact that the implemented ideal model of the DST has a coupling factor equal to one. Fig. 4.12 shows the a.c. content of the EHT during the creation of two lines on the CRT while Fig. 4.13 and Fig. 4.14 shows the a.c. content during the creation of two frames. The smaller value of the simulated a.c. content in Fig. 4.14, in comparison with the measured in Fig. 4.13, is most probably due to the value of the capacitor C_{CRT} which both influence the actual shape of the voltage and the ratio of the voltage divider in the built deflection/EHT circuit.

As a final remark it can be concluded that the general tendency is that the simulated waveforms have the same shape as the measured waveforms, were it not for the ringing in the DST, the current pump and the reverse recovery in the diode D_6. In the next section the current pump and the drive circuit are implemented along with the reverse recovery in the diode D_6.

4.4 Simulation with existing component models

The simplified deflection/EHT circuit for simulation II is implemented as shown in the schematic diagram in Fig. 4.15. As seen from the diagram a base resistance $R_{base} = 10\ \Omega$ is added to the circuit even though it is not used in the test system. The resistance is requisited in order to damp the oscillation in the base-emitter voltage in the simulation. The reason for the necessity of the base resistance in the simulation and not in the test system is the use of another transistor model as explained in section 4.2.4.

The obtained simulations are compared to the measured waveforms as shown in Fig. 4.16 to Fig. 4.32. The results in Fig. 4.16 to Fig. 4.27 will not be treated in details as the discussion in section 4.3 already has covered the most significant differences between the simulations and the measurements. However, a significant difference between the simulation with idealized component models and the simulations in this section is visible in Fig. 4.16 and Fig. 4.19. The modelling of the reverse recovery in the diode D_6 is very good, and by comparing Fig. 4.16 and Fig. 4.3 it is clearly seen that the reverse recovery influences the collector current in the transistor.

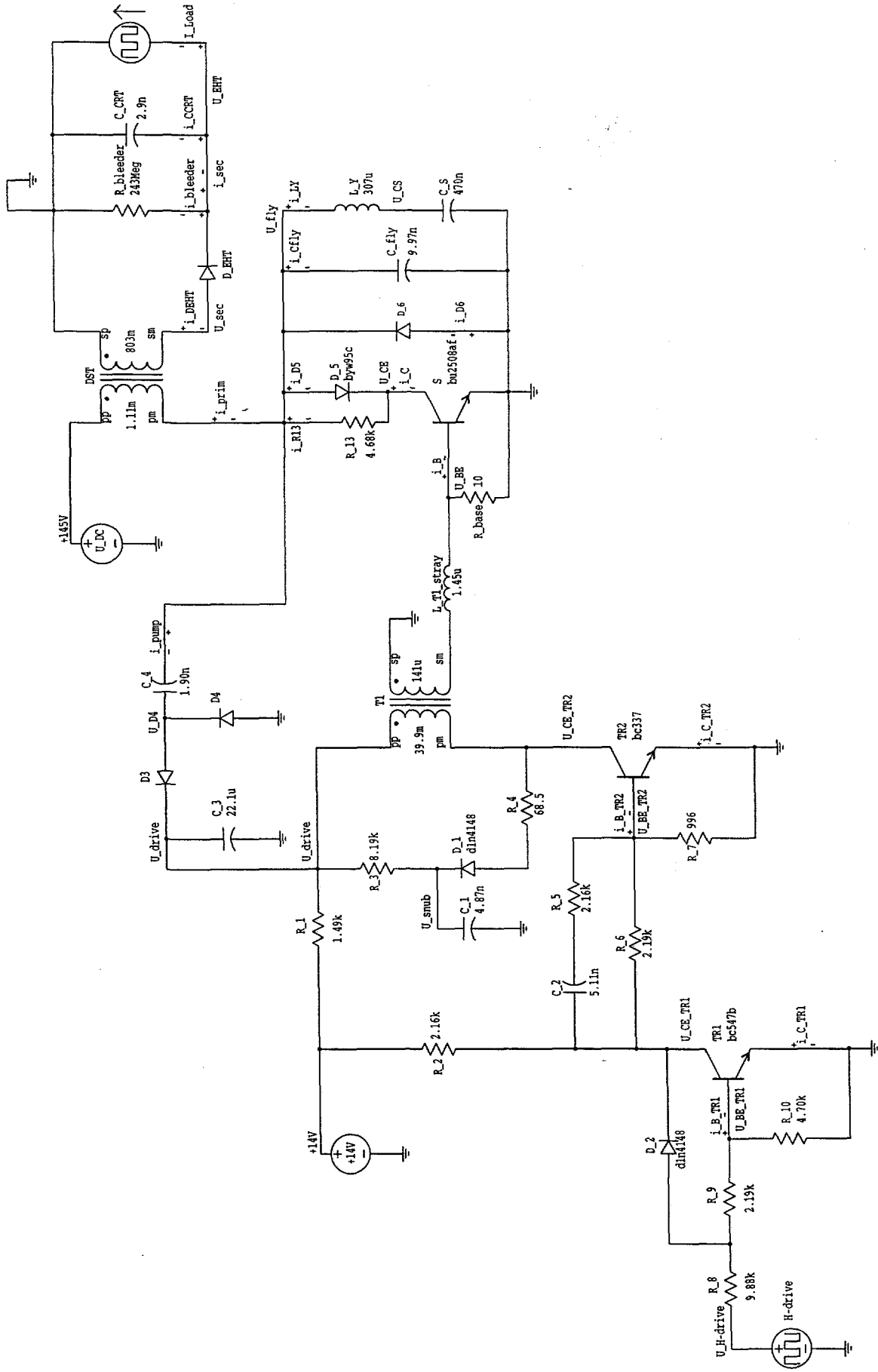


Fig. 4.15: *The created schematic circuit of the simplified deflection/EHT circuit in DesignStar. The circuit is used in simulation II.*

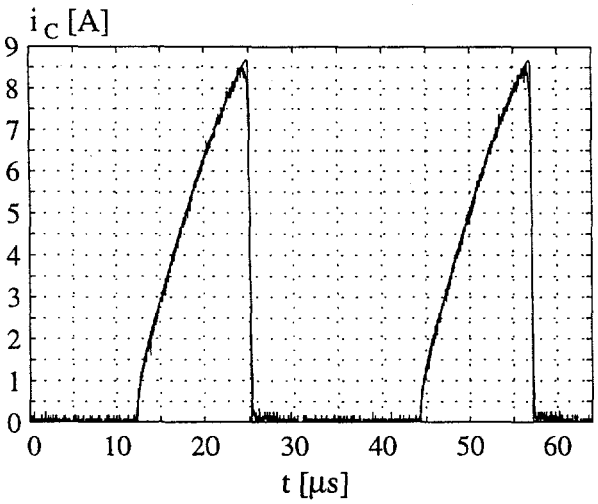


Fig. 4.16: *The measured and the simulated collector current at I_{Load} = 1 mA.*

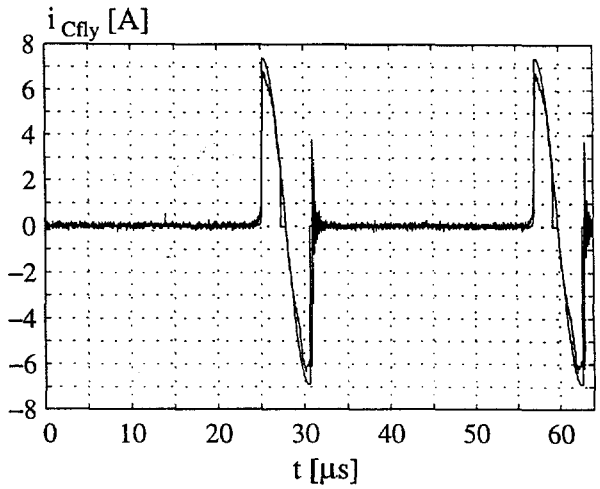


Fig. 4.17: *The measured and the simulated current in the flyback capacitor at I_{Load} = 1 mA.*

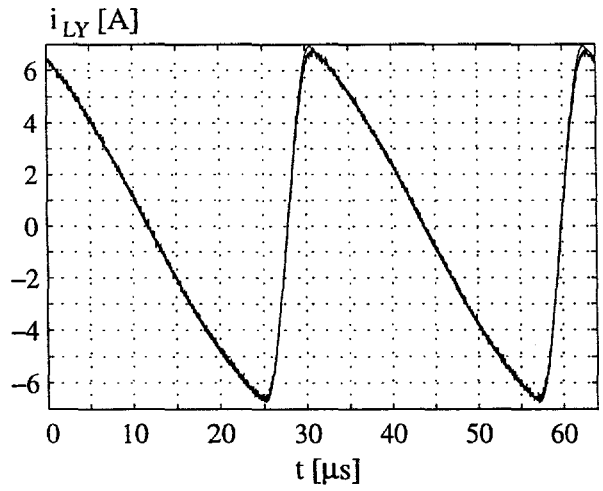


Fig. 4.18: *The measured and the simulated deflection current at I_{Load} = 1 mA.*

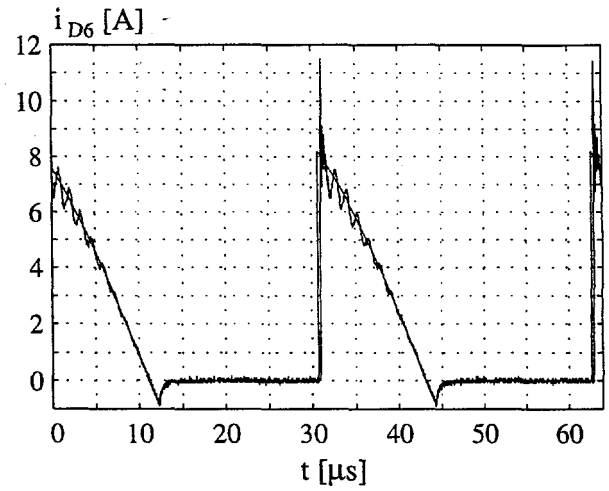


Fig. 4.19: *The measured and the simulated current through the diode D_6 at I_{Load} = 1 mA.*

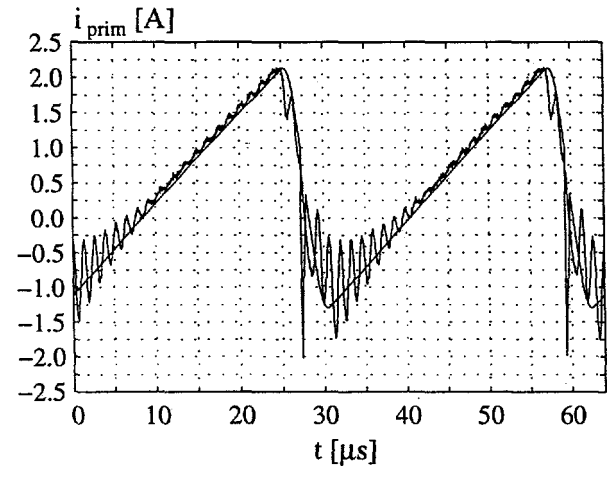


Fig. 4.20: *The measured and the simulated primary current at I_{Load} = 1 mA.*

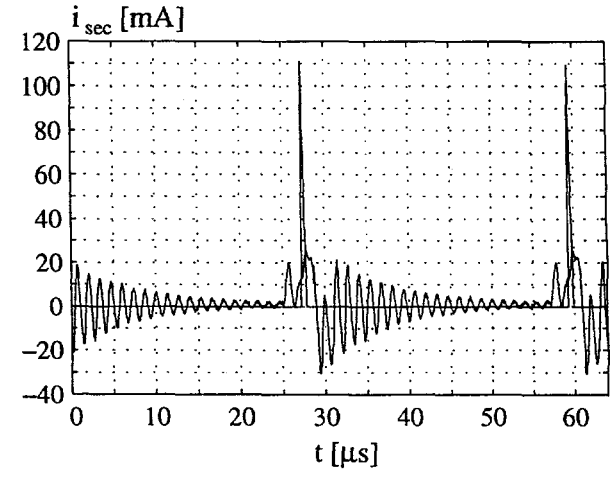


Fig. 4.21: *The measured and the simulated secondary current at I_{Load} = 1 mA.*

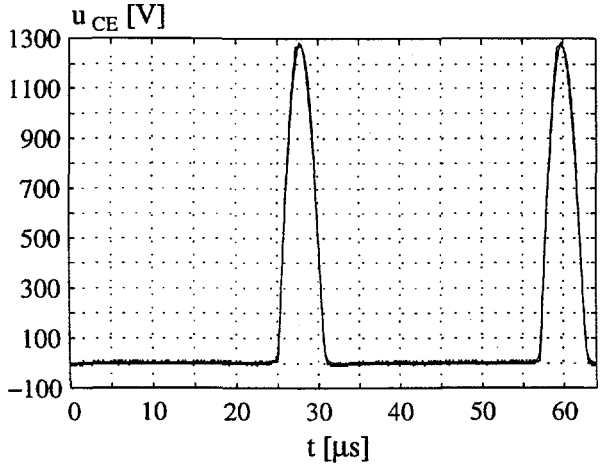


Fig. 4.22: *The measured and the simulated collector-emitter voltage at I_{Load} = 1 mA.*

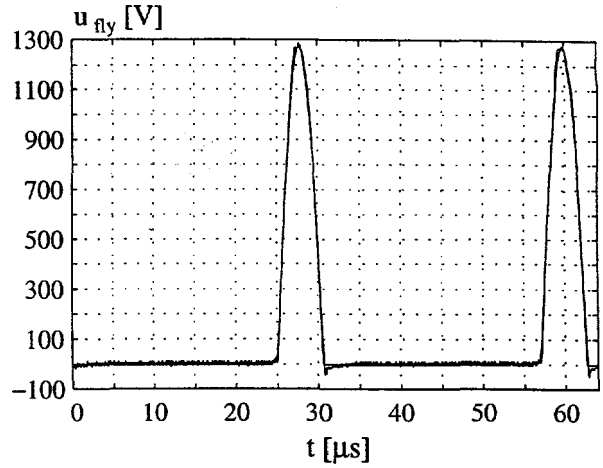


Fig. 4.23: *The measured and the simulated flyback voltage at I_{Load} = 1 mA.*

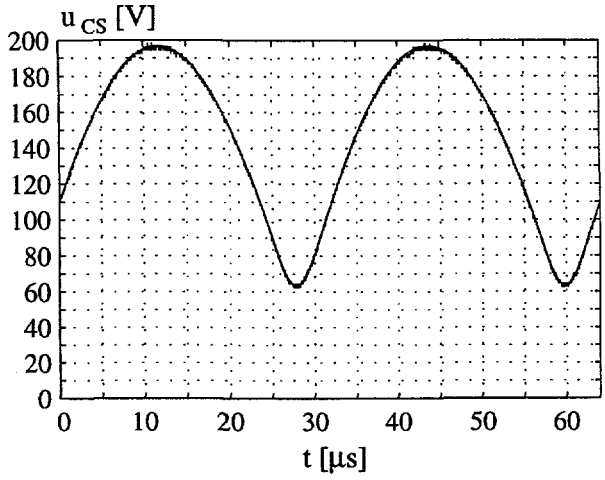


Fig. 4.24: *The measured and the simulated voltage across the S-capacitor at I_{Load} = 1 mA.*

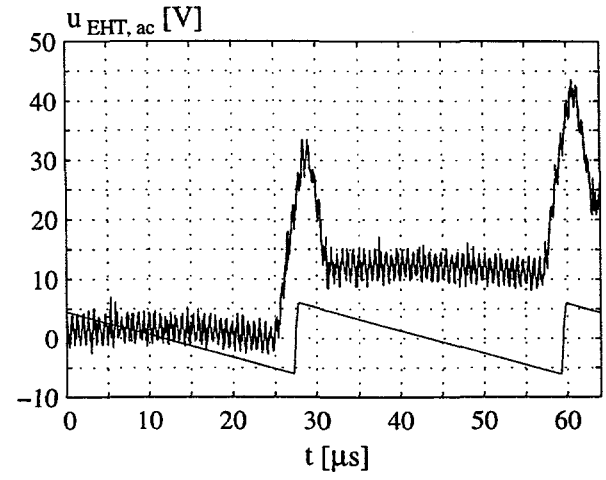


Fig. 4.25: *The measured and the simulated a.c. content of the EHT at I_{Load} = 1 mA.*

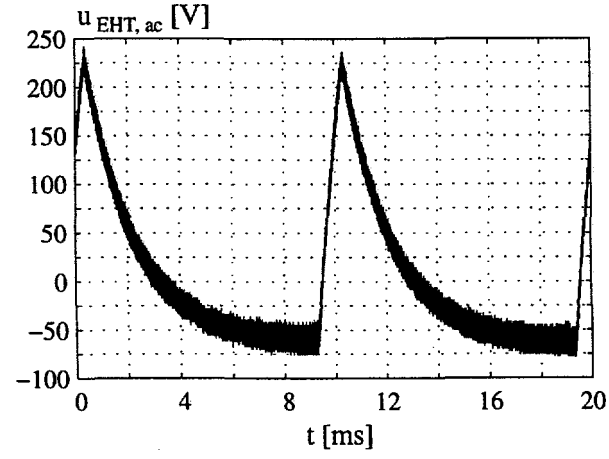


Fig. 4.26: *The measured a.c. content of the EHT at I_{Load} = 1 mA.*

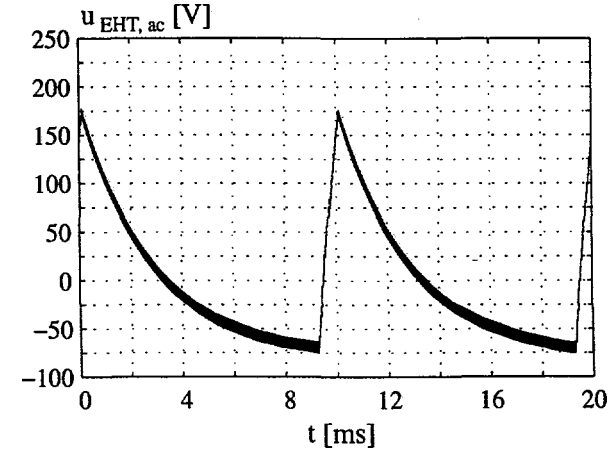


Fig. 4.27: *The simulated a.c. content of the EHT at I_{Load} = 1 mA.*

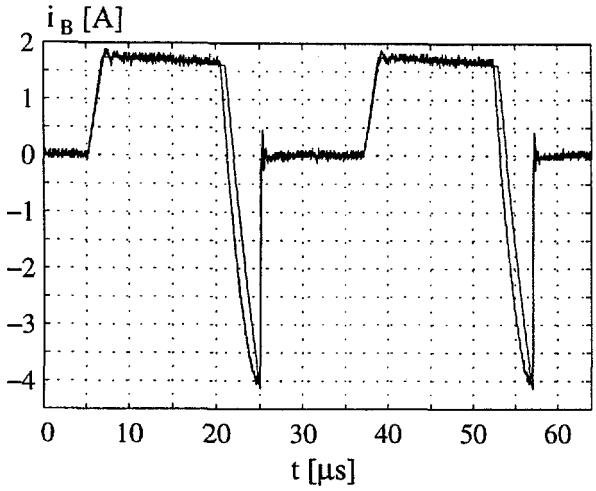


Fig. 4.28: *The measured and the simulated base current to the transistor at I_{Load} = 1 mA.*

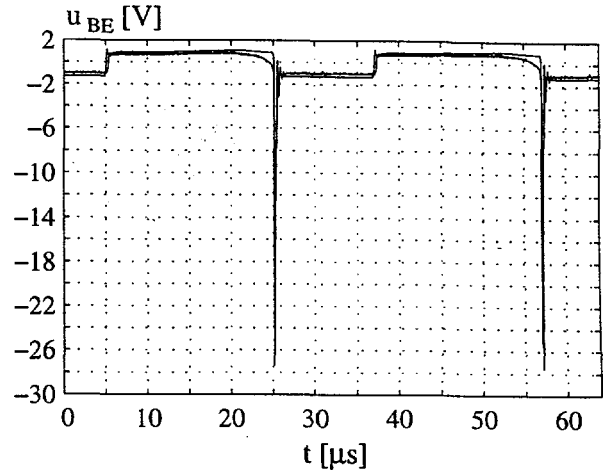


Fig. 4.29: *The measured and the simulated base-emitter voltage at I_{Load} = 1 mA.*

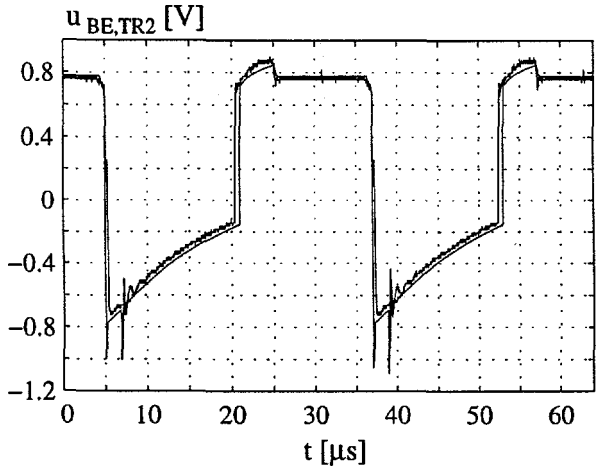


Fig. 4.30: *The measured and the simulated base-emitter voltage for transistor TR2 at I_{Load} = 1 mA.*

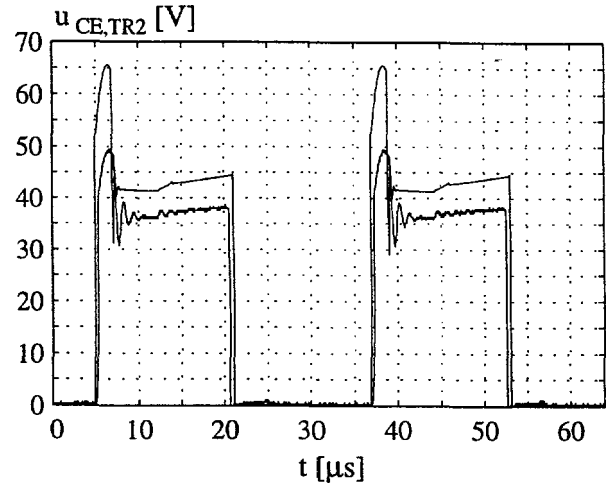


Fig. 4.31: *The measured and the simulated collector-emitter voltage for transistor TR2 at I_{Load} = 1 mA.*

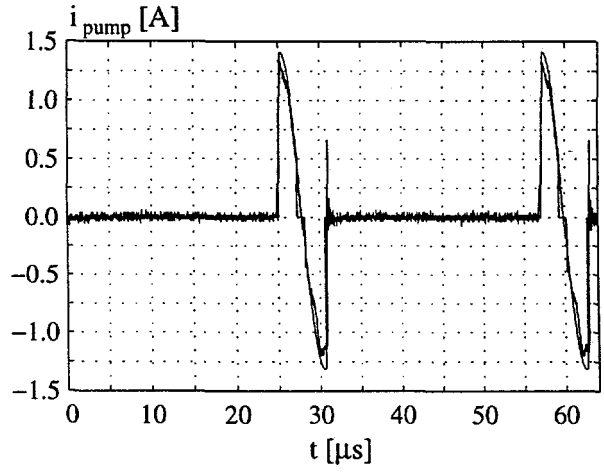


Fig. 4.32: *The measured and the simulated current to the current pump at I_{Load} = 1 mA.*

The shape of the simulated base current in Fig. 4.28 is nearly identical to the measured current. The only difference is during the turn-off of the transistor where the simulated base current starts to decrease a little later than the measured one. Thus, the stored charge in the simulation model of the transistor is less than the stored charge in the actual transistor.

The base-emitter voltage of the transistor in the deflection circuit is greater in the simulation than in the measurements, see Fig. 4.29. This is also caused by the difference in the parameters for BU2508AX and BU2525AX as the base-emitter voltage for BU2508AX is greater than the base-emitter voltage for BU2525AX, see the data sheets. This greater base-emitter voltage is transformed to the primary of transformer T1 and the collector-emitter voltage for TR2 is therefore greater in the simulation, see Fig. 4.31. The mean value of $u_{CE,TR2}$ is 23.3 V and is equal to the mean value of the voltage to the drive circuit, u_{drive}. The measured value of this voltage was only 19.7 V corresponding to an increase in u_{drive} of 18 percent.

Finally, it shall be pointed out that it takes approximately 3-4 seconds to simulate a switching period of 32 μs for simulation 2). However, it takes approximately 10 ms, corresponding to a simulation time of approximately 10 minutes, until the circuit has stabilized. This rather long simulation time is primarily coursed be the lack of a control circuit in the simulation program, but this is not considered as critical because the initial points for the remaining simulations are extracted from this simulation. Besides, the simulations have been performed without any problems concerning numerical convergence.

5 Mapping the power losses by measurements

In order to be in a position to point out the most critical components in relation to the power losses in the simplified deflection/EHT circuit, the power losses are mapped experimentally. This means that the power losses are measured for the individual components at different loads of the diode split transformer. This chapter documents the results and experiences obtained from these measurements and contributes in this way to a better understanding of the distribution of the power losses in the deflection/EHT circuit and presents as well some possible ways of measuring the power losses in the individual components.

The chapter briefly introduces the measuring system, the general measuring process, and the data processing. The more detailed measuring processes for the different measurements are explained, and the results from the measurements are presented. In the light of the measurements it is finally concluded which components to focus on when minimizing the overall power loss in the deflection/EHT circuit.

5.1 The measuring system

The measurements of the power losses are performed on the simplified deflection/EHT circuit described in chapter 3 and shown in Fig. 5.1.

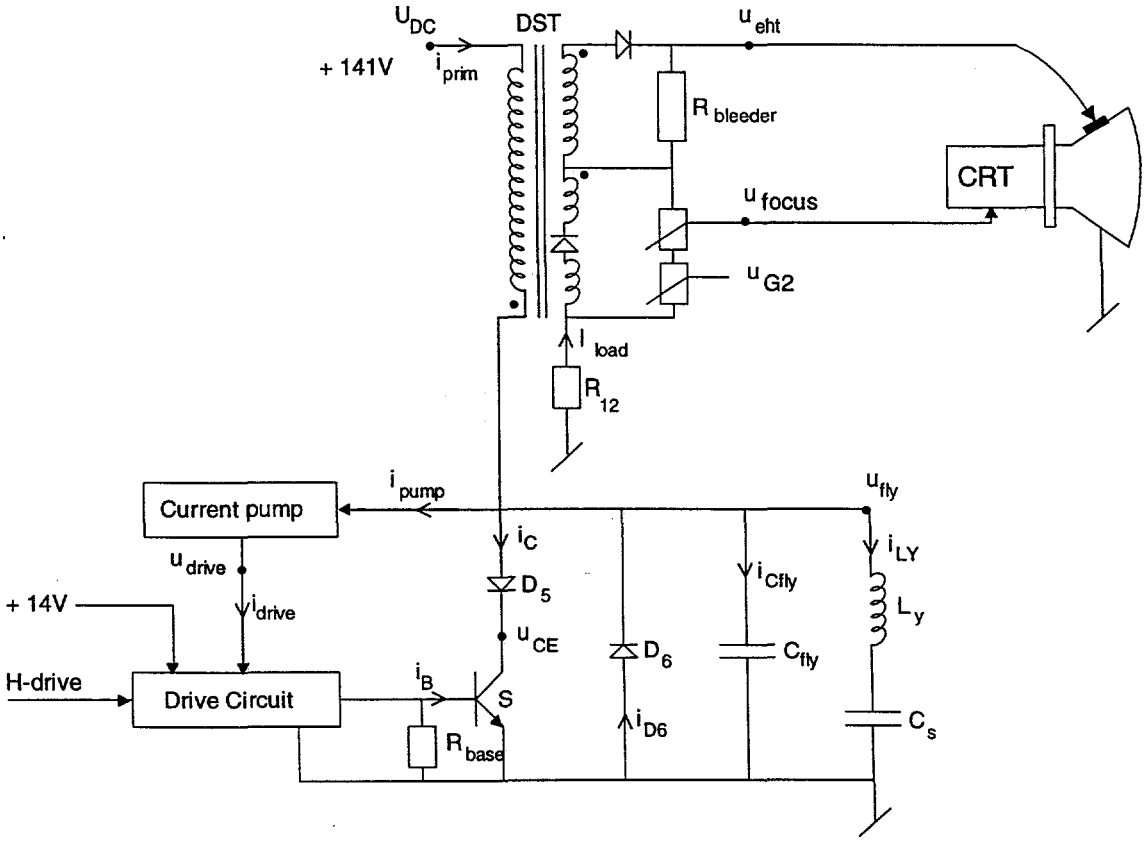


Fig. 5.1: *The simplified deflection/EHT circuit in which the power losses are measured.*

Compared with the circuit used in chapter 3 only a few changes are made:

- A resistance, R_{base}, in parallel with the transistors base-emitter is added to the circuit in order to reduce the ringing on the base-emitter voltage during turn-off.
- The supply to the deflection/EHT circuit is decreased from +145 V to +141 V due to less demands from the deflection circuit. This change in supply voltage results for instance in a lower EHT due to the reduced voltage during the flyback period.
- The grid 2 is no longer supplied from the simplified circuit but from the chassis running in parallel. The only load of the DST is then from the EHT supply and from the focus and grid 2 potentiometers.

In order to get the same conditions as in a commercial television set, the deflection/EHT circuit runs in a continuous mode when mapping the power losses in the circuit. In this way it is not possible to control the temperature of the individual components, and the measurements are therefore performed at the working temperature of the components. Each measurement is performed when the temperature is stabilized in the circuit which in reality takes some minutes after the circuit has been warmed up the first time. Besides, the measurements are all done with standard components with the component values given in the diagram in supplement 4.

5.1.1 The measuring instruments

The measurements of the power losses are carried out by the following instruments:

Instrument	Type
Oscilloscope	Tektronix, TDS 744A (500 MHz, 2 GS/s)
Current probe amplifier	Tektronix, AM 503
Current probe	Tektronix, A6302
Voltage probe	Tektronix, P6139A (10x)
Voltage probe	Tektronix, P5100 (100x)
EHT probe (DC)	B&O (1000x)
Multimeter	Fluke, (connected to the EHT probe)
Multimeter	Fluke, 8020B
Multimeter	Fluke, 8060A (True RMS)
Shunt resistance	LEM 10-5, 81 (R_{shunt} = 10 mΩ)
LF Impedance Analyzer	Hewlett Packard, HP 4192A (5 Hz - 13 MHz)

A special attention shall be paid to the voltage probe used to measure the EHT voltage. This probe is designed and manufactured at B&O with an internal impedance of approximately 1 GΩ and a maximum voltage of 30 kV_{DC}. The calibration of this "home-made" probe is very difficult due to the high frequency, the high voltage, and the high internal resistance. The EHT probe is calibrated at B&O at 1 kV from which the measured value is extrapolated to 30 kV. This is not an accurate method because the impedance might be voltage dependent [2, pp. 117], and the degree of accuracy is therefore

unknown. In order to investigate the accuracy of the probe, the probe has been compared with the available high voltage measurement system at The Institute of Energy Technology, Aalborg Univer-sity, and the results of these measurements are shown in supplement 5. The conclusion is that the EHT probe from B&O is a class 2.5 instrument and that it would be very expensive to get a probe with a better accuracy and to keep it calibrated.

The shunt resistance is produced with special reference to minimize the stray inductance in the resistor. The delay in this shunt resistance has been measured at the turn-off of the transistor and compared to the delay of the current probe. From these measurements it is concluded that the current probe has a higher delay than the shunt resistance, whereby the shunt resistance is necessary when measuring the power losses in the components, but due to the lack of galvanic isolation it is only suitable for the components placed at the ground potential in the circuit. The other currents are therefore measured with the current probe from Tektronix. Even though the inaccuracy of some of the instruments is considerable, it has not been possible to perform any calculation of the overall accuracy of the individual measurements due to the limited available project time. Anyway, this is not that critical because the results shall only show the tendency in the distribution of the power losses in order to fulfil the purpose: "to be in a position to pick out the most critical components in relation to the power losses".

5.1.2 The general measuring process and the data processing

The measurements of the power losses in the individual components are primarily based on the digital storage oscilloscope where the current through and the voltage across the actual component are measured. The only exception from this procedure is the measurement of the power losses in the deflection coil, the DST, and the capacitors which is explained in details in the respective sections dealing with the components. The general measuring process and the data processing are shown in Fig. 5.2.

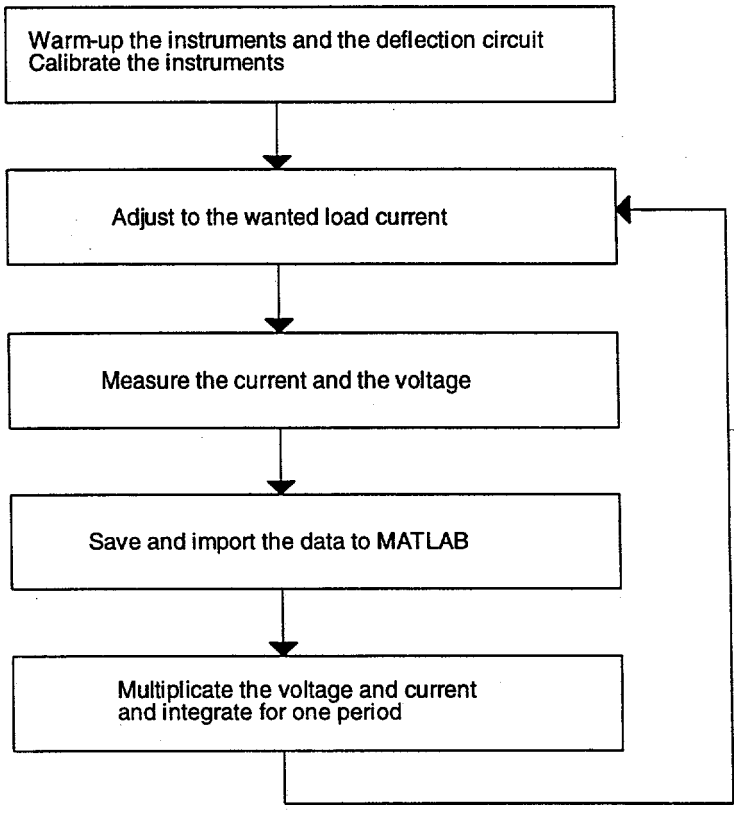


Fig. 5.2: *The general measuring process when using the digital storage oscilloscope.*

After the warm-up of the instruments, both the current and the voltage probes are calibrated. This is straightforward for the current probe and the 10x voltage probe, but the 100x voltage probe cannot be calibrated satisfactorily only by use of the oscilloscope. Instead this calibration is carried out by rectifying the flyback voltage and by measuring it by a multimeter. The probe is then calibrated in order to equal the peak voltage on the oscilloscope to the DC value on the multimeter minus a diode voltage of 0.7 V.

It was experienced that an offset error on the individual channels of the oscilloscope was impossible to remove by calibration. To overcome this problem, measurements are taken with the voltage probes short circuited and the current probe no-loaded. The measured value of the individual channels are by use of the PC subtracted all the measurements performed on the same channel. This "calibration" measurements are done at each new value of the "voltage per division" on the oscilloscope due to the errors dependence on the actual "voltage per division".

In order to get rid of the apparent noise on the measured waveforms and hence the uncertainty on the determined power losses, the average acquisition mode in the oscilloscope is applied. In this mode the oscilloscope acquires data as in the normal sample mode and then averages it according to the specified number of averages which is chosen to be 100.

The measured waveforms are saved in ASCII code and imported to MATLAB ver. 4.2c.1. The integration of the multiplication of the voltage and current is performed by Simpson´s rule of integration where a piecewise quadratic approximation is used [1, pp. 981].

5.2 The overall power flow

The knowledge of the overall power flow in the simplified deflection/EHT circuit is important for two reasons: The first is the interest in the overall efficiency of the deflection/EHT circuit, and the second is caused by the indirect method of measuring the power losses in the DST and the deflection coil. These indirect methods are explained in section 5.7 and section 5.4, respectively, while the input and the output power and the overall efficiency are presented in this section.

5.2.1 The measuring method

All the measurements are performed at different loads of the diode split transformer which in practice means as a function of the beam current to the CRT. As mentioned in chapter 2, the mean value of this load current, $I_{Load,}$ is limited by a current limiter adjusted to 1.8 mA. The current limiter accepts a peak current of $\hat{i}_{Load}$ = 10 mA to the CRT, with a duration of maximum 1 ms. In this way the television set operates with a mean beam current in the interval I_{Load} = 0 mA to I_{Load} = 1.8 mA under normal conditions. The measurements of the power losses are performed at I_{Load} = 0 mA to I_{Load} = 1.9 mA with steps of 100 µA. The load current is measured with a standard 1 kΩ resistor in series with the lower potential of the secondary winding of the DST, see Fig. 5.1. The value of the resistor is measured to R_{12} = 1016 Ω, and the resistor is connected in parallel to a capacitor with a value of 2 µF, which results in a time constant of 2 ms. The primary current in the DST is measured by the current probe amplifier and the current probe.

The EHT is measured by the voltage probe from B&O and the measured supply voltage is the sum of the DC voltage measured with a multimeter and the AC voltage measured with the 10x voltage probe.

The mean value of the supply voltage is constant U_{DC} = 140.7 V independent of the load current contrary the AC content of the supply voltage. An example of the measured AC content of the supply voltage is shown in Fig. 5.3 and the primary current is shown in Fig. 5.4.

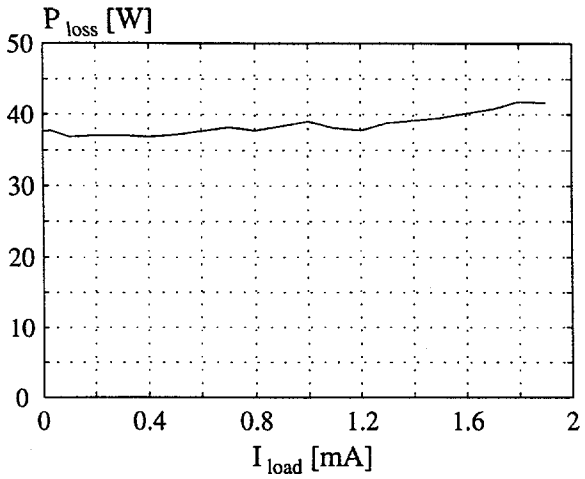


Fig. 5.7: *The total power loss in the deflection/EHT circuit.*

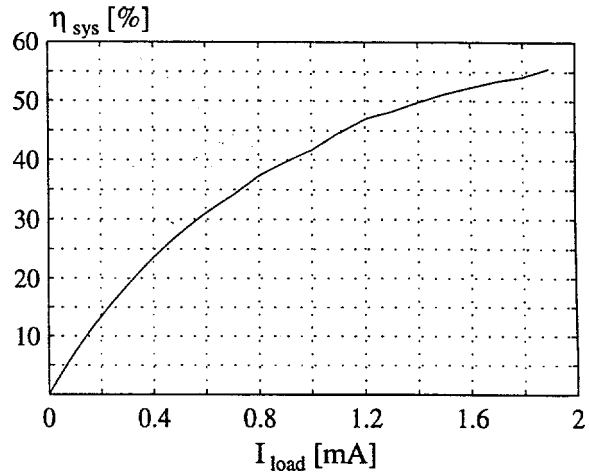


Fig. 5.8: *The overall efficiency of the deflection/EHT circuit.*

The total power loss in the deflection/EHT circuit is in average 37.5 W in the normal working area of an average picture in a television which is at a mean load current of 0.5 mA to 0.7 mA. This power loss results in an overall efficiency of approximately 30 percent It shall be stressed that the accuracy of the measurements are not investigated, but the tendency in the measurements are clear.

5.3 The transistor and the drive circuit

The power losses in a transistor are normal divided into three portions: the turn-on losses, the on-state losses, and the turn-off losses. In the deflection/EHT circuit the turn-on losses are negligible due to the zero-voltage switching, and the overall power losses in the transistor are therefore only determined by the on-state and the turn-off losses.

The measurements on the transistor and the drive circuit are divided into five separate measurements:

- The power to the current pump.
- The power to the drive circuit.
- The power to the base of the transistor.
- The power loss during the on-state of the transistor.
- The power loss during the turn-off of the transistor.

The first three measurements are straightforward while the last two are rather complicated due to the high flyback voltage during turn-off. In the presentation of the measuring method, considerations are presented in order to highlight some of the problems that have to be taken into account when measuring the power losses in the transistor. After that the obtained results are presented.

5.3.1 The measuring method

The power to the current pump

The power to the current pump consists of the power to supply the base of the transistor and the power losses in the drive circuit and the current pump itself. In the deflection/EHT circuit the power to the current pump is supplied during the flyback period through a capacitor, see enclosure 4. In consequence of the poor resolution of the voltage measurements caused by the high flyback voltage, the power to the current pump is measured after this input capacitor in order to be able to use a 10x voltage

At different load currents the power to the drive circuit is calculated as:

$$P_{drive} = \frac{1}{T}\int_0^T \left(U_{drive} + u_{drive}\right) i_{drive}\, dt \tag{5.3}$$

It shall be pointed out that the DC content of the voltage to the drive circuit U_{drive} is almost load independent as it changes with less than 1 percent from zero load to I_{Load} = 1.9 mA. In order to explain this, the idealized expression for the transfer ratio in a flyback converter is considered for the transformer in the drive circuit [10, pp. 216]:

$$U_{drive} = n_{TI} \frac{\delta}{1-\delta} U_{BE} \tag{5.4}$$

where n_{TI} is the winding ratio, δ the duty cycle of the transistor in the drive circuit, and U_{BE} is the base-emitter voltage of the transistor in the deflection circuit. For a constant duty cycle it is seen from (5.4) that the voltage to the drive circuit is directly proportional to the base-emitter voltage. Because the base-emitter voltage is fairly constant as a function of the load current, the voltage to the drive circuit is kept constant.

The power to the base of the transistor

The base-emitter voltage and the base current are shown in Fig. 5.13 and Fig. 5.14, respectively.

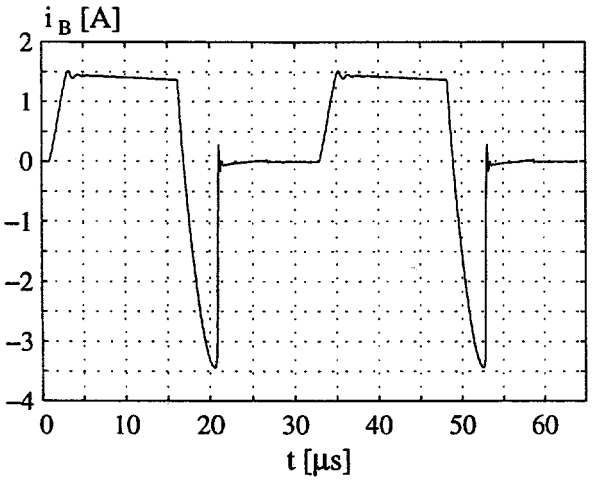


Fig. 5.13: *The current to the base of the transistor at I_{Load} = 1 mA.*

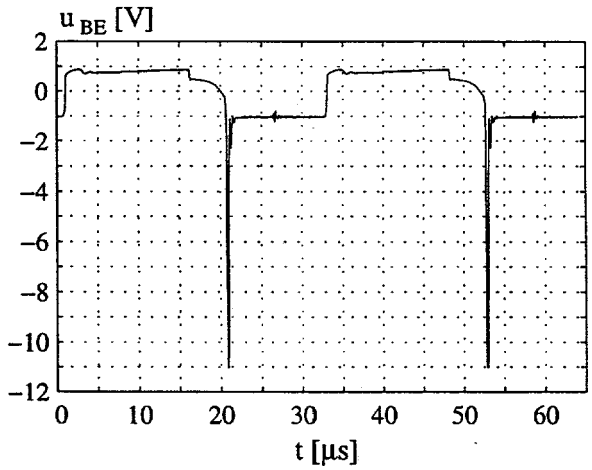


Fig. 5.14: *The base-emitter voltage of the transistor at I_{Load} = 1 mA.*

At different load currents the power to the base of the transistor is calculated as:

$$P_{base} = \frac{1}{T}\int_0^T u_{BE} i_B\, dt \tag{5.5}$$

The power loss during the on-state of the transistor

The flyback voltage is a major problem when measuring both the on-state and the turn-off losses. The voltage range from 0 V to 1300 V demands a 100x voltage probe and gives a very poor resolution when using an 8 bits oscilloscope. In order to overcome this problem when measuring the on-state power losses, the collector-emitter voltage is divided by using the circuit shown in Fig. 5.15. The mode of operation of this circuit is as follows: Before the measurements of the on-state voltage, the cathode of the diode 2xBA159 is connected to ground and the +4 V´s supply forces a current through the resistor

and the diode. With the shown component values this gives a current of 17.8 mA corresponding to a diode voltage of 1.4 V. This voltage is subtracted the measured voltage during the on-state of the transistor with the cathode of the diode 2xBA159 connected to the collector of the transistor. In this way it is possible to use a 10x probe and "1 V per division" at the oscilloscope which gives a much better resolution.

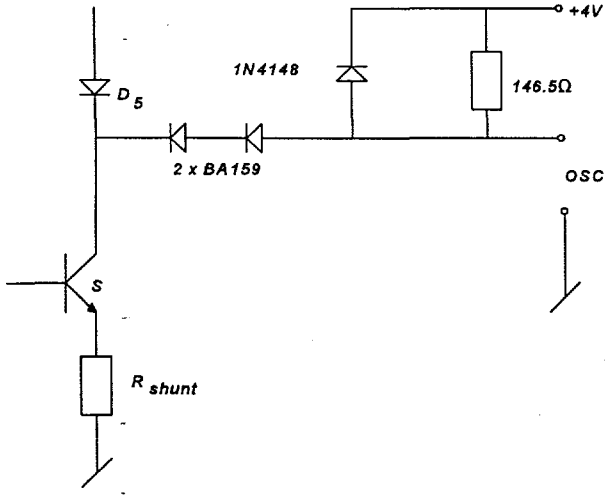


Fig. 5.15: *The measuring circuit used when measuring the on-state power losses in the transistor.*

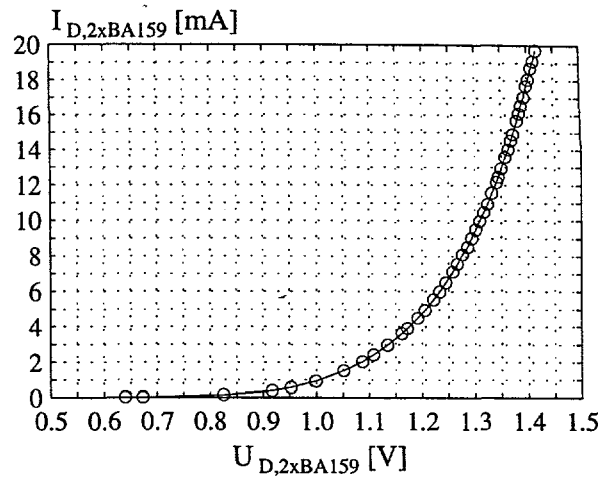


Fig. 5.16: *The "diode characteristic" for the series connection of the two diodes BA159.*

By using the above procedure, it is assumed that the diode voltage is independent of the current through it which is of course not the case, see the diode characteristic at Fig. 5.16. As an estimate of the worst case situation, the current through the diode is 12 mA and the diode voltage is 1.35 V at an actual collector-emitter voltage of 0.95 V. When subtracting the 1.4 V from the measured value on the oscilloscope, this gives an error in the calculated collector-emitter voltage of 0.05 V corresponding to an error of 5 percent. It is possible to compensate for this error caused by the diode characteristic by use of numerical calculations. Anyway, it is chosen not to compensate because the use of the diode characteristic in Fig. 5.16 in a compensation routine gives no meaning. This is because the diode characteristic is not determined by a curve tracer but by standard voltage and current measurements resulting in a variable temperature of the diode during the measurements. As a result a small error is introduced in the measurements which could be minimized by using a compensation routine with a diode characteristic obtained by a curve tracer

In Fig. 5.17 and Fig. 5.18 the measured voltage and the current at the on-state of the transistor are shown, respectively. At different load currents the power loss during the on-state of the transistor is calculated as:

$$P_{on\text{-}state} = \frac{1}{T}\int_0^{t_{on}} u_{CE} i_C dt \qquad (5.6)$$

The voltage drop for the shunt resistor is of course substracted the measured voltage.

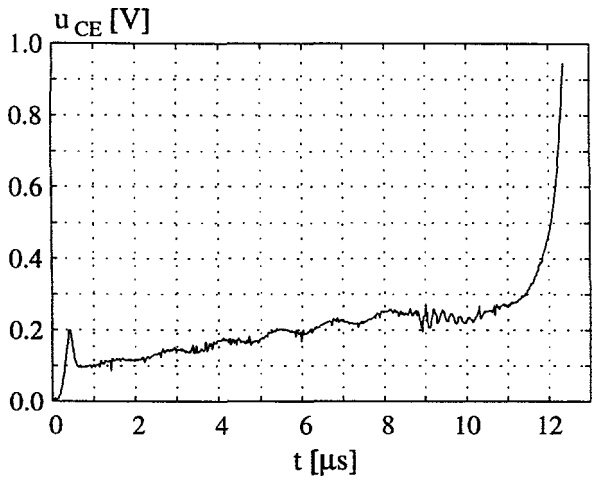


Fig. 5.17: *The collector-emitter voltage during the on-state of the transistor at* I_{Load} = *1 mA.*

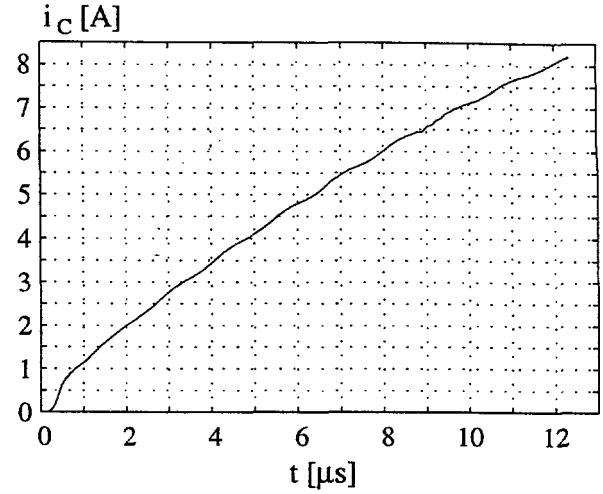


Fig. 5.18: *The collector current during the on-state of the transistor at* I_{Load} = *1 mA.*

The power loss during the turn-off of the transistor

In [4, pp. A8] it is pointed out that the capacitive component of the collector current can lead to a wrong conclusion of the turn-off losses in the transistor. The capacitive current is caused by the internal capacitor between collector and emitter C_2, and the external capacitor between collector and the heat sink C_1, see Fig. 5.19.

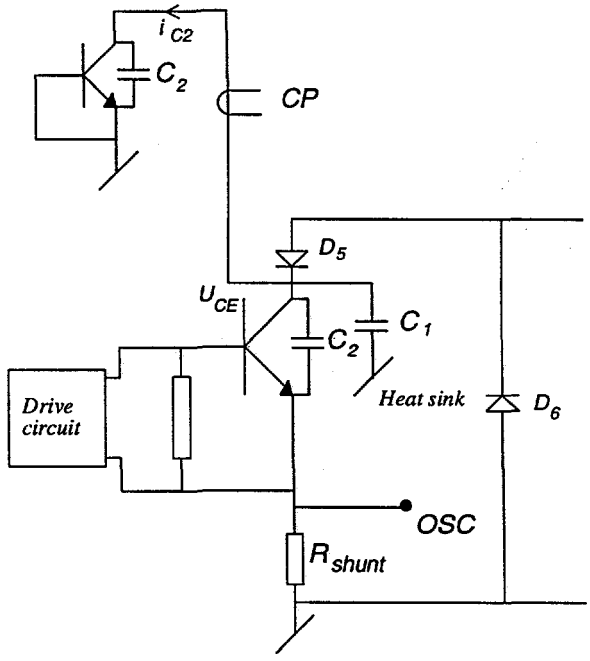


Fig. 5.19: *Part of the deflection circuit illustrating the transistor's internal capacitor* C_2 *and the capacitor* C_1 *to the heat sink.*

By measuring the collector current by the shunt resistance R_{shunt} also the current through the capacitor C_2 is included. This current can only be removed via compensation which can be realized by connecting a similar transistor type with the base-emitter shorted as shown in Fig. 5.19. The base-emitter is shorted because the internal base-emitter capacitor in the transistor is eliminated by the constantly negative base-emitter voltage during the flyback period. The internal capacitors of importance are then the base-

collector and the collector-emitter capacitances. If a current probe was used instead of the shunt resistor, the connecting-lead to the extra transistor could be fed through the current probe measuring the collector current of the original transistor. In this way the capacitive current would automaticly be removed from the measurement. Unfortunately, the shunt resistor is necessary in order to have a fast response time when measuring the turn-off current, and the above compensation method is therefore impossible.

In order to get an idea of the amount of current through the capacitor C_2, the current is measured as shown in Fig. 5.19 with the current probe called CP. The measured capacitive current and the collector-emitter voltage are shown in Fig. 5.20 and Fig. 5.21, respectively. The maximum slope of the collector-emitter voltage is measured to approximately 600 V/µs and the maximum current through the capacitor to 45 mA which results in an approximated value of the internal capacitor C_2 to 75 pF.

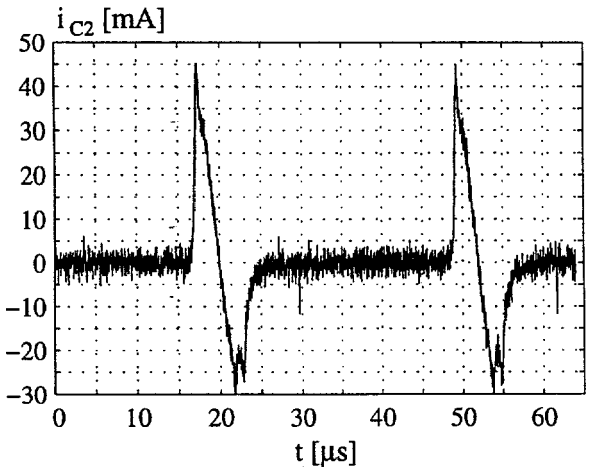


Fig. 5.20: *The current through the internal capacitor C_2 in the transistor at I_{Load} = 1 mA.*

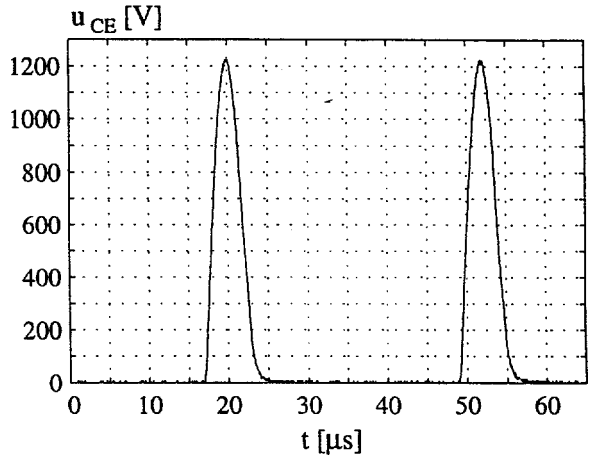


Fig. 5.21: *The collector-emitter voltage at I_{Load} = 1 mA.*

If not recognized, this capacitive current can easily lead to the conclusion that turn-off tails are present. The used method to prevent this is done in the data processing by forcing the current to zero after the turn-off is finalized. An example of the collector current and the collector-emitter voltage is shown in Fig. 5.22 and in Fig. 5.23.

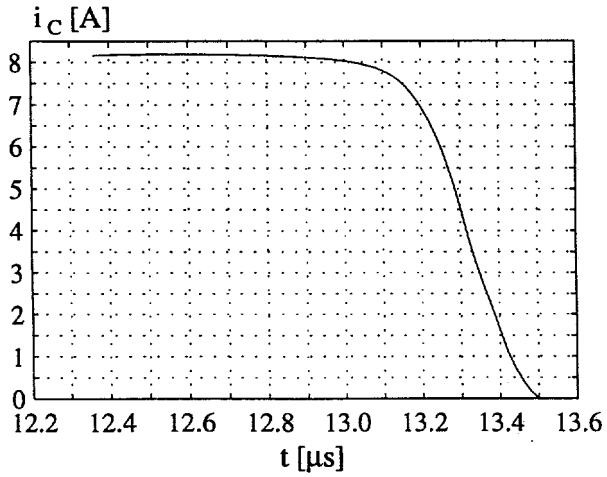


Fig. 5.22: *The collector current during turn-off of the transistor at I_{Load} = 1 mA.*

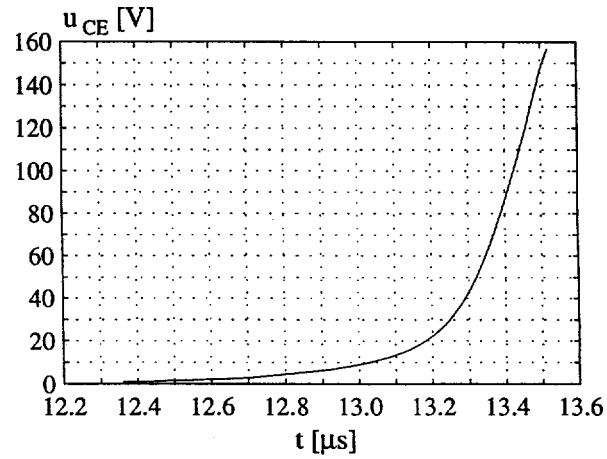


Fig. 5.23: *The collector-emitter voltage during turn-off of the transistor at I_{Load} = 1 mA.*

The measurement of the collector-emitter voltage is done by the same circuit topology as the one shown in Fig. 5.15. The only difference is the supply voltage which is increased to 160 V and the resistor that is increased to 6.6 kΩ.

At different load currents the power loss during the turn-off of the transistor is calculated as:

$$P_{turn-off} = \frac{1}{T}\int_{t_{on}}^{T} u_{CE} i_C dt \tag{5.7}$$

The voltage drop for the shunt resistor is of course substracted the measured voltage.

5.3.2 The measuring results

The results from the measurements on the drive circuit and the current pump are shown in Fig. 5.24 to Fig. 5.27 where the efficiency of the current pump and the drive circuit is calculated as

$$\eta_{pump,drive} = \frac{P_{base}}{P_{pump}} 100 \tag{5.8}$$

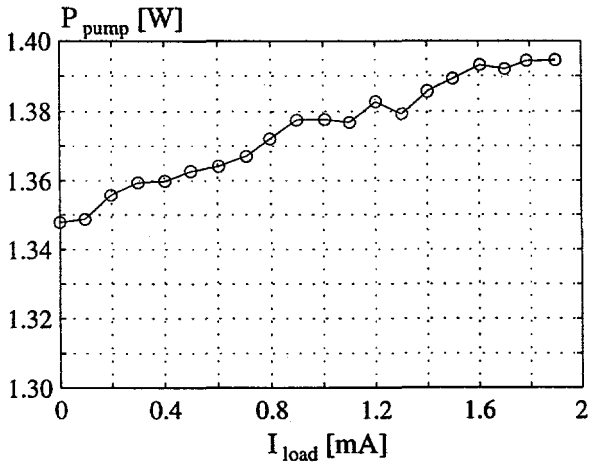


Fig. 5.24: *The power to the current pump.*

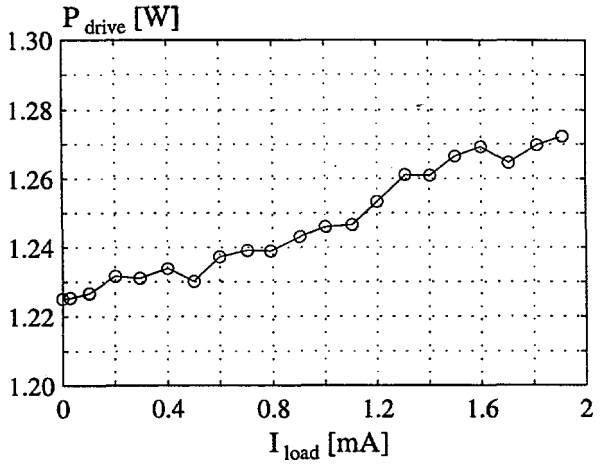


Fig. 5.25: *The power to the drive circuit.*

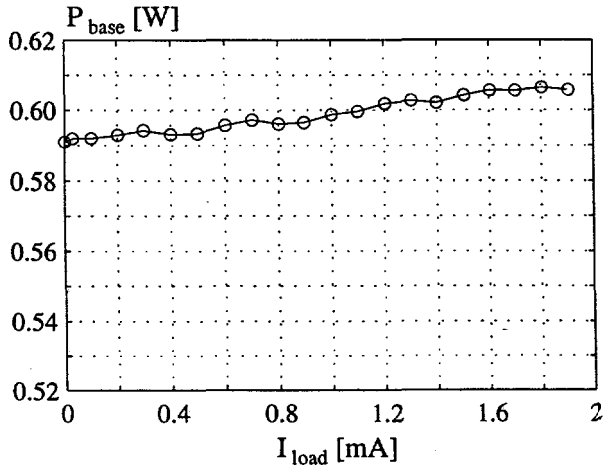


Fig. 5.26: *The power to the base of the transistor.*

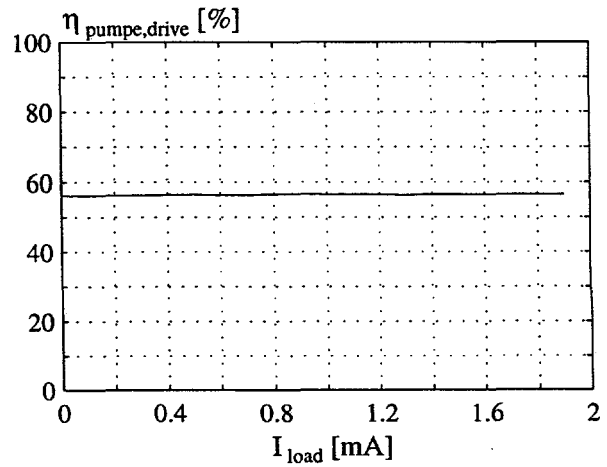


Fig. 5.27: *The efficiency of the current pump and the drive circuit.*

The power to the base of the transistor increases as a function of the load current due to the increased collector current. This demands more power to the drive circuit and the current pump as seen in the figures. The efficiency of the current pump and the drive circuit is nearly constant at a value of 58 percent.

The power losses in the on-state and the turn-off of the transistor are shown in Fig. 5.28 and Fig. 5.29 while the total power loss in the transistor is calculated by (5.9) and shown in Fig. 5.30.

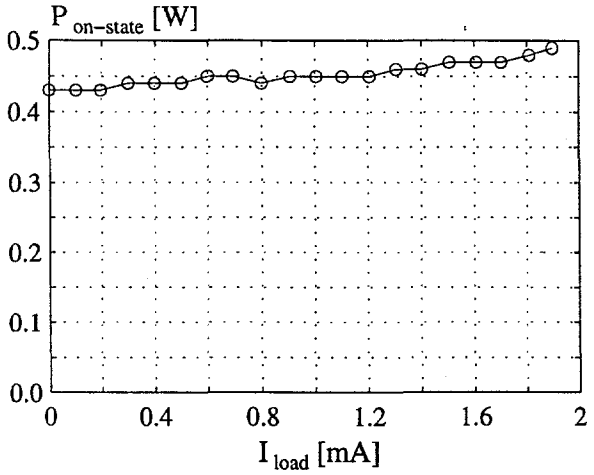


Fig. 5.28: *The on-state losses in the transistor.*

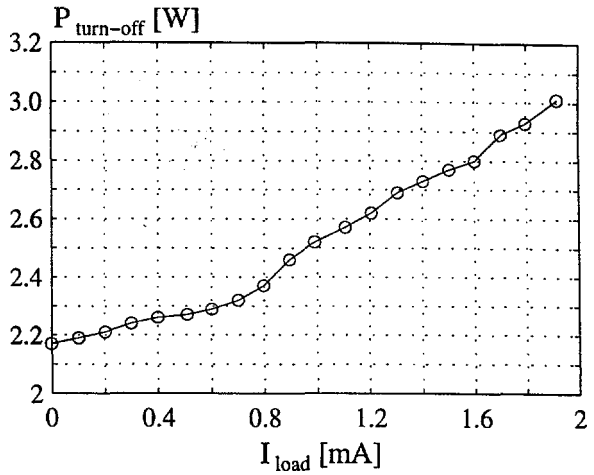


Fig. 5.29: *The turn-off losses in the transistor.*

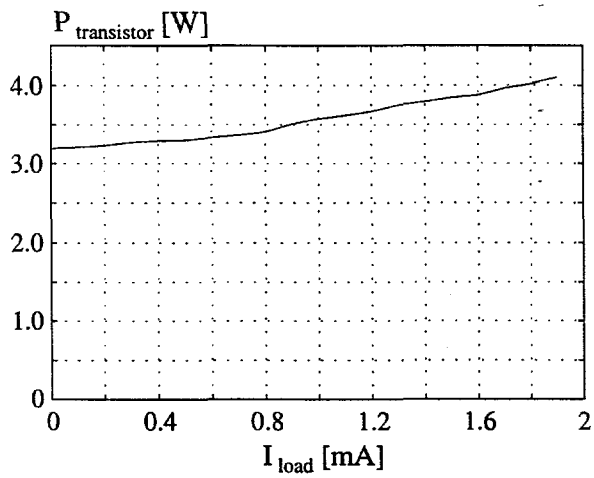


Fig. 5.30: *The overall power losses in the transistor.*

$$P_{transistor} = P_{on-state} + P_{turn-off} + P_{base} \qquad (5.9)$$

The measurements show that especially the turn-off power losses are very load dependent. It is therefore important to minimize the turn-off losses in the normal working area when the drive circuit is designed. It shall further be noticed that the power losses in the transistor are dependent on the width of the picture on the CRT in the original circuit at B&O. This phenomenon is of course not present due to the fact that the east/west transistor is ignored in the simplified deflection/EHT circuit. Thus, the width of the picture is always maximum which results in the maximum collector current at the actual load of the DST. If the east/west transistor was included, the power loss in the transistor would decrease due to the smaller collector current. Thus, the phenomenon has to be taken into account when designing the circuit in the original deflection circuit.

5.4 The deflection coil

The power loss in the deflection coil is impossible to measure by integrating the product of the voltage and the current due to the problem to measure the flyback voltage with a good accuracy.

Because thermal methods are disregarded, the only way, in the knowledge of the author, is to use the knowledge of the Fourier components in the deflection current. A method built on this knowledge is explained and the obtained results are presented.

5.4.1 The measuring method

The used method to measure the power loss in the deflection coil is built on the fact that it is the

reactive component in the deflection coil that primarily determines the shape of the current in the coil. In the light of this an air coil with the same inductance is used to replace the deflection coil by which the currents and the voltages in the rest of the deflection/EHT circuit remain the same.

The power losses in the deflection coil, P_{LY}, are then determined by the following method: The sum of the input power with the deflection coil replaced by the air coil and the power losses in the air coil is subtracted the input power measured in section 5.2, see (5.10).

$$P_{LY} = P_{input} - \left(P_{input,air\,coil} - P_{air\,coil}\right) \tag{5.10}$$

In Fig. 5.31 the measured inductance of the deflection coil and the constructed air coil are shown as a function of the frequency. The inductances in the deflection coil and the air coil are not completely alike, and another air coil should perhaps have been constructed with an inductance closer to the value in the deflection coil. This can be achieved by using a deflection coil with the ferrite shield removed.

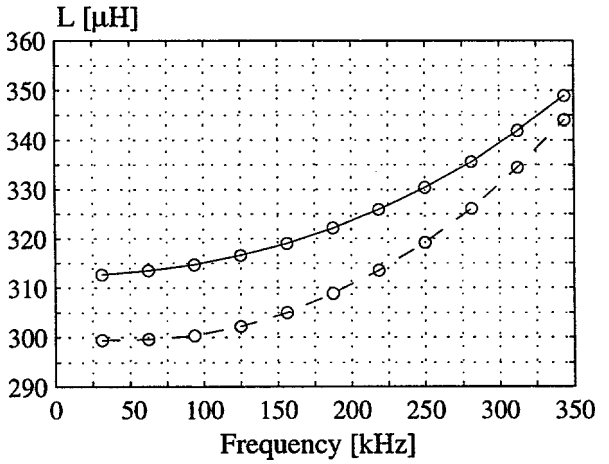


Fig. 5.31: *The inductance of the deflection coils (--: air coil, -: deflection coil).*

Anyway, the air coil is retained, and it can also be argued that the value of the inductance of the deflection coil shall be higher than the one in the air coil. This is because the inductance of the deflection coil might decrease due to saturation in the ferrite shield placed around the deflection coil when the deflection current is present instead of the signal current from the impedance analyzer.

In Fig. 5.32 the measured equivalent resistance of the deflection coil and the air coil are shown, and in Fig. 5.33 the current harmonics in the deflection coil are shown.

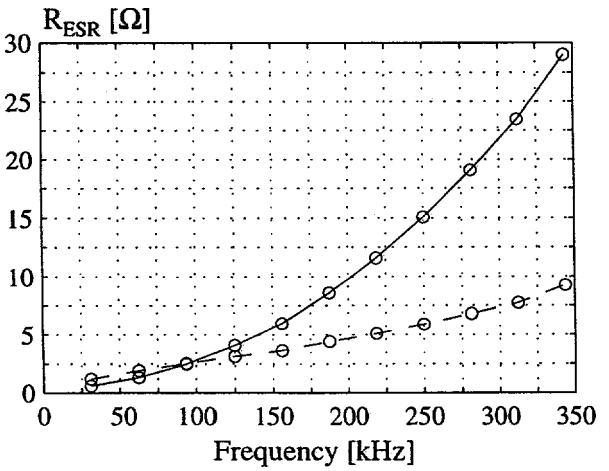


Fig. 5.32: *The equivalent resistance of the deflection coils (--: air coil, -: deflection coil).*

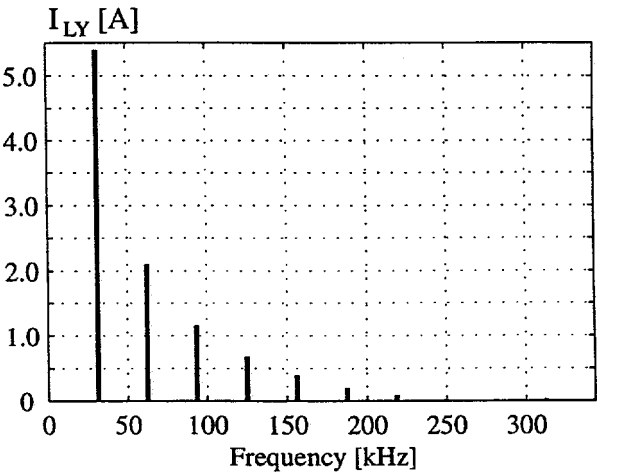


Fig. 5.33: *The current harmonics in the deflection current I_{LY}.*

The equivalent resistance of the coils is defined by

$$R_{ESR} = \frac{2\pi fL}{Q} \tag{5.11}$$

and is measured by the impedance analyzer. This resistance is measured at an ambient temperature of 20°C and is corrected to the actual temperature T of the windings during normal operation by

$$R_{ESR} = R_{ESR,20°C}\left(1+\alpha_{CU}(T-20)\right) \tag{5.12}$$

The overall power losses in the air coil are determined by adding the individual components at the most significant harmonics of the current. Taking the first 11 of the harmonics, the power loss in the air coil is calculated as

$$P_{aircoil} = \sum_{i=1}^{11} R_{ESR,aircoil}^{(i)}\left(I_{LY}^{(i)}\right)^2 \tag{5.13}$$

The input power to the deflection/EHT circuit with the air coil is measured in the same way as described in section 5.2, and is calculated as

$$P_{input,aircoil} = \frac{1}{T}\int_0^T \left(U_{DC}+u_{DC}\right) i_{prim}\,dt \tag{5.14}$$

The above method to measure the power losses in the deflection coil is encumbered with a lot of potential sources of errors. Some of them are:

- The difference in the inductance of the deflection coil and the air coil.
- The measurement of the actual winding temperature.
- The assumption that the skin and the proximity effects are current independent.

5.4.2 The measuring results

In Fig. 5.34 and Fig. 5.35 the input power and the power loss in the deflection coil are shown, respectively. The power loss in the deflection coil is almost independent of the load current as expected due to the same harmonic content in the deflection current. The mean value of the power loss in the deflection coil is $P_{LY} = 23.3$ W. At a first glance this seems as a rather high value, and in order to investigate the reasonable in the result, the power loss in the deflection coil is also calculated as

$$P_{LY,1} = \sum_{i=1}^{11} R_{ESR,defl.coil}^{(i)}\left(I_{LY}^{(i)}\right)^2 \tag{5.15}$$

where $R_{ESR,defl.coil}$ is the equivalent resistance of the deflection coil at the considered current harmonic and I_{LY} is the rms value of the current harmonic. The power loss in the deflection coil is in this way determined from the equivalent resistance measured by the impedance analyzer. The impedance analyzer does not measure the equivalent resistance at the correct amplitude of the current due to the fact that it only uses small signals. The power losses caused by the amplitude of the currents are in this way disregarded, and the result is expected to give less power loss than found by the method where the air coil was used. The results based on (5.15) are shown in Fig. 5.36.

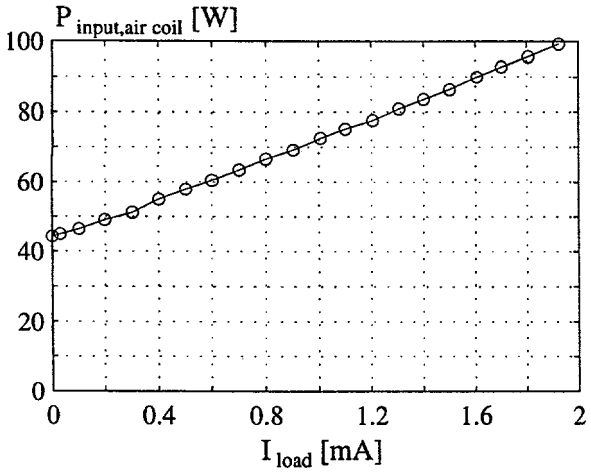


Fig. 5.34: *The input power to the deflection/ EHT circuit with the deflection coil replaced by the air coil.*

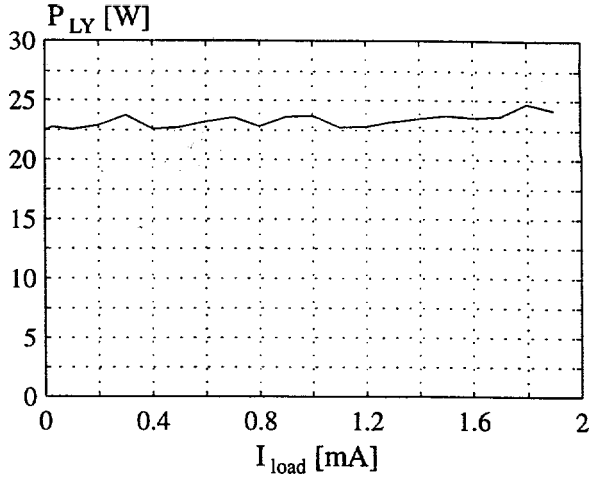


Fig. 5.35: *The power losses in the deflection coil calculated by use of the air coil.*

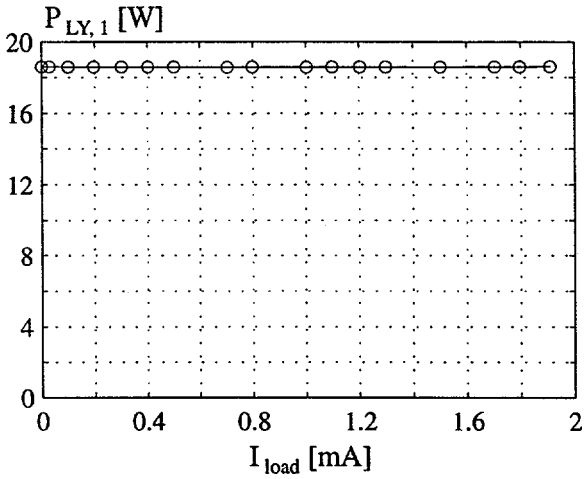


Fig. 5.36: *The power losses in the deflection calculated from (5-15).*

The power loss in the deflection coil calculated from (5-15) has a mean value of 18.5 W which is 4.8 W lower than the power loss measured by use of the air coil. This power loss is assumed to be the extra power loss in the ferrite shield in the deflection coil caused by the actual amplitude of the harmonics in the deflection current rather than the amplitudes used by the impedance analyzer when measuring the equivalent resistance. It would therefore be interesting to measure the equivalent resistance by an impedance analyzer that has the requisite power to deliver the actual current amplitude at the charateristical harmonics in the deflection current.

5.5 The power diodes

There are two power diodes in the deflection circuit, one in series with the transistor, D_5, and one in parallel with the transistor, D_6. The power losses in these diodes are determined in this section as the measuring method and the results are presented.

5.5.1 The measuring method

The power loss in the power diode D_5 is almost only caused by on-state power losses. The turn-on losses are negligible due to the zero-voltage switching of the transistor, and the turn-off losses are negligible because the flyback voltage almost is identical to the collector-emitter voltage. In the light of this, the circuit topology in Fig. 5.15 is used again. The only change from Fig. 5.15 is the connection of the cathode of the diode BA159, see Fig. 5.37.

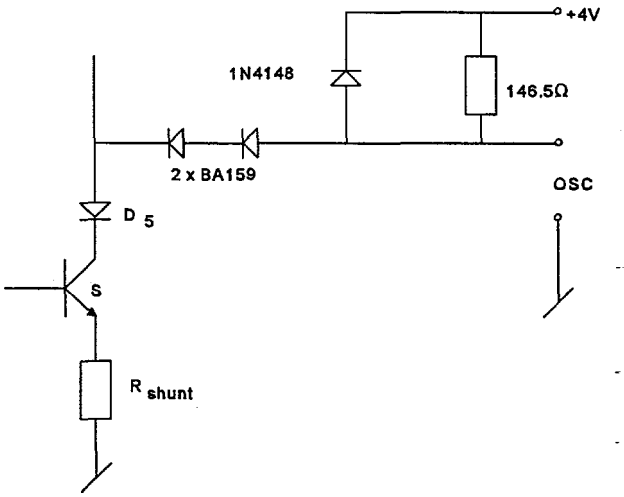


Fig. 5.37: *The measuring circuit used when measuring the on-state power losses in the power diode D_5.*

At different load currents the power loss during the on-state of the power diode D_5 is calculated as:

$$P_{D5,on-state} = \frac{1}{T}\int_0^{t_{on}} u_{fly} i_C dt - P_{on-state} \qquad (5.16)$$

The power loss in the power diode D_6 is caused by the turn-on, the on-state, and the turn-off losses. The on-state and the turn-off losses are measured with the circuit shown in Fig. 5.38. This circuit works in the same way as the circuit used to measure the on-state losses in the transistor except that the measured voltage has a negative polarity. The turn-on losses cannot be measured with the same circuit because the mode of operation of the circuit implies a current in the diodes 2xBA159 in order to measure a correct voltage on the oscilloscope. This is not the case at turn-on of D_6 where a very high forward recovery voltage appears due to the high slope of the current i_{C6}. Because no other circuit topology for measuring the voltage has been developed, the measurement of the voltage during turn-on is done by the 100x voltage probe. To get the best resolution as possible, the oscilloscope is adjusted to 20 V per division at the vertical scale. This causes an oversteering of the oscilloscope with the risk of forcing the oscilloscope into saturation. Anyway, it is the only solution at the present moment and is therefore used. It shall be pointed out that a correct calibration of the voltage probe is very important in this measurement.

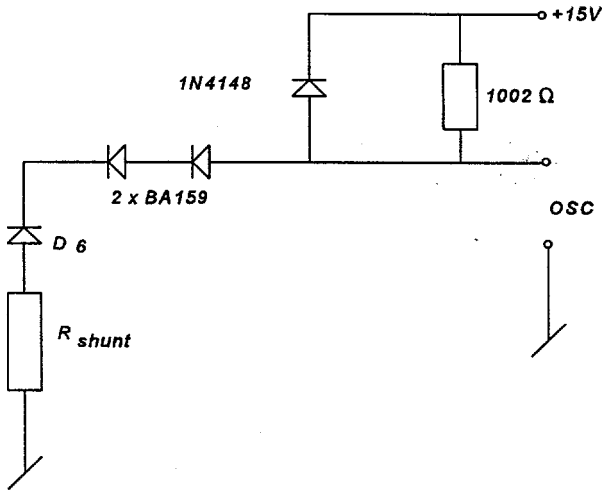


Fig. 5.38: *The measuring circuit used when measuring the on-state and the turn-off power losses in the power diode D_6.*

An example of the measured current and the voltage is shown in Fig. 5.39 to Fig. 5.42.

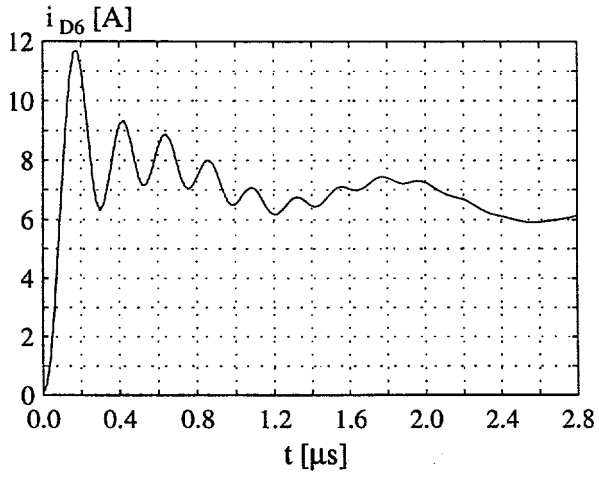


Fig. 5.39: *The current in D_6 during turn-on and the first part of the on-state at I_{Load} = 1 mA.*

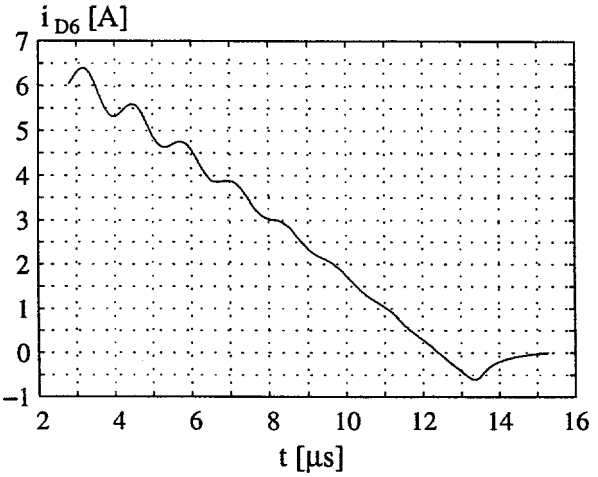


Fig. 5.40: *The current in D_6 during the last part of the on-state and the turn-off at I_{Load} = 1 mA.*

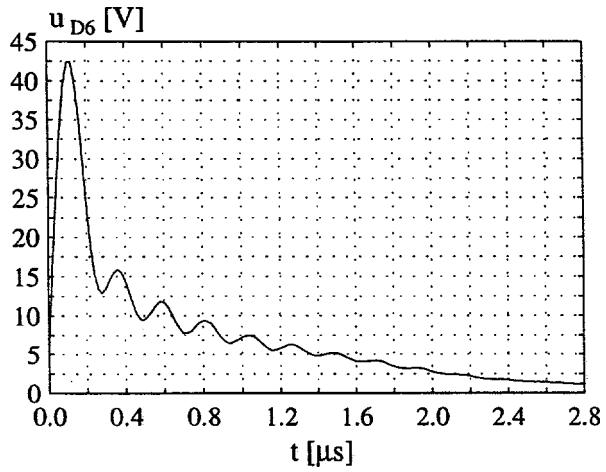


Fig. 5.41: *The voltage of D_6 during turn-on and the first part of the on-state at I_{Load} = 1 mA.*

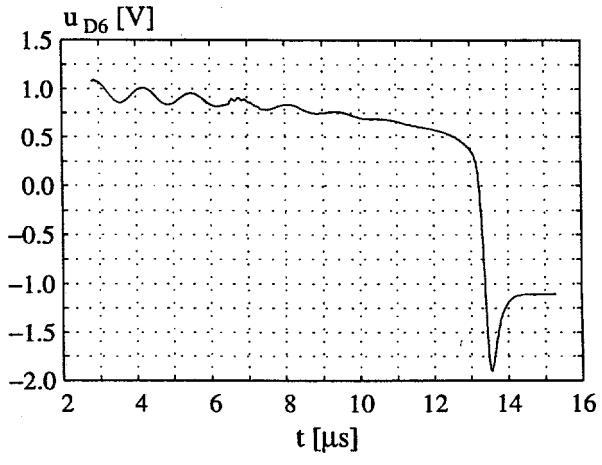


Fig. 5.42: *The voltage of D_6 during the last part of the on-state and the turn-off at I_{Load} = 1 mA.*

At different load currents the power loss in the power diode D_6 is calculated as:

$$P_{D6} = \frac{1}{T}\int_0^T u_{D6} i_{D6} dt \tag{5.17}$$

The voltage drop for the shunt resistor is of course subtracted the measured voltage.

5.5.2 The measuring results

The measured power loss in D_5 is shown in Fig. 5.43 and the power loss in D_6 in Fig. 5.44.

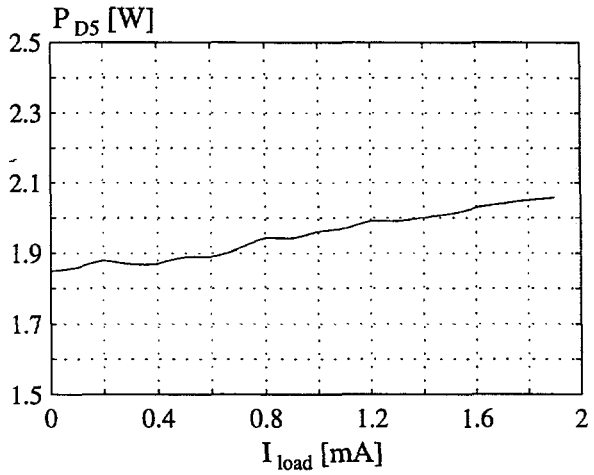


Fig. 5.43: *The power losses in the diode D_5.*

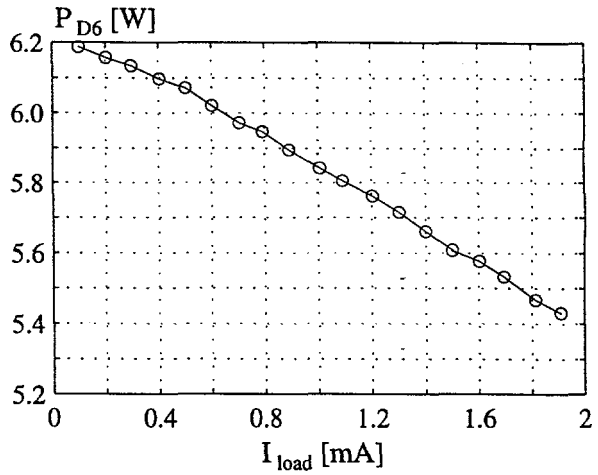


Fig. 5.44: *The power losses in the diode D_6.*

The power loss in the diode D_5 increases as a function of the load current due to the increased current in the diode. This is not the case for the power loss in the diode D_6 that decreases as a function of the load current. This is because the amplitude of the ringing on the current in D_6 decreases at a higher load current as explained in section 3.2.3. From the results it can be concluded that the power loss in the power diode D_6 is significant mainly caused by the high forward recovery voltage at the diode. The power loss in the diode D_6 is very considerable and an obvious source of error is the calibration of the voltage probe. The calibration is performed as described in section 5.1.2. Another and possibly more accurate method would be to rectify the forward recovery voltage on the diode D_6. The probe should then be calibrated in order to equal the peak voltage on the oscilloscope to the DC value on the multimeter minus a diode voltage of 0.7 V. This is not done and it is recommended that the measurements on the diode D_6 are replicated in order to investigate this source of error.

5.6 The capacitors

The power loss in the two capacitors C_S and C_{fly} are determined by using the series resistance in the capacitors, defined by:

$$R_{ESR} = \frac{\tan\delta}{2\pi f C} \tag{5.18}$$

The tanδ is dependent of the frequency, and for the capacitor C_S it is claimed in the data sheet that tanδ is about proportional to the frequency resulting in a constant equivalent series resistance. The maximum tanδ at 100 kHz is $15 \cdot 10^{-4}$ which corresponds to a R_{ESR} = 5 mΩ. Using the Fourier components of the deflection current the power loss in the capacitor C_S is P_{CS} = 90 mW.

As an approximation the same method is used for the capacitor C_{fly} even though the tanδ of the capacitor is frequency dependent. The maximum tanδ at 100 kHz is $15 \cdot 10^{-4}$ which corresponds to a $R_{ESR} = 5$ mΩ for the capacitor C_{fly}. Using the Fourier components of the current in C_{fly}, the power loss in the capacitor C_{fly} is $P_{Cfly} = 30$ mW.

This gives a total power loss in the two capacitor of $P_{capacitors} = 0.12$ W.

5.7 The diode split transformer

The power loss in the DST is measured by a simple indirect method due to the fact that it is very difficult to obtain meaningful measurements of the primary voltage. This is caused by the flyback voltage and its demands of a big voltage range and hence a poor resolution of the measurements. An example of the primary voltage is shown in Fig. 5.45.

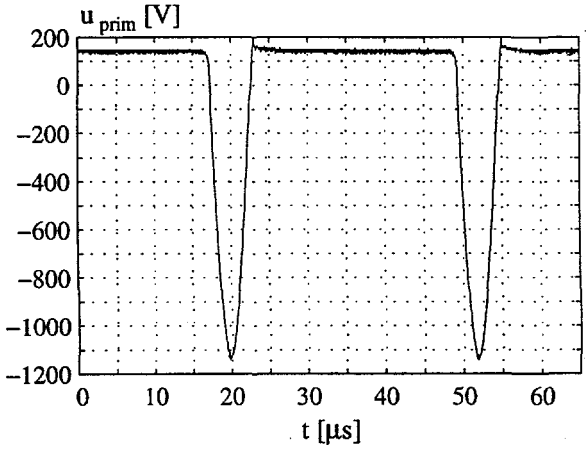


Fig. 5.45: *The primary voltage of the DST at I_{Load} = 1 mA. The measurement is performed on the circuit described in chapter 3.*

The used indirect method is presented in this section along with the results of the calculated power loss in the DST and the power loss in the focus and grid 2 potentiometers.

5.7.1 The measuring method

The used indirect method is as simple as to assume that the power loss in the DST, P_{DST}, is equal to the remaining losses after all the other measured power losses are subtracted the total power loss in the deflection/EHT circuit, see (5.19).

$$P_{bleeder} = \frac{(U_{eht} - U_{focus})^2}{R_{bleeder}}$$

$$P_{focus,G2} = \frac{U_{focus}^2}{R_{focus,G2}} \qquad (5.19)$$

$$P_{DST} = P_{input} - \left(P_{CRT} + P_{focus,G2} + P_{pump} + P_{transistor} + \overline{P}_{LY} + P_{D5} + P_{D6} + P_{Capacitors}\right)$$

In this way it is assumed that all the other measurements are accurate and performed at the same conditions regarding temperature and load. This is a considerable approach, but it is necessary because no other methods are available at the present moment without using thermal methods which are more time-consuming.

The output power from the DST is equal to the measured power to the CRT in section 5.2 as the power to the focus on the CRT is assumed to be zero according to the fact that the focusing is performed by an electrostatic field. All the other contributors to the power loss are measured in the previous sections so it is only the power loss in the bleeder resistance and the focus and grid 2 potentiometers that are to be measured in this section.

The bleeder resistance is a built-in resistance in the DST and has a value of $R_{bleeder} = 580$ MΩ while the focus and grid 2 potentiometers have a total resistance of $R_{focus,G2} = 130$ MΩ [3]. The power losses in these resistances are calculated as stated in (5.19).

5.7.2 The measuring results

In Fig. 5.46 and Fig. 5.47 the measured EHT and focus voltage are shown, respectively, and in Fig. 5.48 and Fig. 5.49 the calculated power loss in the bleeder resistance and focus and grid 2 potentiometers are shown.

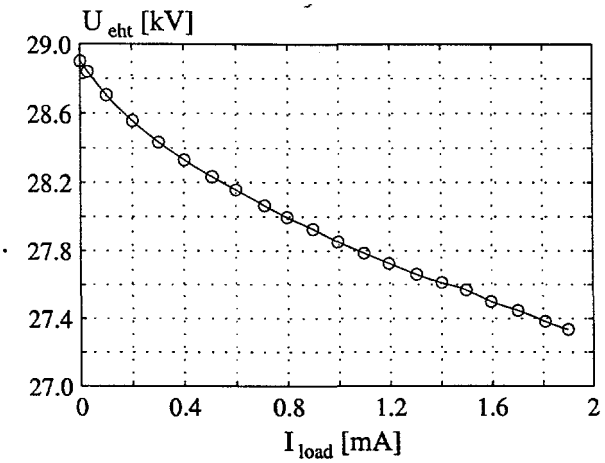


Fig. 5.46: *The generated EHT*

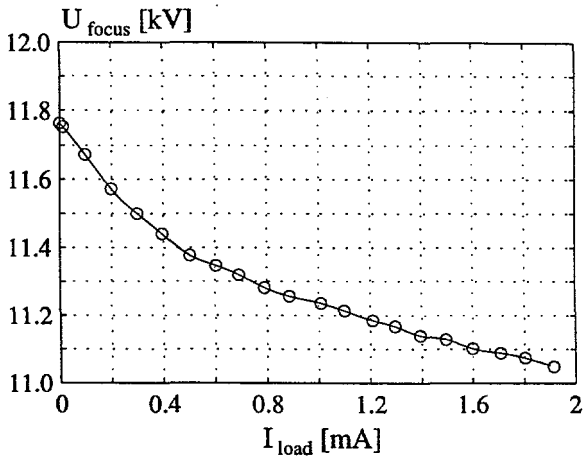


Fig. 5.47: *The voltage to the focus and the grid 2 potentiometers.*

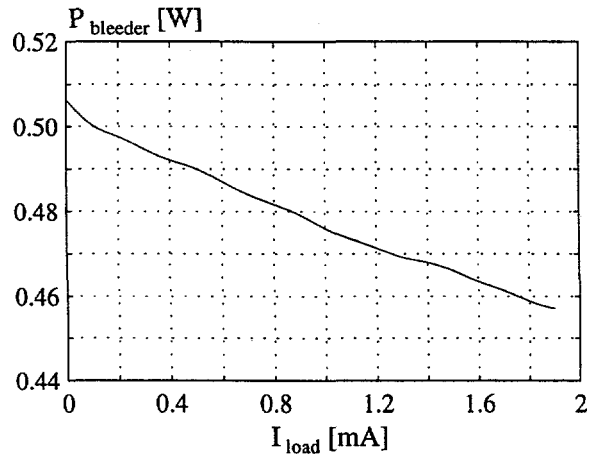


Fig. 5.48: *The power losses in the bleeder resistance.*

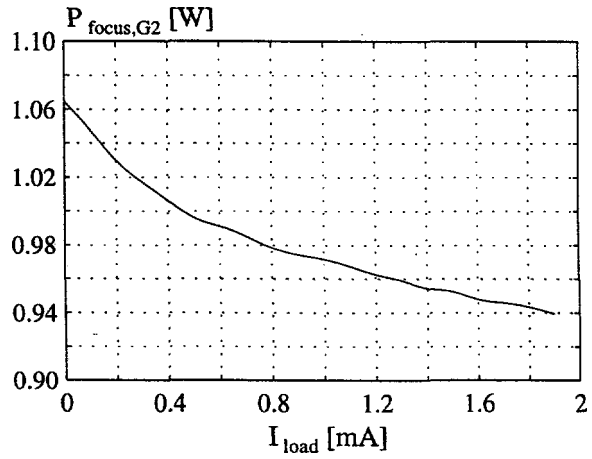


Fig. 5.49: *The power losses in the focus and grid 2 potentiometers.*

It is not surprising that both the EHT and the focus voltage decrease as functions of the load current and that the slope also change as function of the load current because this is due to the load dependent internal resistance in the DST. The power losses are in this way also load dependent and have the quality of decreasing as a function of the load current.

The power loss in the bleeder resistance is here considered as a part of the power loss in the DST due to the placement of the bleeder resistance in the DST which results in the calculated power loss in the DST as shown in Fig. 5.49.

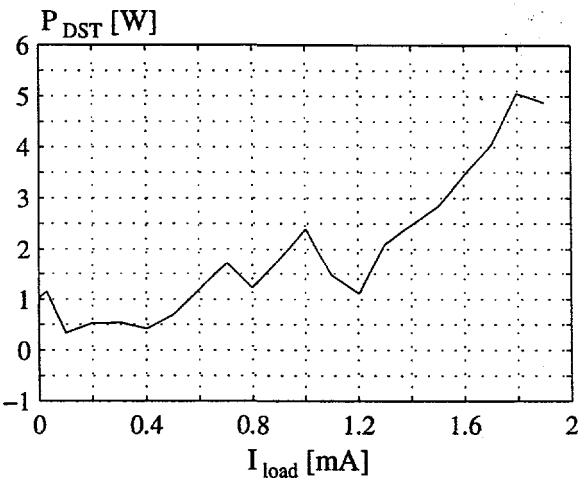


Fig. 5.50*: The power losses in the diode split transformer including the power losses in the bleeder resistance.*

The power loss in the DST is encumbered with errors due to the indirect measurement method. It is especially visible at small load current where the total power loss is below the power loss in the bleeder resistance - resulting in an efficiency above 100 percent! Anyway, an expected tendency is that the power loss increases in the DST as a function of the load current.

In the light of this result it can be concluded that the indirect method is unacceptable due to either the method itself or to the uncertainty of the other measurements as for example the input power and the output power. In order to investigate this, other methods have to be used and to be compared to the results obtained by the indirect method. Such measurements are not performed and documented in this report, but it would be interesting to do in the future work.

5.8 A survey of the power loss

The previous sections covering the measurements of the power losses in the deflection/EHT circuit provide the background for the valuation of the most critical components in relation to the power losses. The valuation is shortly treated in this section and the conclusion in chapter 6 provides further suggestions to interesting areas with relation to the minimization of the overall power loss.

In Fig. 5.51 to Fig. 5.55 the power losses in the deflection/EHT circuit are split up into the individual components in the circuit at different loads of the DST. The figures clearly illustrate that the majority of the power losses are placed in the deflection coil, and for that reason it is obvious to focus on the deflection coil in order to minimize the overall power loss in the deflection/EHT circuit. The diode D_6 and the transistor contribute also with a considerable amount of power loss and will also be of interest in the minimization of the power losses. In spite of the fact that the power losses in the DST are insignificant in the normal working area of the circuit, the ringing in the DST influences the power losses in the diode D_6 and the DST is in this way interesting in relation to the power losses. The other components are not of interest when minimizing the overall power losses.

For the future work it is therefore recommended that the focus shall be on the deflection coil, the transistor, and the diode D_6. These recommendations are treated in more details in chapter 6.

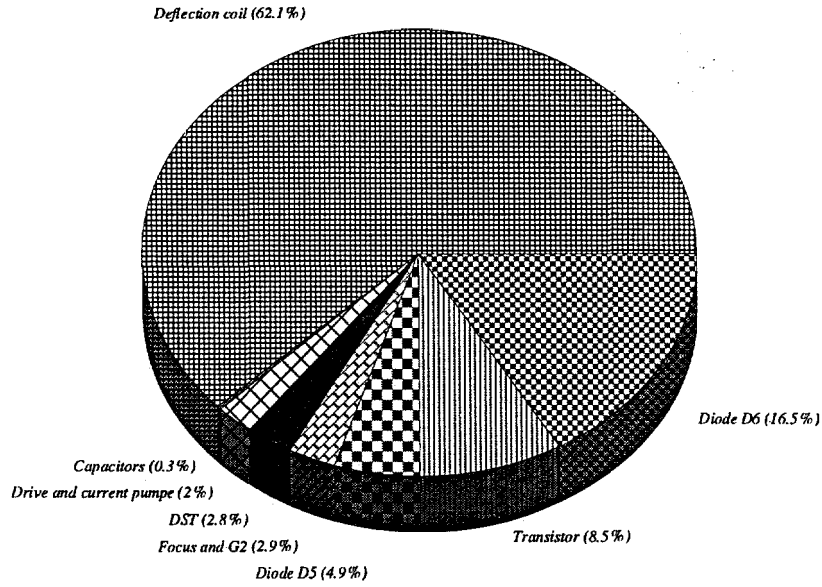


Fig. 5.51: *The power losses in the deflection/EHT circuit at no load where the total power loss is 38.1 W. The losses are split up into the individual components in the circuit.*

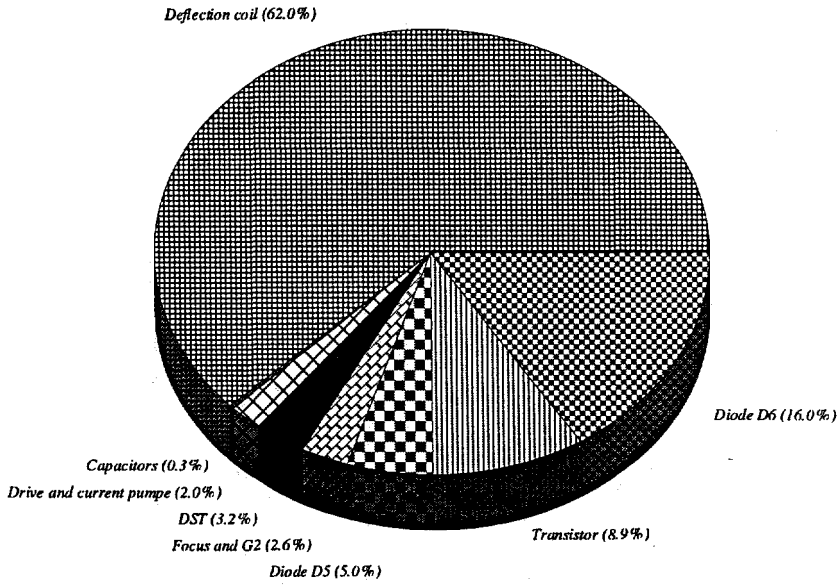


Fig. 5.52: *The power losses in the deflection/EHT circuit at I_{Load} = 0.6 mA where the total power loss is 38.2 W and the overall efficiency is 31.0 percent. The losses are split up into the individual components in the circuit.*

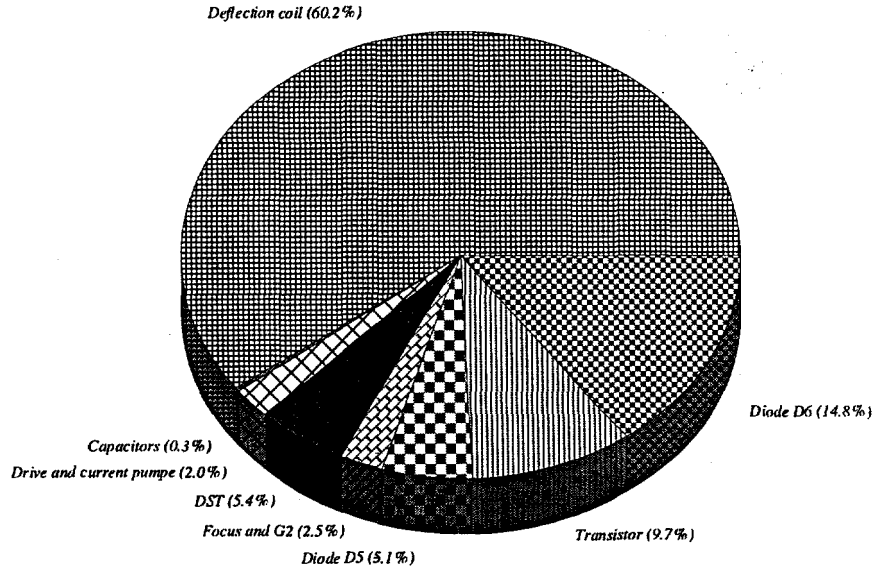


Fig. 5.53: *The power losses in the deflection/EHT circuit at I_{Load} = 1.3 mA where the total power loss is 38.7 W and the overall efficiency is 48.1 percent. The losses are split up into the individual components in the circuit.*

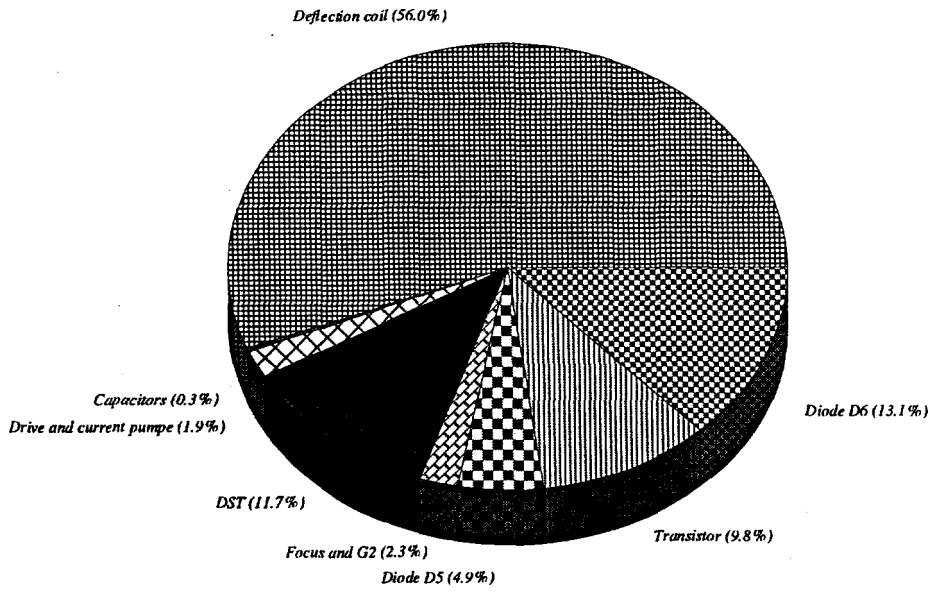


Fig. 5.54: *The power losses in the deflection/EHT circuit at I_{Load} = 1.9 mA where the total power loss is 42.2 W and the overall efficiency is 55.5 percent. The losses are split up into the individual components in the circuit.*

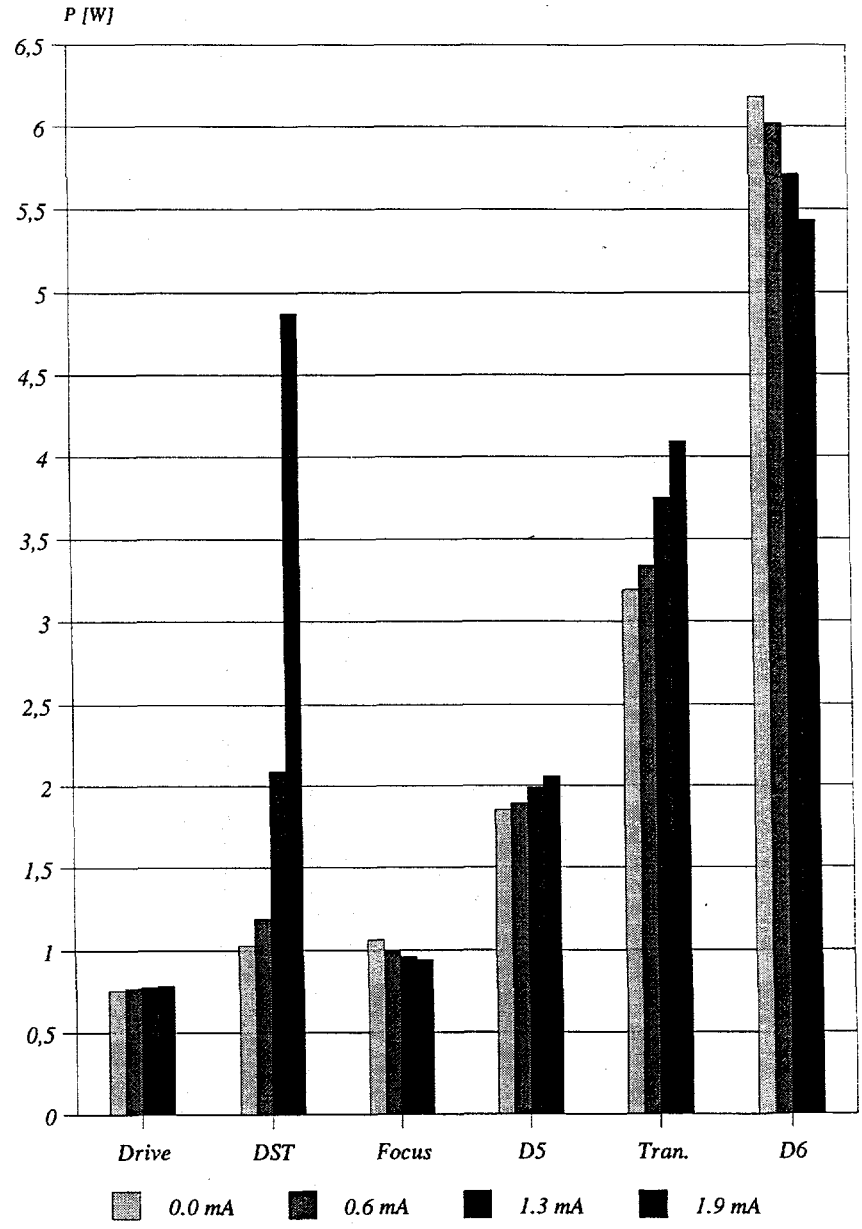


Fig. 5.55: *The measured power loss in the individual components at the four different load currents. The power losses in the capacitors and the deflection coil are considered independent of the load current and are therefore not shown.*

6 Conclusion

The aim of the this period of the project was to deliver the basis for the future work and to point out where to concentrate the work in the minimization of the power losses. The documentation of the obtained results is described in four chapters dealing with the following topics:

- Demarcation and general knowledge of the deflection/EHT circuit.
- Detailed knowledge obtained by evaluation of measured waveforms of a built laboratory model.
- Implementation of the circuit in Saber and comparison between the simulated and the measured waveforms.
- Mapping of the power losses by measurements.

In addition to the above documentation a list of relevant articles is given in supplement 1 and a list of patents in supplement 2. In the following a short summary with the conclusions of the individual chapters is given. Finally, proposals for the future work are presented.

6.1 Summary

In order to achieve a simple and a manageable circuit to analyse, the vertical deflection circuit is disregarded and the horizontal deflection/EHT circuit is simplified. In the simplified circuit the EHT generator and the deflection circuit are fully coupled and the east/west modulation and the linearity coil are among other facilities ignored. It is argued for that the simplification does not influence the basic mode of operation of the deflection/EHT circuit and the mode of operation is discussed by means of idealised considerations.

A laboratory model of the simplified deflection/EHT circuit has been built and connected in parallel to a 100 Hz television set. By doing this no control circuits are needed in the simplified circuit. Measurements on the simplified deflection/EHT circuit are carried out at three different loads of the DST. The measurements are focused on the voltage and the current waveforms on a circuit level and the influence of the parasitic components is discussed. Besides, a comparison of the waveforms at three different loads is performed and comments and conclusions are presented.

A general introduction to the facilities in Saber highlights the primary difference between Spice and Saber with focus on the basic architecture of Saber. The procedure of simulating the simplified deflection/EHT circuit is explained and the demarcations are presented. The simulation is performed with both idealised models of the components and with existing models of the components in Saber. The models of both types of components are shortly presented. The simulated waveforms are in close agreement with the measured waveforms apart from the ringing primary caused by the parasitic components in the DST which are not included in the simulation model.

The measuring system, the general measuring process and the data processing used when mapping the power losses in the simplified deflection/EHT circuit are explained. The measurements are performed at the working temperature of the components and at different loads of the DST. The power losses in the individual components are determined by the current through and the voltage across the components. The only exception from this procedure is the measurement of the power losses in the deflection coil, the DST, and the capacitors. The power losses in these components are found by indirect methods. In the normal working area of an average picture in a television, the overall efficiency is approximately 30 percent and the major part of the power loss is concentrated in the deflection coil. Moreover, the transistor, the diodes, and the DST contribute significantly to the overall power loss.

The results and the conclusions from the work documented in this report can be outlined as:

- The simplified deflection/EHT circuit is capable of showing the basic mode of operation of the deflection/EHT circuit.
- Idealized considerations are usable to explain the basic mode of operation, but a more detailed understanding of the circuit is only achieved by considering the parasitic components.
- Especially the operation of the DST is connected with parasitic components, as the stray capacitors and the stray inductors strongly influence the current and the voltage waveforms.
- The simulations in Saber give rather good results on a circuit level even with idealised component models.
- A model of the DST is necessary in order to achieve more accurate simulation results both of the generation of the EHT and of the waveforms in the deflection circuit.
- The existing models of the semiconductor devices are sufficient in circuit level simulations. However, it is necessary to alter the values of the model parameters for some of the components.
- Simulating a time period in the circuit takes only a 3-4 seconds after the circuit has been stable which takes approximately 10 minutes.
- Simulation of the power losses has not been performed. The models of the semiconductors might be accurate enough but a model of the DST and of the deflection coil are necessary. These models should describe both the iron losses and the winding losses.
- The measurements of the power loss in the deflection/EHT circuit are critical due to the available instruments. Especially the equipment used to measure the EHT is difficult to get with satisfactory accuracy.
- The used method to measure the power loss in the deflection coil and in the DST is critical.
- The power loss in the diode D_6, see supplement 4, seems rather high and it might be due to wrong measurements or the calibration procedure.
- The ringing in the DST influences the power loss in especially the diode D_6.
- The power losses are mainly concentrated in the deflection coil - approximately 60 percent of the overall power loss in the deflection/EHT circuit. However, the power losses in the transistor, the diodes, and the DST are also significant.

In addition to the above concrete results from the performed work, the author has obtained some experience in the following areas:

- The basic mode of operation of the deflection/EHT circuit
- The simulation with Saber
- The method of measuring the power losses

These experiences are of course available for the person who takes over the project.

6.2 The future work

In order to fulfil the purpose of the project the remaining two thirds of the project time shall focus on the critical components in relation to the power losses. The critical components are as mentioned the deflection coil, the diode split transformer, the power diodes, and the transistor. However, the diode split transformer will be treated in details in the Ph.D. project "Modelling and Design of Deflection/EHT in Televisions", and it serves no purpose to treat it in this project too.
The following topics are of interest in order to fulfil the purpose of the project, and the person who takes over the project can use them as a platform when he makes up the schedule for the remaining of the project:

The transistor:

a) To determine the parameters for the transistormodel in Saber so that it is possibly to simulate the power losses in the transistor as a function of the design of the drive circuit.
b) To analyse the possibility of using an IGBT or a MOSFET instead of the bipolar transistor in order to obtain a more simple drive circuit and/or a less amount of power loss.
c) If the result from b) is positive, a deflection circuit with the chosen switch and the chosen drive circuit could be designed and built.

The diodes:

a) To carry out new measurements of the power loss in the diode D_6.
b) To analyse the possibility of using new types of diodes with reference to minimize the power loss.
c) To determine the parameters for the diode models in Saber so that it is possible to simulate the power losses and thereby especially the turn-on.

The deflection coil:

a) To investigate other ways of measuring the power loss in the deflection coil. Thermal methods might be a solution.
b) To investigate the possibilities of using e.g. lits wire and/or other ferrite materials in the deflection coil.
c) To make a model in Saber of the deflection coil that takes into account the winding losses and the ferrite losses.

As mentioned in chapter 2 a linearity coil is placed in series with the deflection coil in the deflection circuit in use at B&O. This linearity coil is omitted in the power measurements in order to simplify the circuit and to get a less number of measurements. In this way the power loss in the linearity coil and its influence on the overall power losses are unknown, and it might be of interest to investigate the influence of this demarcation. In relation to this a model in Saber of the linearity coil is of course of interest in order to simulate both its influence on the deflection circuit and its power loss.

Besides the above, the following topics are of interest:

- To set up simple equations for the power losses in the individual components in the deflection/ EHT circuit.
- To consider new topologies for the deflection circuit and the EHT generator.
- To change the voltage level U_{DC} and u_{fly} in the deflection circuit so for instance semiconductors rated to a lower voltage could be used and thus result in a lower power loss. However, this might be very difficult due to the design of the deflection coil, because the value of the inductance is strongly determined by the actual picture tube. If changes in the value of the inductance are wanted it is therefore necessary to involve the manufacturer of the deflection coil and the picture tube.
- To make it possible to simulate the temperature of the components in Saber.

List of abbreviations

ABSTOL	: Best accuracy of currents
A/D	: Analog to digital converter
B	: The base of a BJT
B	: Blue
BJT	: Bipolar Junction Transistor
B&O	: Bang & Olufsen
CAE	: Computer Aided Engineering
CHGTOL	: Best accuracy of charges
CP	: Current Probe
CRT	: Cathode Ray Tube
CTV	: Color TeleVision
D/A	: Digital to analog converter
DST	: Diode Split Transformer
E	: The emitter of a BJT
EHT	: Extreme High Tension
EMI	: ElectroMagnetic Interference
G	: Green
H	: Horizontal
IF	: Intermediate Frequency
OSC	: OscilloSCope
PLL	: Phase-Locked Loop
R	: Red
RELTOL	: Relative accuracy of voltages and currents
Sync.	: Synchronization
TV	: TeleVision
V	: Vertical

List of symbols

a	:	The slope of the decreasing diode current.
C	:	Capacitor.
C_1	:	The parasitic capacitor between the collector and the heat sink.
C_2	:	The internal capacitor between collector and emitter of the transistor S.
$C_{1,2}$	:	The capacitors in the drive circuit.
$C_{3,4}$	:	The capacitors in the current pump.
C_5	:	Equal to C_{CRT}.
$C_{6,7}$	:	The capacitors used in the measurements of the EHT and I_{Load}.
C_{CE}	:	The internal collector-emitter capacitor in the transistor S.
C_{CRT}	:	The equivalent capacitor from the cathode to the aquadag coating of the CRT.
C_{fly}	:	The flyback capacitor in the deflection circuit.
C_k	:	The coupling capacitor between the EHT generator and the deflection circuit in the original deflection/EHT circuit.
C_m	:	The capacitor in the east/west modulation circuit.
C_S	:	The S-capacitor in the deflection circuit.
C_{sf}	:	The series connection of C_S and C_{fly}.
$D_{1,2}$	:	The diodes in the drive circuit.
$D_{3,4}$	:	The diodes in the current pump.
D_5	:	The diode in series to the transistor S.
D_6	:	The diode in parallel with the transistor S.
f	:	Frequency.
H-drive	:	The drive signal to the horizontal drive circuit.
i	:	Counter.
i_B	:	The base current in the transistor S.
i_C	:	The collector current in the transistor S.
i_{C2}	:	The current through the capacitor C_2.
i_{Cfly}	:	The current through the capacitor C_{fly}.
$i_{D,2xBA159}$	:	The current through the two diodes BA159.
i_{D6}	:	The current through the diode D_6.
i_{drive}	:	The current to the drive circuit.
I_{Load}	:	The mean value of the current to the CRT.
$\hat{I}_{Load}$	:	The peak value of the current to the CRT.
i_{LY}	:	The current through the inductance L_Y.
i_{prim}	:	The primary current in the DST.
i_{pump}	:	The current to the current pump.
I_{RM}	:	The minimum value of the current through the diode D_6.
i_{sec}	:	The current to the CRT.
L	:	Inductance.
L_{Lin}	:	The linearity coil.
L_{supply}	:	The inductance in series with the supply voltage in the original deflection circuit.
$L_{T1,prim}$	:	The inductance of the primary of the drive transformer T1.
$L_{T1,stray}$	:	The stray inductance of the drive transformer T1.
L_Y	:	The deflection coil.
L_{yp}	:	The parallel connection of L_Y and L_{prim}.
n_{DST}	:	The winding ratio of the DST.
N_{focus}	:	The number of windings on the focus tab.
N_{sec}	:	The total number of the secondary windings on the DST.
n_{T1}	:	The winding ratio of the transformer T1.
$P_{air\ coil}$	:	The power loss in the air coil.
P_{base}	:	The power to the base of the transistor S.
$P_{bleeder}$	:	The power loss in bleeder resistance.
$P_{capacitor}$	:	The power loss in the capacitors C_S and C_{fly}.
P_{Cfly}	:	The power loss in the flyback capacitor C_{fly}.
P_{CRT}	:	The power to the CRT.
P_{CS}	:	The power loss in the S-capacitor C_S.
P_{D5}	:	The total power loss in the diode D_5.
$P_{D5,\ on\text{-}state}$	:	The power loss during the on-state of the diode D_5.
P_{D6}	:	The total power loss in the diode D_6.
P_{drive}	:	The power to the drive circuit.
$P_{focus,\ G2}$	:	The power loss in the focus and grid 2 resistance.
P_{input}	:	The input power to the deflection/EHT circuit.
$P_{input,\ air\ coil}$	:	The input power with the deflection coil replaced by the air coil.
P_{loss}	:	The total power loss in the deflection/EHT circuit.
P_{LY}	:	The power loss in the deflection coil.
$P_{LY,1}$	:	The power loss in the deflection coil determined from the equivalent resistance.
$P_{on\text{-}state}$	:	The power loss during the on-state of the transistor S.
P_{pump}	:	The power to the current pump.
$P_{transistor}$	:	The total power loss in the transistor S.
$P_{turn\text{-}off}$	:	The power loss during the turn off of the transistor S.
Q	:	The Q-factor of an inductance.
Q_s	:	The charge transformed to the primary of transformer T1 that accounts for the negative base current during turn-off.
r	:	The ratio of N_{focus} and $N_{bleeder}$.
R_{1-13}	:	The resistors in the simplified deflection/EHT circuit.
R_{base}	:	The resistor connected in parallel with the base of the transistor S.
$R_{bleeder}$	:	The bleeder resistance in the DST.
R_{eq}	:	The equivalent resistor for the bleeder and the focus resistor.
R_{ESR}	:	The equivalent resistance of a coil.
$R_{ESR,20°C}$	:	The equivalent resistance of a coil at a temperature of 20°C.
$R_{ESR,\ air\ coil}$	:	The equivalent resistance of the air coil.
$R_{ESR,defl,coil}$	:	The equivalent resistance of the deflection coil.
R_{focus}	:	The focus resistor.

R_{shunt} : The shunt resistance.
S : The transistor in the deflection circuit.
S_{EW} : The transistor in the east/west modulation circuit.
t : Time.
T : The time periode of the deflection circuit, 32 µs.
T1 : The drive transformer in the drive circuit.
T_I : The time from the diode current starts to decrease untill it is at the minimum value I_{RM}.
tanδ : The dissipation factor in the capacitors.
T : Temperature in °C.
T_{fly} : The flyback time in the deflection circuit.
tm : The transit time of the base.
t_{on} : The time in which the transistor is in the on-state.
TR1 : Transistor in the drive circuit.
TR2 : Transistor in the drive circuit.
TR3 : Equal to S.
tsw : The charge sweep-out time.
tt : The carrier life time.
u_{BE} : The base-emitter voltage of the transistor S.
$u_{BE,TR2}$: The base-emitter voltage of the transistor TR2.
u_{CE} : The collector-emitter voltage of the transistor S.
$u_{CE,TR2}$: The collector-emitter voltage of the transistor TR2.
u_{CS} : The voltage across the S-capacitor C_S.
$u_{D,2xBA159}$: The voltage across the two diodes BA159.
u_{D4} : The voltage across the diode D_4.
u_{D6} : The voltage across the diode D_6.
u_{DC} : The supply voltage to the deflection/EHT circuit.
u_{drive} : The voltage to the drive circuit.
$u_{drive,ac}$: The a.c. content of the voltage to the drive circuit.
u_{EHT} : The EHT voltage.
$u_{EHT,ac}$: The a.c. content of the EHT voltage.
u_{fly} : The flyback voltage.
$\hat{u}_{fly}$: The peak value of the flyback voltage.
u_{focus} : The voltage to the focus on the CRT.
u_{G2} : The voltage to grid 2 on the CRT.
u_{prim} : The voltage across the primary of the DST.
u_{pump} : The voltage across the input to the current pump.
u_{snub} : The voltage across the snubber capacitor in the drive circuit.
α_{CU} : The temperature coefficient for copper.
δ : The duty-cycle of the transistor TR2.
$\eta_{pump,drive}$: The efficiency of the current pump and the drive circuit.
η_{sys} : The overall efficiency of the deflection/EHT circuit.
τ_{rr} : The reverse recovery time constant.

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Supplement 1

List of articles

List of articles

The list of articles is divided into the following areas:

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- Various on High Frequency Techniques

- Power Diodes
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