Audio Power Amplifier Techniques With Energy Efficient Power Conversion

Volume I

Ph.D. Thesis

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Contents

Preface

This thesis is submitted to the Technical University of Denmark in partial fulfillment of the requirements for the Doctor of Philosophy degree (Ph.D degree). The work has been carried out at the Department of Applied Electronics, DTU (until 1/12-1997 Institute of Automation) and at Bang&Olufsen A/S, Denmark during the period April 1. 1995 to April 30. 1998. The project has involved four cooperating parties: Department of Applied Electronics, Bang&Olufsen A/S, CETEC and The Danish Energy Agency. All parties are thanked for the optimal working conditions in the project.

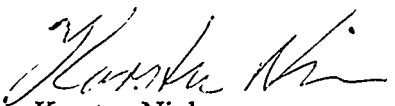
After receiving the M.Sc.E.E. degree in October 1994 at the Technical University of Denmark, I was recommended for the present project by assoc. professors Michael A. E. Andersen and John. Aa. Sørensen. I am deeply grateful for the confidence that made my participation in this exiting project possible. Michael A. E. Andersen has functioned as main supervisor in the project, and is thanked for the never failing support, and for sharing his knowledge in power electronics.

I should like to thank a number of people at Bang & Olufsen A/S for their contributions, help and support. Senior Technology Manager Palle Nissen is thanked for providing everything I needed during my stays at B&O. Audio Design Manager Egon Bjerre is thanked for sharing his invaluable knowledge on analog design. Everybody at the Electroacoustics R&D department are thanked for providing a stimulating frame during the numerous stays there. Especially, the assistance with practical implementation and subjective evaluation of various concepts has been of great value to the research.

My students at DTU during three years, in particular Frank. S. Christensen, Thomas Frederiksen, Thomas Taul, Poul Ciok, Søren Due, Niels Anderskouv and Claus Neesgaard are thanked for their contributions to the present work. All have helped with the implementation and evaluation of various ideas and concepts during their M. Sc. and graduate projects. Furthermore, I am grateful to a number of other experts in the field with whom I have had enlightening discussions. Professor Keyue Smedley and Ph.D student Mark Smith Jr. are thanked for many interesting discussions on various topics at the University of California, Irvine during the four months I spent there in 1997. Professor John Vanderkooy, University of Waterloo, Canada, is thanked for inspiring discussions on various subjects in the field during his stay at B&O. My friend Mohammad Shajaan is thanked for his assistance in proofreading the manuscript.

Lastly, I should like to thank my fianceé and family or years of support and patience. This foundation has been of primary importance during the three years.

Lyngby, April 30, 1998



Karsten Nielsen

Abstract

The audio power amplifier pays an essential role in every system that generates audible sound. General power amplifies are voluminous, heavy, expensive, unreliable and have a very poor energy utilization, all due to a low efficiency. Solutions to this very fundamental problem is the topic of the present thesis. The ultimate goal is to develop practical metods for power amplifcation with a signifiantly higher efficiency at all levels of operation without compromises on the audio performance. The problem is addressed by investigating new methods for efficient power amplification using pulse modulation techniques. A general *Pulse Modulation Amplifier* (PMA) consists of a pulse modulator (analog or digital), a switching power stage for power conversion and a control system.

A fundamental study of both analog and digital pulse modulation methods is carried out. A novel class of multi-level pulse modulation methods - *Phase Shifted Carrier Pulse Width Modulation (PSCPWM)* - is introduced and show to have several advantageous features, primarily caused by the much improved synthesis of the modulating signal. Enhanced digital pulse modulation methods for digital PMA systems are investigated, and a simple methodology for digital PWM modulator synthesis is devised. It is concluded, that the modulator performance is not a limitation in the system, regardless of the domain of modulator implementation.

Power conversion in PMA systems is addressed from the perspectives of both linearity and efficiency optimization. Based on detailed studies of the distortion mechnanisms in the power conversion stage it is concluded, that this is the fundamental limitation on system performance due to several physical limitations. The analysis of general power stage efficiency concludes that dramatic improvements in energy efficiency are possible with PMA systems that are optimized for efficiency.

Control systems has been a focal point in the research. A control system design methodology is devised as a platform for synthesis of robust control systems. Investigations of three fundamental control structures show that even simple control systems offer a remarkable value, although the considered topologies also have their limitations which is verified by practical evaluation in hardware. A novel control method is introduced - *Multivariable Enhanced Cascade Control (MECC).* Essentially, the topology offers a practical method for higher order control system implementation by an enhanced cascade structure. MECC provides flexible control over all essential system parameters and is furthermore simple in realization. Practical evaluation of a MECC based PMA shows state-of-the-art performance.

The application of non-linear control methods is investigated with the introduction of an enhanced non-linear control/modulator topology. Although the non-linear controller is theoretically interesting, the method proves to suffer from various practical limitations.

As a contribution to the field of digital PMA systems, a novel pulse referenced control method – *Pulse Edge Delay Error Correction (PEDEC)* – is introduced for enhanced amplification of an already pulse modulated signal. The principle proves to force equivalence between the digital modulator output and the digital PMA output. PEDEC is believed to be the first documented method for practical, efficient and high quality digital PMA realization including compensation for the non-linear power conversion.

Resumé på dansk

Audio effektforstærkeren er en helt grundlæggende komponent overalt hvor der skal laves hørbar lyd. Generelle effektforstærkere er volumiøse, tunge, kostbare og har tillige en meget dårlig energivirkningsgrad, altsammen som følge af en dårlig effektivitet. Løsninger på dette helt fundamente problem er emnet for denne afhandling. Målet med projektet er således at udvikle pratiske metoder til effektforstærkning med et signifikant lavere effekttab i alle brugssituationer uden at kompromitere kvaliteten. Problemet angribes ved at undersøge nye methoder for effektiv effekforstærkning baseret på pulsmodulations-teknikker. En generel *Pulse Modulation Amplifier* (PMA) er opbygget af en puls modulator (analog eller digital), en switchende effektsomsætningsenhed og et reguleringssystem.

En fundamental analyse analoge og digitale pulsmodulationsmetoder gennemføres. En ny klasse af multi-niveau pulse bredde modulation methoder - *Phase Shifted Carrier Pulse Width Modulation (PSCPWM)* – introduceres herunder og viser at have flere fordelagtige egenskaber, primært skabt som følge af den meget forbedrede synthese af det modulerende signal. Metoder til realisering af digital pulsmodulation undersøges endvidere, og der udvikles en simpel design metodologi til digital PWM modulator syntese. Det konkluderes generelt, at modulatoren ikke er en begrænsning i systemet uanset hvilket domæne der vælges for implementeringen.

Effektomsætning til PMA systemer analyseres udfra såvel et linearitets- og effektivitets-perspektiv. På basis af detaljerede analyser af forvrængningskilder i effektomsætningen konkluderes det at dette element er den væsentlige begrænsning is systemet, som følge af en række fysiske begrænsninger. Analyserne af udgangstrin omfatter også en generaliseret teoretisk analysis af effektiviten i effektomsætningen. Det komkluderes, det der kan opnås dramatiske forbedringer i energi effektivitet i PMA systemer optimeret mht. effektivitet.

Reguleringsmetoder udgør en helt central del af undersøgelserne. En metodologi til design af reguleringmetoder introduceres som en platform for syntese af robuste reguleringssystemer. Der undersøges tre basale reguleringstopologier, og det konkluderes at selv simple reguleringssystemer giver markante forbedringer af PMA systemet, selvom en evaluering af de tre metoder i hardware viser visse begrænsninger. Et nyt generelt reguleringsprincip introduceres – *Multivariable Enhanced Cascade Control (MECC).* Princippet er en praktisk fremgangmåde til realisering af højere orders reguleringssystemer under anvendelse af en *enhanced cascade* struktur. MECC giver flexibel kontrol over all væsentlige system parametre og er envidere simpel mht. realisering. Praktisk evaluering af en MECC baseret system viser state-of-the-art specifikationer.

Anvendelsen af ikke-lineære reguleringssystemer undersøges, ved introduktionen af et ikke lineært reguleringssystem der også fungerer som modulator. Til trods for teoretiske interessante egenskaber, viser metoden sig at lide under væsentlige fysiske begrænsninger.

Som et bidrag til området digitale PMA systemer, præsenteres en ny puls refereret reguleringsmetode – *Pulse Edge Delay Error Correction (PEDEC)* – for forbedret forstærkning af et allerede pulse moduleret signal. Det vises at at princippet fremtvinger ækvivalens mellem det puls modulerede indgangssignal og udgangssignalet. PEDEC menes at være den første dokumenterede methode for praktisk og effektiv realisering af højkvalitets digitale PMA systemer, der inkluderer kompensation for den ikke lineære effektomsætning.

List of Abbreviations

The thesis defines a range of important abbreviations to ease the discussion and comparison of principles and methods. The abbreviations are described below for reference.

Abbreviation	Description
PMA	Pulse Modulation (power) Amplifier. General definition of a system where the amplification is based on pulse modulation techniques and a switching power conversion stages. There are two alternatives: *Analog PMA* or *Digital PMA* referring to the use of analog or digital pulse modulation techniques.
NADS	Natural sampling – AD – Single Sided
NBDS	Natural sampling – BD – Single Sided
NADD	Natural sampling – AD – Double Sided
NBDD	Natural sampling – BD – Double Sided
UADS	Uniform sampling – AD – Single Sided
UBDS	Uniform sampling – BD – Single Sided
UADD	Uniform sampling – AD – Double Sided
UBDD	Uniform sampling – BD – Double Sided
LADS	Hybrid sampling – AD – Single Sided
LBDS	Hybrid sampling – BD – Single Sided
LADD	Hybrid sampling – AD – Double Sided
LBDD	Hybrid sampling – BD – Double Sided
PSCPWM	Phase Shifted Carrier Pulse Width Modulation.
MLCPWM	Multiple Leveled Carrier Pulse Width Modulation
NS / US	Naturally sampled Single Sided PSCPWM
ND / UD	Naturally sampled Double Sided PSCPWM
BNDX / BUDX	Balanced – Naturally/Uniformly sampled Double Sided PSCPWM
BNSX / BUSX	Balanced – Naturally/Uniformly sampled Single Sided PSCPWM
PSC	Power stage circuit topology for PSCPWM
BPSC	Balanced PSC power stage circuit topology for the balanced PSCPWM methods
US	Uncertainty set
NS	Nominal Stability
NP	Nominal Performance
RS	Robust Stability
RP	Robust Performance
SRI	Slew Rate Instability
VFC1	Voltage Feedback Control topology 1
VFC2	Voltage Feedback Control topology 2
CVFC	Current – Voltage Feedback Control topology
PEDEC	Pulse Edge Delay Error Correction.
PEDEC VFCX	PEDEC Voltage Feedback topology X (X = 1, 2 and 3)
TOCC	Three level One Cycle Controller
PAE	Pulse Amplitude Errors
PTE	Pulse Timing Errors

Chapter 1

Introduction

Fundamentally, only little has changed in the final stages of the audio reproduction chain for decades. The electrodynamic transducer as invented by C.W. Rice and E.W. Kellog in 1925 still forms the basis for the majority of loudspeakers in use today and the principle has only seen marginal changes within nearly 75 years. The widespread use can not be justified by superior performance, in fact the principle of electric-acoustic conversion is limited by numerous fundamental problems, that makes this ultimate stage in the audio chain the weakest – by far. One essential limitation is the striking inefficiency. Generally, a given amount of acoustic power requires orders of magnitude higher power input delivered by the power amplifier. The power amplifier has the task of amplifying the audio signal to a level that, combined with sufficient current to move the coil, produces the desired acoustic level from the loudspeaker. The poor loudspeaker efficiency is very unfortunate, since power amplifiers generally have to be capable of delivering large amounts of undistorted power, to produce the subjective levels demanded by the consumer.

The field of audio power amplification has equally suffered from a lack of real break-through inventions for decades. Thus, sound reproduction today is founded on a few power amplifier principles that are characterized by a linear operation of the output transistors. The advantages include topological simplicity and good performance, but the linear amplifier principles suffer from low efficiency, which is critical since the power amplifier handles considerably amounts of power. Accordingly, power amplifiers are in general provided with massive heat sinks of extruded aluminum to cope with the heat development. Negative side effects of inefficient power amplification include high volume, weight, cost and reliability problems. Moreover, the power amplifier has low energy utilization, which is clearly not an attractive feature in this energy-conscious area.

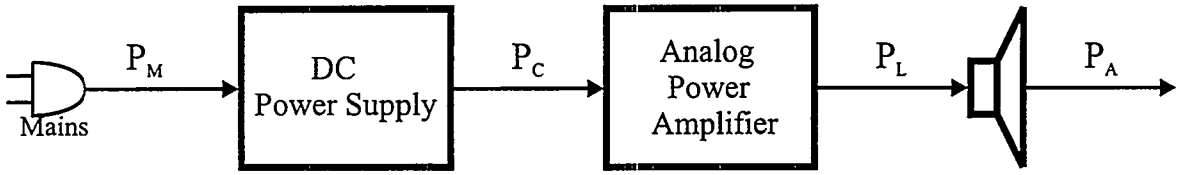


Fig. 1.1 Power flow in audio reproduction chain.

Consider the model of essential power flow in a typical audio system, shown in Fig. 1.1. To illustrate the low power utilization, a typical 100W power amplifier is considered. The power flow at two specific output levels is given below.

Situation	P_M	P_C	P_L	P_A
Typical	15W	10W	100mW	1mW
1/3 of max.	115W	90W	30W	300mW

Clearly, the transducer is the fundamental source of the efficiency problems, i.e. an efficiency improvement by and order of magnitude would virtually eliminate the need for power amplification, as we know it today. However, most of the power is dissipated in the *power amplifier* due to low efficiency in this stage.

The primary objective of the research resulting in the present dissertation has been to invent practical power amplification methods with *significant* improvements in efficiency at all levels of operation – without any compromises on audio performance. Improving power amplifier efficiency isolated will have significant influences on overall system efficiency, especially at lower levels of operation where much can be gained.

It might seem paradoxical, that this level of efficiency is tolerated in the industry, especially since a low efficiency only has negative side effects. There are several answers to this apparent paradox. Principles for more high efficiency power amplification – so called Class D or swithing power amplifiers - have been known for decades, however previous findings have shown several problems in terms of achieving the e.g. desired efficiency and audio specifications. On the other hand, methods to achieve sufficient levels of performance with linear power amplification are well known, and linear power amplification have over several decades of time established a reputation for good quality. A second problem is, that the audio community is highly conservative, often dominated by religious belief rather that scientific documentation and objective evaluation. Furthermore, only few have been interested in environmental issues despite the potential for dramatic improvements. Finally, amplifier weight, volume and energy consumption (!) has actually been considered a quality parameter (the larger and heavier the better), although there has never been any scientific documentation for any correlation between sound quality and these parameters. It is to expect however, that environmental issues will also reach consumer products. A high efficiency could become an attractive parameter in the future especially since labeling or standardization in consumer electronics is on its way [Ni95].

1.1 Audio power stage topologies

A brief introduction to commonly used circuit techniques for audio power amplification is given in the following with focus on their efficiency characteristics. It is common to differentiate between the different amplifier principles are by their *class*. A list of used

Class	Characteristics
A	Conducts signal current throughout the cycle of the signal waveform (360^0 conduction)
B	Conducts signal current exactly for one-half of the cycle of the input-signal waveform (180^0 conduction)
AB	Class B with bias to avoid crossover distortion.
C	$<180^0$ conduction with resonant loading. This method is primarily for RF frequency, and is only rarely used in the audio frequency range.
D	0^0 conduction. The power stage transistors are switched which in theory prevents the system from entering the active region.
B2, G, H	Extension of class B where more complex power supply circuitry is used to improve efficiency.

Fig. 1.2 Amplifier techniques reviewed.

classifications is listed in Fig. 1.2, with a short description of the characteristics [Be88]. The Class AB and B output stage topology, shown in Fig. 1.3 (top), forms the basis for the majority of power amplifiers today, and design techniques to realize high quality class B amplifiers have been known for decades. However, since the output voltage is derived form the supply voltage via the output transistors, it follows that the difference between the output voltage and the rail voltage must be dropped *across* the output transistors. This results in a wasteful dissipation of energy in the output transistors. The effective voltage drop across the output stage transistors can be reduced by the complex class B2 or class G configuration shown in Fig. 1.3.

1.1.1 Power and energy efficiency

Since amplifier efficiency is an essential parameter throughout the thesis, the efficiency of the most widely used power amplifier principles is investigated and compared. It is trivial to derive analytic expression for the efficiency vs. relative output level as shown in Appendix A for the three amplifier principles. The *power efficiency* is the ratio of utilized power over the supplied power:

$$\eta_P(x) = \frac{P_L(x)}{P_S(x)} \tag{1.1}$$

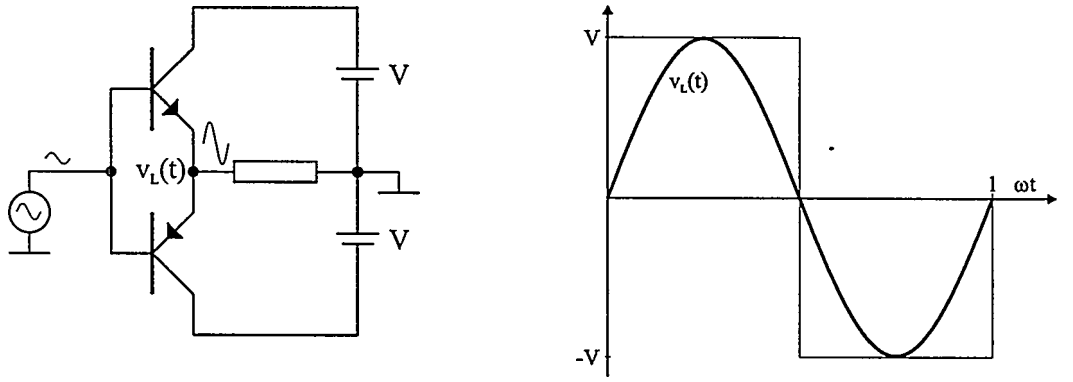
Where x denotes the relative output level. The amplifier output power is:

$$P_L(x) = x^2 \frac{V^2}{2R_L} \tag{1.2}$$

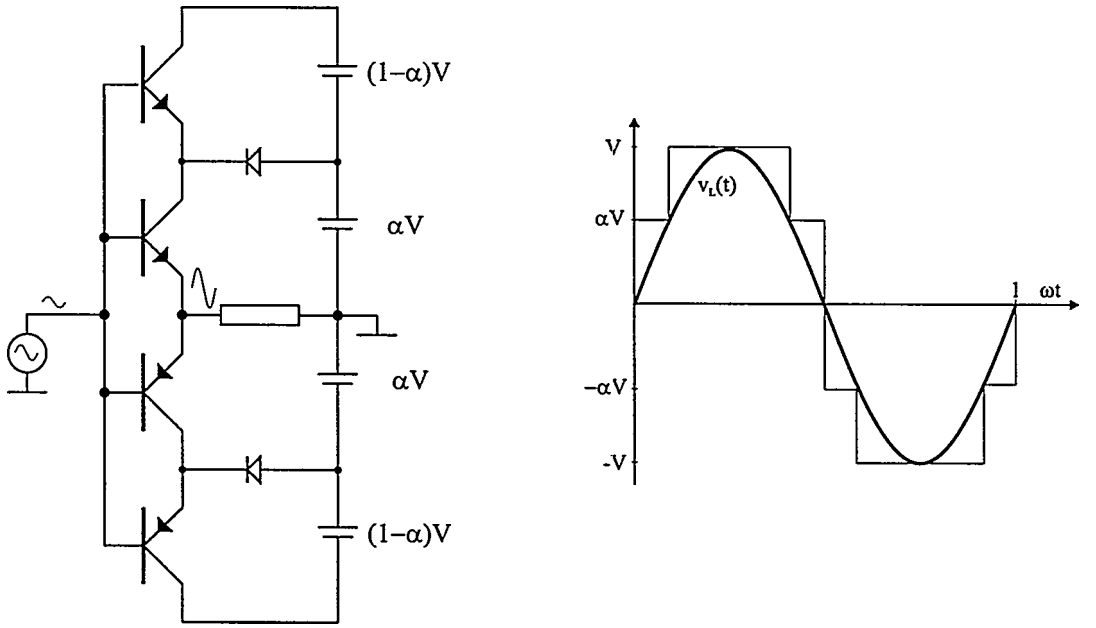
As shown in appendix A, the efficiency for the three output stage configurations are:

$$\eta_B(x) = x\frac{\pi}{4} \tag{1.3}$$

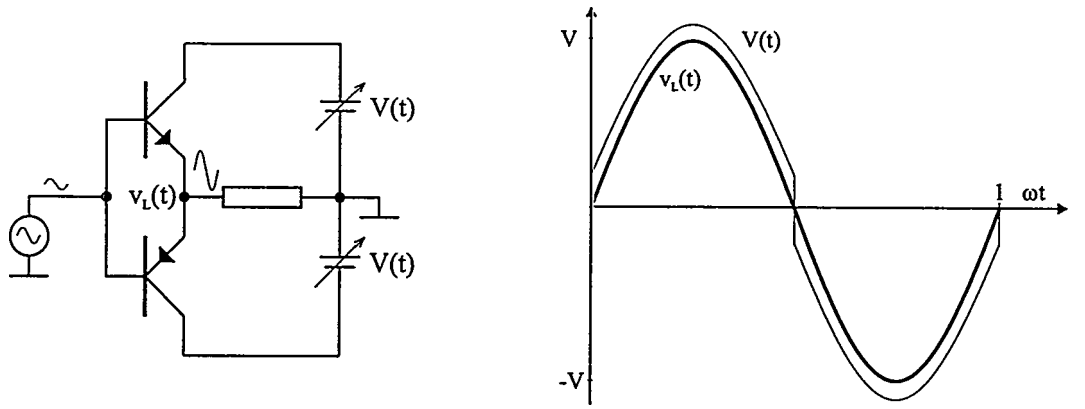
$$\eta_{B2}(x,\alpha) = \begin{cases} \frac{\pi}{4}\frac{x}{\alpha} & (x<\alpha) \\ \frac{\pi}{4}x\frac{1}{\alpha+(1-\alpha)\int_{\alpha\sin(\frac{\alpha}{x})}^{\frac{\pi}{2}}\sin(\omega t)d(\omega t)} & (x\geq\alpha) \end{cases} \tag{1.4}$$



Class B



Class B2



Class G

Fig. 1.3 Three widely used output stage configurations Class B, Class B2 and Class G.

$$\eta_G(x,\beta) = x\frac{\pi}{4}\left(\frac{1}{\beta + x\frac{\pi}{4}}\right) \tag{1.5}$$

Fig. 1.4 shows the ideal efficiency vs. relative output level for the three amplifier principles, and Fig. 1.5 equally shows the relative power dissipation vs. x. Class B2 and G and achieve reasonable efficiencies at higher output powers, but all topologies still have significant power dissipation at all output levels. In more aspects, these idealized models are not sufficient to estimate the real output stage efficiency especially at lower output levels. There are practical limitations further decreasing the efficiency of the output stage topologies, such as the necessary quiescent current to linearize the output stage and the saturation voltages in the output stage transistors. Subsequently, more realistic models of the three output stage topologies have been investigated that incorporate these important effects. Fig. 1.6 and Fig. 1.7 shows the efficiency and relative power dissipation of these more realistic output stage topologies. Note how the typical efficiency of all topologies is extremely low, primarily due to the significant power loss at quiescence.

1.1.2 Energy efficiency considerations

There is only little correlation between power efficiency and the amplifier energy consumption, since the power efficiency is typically specified at the level of maximal power dissipation or at the maximal output level. An alternative efficiency measure - the energy efficiency - is defined in the following. The basis is investigations of the general consumer behavior in terms of an average time distribution of volume control positions. Such a distribution will vary as a consequence of e.g. loudspeaker sensitivity, room size, user age and numerous other parameters. However, it is possible to generalize [Ha94b] and define four subjective listening levels as given in Table 1.1. The distribution should be interpreted as: In 89% of the time, the average user listens to background music with an average output level of -40dB etc. Since the distribution might vary dependent on application (e.g. in professional systems the distribution would be different), a general time distribution is considered:

$$(n_1, P_{L,1}, P_{S,1}), (n_2, P_{L,2}, P_{S,2}), \ldots (n_N, P_{L,N}, P_{S,N}) \tag{1.6}$$

$(n_j, P_{L,j}, P_{S,j})$ refers to that the output power in average is $P_{S,j}$ in n_j percent of the time and $P_{S,j}$ refers to the supplied power at the given output power. The *energy efficiency* is derived as the ratio of the average output power and the average supplied power:

$$\eta_E = \frac{\sum_{i=1}^{N} n_i \cdot P_{L,i}}{\sum_{i=1}^{N} n_i \cdot P_{S,i}} \tag{1.7}$$

Distribution in time	Output level (rel.)	Subjective level
0 %	0 dB	Clipping
1 %	-9 dB	Party
10 %	-24 dB	Listening
89 %	-40 dB	Background

Table 1.1 Average time distribution of volume control positions.

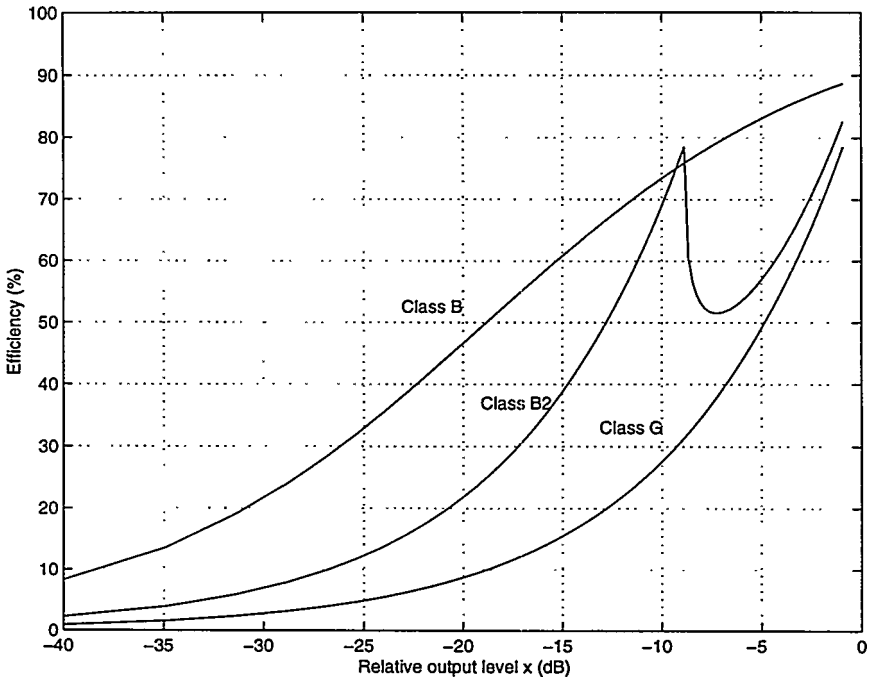


Fig. 1.4 Efficiency vs. relative output level for ideal power amplifier output stages.

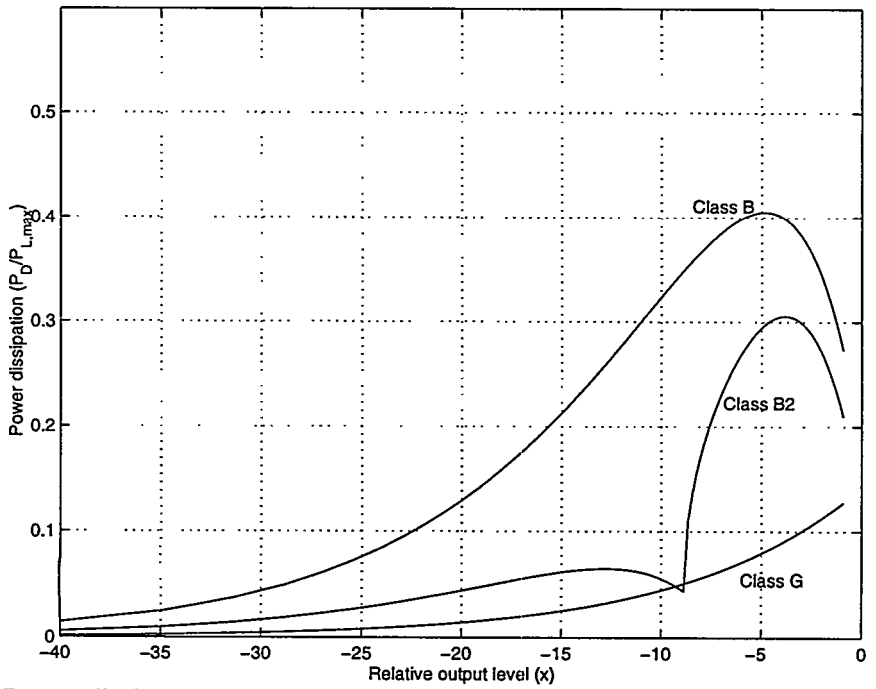


Fig. 1.5 Power dissipation vs. relative output level for ideal power amplifier output stages.

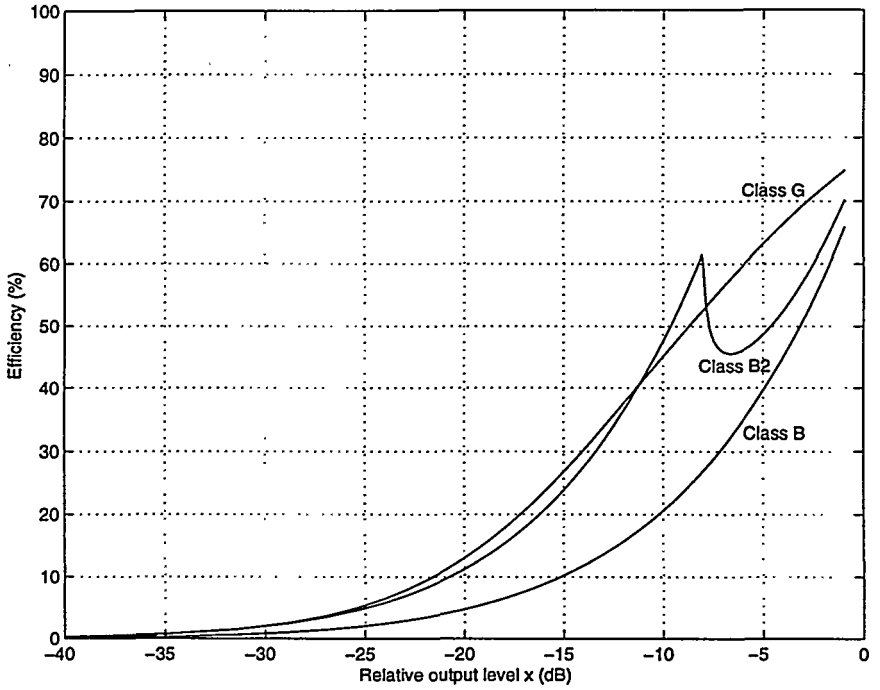


Fig. 1.6 Efficiency and power dissipation for realistic models of class B, B2 and G power amplifier output stages topologies.

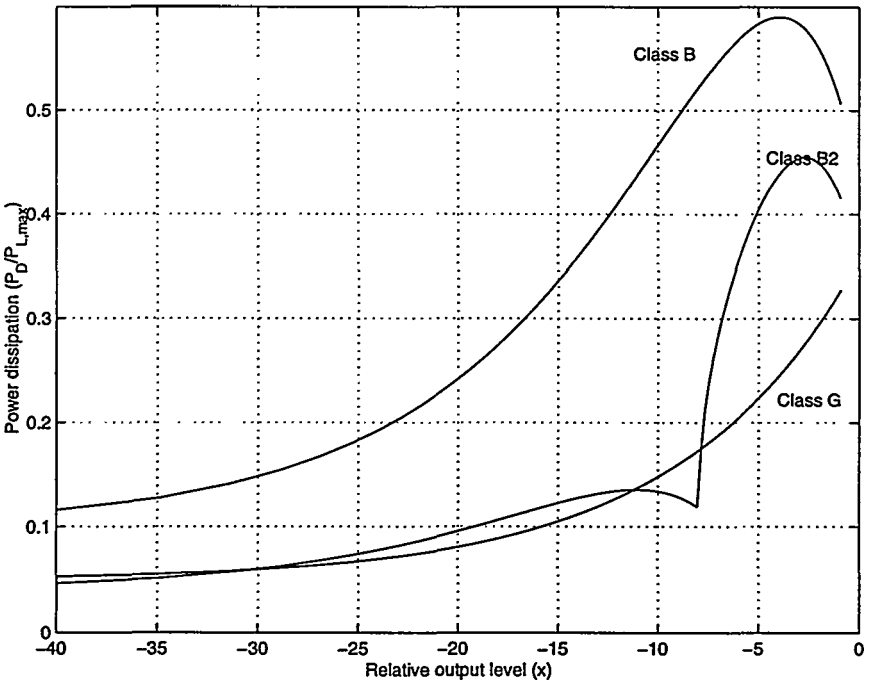


Fig. 1.7 Efficiency and power dissipation for realistic models of class B, B2 and G power amplifier output stages topologies.

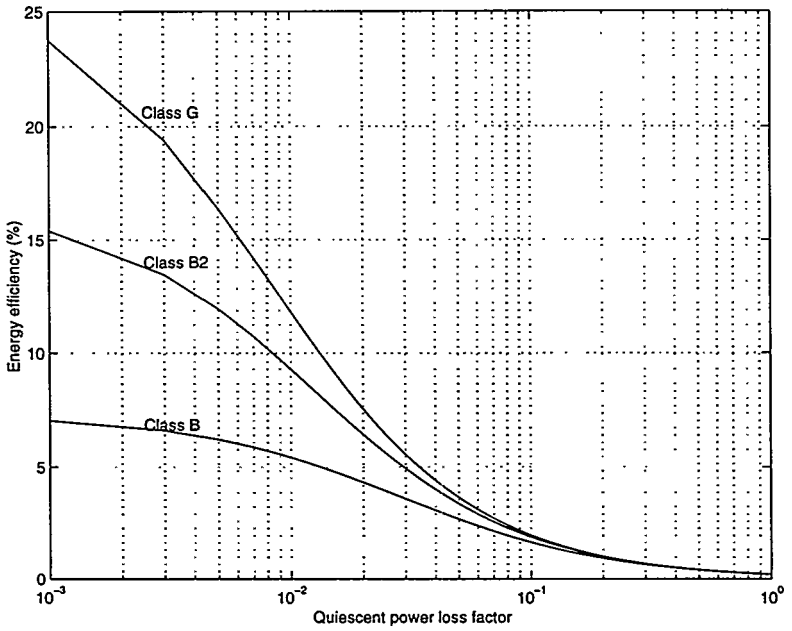


Fig. 1.8 Energy efficiency of Class B, Class B2 and Class G.

The parameter can be used to minimize the energy consumption in any system. Let the *quiescent power loss factor* λ be defined as:

$$\lambda = \frac{P_S(0)}{P_{L,\max}} \tag{1.8}$$

Fig. 1.8 illustrates the energy efficiency for the realistic models of class B, B2 and G power output stages, as a function of λ. The typical energy efficiency for a class B output stage is only:

$$n_E \cong 1 - 2\% \tag{1.9}$$

This holds for λ between 0.1 and 0.2, which is typical for a class B output stage. Note that the energy efficiency for an *ideal* class B amplifier is only 7.1%, due to the inherent losses bound to the linear operation of the output transistors. Since the power amplifier operates in the "background music" mode most of the time, the important parameters in terms of energy efficiency are not surprisingly the power dissipation at low output levels and especially the quiescent power dissipation. The energy efficiency of class B2 and class G can be made considerably better (see Fig. 1.8) if the λ is sufficiently low. However, this is not easy to obtain in any of the two alternatives. For class B2, lowering α will compromise the efficiency at higher output levels (no gain compared to class B) and for class G, the switching power supplies will cause the quiescent power loss λ factor to be high. To conclude, all output stages have their limitations, and more than a doubling in energy efficiency by optimization cannot be expected.

1.1.3 The switching (Class D) power stage topology

Based on this initial investigation of output stage topologies it is concluded that considerable improvements in efficiency cannot be achieved with output transistors operating in the linear range. A completely switching power stage is needed. This approach

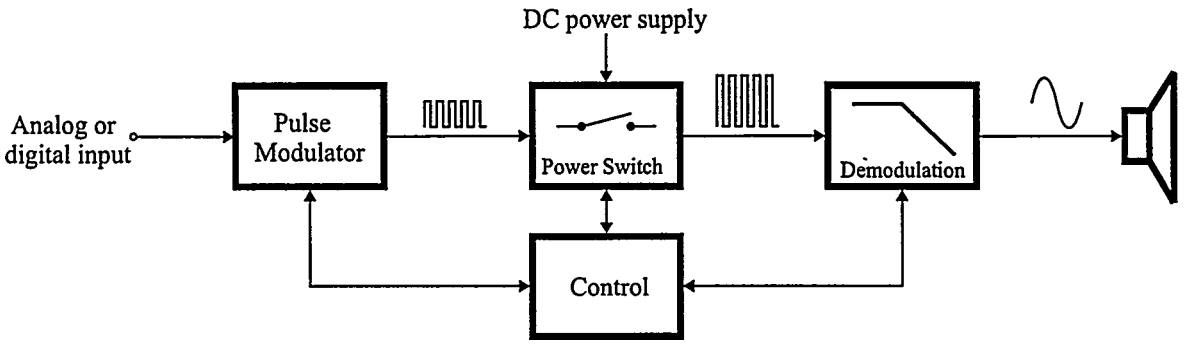


Fig. 1.9 General Pulse Modulation Amplifier (PMA) utilizing a class D power stage.

has the inherent advantage of a 100% theoretical efficiency. With the continuing improvements in power switching devices, the efficiency will converge towards this theoretical optimum as time progresses. Throughout the years the fundamental principle of power amplification using switching technology has been called class D, switching power amplification, digital power amplification and PWM power amplification. Recently, what is believed to be a more suitable and general designation – Pulse Modulation Amplifiers (PMA) – has been introduced by the author [Ni97a]. This general designation will be used henceforth.

1.2 The Pulse Modulation Amplifier (PMA)

Fig. 1.9 shows the general PMA topology. The four fundamental blocks are the *pulse modulator*, the *switching power stage*, the *demodulation filter* and the *error correction* block. The pulse modulator may be based on either analog or digital pulse modulation techniques, correspondingly referenced to as analog PMA and digital PMA systems. The power switch converts the pulse modulated signal to power level. Following, the power pulse modulated signal is feed to a filter to reconstitute the modulated signal. The control system serves to compensate any errors that are introduced in each of the three essential blocks of the system.

The pulse modulator is the heart of the PMA system. Two analog pulse modulation methods for PMAs are PWM and PDM, shown in Fig. 1.10. The methods may be implemented in both the analog and digital domain. The modulator output generally contains three distinct elements:

- The modulated signal.
- Distortion components related to the modulated signal.
- A high frequency spectrum.

The high frequency output is composed of either discrete components related to the carrier, noise shaped noise or a combination of both. The pulse modulator can be based any scheme performing a coding of the modulating signal to a pulse modulated form. One of the objectives of this thesis is to research in coding schemes that provides optimal PMA performance.

Power amplification based on pulse modulation techniques in combination with a switching class D power stage have been known for decades. Some of the first designs were already presented by e.g. Sinclair and Johnson [Jo67], [Jo68] some 30 years ago. However, until recently the research has been quite modest with only a few noteworthy publications as e.g. [At83], [Ha91]. Within the last decade, the field has "resurrected" now with focus on digital pulse modulation methods for digital PMA systems. An exhaustive

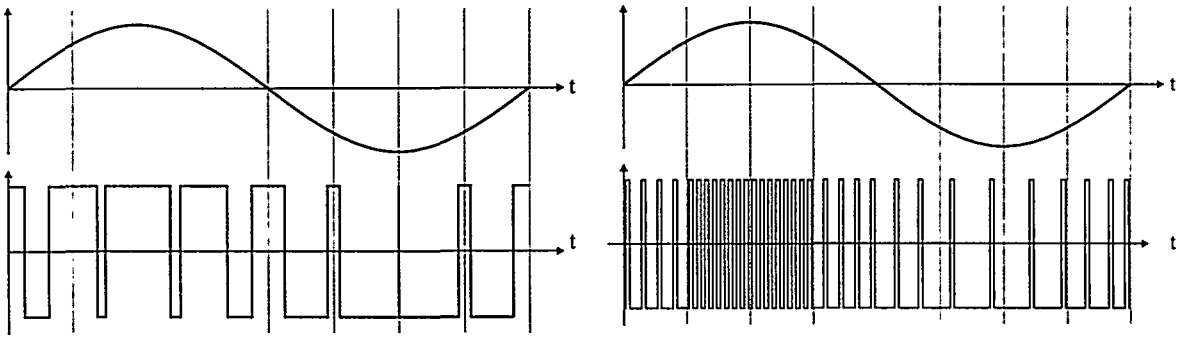


Fig. 1.10 PWM and PDM pulse modulation methods.

set of publications exists on this specific subject, e.g. [Sa86], [Le91], [Go91], [Go92], [Ha92] and [Hi94]. The digital PMA approach was considered a break-through in audio power amplification. Nevertheless, it has proven very difficult to realize the acceptable audio performance in both analog PMA and digital PMA system. The problems relate to the non-linear power conversion and demodulation.

1.2.1 Design problems and challenges

PMA systems and audio power amplifiers in general are complex non-linear systems. Thus, power amplifiers are subject to varying input signals, generally drive reactive loads, are most often supplied by non-regulated power supplies which supply the other channels for sound reproduction. Furthermore, power amplifiers might be subjected to overload situations if not prevented. No power amplifier can be optimized without a simultaneous consideration of a broad range of desired specifications. Furthermore, the tolerance of these specifications has to be considered. The essential issues to consider when designing and evaluating power amplifier systems are outlined below.

Gain

A specification of the insertion gain of the system typically specified in dB.

Frequency response / Bandwidth

The ability of amplifier to amplify signals over a range of frequencies, with defined source and load. Specifications are generally a –3dB bandwidth, and a tolerance on the deviation from the desired response at any frequency up to the bandwidth limit.

Harmonic distortion / Intermodulation distortion

The non-linear behavior of the amplifier causes harmonic distortion (THD) and intermodulation distortion (IMD). Moreover, the distortion will in general depend on parameters as signal level, frequency and load parameters. Distortion has to be well controlled within this parameter space. Distortion is normally specified in percentage or dB. Various IMD measurement methods exist as the two-tone CCIF, SMPTE or Transient Intermodulation Distortion (TIM).

Noise / Signal-to-noise ratio / Dynamic range

All amplifiers have internal noise sources that contribute to the output noise. Typical specifications are the residual noise referred to the output with terminated input or the Signal-to-noise ratio relative to a given output level e.g. 1W. Also frequently used is the dynamic range, which is the relationship between the maximal RMS voltage output before clipping and the RMS of the residual noise.

Output impedance / Loading

The load impedance is generally frequency dependent with resonant peaks etc. The influences of a variable load in system frequency response should be minimized. Furthermore, the amplifier output impedance should be as low as possible to cope with variations in nominal load impedance.

Power Supply Rejection

The power amplifier has to cope with the inevitable power supply perturbations. The amplifier should be able to suppress these perturbations such that the output is not influenced. A widely used specification is the power supply rejection ratio (PSRR), which is the sensitivity of the output to perturbations on the power supply. The rejection of such perturbations has to be controlled over the complete bandwidth.

Stability

A control system is generally required to secure robust performance for the power amplifier. This introduces a potential risk of instability. The amplifier should be prevented from instability under all circumstances, since this will generally have dramatic consequences as a burn out of the speaker of the amplifier itself.

There are no definitive margins between what is required to be acceptable and unacceptable. However, a set of parameters corresponding to satisfying performance in most applications can be specified:

Parameter	Condition	Value
Bandwidth	-3dB	> 60KHz
Power bandwidth	-3dB	> 20KHz
Frequency response	20Hz – 20KHz	<± 0.2dB
THD	@ 1W / 1KHz	< 0.01 %
THD	20Hz-20Hz (complete range)	< 0.05 %
IMD	CCIF two tone	< 0.01%
SNR	A weighted @ 0dBW	>90 dB
Dynamic range	A weighted	> 110dBA
Load range		2-16 Ω
PSRR	All frequencies	> 40dB

A power amplifier with a reasonable power handling capability (e.g. 100W) is considered.

1.2.2 Other considerations

The application range for high efficiency power amplification is very broad. Active speaker systems with dedicated speakers and power amplifiers for each frequency band is a specifically interesting application. This enclosed environment offers some special advantages:

- The load and amplifier can be matched perfectly. Load variations (typically 2, 4 and 8 ohms) do not have to be considered.
- Connection wires from amplifier to speaker can be minimized.
- Bandwidth limited amplification can be utilized to optimize the efficiency.

The general spectral amplitude distribution of music material only emphasizes that the technology has certain advantages in active speaker systems. Almost independent of music material, the average acoustic power in the tweeter band 4KHz – 20KHz is much lower

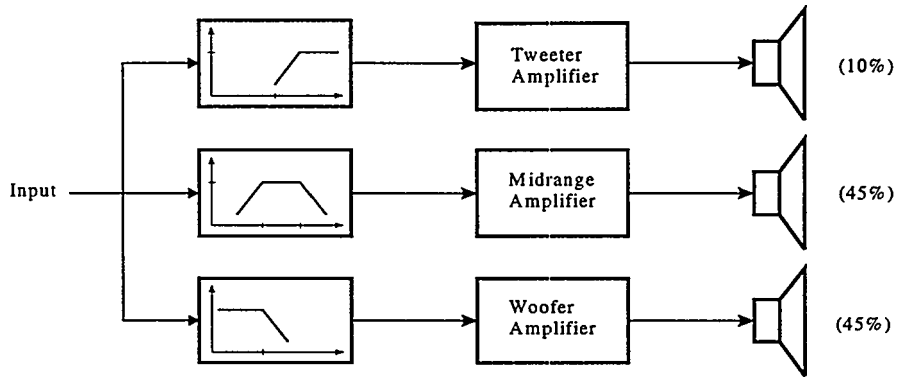


Fig. 1.11 An active speaker system (here 3 way) based on separate amplifiers for each band.

than in the other bands. Fig. 1.12 illustrates a more specific analysis. This will be reflected in the power amplifier size for each band as illustrated with a typical active 3-way speaker system in Fig. 1.11. Thus, the power handling capability is only around 10-15% of the total power in the tweeter band. Optimization of energy efficiency in active speaker systems can as such be carried out by improving efficiency in the lower 20% of the frequency band only. In this particular environment, the PMA design challenge is clearly somewhat different from the general case.

1.3 Thesis structure

The primary objective of the research resulting in the present dissertation has been to invent practical power amplification methods with significantly improved efficiency at all levels of operation – without any compromises in terms of audio performance. It will become apparent when reading the thesis, that this has required multi-disciplinary research involving such diverse fields as e.g.; analog and digital modulation theory, power electronics, DSP, semi-conductor physics and control systems.

The thesis is divided in two volumes, the main part consisting of 11 chapters divided in four parts, and a second volume consisting of the three appendices A, B and C.

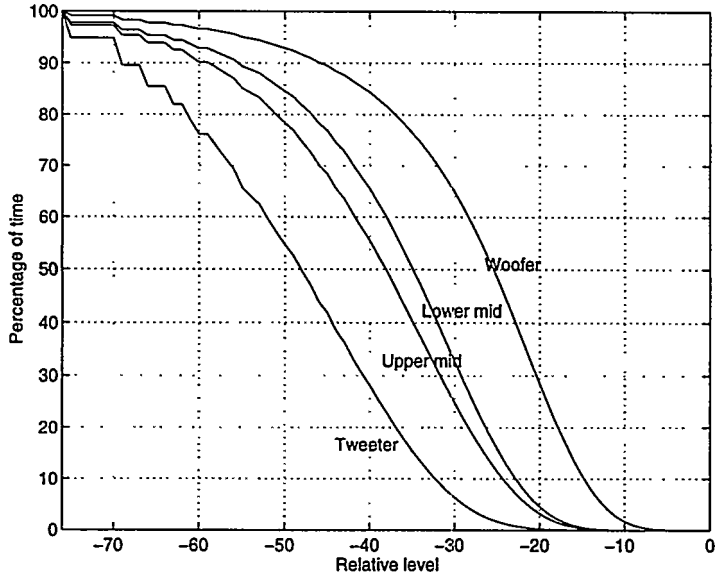


Fig. 1.12 An example of the distribution of signal levels on a CD in four bands. The bands are divided at 650hz, 1500hz and 4.5KHz. The programme material is "The Division Bell" by Pink Floyd.

Chapter 1 has introduced the motivating factors and the foundation for the research.

Part I (Chapters 2-3) presents a comprehensive analysis of analog and digital pulse modulation methods suitable for analog PMAs and digital PMAs, respectively.

Chapter 2 is devoted to analog pulse modulation methods. A broad set of pulse modulations methods are subjected to a fundamental analysis of their suitability in analog PMA systems. The chapter contributes to fundamental modulation theory by introducing a novel family of modulation methods – Phase Shifted Carrier Pulse Width Modulation (PSCPWM).

Chapter 3 is devoted to digital pulse modulation methods for digital PMAs. Previously presented methods are reviewed. A simple design methodology is presented for digital PWM modulators.

Part II (Chapters 4-5) continues to the second major block of the PMA - the power stage. Power stage structures are synthesized and analyzed, and methods for optimal power stage implementation are devised.

Chapter 4 is dedicated to a fundamental analysis of error sources within PMA systems. It is shown how the power conversion stage seriously effects all the important parameters of the system, i.e. linearity, noise and efficiency. Modulator error sources are also investigated.

Chapter 5 is devoted to efficiency optimization in the power conversion stage of PMAs. Starting with a simple switching leg, the analysis extends to the general multi-level PSCPWM power stage topologies.

Part III (Chapters 6-9) continues to the third major block of the PMA – control system design.

Chapter 6 investigates the application of robust linear control to analog PMA systems. A methodology for control system design is introduced. Three fundamental linear control methods are investigated, and robust case example designs are synthesized and analyzed.

Chapter 7 is devoted the presentation of a control method, dedicated to solve the fundamental problems in analog PMA systems – Multivariable Enhanced Cascade Control (MECC).

Chapter 8 investigates the application of non-linear control methods for analog PMAs. The focus in on a new non-linear modulator/controller structure – Three level One Cycle Control (TOCC). Advantages and disadvantages compared with linear control are emphasized.

Chapter 9 is dedicated to the complex issues of error correction in digital PMA systems. A new control method for enhanced power amplification of a pulse modulated signal is presented – Pulse Edge Delay Error Correction (PEDEC). PEDEC based digital PMA topologies are presented and evaluated.

Part IV (Chapter 10) is devoted to implementation and evaluation.

Chapter 10 is dedicated to the practical evaluation of all investigated principles and topologies. Performance specifications for the various prototypes developed during the project are presented.

Chapter 11 summarizes the essence of the thesis and draws the essential conclusions.

Volume II contains three appendices:

Appendix A supplements Chapter 1. Investigations of power and energy efficiency for various amplifier concepts are carried out.

Appendix B supplements Chapter 2. Details of the derivation of analytical double Fourier series expressions for a broad range of analog pulse modulation methods are given.

Appendix C is a complete reproduction of the conference and journal papers that have been published at during the project.

Part I

Chapter 2

Analog Pulse Modulation

This chapter is dedicated to *analog* pulse modulation characterized by the use of an analog reference input to the pulse modulator. It is attempted to devise modulation strategies that will lead to the optimal PMA performance. This is carried out by a fundamental review and comparison of known pulse modulation methods, followed by investigations of new enhanced pulse modulation methods with improved characteristics. The analysis is based on the derivation of Double Fourier Series (DFS) expressions for all considered methods, and the introduction for a spectral analysis tool – the Harmonic Envelope Surface (HES) – based on the analytical DFS expressions. The HES offers detailed insight in the (for PMAs) interesting aspects and the tool proves indispensable of a coherent analysis and comparison of extensive set of pulse modulation methods that are investigated throughout this central chapter. A new multi-level modulation method – Phase Shifted Carrier Pulse Width Modulation (PSCPWM) [Ni97b] – is introduced and subjected to a detailed investigation. A suite of PSCPWM methods are defined each with distinct characteristics, and it will appear that the principle provides optimal pulse modulation for PMAs from a theoretical point of view.

2.1 Fundamental pulse modulation methods

Pulse modulation systems represent a message-bearing signal by a train of pulses. The four basic pulse modulation techniques are [Bl53] *Pulse Amplitude Modulation* (PAM), *Pulse Width Modulation* (PWM), *Pulse Position modulation* (PPM) and *Pulse Density*

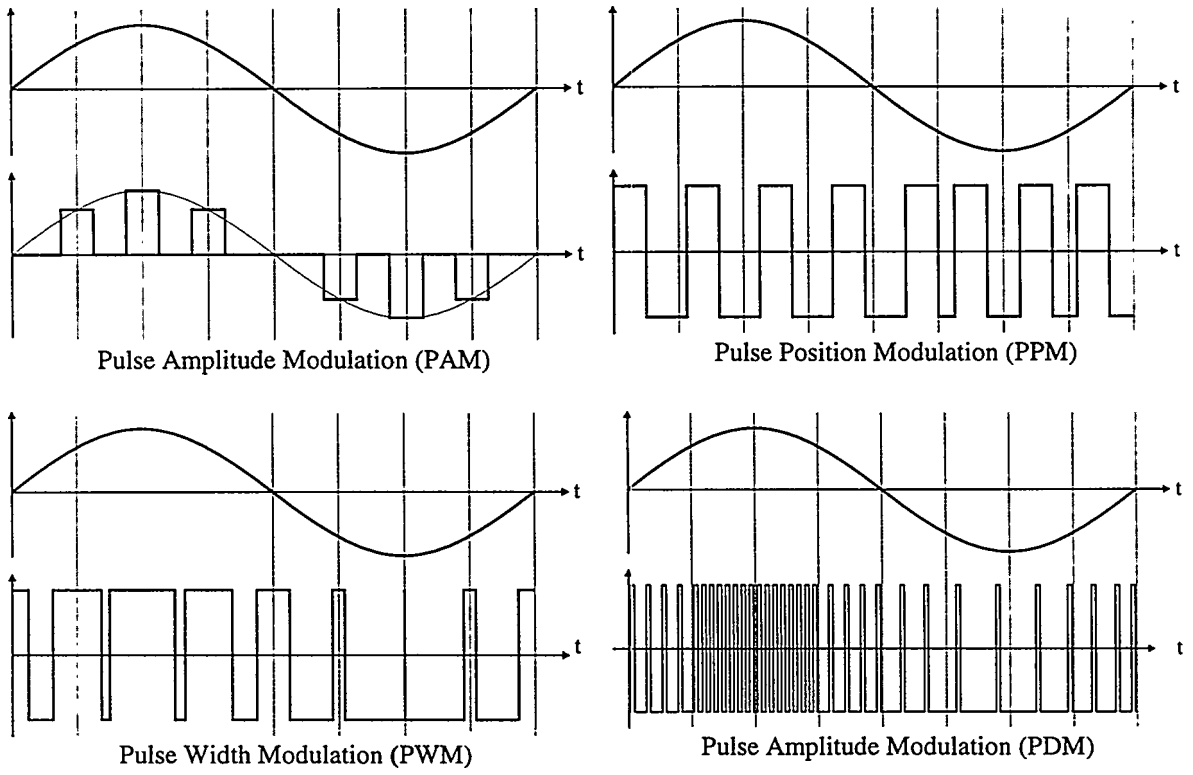


Fig. 2.1 Fundamental pulse modulation methods

Modulation (PDM). Fig. 2.1 illustrates these four fundamental principles of analog pulse modulation. Pulse Amplitude Modulation (PAM) is based on a conversion the signal into a series of amplitude-modulated pulses as illustrated in Fig. 2.1. The bandwidth requirements are given by the Nyquist sampling theorem, so the modulated signal can be uniquely represented by uniformly spaced samples of the signal at a rate higher or equal to two times the signal bandwidth. An attractive feature of PAM is this low bandwidth requirement resulting in a minimal carrier frequency, which would minimize the power dissipation in a switching power amplification stage. Unfortunately, PAM is limited by the requirements for pulse amplitude accuracy. It turns out to be problematic to realize a high efficiency power output stage that can synthesize the pulses with accurately defined amplitude. If only a few discrete amplitude levels are required, as it is the case with the other three pulse modulation methods, the task of power amplification of the pulses is much simpler.

Pulse Width Modulation (PWM) is dramatically different form PAM in that it performs sampling *in time* whereas PAM provides sampling in amplitude. Consequently, the information is coded into the pulse time position within each switching interval. PWM only requires synthesis of a few discrete output levels, which is easily realized by topologically simple high efficiency switching power stages. On the other hand, the bandwidth requirements for PWM are typically close to an order of magnitude higher than PAM. This penalty is well paid given the simplifications in the switching power stage / power supply.

Pulse Position Modulation (PPM) differs from PWM in that the value of each instantaneous sample of a modulating wave is caused to vary the position in *time* of a pulse, relative to its non-modulated time of occurrence. Each pulse has identical shape independent of the modulation depth. This is an attractive feature, since a uniform pulse is

Type	Bandwidth Requirements	Modulation depth	Efficiency	Complexity
PAM	+	+	-	-
PPM	-	-	-	-
PWM	-	+	+	+
PDM	-	+	+	+

Table 2.1 Qualitative comparison of basic pulse modulation methods

simple to reproduce with a simple switching power stage. On the other hand, a limitation of PPM is the requirements for pulse amplitude level if reasonable powers are required. The power supply level of the switching power stage will have to be much higher than the required load voltage. This leads to sub-optimal performance on several parameters as efficiency, complexity and audio performance.

Pulse Density Modulation is based on a unity pulse width, height and a constant time of occurrence for the pulses within the switching period. The modulated parameter is the *presence* of the pulse. For each sample interval it is determined if the pulse should be present or not, hence the designation *density* modulation. It is appealing to have a unity pulse since this is easier to realize by a switching power stage. Another advantage is the simplicity of modulator implementation. However, PDM requires excess bandwidth generally beyond what is required by e.g. PWM.

A qualitative comparison of the four fundamental methods is shown in Table 2.1. Only PDM and PWM are considered relevant, i.e. potential candidates to reach the target objectives.

2.2 Analog Pulse Density Modulation (PDM)

Pulse density modulation is now investigated more closely. A simple way to realize a PDM based amplifier is the use of a conventional analog pulse density modulator with a linear loop filter, followed by a switching power stage [Kl92]. However, by integrating a switching amplification stage in the noise shaping loop an interesting power PDM topology arrives as shown in Fig. 2.2. This power PDM was first introduced as a method for switching amplifiers in [Kl92] followed by subsequent investigations in [Kl93] and recently in [Iw96]. Unfortunately, there are several inherent complications with PDM for pulse modulated power amplifier systems. The loop filter has to be of higher order for satisfactory performance within the target frequency band, due to the immense amount of noise generated by the pulse modulating quantizer. The realization of higher order loop filters for both analog and digital pulse density modulators have received much attention in previous research. An attractive higher order topology was presented in [Ch90], and is shown in Fig. 2.3. This higher order structure is suited for analog power PDM systems as

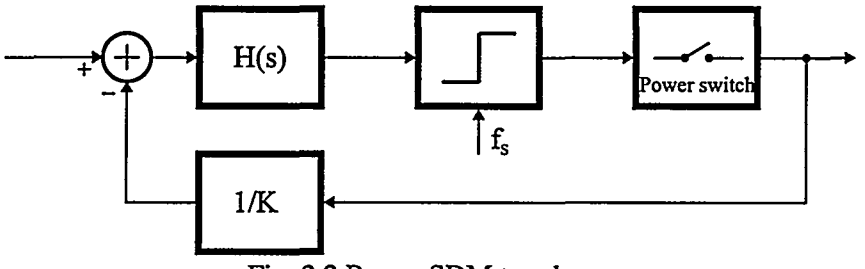


Fig. 2.2 Power SDM topology.

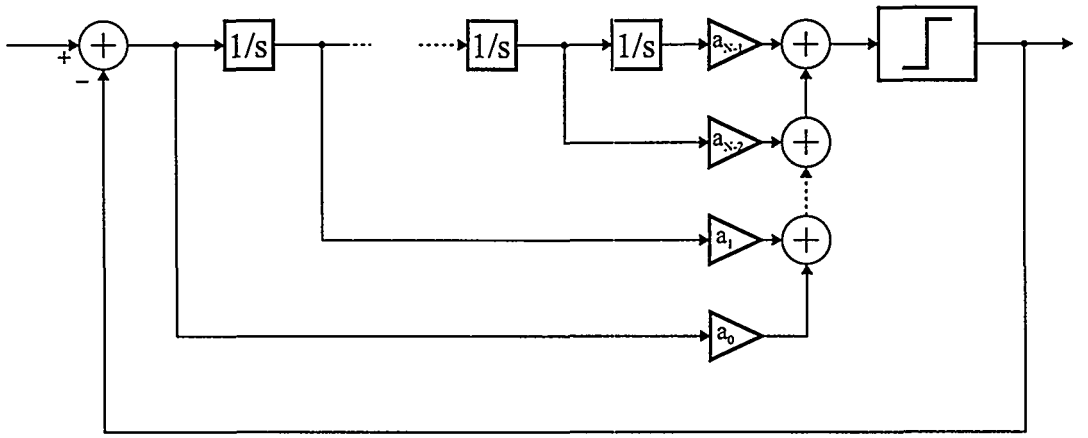


Fig. 2.3 Higher order analog PDM loop filter realization.

shown in [kl93]. Unfortunately, there are limits on filter order when implemented in the analog domain due to tolerances and other analog imperfections. A fourth (or higher) order filter is generally necessary for optimal implementation of power PDM system in reasonable quality. Even with a fourth order filter, the resulting sampling frequency is in the range 2.5MHz - 3MHz for reasonable audio performance in the general case where the target bandwidth is 20KHz. Subsequently, the pulse repetition frequency will be 50-100 times the bandwidth limit of a full audio range system [Kl92]. This is problematic since physical limitations within the switching power amplification stage will introduce switching losses and error that increase with switching frequency. Especially the quiescent power dissipation will be compromised by a high switching frequency. A further drawback is the limits on modulation depth with a higher order PDM [Kl92, Kl93]. This will further compromise efficiency and quiescent power dissipation since the pulse amplitude levels will get relatively higher. In conclusion, the simple and elegant analog power PDM topology is compromised by several essential limitations, mostly relating to the power amplification stage. Consequently, analog PDM is not considered optimal for PMA implementation since PWM as it will become apparent does not suffer from such drawbacks to the same degree.

2.3 Analog Pulse Width Modulation

In general, previous research in the field of pulse width modulation as e.g. [Bl53], [Ma67], [Bo75a], [Bo75b], [Se87], [Me91], [Go92], [Hi94] has focused on a limited set of schemes. No coherent work exists with a comprehensive analysis and comparison of pulse width modulation methods, and certainly not with PMAs as a specific application. Further motivating factors for a detailed review and comparison of PWM methods schemes is that interesting characteristics of the more known modulation schemes have not drawn sufficient attention. Traditionally, pulse width modulation is categorized in two major classes by the sampling method: natural sampled PWM (NPWM) and uniform sampled PWM (UPWM). Alternative sampling methods exists which can be categorized as hybrid sampling methods since the nature of sampling lies between the natural and uniform sampling. The principles of the different sampling methods are illustrated in Fig. 2.4. This section focuses on inherently analog pulse modulation methods. The "digital" UPWM and hybrid sampled PWM are discussed in the next chapter. Besides the sampling method, PWM is traditionally also differentiated by the *edge modulation* and by the *class*. The edge modulation may be *single sided* or *double sided*. The modulation of both edges doubles the information stored in the resulting pulse train, although the pulse train frequency is the same. *Class AD* and *Class BD* are the (somewhat misleading but standardized)

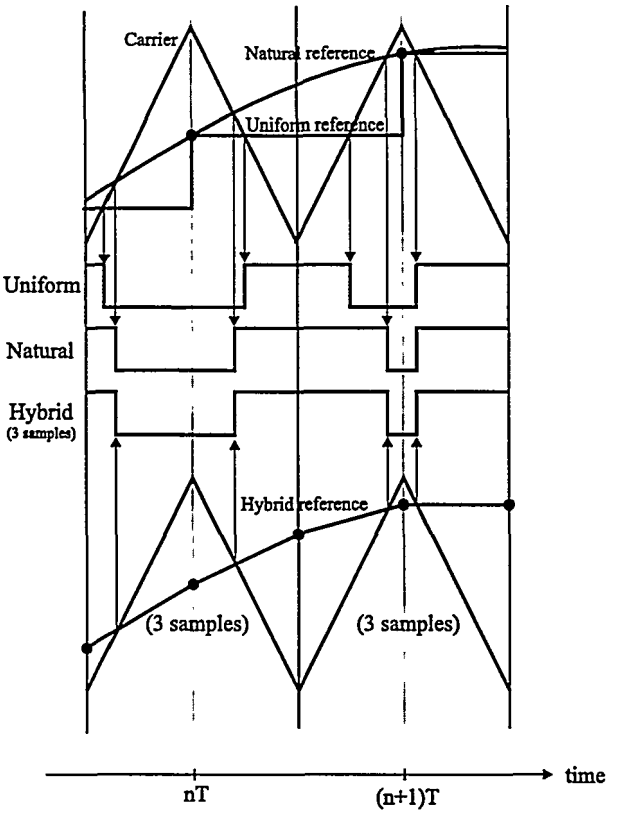


Fig. 2.4 Samplings methods in PWM.

abbreviations to differentiate between two-level and three-level switching as introduced in [Ma70]. Although the approach of synthesizing three-level waveforms here differ from the method in [Ma70], the designation BD is kept during this fundamental analysis for coherence with previous work. The resulting four fundamental NPWM schemes are summarized in Table 2.2. An abbreviation has been assigned for each scheme in order to able to differentiate between the methods:

{Sampling Method}{Switching}{Edge}

An example is NADS for Natural sampling - **AD** switching - Single sided modulation. All methods can be realized by 4 independently controlled switches using the bridge switching power stage topology shown in Fig. 2.5. Fig. 2.6 - Fig. 2.9 illustrates the essential time domain waveforms for the considered 4 variants of NPWM. The figures illustrates from top to bottom the modulating signal and carrier, the signal waveforms on each of the bridge phases and the differential- and common-mode output signals, respectively. From this time domain investigation is clear that significantly different modulation schemes in terms of both differential and common mode output, can be synthesized with the simple 4 switch H-bridge topology.

Sampling method	Edge	Levels	Abbreviation
Natural sampling (NPWM)	Single sided	Two (AD)	NADS
		Three (BD)	NBDS
	Double sided	Two (AD)	NADD
		Three (BD)	NBDD

Table 2.2 Fundamental pulse width modulation schemes

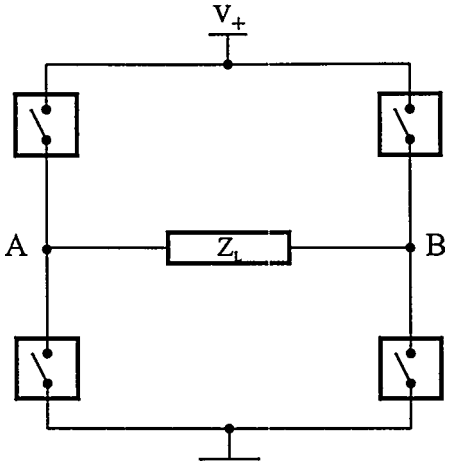


Fig. 2.5 H-bridge switching topology

2.3.1 Analysis methodology

The analysis and comparison of the different modulation schemes is based on PWM responses to single tone input, since analytical treatment of modulated multi-tone and noise signals is highly complicated. Investigations of the response to such stimuli can be carried out by computer simulation. However, the response to single tone input provides all interesting information about the complex behavior of the modulation process. Thus, the response to multi-tone and noise inputs can in general be well predicted from the response to tonal input. The tonal behavior is analyzed by a double Fourier series approach from communications theory, and the method has been applied to a few PWM variants by Black [Bl53]. Further treatment of the subject has been given by Bowes [Bo75a, Bo75b] and in some more recent publications [Se87, Go92, Hi94]. The fundamental advantage of an analytical approach is that no computer simulation will provide the same detailed information as concise analytical expressions.

It has proven difficult to analyze PWM in detail since the modulation depends in a complex way of several parameters; e.g. modulation index, reference frequency and carrier frequency. The essential parameters for a coherent analysis and comparison of PWM methods are discussed below.

Maximal frequency ratio

The *frequency ratio* or *normalized frequency* f_r is defined as the ratio between signal angular frequency ω and carrier angular frequency ω_c:

$$f_r = \omega_r = \frac{\omega}{\omega_c} \tag{2.1}$$

An interesting parameter of comparison is the *maximal frequency ratio* defined as the limit where the quality of the modulator output is still acceptable. The Nyquist sampling criteria puts a restriction on the allowable frequency ratio:

$$f_{r,\max} = \frac{1}{2} \tag{2.2}$$

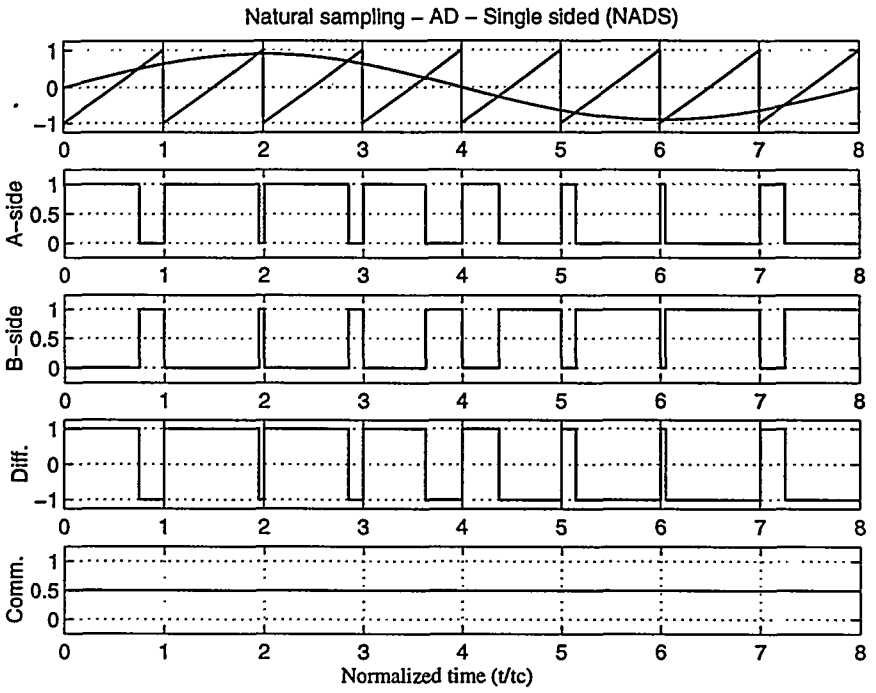


Fig. 2.6 Time domain waveforms for NADS. $f_r = \frac{1}{8}$.

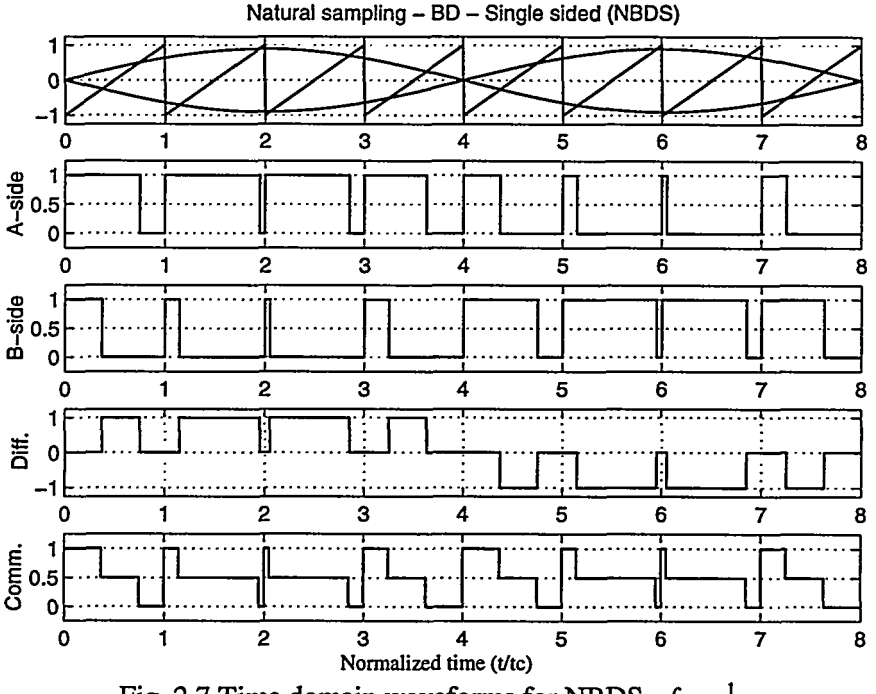


Fig. 2.7 Time domain waveforms for NBDS. $f_r = \frac{1}{8}$.

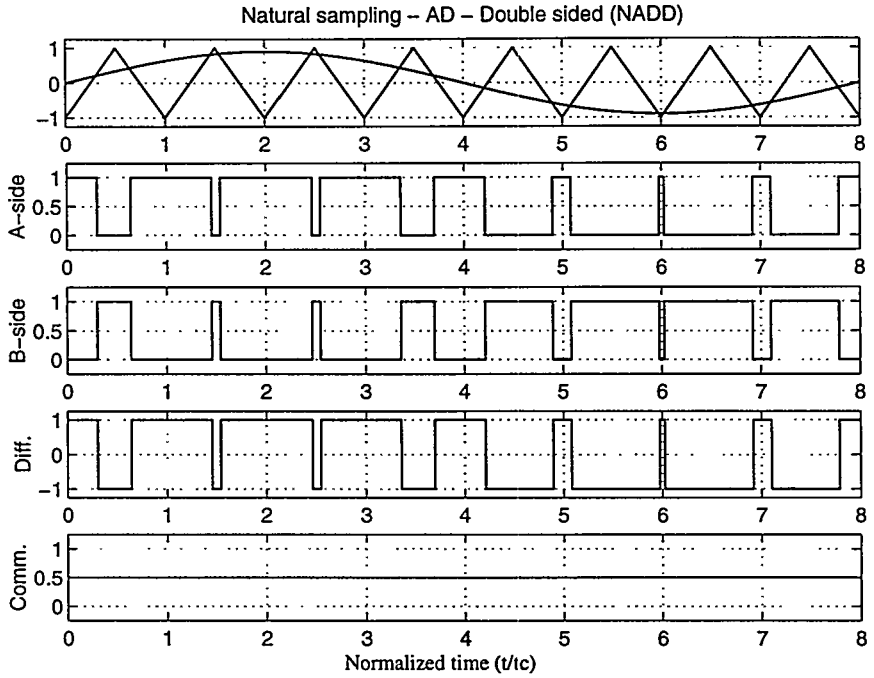


Fig. 2.8 Time domain waveforms for NADD. $f_r = \frac{1}{8}$.

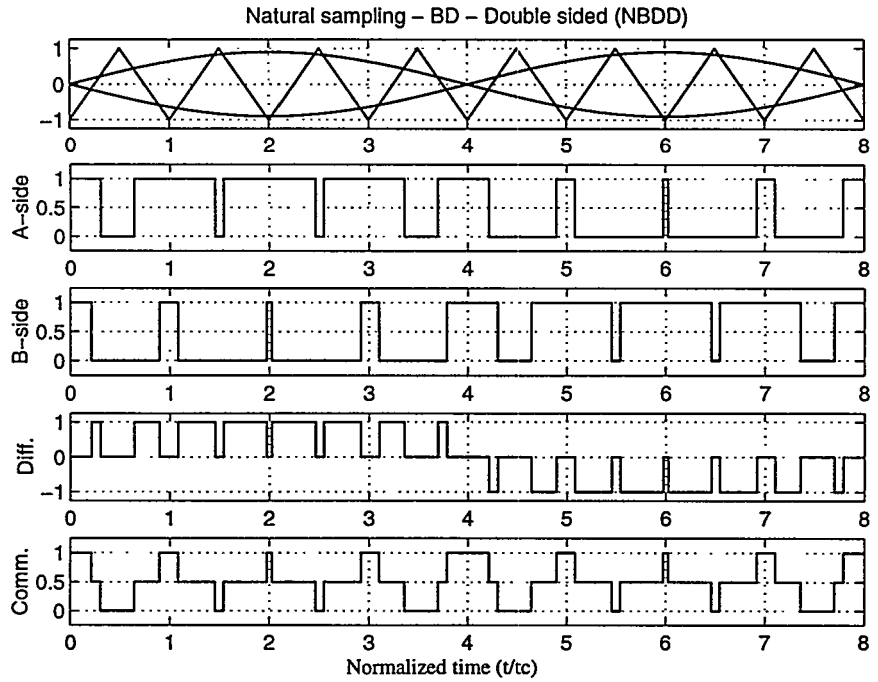


Fig. 2.9 Time domain waveforms for NBDD. $f_r = \frac{1}{8}$.

Another constraining factor for the maximal frequency ration is observed by considering the slew-rates of the carrier and modulating reference signal (assuming unity amplitudes on carrier and signal):

$$SR_{carrier} = 2f_c \quad and \quad SR_{reference} = 2\pi f \quad (Single\ sided\ modulation) \tag{2.3}$$

This leads to the following more strict limitation on frequency ratio:

$$SR_{carrier} > SR_{reference} \Leftrightarrow f < \frac{f_c}{\pi} \Leftrightarrow f_{r,max} = \frac{1}{\pi} \quad (Single\ sided\ modulation) \tag{2.4}$$

Similarly for double sided modulation:

$$SR_{carrier} > SR_{reference} \Leftrightarrow f \leq \frac{2f_c}{\pi} \Leftrightarrow f_{r,max} = \frac{2}{\pi} \quad (Double\ sided\ modulation) \tag{2.5}$$

Harmonic Envelope Surface (HES)

The HF characteristics vary considerably between modulation principles. Subsequently, a detailed investigation of the high frequency spectral characteristics is carried out for each considered scheme. The non-linear nature of PWM causes intermodulation between the carrier and the modulating signal such that $f_{r,max}$ is further constrained. A visualization tool - the **Harmonic Envelope Surface (HES)** – is utilized to provide clear picture of the HF spectral characteristics. The basic idea is to envision the amplitude spectrum vs. the modulation index M and normalized frequency f_r with color or grayscale defining amplitude. The HES parameter space used throughout the following sections is:

Parameter	Symbol	Space
Modulation index	M	-100dB to 0dB.
Frequency ratio	f_r	$\frac{1}{16}$
Normalized frequency	f/f_c	0 - 4

Definition of HES parameter space

The HES thus represents an infinite set of discrete amplitude spectra in a single compact figure where the modulation index is swept within the defined range. This provides an excellent insight into the spectral characteristics of the modulation scheme over the total dynamic range of typical power amplifiers. It has been found appropriate to chose a frequency ratio close to a worst case situation, which in case of the four fundamental schemes is $f_r = \frac{1}{16}$. The choice of frequency ratio is not of primary importance in order to reveal the characteristics and between modulation schemes. The conclusions from a single HES can be generalized to other frequencies.

Total Harmonic Distortion

An important comparison parameter is the forward harmonic distortion of the modulated signal. This parameter differs widely between the general sampling schemes of PWM. THD is generally dependent on both frequency and modulation index, so an investigation vs. both of theses parameters are required.

Other parameters

The above parameters focus on the isolated signal processing aspects of PWM without considering the influences on other parts of the PMA system. In terms of the switching power stage, this is reasonable since all the considered methods are realized effectively by the same H-bridge topology. Issues regarding power stage synthesis and optimization are discussed more closely in Chapter 4. However, the demodulation filtering requirements will depend on the modulation scheme. This is mainly due to the differences in terms of common mode output, which differs considerably between the methods, as shown in Fig. 2.6 - Fig. 2.9. The demodulation filtering is notably simpler for schemes without common mode output and this should be considered in their favor. Besides demodulation, the HF-characteristics also influence control systems that rely on sensing output variables for feedback. Here a minimal amount of HF, both differential and common mode, is desirable.

2.4 DFS synthesis for NPWM methods

The basic theory for the development of double Fourier series expressions to represent double periodic waveforms is described in detail Appendix B.1. DFS expressions for both the differential and common mode for the four schemes are derived in Appendix B.2. The resulting expressions are repeated below.

The DFS for the differential output for the four modulation methods are:

$$\begin{aligned} F_{NADS} &= M\cos(y) \\ &+2\sum_{m=1}^{\infty}\frac{1-J_0(m\pi M)\cos(m\pi)}{m\pi}\sin(mx) \\ &-2\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\infty}\frac{J_n(m\pi M)}{m\pi}\sin(mx+ny-m\pi-\frac{n\pi}{2}) \end{aligned} \tag{2.6}$$

$$\begin{aligned} F_{NBDS} &= M\cos(y) \\ &-2\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\infty}\frac{J_n(m\pi M)}{m\pi}\cos(mx+ny-m\pi)\sin(\frac{n\pi}{2}) \end{aligned} \tag{2.7}$$

$$\begin{aligned} F_{NADD} &= M\cos(y) \\ &+2\sum_{m=1}^{\infty}\frac{J_0(m\pi\frac{M}{2})}{\frac{m\pi}{2}}\sin(\frac{m\pi}{2})\cos(mx) \\ &+2\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\infty}\frac{J_n(m\pi\frac{M}{2})}{\frac{m\pi}{2}}\sin(\frac{(m+n)\pi}{2})\cos(mx+ny) \end{aligned} \tag{2.8}$$

$$\begin{aligned} F_{NBDD} &= M\cos(y) \\ &-4\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\infty}\frac{J_n(m\pi\frac{M}{2})}{m\pi}\sin(\frac{(m+n)\pi}{2})\sin(\frac{n\pi}{2})\sin((mx+ny)-\frac{n\pi}{2}) \end{aligned} \tag{2.9}$$

Where:

M	Modulation index. $M \in [0;1]$.
$x = \omega_c t$	ω_c = Carrier signal angle frequency.
$y = \omega t$	ω = Audio signal angle frequency.
J_n	Bessel function of nth order.
n	Index to the harmonics of the audio signal.
m	Index to the harmonics of the carrier signal.

It is assumed that the output pulse width is unity corresponding to the basic switching topology in Fig. 2.5. The DFS for the common mode output are:

$$F_{NADS,C} = 0 \tag{2.10}$$

$$F_{NBDS,C} = +2\sum_{m=1}^{\infty}\frac{1-J_0(m\pi M)\cos(m\pi)}{m\pi}\sin(mx) - 2\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\infty}\frac{J_n(m\pi M)}{m\pi}\sin(mx+ny-m\pi)\cos(\frac{n\pi}{2}) \tag{2.11}$$

$$F_{NADD,C} = 0 \tag{2.12}$$

$$F_{NBDD,C} = +2\sum_{m=1}^{\infty}\frac{J_0(m\pi\frac{M}{2})}{\frac{m\pi}{2}}\sin(\frac{m\pi}{2})\cos(mx) + 2\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\infty}\frac{J_n(m\pi\frac{M}{2})}{\frac{m\pi}{2}}\sin(\frac{(m+n)\pi}{2})(1+\cos n\pi)\cos(mx+ny) \tag{2.13}$$

2.4.1 Analysis and comparison

For **NADS PWM,** the individual components present in the output spectrum are identified to be:

Component	Amplitude
Fundamental	M
m'th harmonic of carrier my	$2\frac{1-J_0(m\pi M)\cos(m\pi)}{m\pi}$
Intermodulation (IM) components $mx \pm ny$	$\frac{2J_n(m\pi M)}{m\pi}$

One of the most important conclusions is that the modulating signal is left unchanged by the modulation. There are no direct forward harmonics of the modulating reference signal, i.e. the pulse width modulation process can be considered *ideal* in terms of harmonic distortion. This very pleasant characteristic is general for natural sampling.

Fig. 2.10 illustrates the spectral characteristics for NADS by the amplitude spectra at M=0dB and M=-40dB with a frequency ratio of $f_r = 1/16$. The Harmonic Envelope Surface (HES) further illustrates the spectral characteristics in the interesting frequency range and the interesting range of modulation depths from –100dB to 0dB. The color map of the HES has been chosen to be grayscale for the present black and white reproduction. Black indicates full scale relative amplitude or 0dB and white indicates –100dB. According the DFS for NADS, amplitude of the modulated component will be exactly M. Subsequently, the fundamental modulated component in the HES at f_r (to the left) can be used as reference color scale to determine the amplitude of other components in the HES.

The spectral analysis reveals the following interesting facts for NADS:

- The intermodulation components are very pronounced at $mx \pm ny$, and depend heavily on the modulation index M. This is seen as 'skirts' around harmonics of the carrier, a general characteristics for pulse width modulation.
- The idle spectrum has significant harmonic components around odd harmonics of the carrier. This is to expect since the idle spectrum is a pure squarewave.
- Only the components related to the even harmonics of the carrier reduce with M and are totally eliminated at idle.

For **NBDS PWM,** the individual harmonic components are identified to be:

Component	Amplitude
Fundamental	M
IM – component $mx \pm ny$ (Differential)	$\frac{2J_n(m\pi M)}{m\pi}\sin(\frac{n\pi}{2})$
m'th harmonic of carrier my (Common-mode)	$2\frac{1-J_0(m\pi M)\cos(m\pi)}{m\pi}$
IM – component $mx \pm ny$ (Common-mode)	$\frac{2J_n(m\pi M)}{m\pi}\cos(\frac{n\pi}{2})$

Fig. 2.11 shows the spectral characteristics. Several important differences are observed compared to NADS:

- The HES-surface shows very pleasant spectral characteristics at lower modulation depth. All high frequency components disappear at idle.
- No harmonics of the carrier are present in the output spectrum.
- The IM components are proportional to M at lower modulation index.
- Half of the IM-components are eliminated, i.e. the HES has a 'striped' nature.
- The maximal IM-component amplitudes are lower since three levels are synthesized.

In general, NBDS is concluded to be superior in terms of HF-characteristics of the differential output. Unfortunately, the NBDS common mode output contains severe common mode output, as illustrated by the HES in Fig. 2.14.

For **NADD PWM,** the components are:

Component	Amplitude
m'th harmonic of carrier *my*	$\frac{2J_0(m\pi\frac{M}{2})}{\frac{m\pi}{2}}\sin(\frac{m\pi}{2})$
IM-component $mx \pm ny$	$\frac{2J_n(m\pi M)}{\frac{m\pi}{2}}\sin((m+n)\frac{\pi}{2})$

Fig. 2.12 shows the general spectral characteristics for NADD. The following interesting facts are concluded:

- The argument to the Bessel functions is *halved* in comparison with NADS and NBDS. Thus, the IM-components are considerably lower than for single sided modulation.
- The HF-spectrum has a 'striped' character, i.e. half of the components are eliminated.

From the modulation spectral characteristics, NADD must be concluded to be superior to NADS, but not as attractive as NBDS mainly due to the characteristics at lower modulation index.

For **NBDD PWM,** the output amplitude spectrum is composed of the following components:

Component	Amplitude
Fundamental	M
IM-component $mx \pm ny$ (Differential)	$\frac{4J_n\left(m\pi\frac{M}{2}\right)}{m\pi}\sin(\frac{(m+n)\pi}{2})\sin(\frac{n\pi}{2})$
IM-component $mx \pm ny$ (Common-mode)	$\frac{4J_n\left(m\pi\frac{M}{2}\right)}{m\pi}\sin(\frac{m\pi}{2})$
IM-component $mx \pm ny$ (Common-mode)	$\frac{4J_n\left(m\pi\frac{M}{2}\right)}{m\pi}\sin(\frac{(m+n)\pi}{2})(1+\cos(n\pi))$

Fig. 2.13 shows the spectral characteristics for NBDD. The effective sampling frequency is *doubled* for the differential output, by the elimination of all harmonics around odd multiples of the carrier. In terms of differential output, NBDD has by far the most attractive spectral characteristics for all four NPWM methods. However, as with NBDS there is a drawback in terms of the common mode on the output terminals. This is obvious from the HES for the common mode shown in Fig. 2.15. Observe, how the common mode characteristics have improved slightly compared to NBDS. The components around the first harmonic of the carrier are the most problematic since these components puts leads to strong demands on common mode filtering. Note that the common-mode components are present at full scale even at zero modulation.

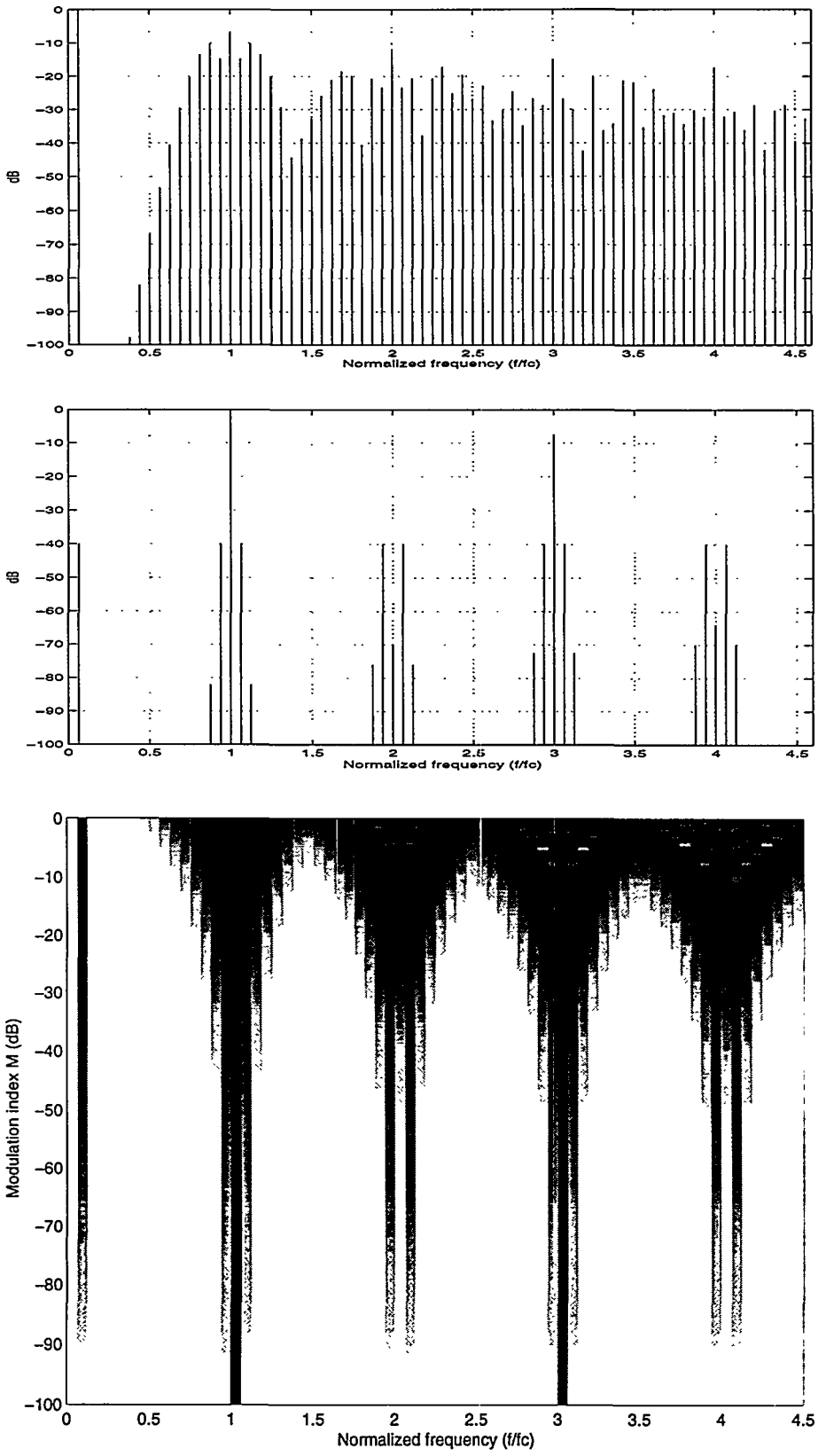


Fig. 2.10 Frequency domain characteristics for NADS. Top and mid subfigure shows amplitude spectrum at *M=0dB* and *M=-40dB*. Bottom subfigure shows the HES-plot for NADS. The HES color map is defined as: black indicates 0dB relative magnitude or full scale and white –100dB.

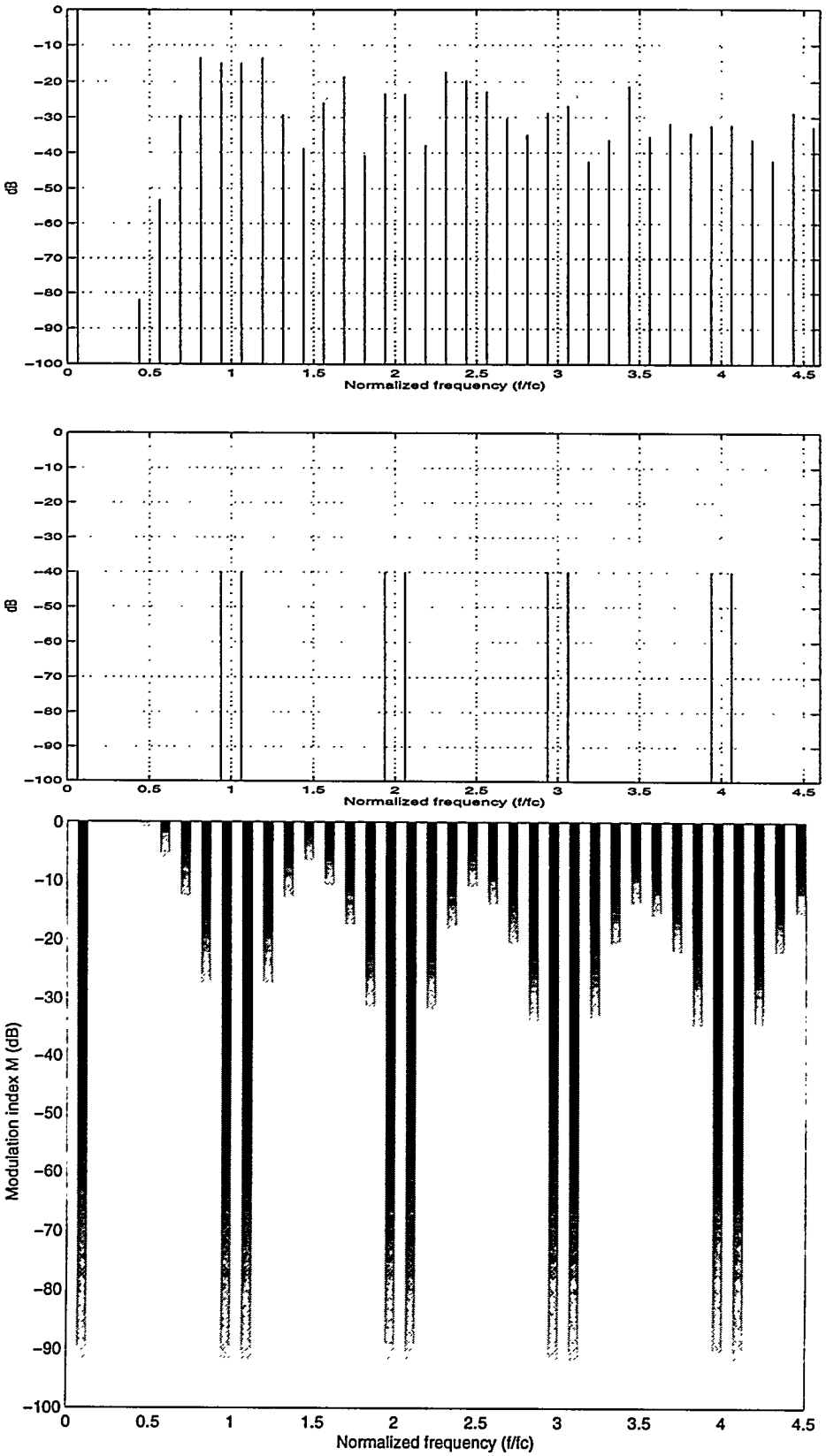


Fig. 2.11 Frequency domain characteristics for NBDS.

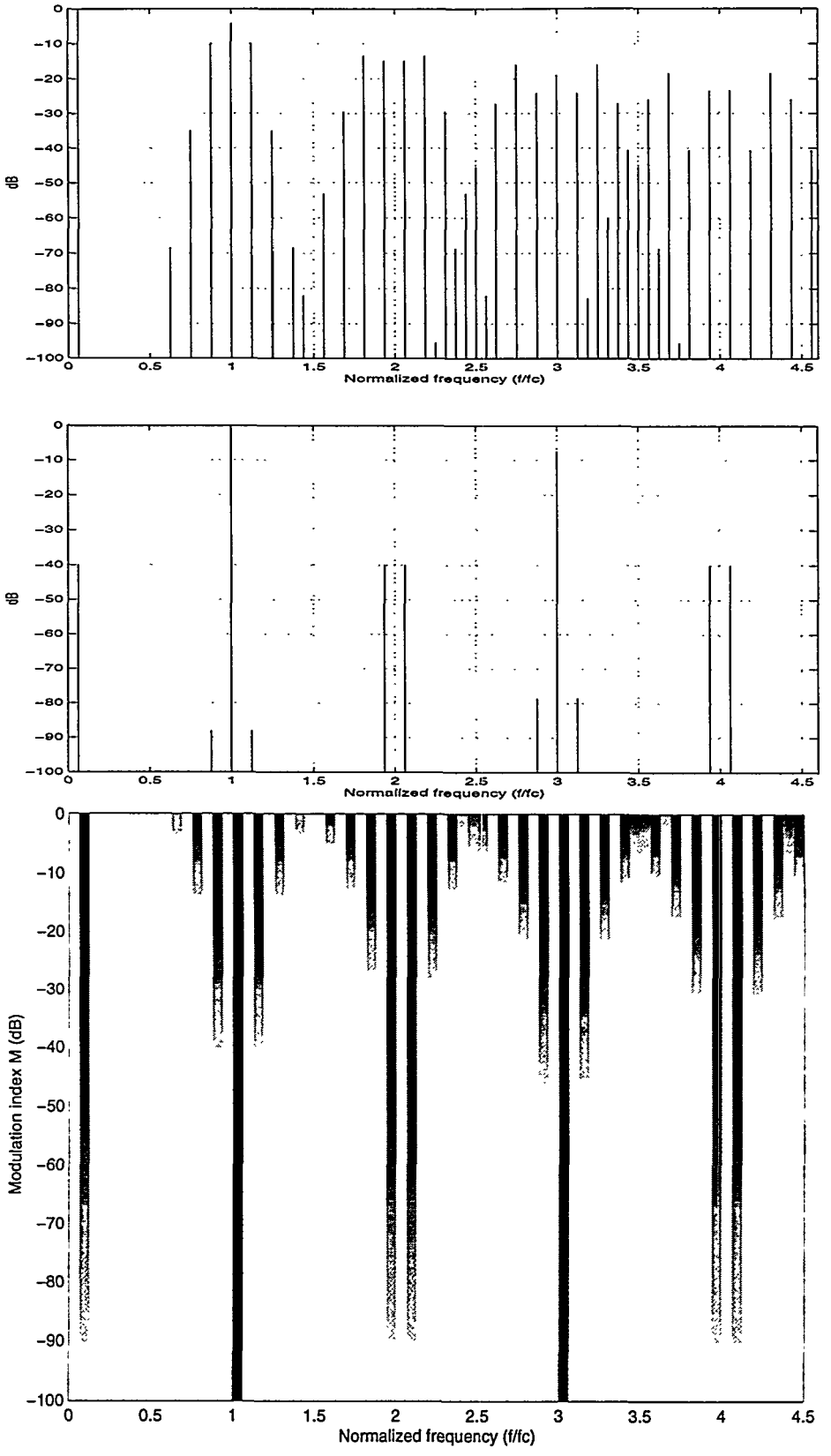


Fig. 2.12 Frequency domain characteristics for NADD.

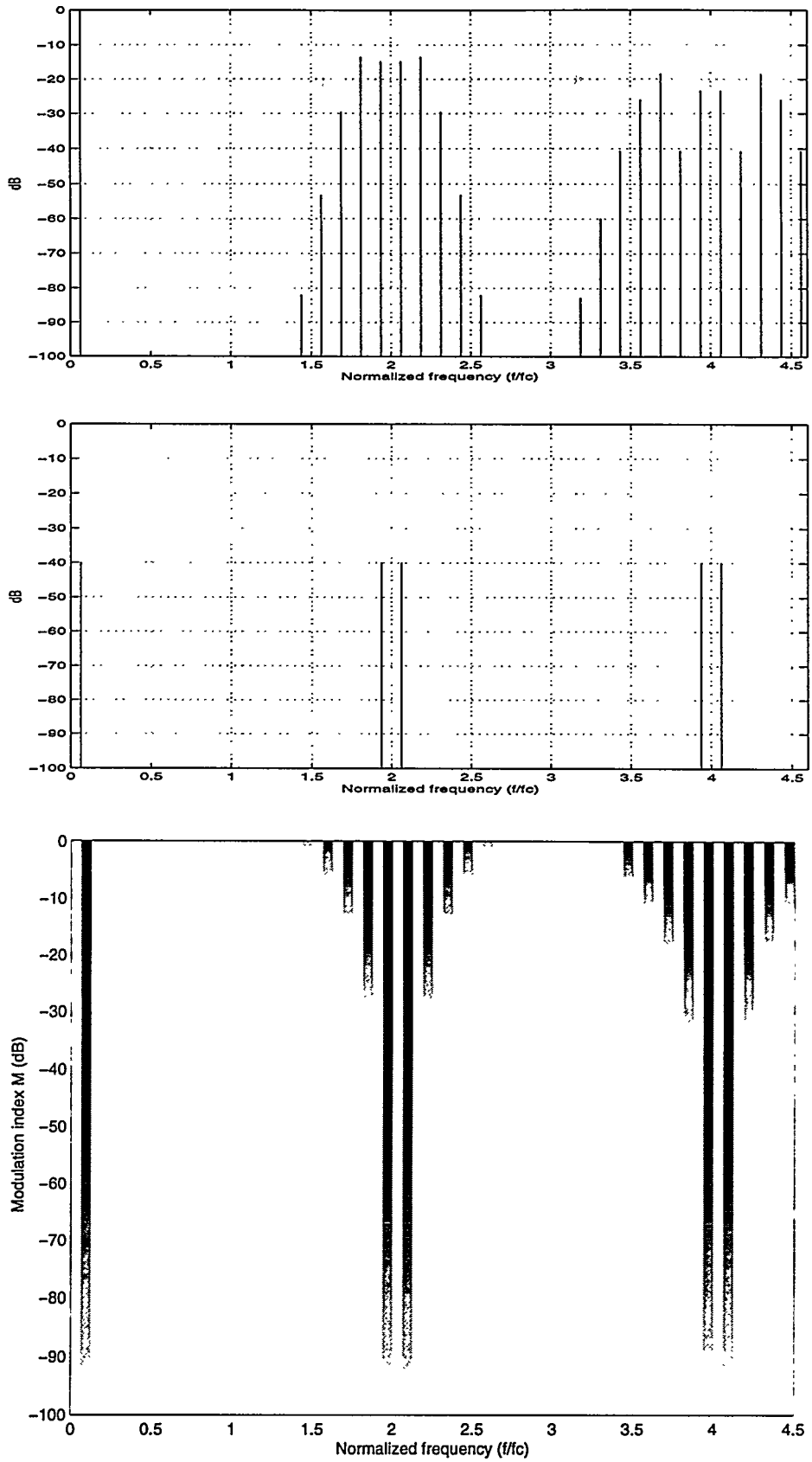


Fig. 2.13 Frequency domain characteristics for NBDD.

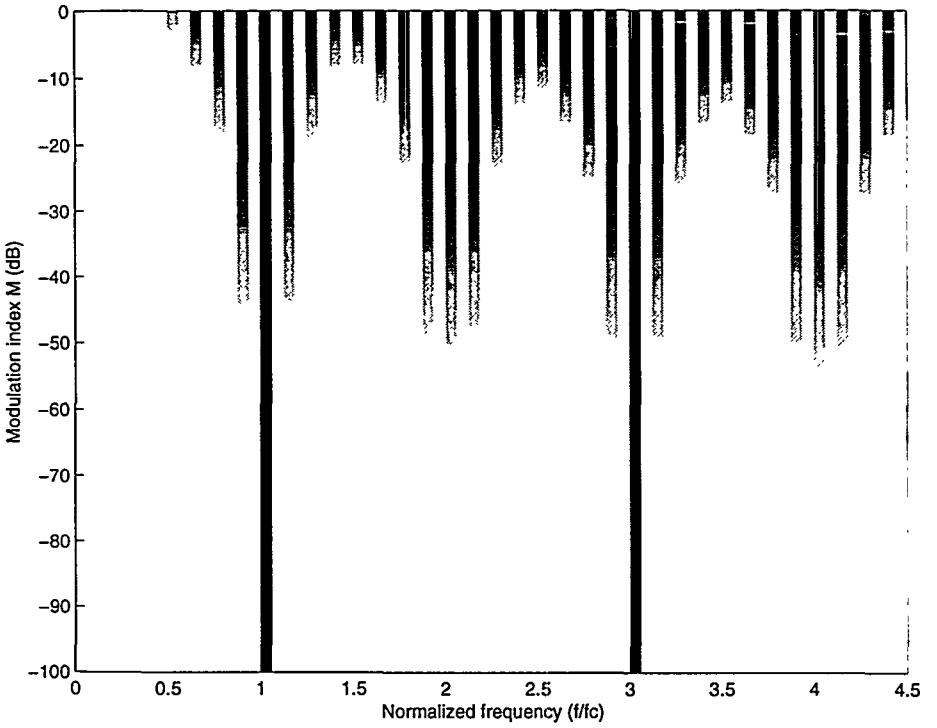


Fig. 2.14 HES for the NBDS common mode output

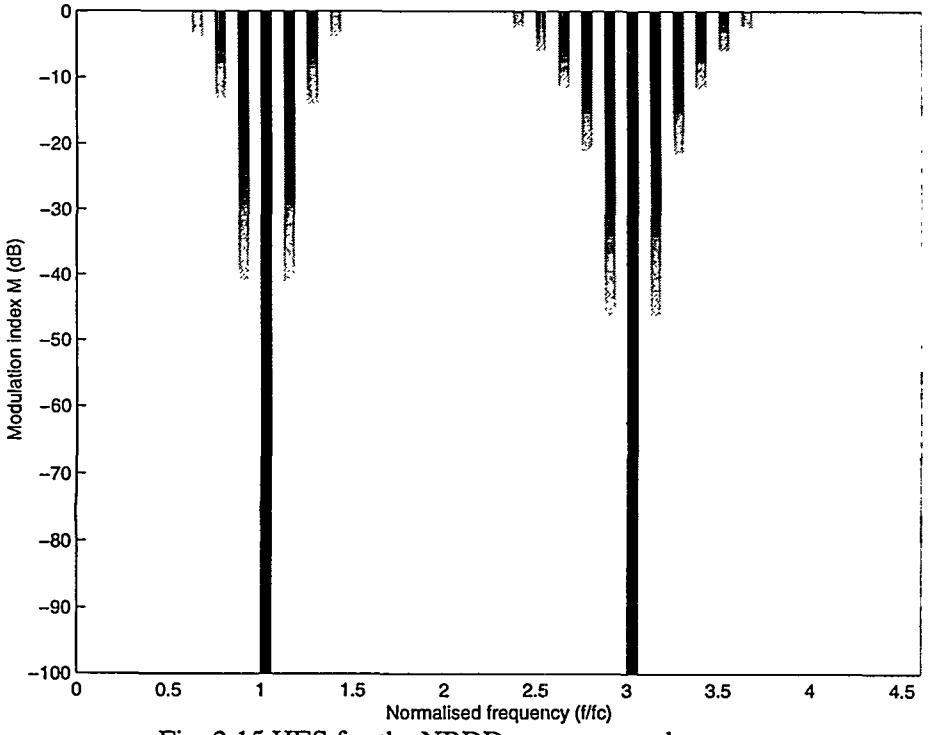


Fig. 2.15 HES for the NBDD common mode output

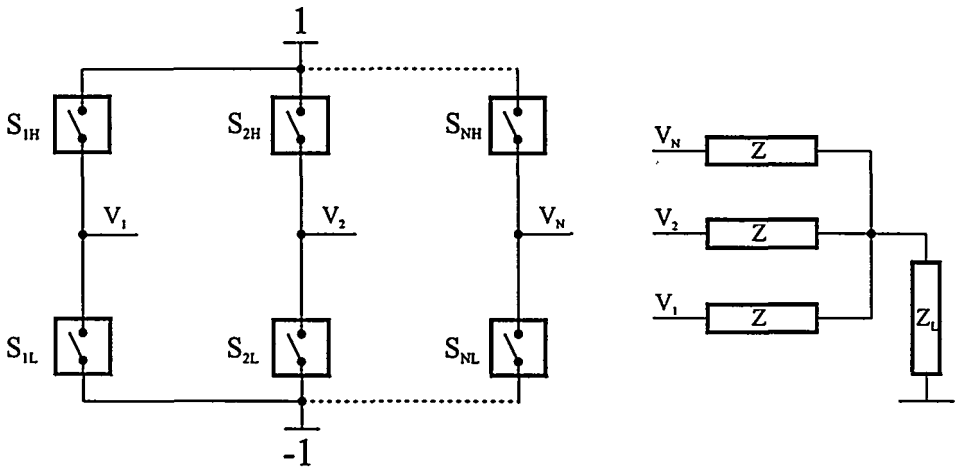


Fig. 2.16 General PSCPWM switching power stage topology.

2.5 Phase Shifter Carrier PWM (PSCPWM)

From the analysis of the fundamental PWM methods the question arises if it is possible, by simple means, to synthesize even more efficient PWM waveforms than NBDD ? An enhanced pulse modulated waveform with minimal HF content would certainly be interesting. There is enough motivating factors, as improved demodulation, lower switching frequency and a reduction of switching noise in measured variables for control systems. However, enhanced pulse modulation methods are only interesting if:

- There are simple implementation strategies.
- There is a possibility for single or dual supply operation for minimal power supply complexity.
- The power stage linearity is not be compromised. The linearity should be comparable to what can be achieved with the four fundamental PWM methods using the H-bridge topology.

A new scheme is introduced in the following called *Phase Shifted Carrier Pulse Width Modulation (PSCPWM or PSC in short)* - that can be considered a multi-level PWM method. Multi-level PWM has never been considered for PMAs before and the subject is therefore new in the field. The general switching power stage structure for PSCPWM is shown in its most general form in Fig. 2.16.

A typical approach to obtain higher powers in a switching power stage is to parallel switches or bridge legs that are driven with the same modulator. The PSCPWM power stage topology in Fig. 2.16 is equally based on paralleling of switching legs, i.e. the topology has some resemblance with this approach. However, instead of just paralleling

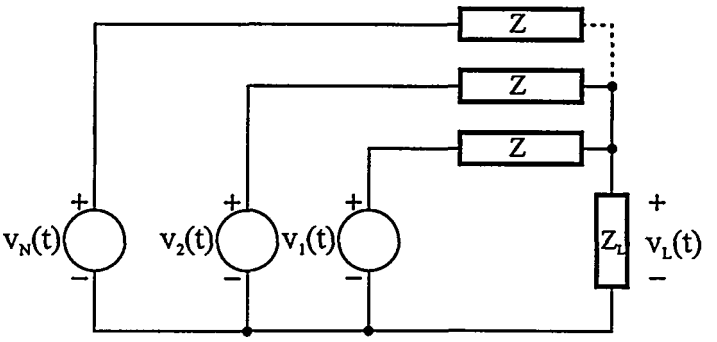


Fig. 2.17 Model of PSC power stage topology.

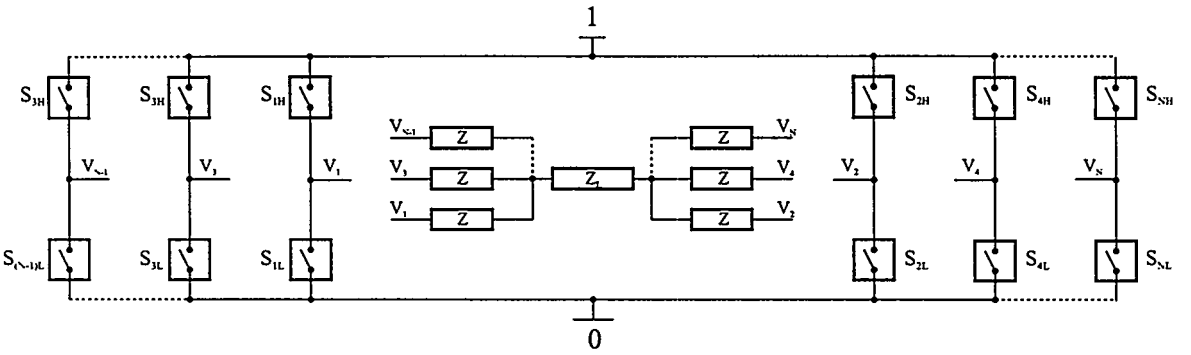


Fig. 2.18 Balanced PSCPWM switching power stage topology.

similar controlled switching legs, it is possible to synthesize highly interesting multi-level modulation waveforms with a more intelligent control of the individual switching legs. The method is based on *interleaving the phase of carrier and/or the modulating signal* to each switching leg by intelligently controlled phase shifts. Fig. 2.17 illustrates a circuit equivalent for PSCPWM where N switching legs are paralleled. The contribution of each generator to the idle output voltage $v_{th}(t)$ (no load) is found by Kirchoff's voltage law. Thus, $v_{p,th}(t)$ can be written as:

$$v_{p,th}(t) = \frac{v_1(t) + \ldots v_N(t)}{N} \tag{2.14}$$

An alternative switching power stage topology for PSCPWM is the balanced topology shown in Fig. 2.18. The topology will be referenced to as the BPSC topology. The advantages of this bridging of the low are well known from the simple H-bridge: the required break down voltage on each switch is halved compared to the single ended topology in Fig. 2.17. Furthermore, only a single supply voltage is required. The disadvantage of the BPSC topology is the potential risk for common mode problems.

2.5.1 PSCPWM control algorithms

The *control algorithm* refers to how the carrier and modulating signal interleaving are controlled. An attractive control method for the PSC topology is:

$$\begin{aligned} \theta_p &= (p-1)\frac{2\pi}{N} \qquad p \in \{1, N\} \\ \varphi_p &= 0 \qquad p \in \{1, N\} \end{aligned} \tag{2.15}$$

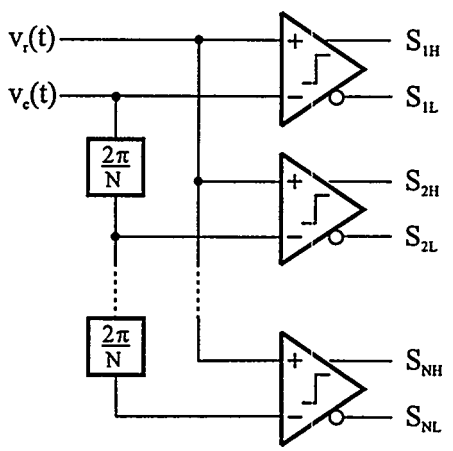


Fig. 2.19 Proposed PSCPWM Modulator structure.

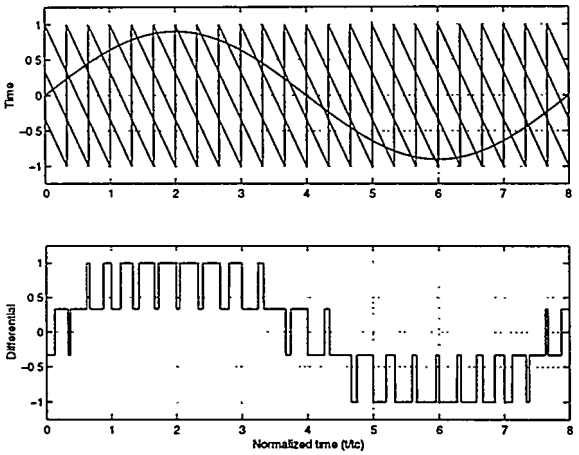
Where θ_p is the phase shift of the $p'th$ carrier relative to some fundamental carrier waveform v_{carr}, and φ_p is the phase shift of the $p'th$ modulating reference v_r. v_{carr} may be both a single sided and a double sided carrier, and the control algorithm will henceforth be referenced to as ***NS*** and ***ND*** for **N**atural sampled **S**ingle sided PSCPWM and **N**atural sampled **D**ouble sided PSCPWM, respectively. The modulator structure corresponding to this control algorithm is shown in Fig. 2.19. The equal distribution of the carrier phase shifts in (2.15) provides some extremely attractive HF-characteristics as it will be shown during the analysis of the different methods in the following. Clearly, the complexity of PSCPWM increases linearly with N in terms of the number of transistors, comparators and carriers. This is one of the drawbacks of using PSCPWM.

Fig. 2.20 shows the time domain waveforms for *NS* and *ND* PSCPWM with N=3, 4 and 8 switching legs. The structure of each subfigure is the same: Top figure illustrates the modulating signal and the interleaved carriers with the given parameters. Bottom figure illustrates the resulting differential output (the single ended topology does not generate any common mode output). From this time domain analysis the following distinct properties are observed:

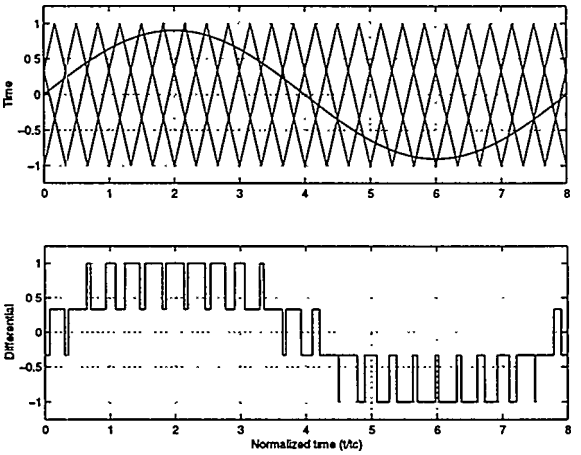
- The control strategy leads to a *N+1 level* effective pulse width modulated waveform with N switching legs. This is a general feature of the control strategy independent on edge modulation and N.
- The multiple level characteristic causes the effective switching amplitude to be *reduced* by a factor $\frac{1}{N}$ compared to the 2-level (N=1) situation. It is apparent from the time domain figures that the HF-content in the switching waveform reduces dramatically with N.

Note, that it is not possible to *physically* measure the multi-level signal at any point in the power stage, since the PSCPWM waveform is generated as an effective superposition of the individual bridge phase signals. This summation takes place via. summing currents that flow in the summing impedance's Z. However, it is possible to measure the filtered version of the PSCPWM waveform on the output of the system.

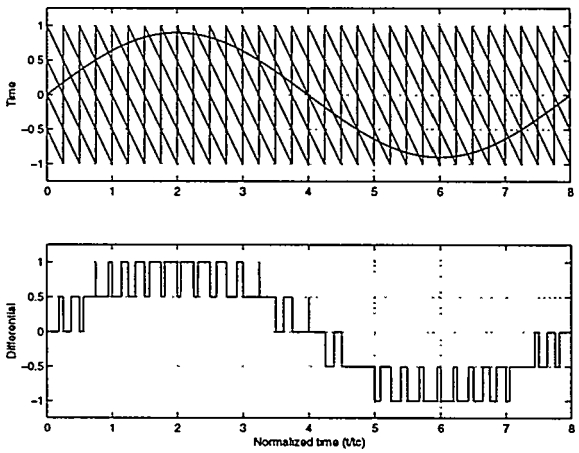
For PMAs the most interesting cases are *N=3* and *N=4* since the modulator and power stage complexity should be kept low. The time domain waveforms for *N=8* above mainly serves to illustrate how *near perfect synthesis* of the modulating sine wave can be implemented with the general PSCPWM principle. In other applications, i.e. in high power inverter systems the use of more 8 switching legs is much more realistic. The specified control algorithm (2.15) in the sense that no other control algorithm will provide better synthesis of the modulating signal with N independently controlled modulators



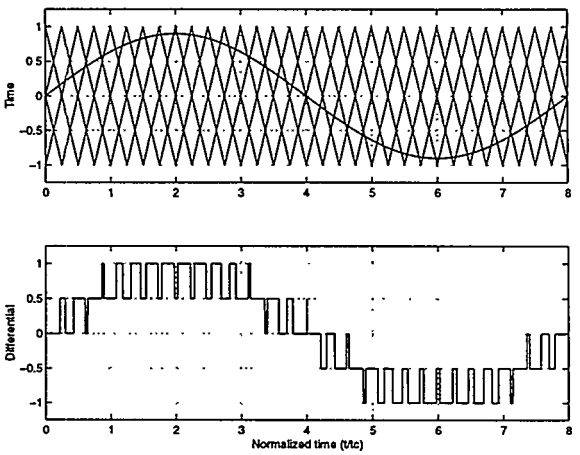
NS. N=3. f_r =1/8. M=0.9.



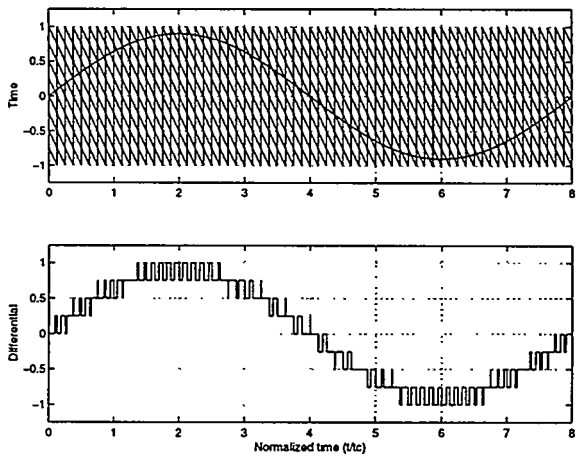
ND. N=3. f_r =1/8. M=0.9.



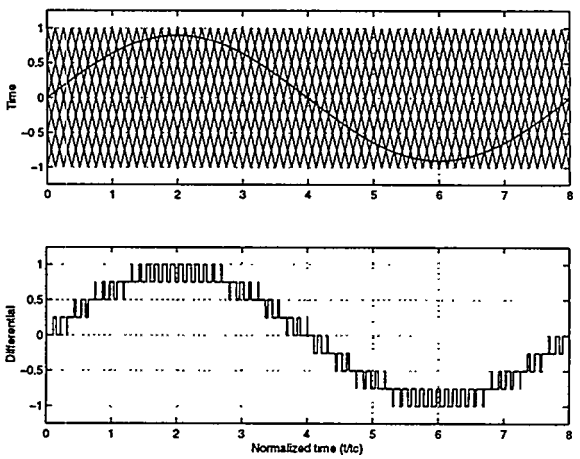
NS. N=4. f_r =1/8. M=0.9.



ND. N=4. f_r =1/8. M=0.9.



NS. N=8. f_r=1/8. M=0.9.



ND. N=8. f_r =1/8. M=0.9.

Fig. 2.20 Comparing time domain characteristics for PSCPWM with *N*=3, 4 and 8. *NS* (single sided) output waveforms are shown left and *ND* (double sided) output waveforms are shown right. The structure of all time domain plots is the same: Top: Modulating signal and interleaved carriers, Bottom: resulting effective output waveform $v_{p,th}$.

2.5.2 Control algorithms for balanced PSCPWM

The BPSC power stage topology in Fig. 2.18 differs significantly from the PSC topology in that the modulators drive each side of the load. Thus, $v_{p,th}(t)$ is:

$$v_{p,th}(t) = \frac{v_1(t) + v_3(t) \ldots + v_{N-1}(t)}{N} - \frac{v_2(t) + v_4(t) \ldots v_N(t)}{N} \tag{2.16}$$

The optimal control algorithm that has been specified for the basic PSCPWM switching topology above, can not be used directly applied to the BPSC switching topology. Three different control algorithms have been devised for the balanced topology, all with interesting properties.

Balanced PSCPWM type 1 is defined by the following control algorithm:

$$\begin{aligned} &\theta_{L,p} = (p-1)\frac{2\pi}{N_s} \quad and \quad \theta_{R,p} = (p-1)\frac{2\pi}{N_s} + \frac{\pi}{N_s} \qquad p \in \{1 \ldots N_s\} \\ &\varphi_{L,p} = 0 \quad and \quad \varphi_{R,p} = \pi \qquad , p \in \{1 \ldots N_s\} \end{aligned} \tag{2.17}$$

Where $N_s = N/2$ and $\theta_{L,p}/\theta_{R,p}$ is the phase shift of the $p'th$ carrier on the left/right side of the load relative to some fundamental carrier waveform $v_c(t)$. Similarly, $\varphi_{p,L}/\varphi_{p,R}$ denotes the phase shift of the $p'th$ modulating signal on the left and right side of the load, relative to the fundamental modulation signal $v_r(t)$. The basic principle is to distribute the N interleaved carries equally on each side of the load and invert the modulating signal to the right side of the load.

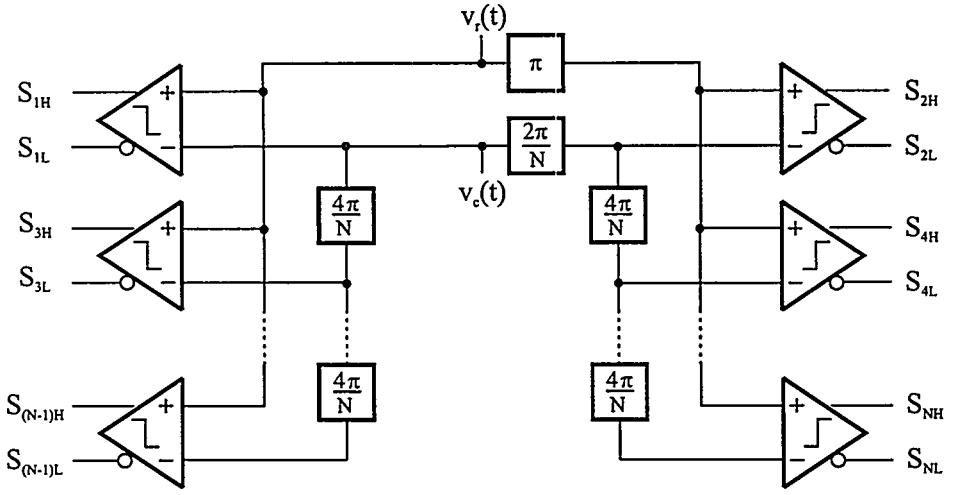
Balanced PSCPWM type 2 is a simplified control algorithm where the numbers of carriers are halved compared to type 1. The control algorithm is defined as:

$$\begin{aligned} &\theta_{L,p} = (p-1)\frac{\pi}{N_s} \quad and \quad \theta_{R,p} = (p-1)\frac{\pi}{N_s} \qquad p \in \{1 \ldots N_s\} \\ &\varphi_{L,p} = 0 \quad and \quad \varphi_{R,p} = \pi \qquad p \in \{1 \ldots N_s\} \end{aligned} \tag{2.18}$$

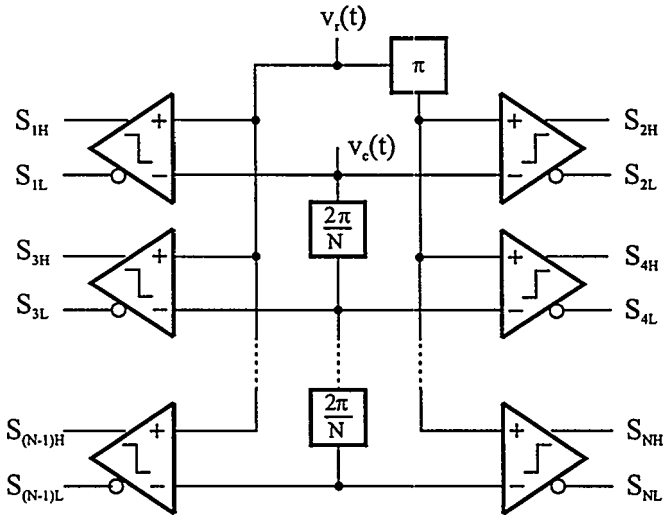
Balanced PSCPWM type 3 is familiar to type 2 by only utilizing N/2 carriers. However, the interleaving of carriers is different:

$$\begin{aligned} &\theta_{L,p} = (p-1)\frac{2\pi}{N_s} \quad and \quad \theta_{R,p} = (p-1)\frac{2\pi}{N_s} \qquad p \in \{1 \ldots N_s\} \\ &\varphi_{L,p} = 0 \quad and \quad \varphi_{R,p} = \pi \qquad p \in \{1 \ldots N_s\} \end{aligned} \tag{2.19}$$

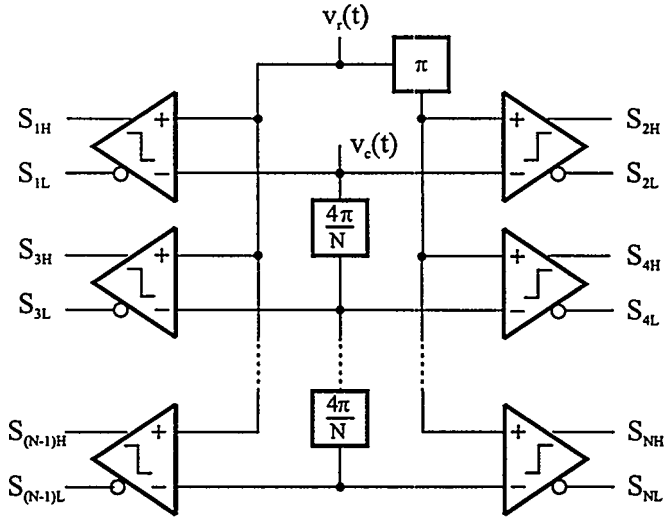
The three balanced control algorithms can be visualized by modulator structures as shown in Fig. 2.21.



Modulator structure for BPSC – Type 1.

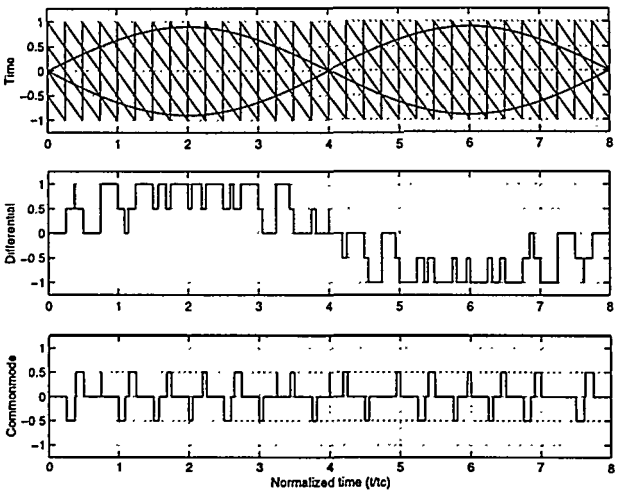


Control algorithm for BPSC – Type 2.

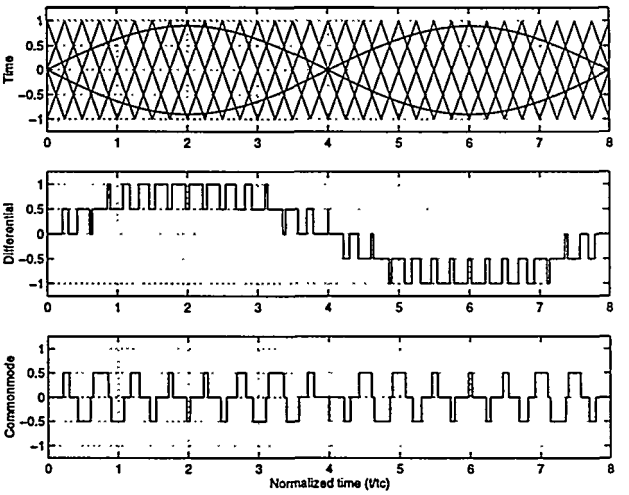


Modulator structure for BPSC – Type 3.

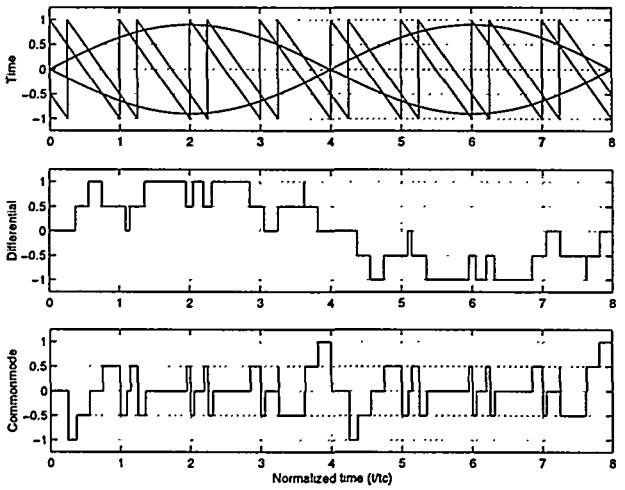
Fig. 2.21 Modulator structures for Balanced PSCPWM. From top to bottom the type 1, 2 and 3 general modulators are shown.



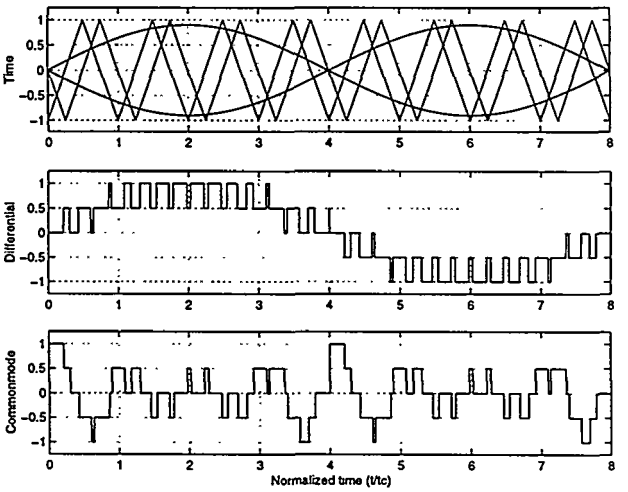
Method : BNS1 .N=4. f_r=1/8. M=0.9.



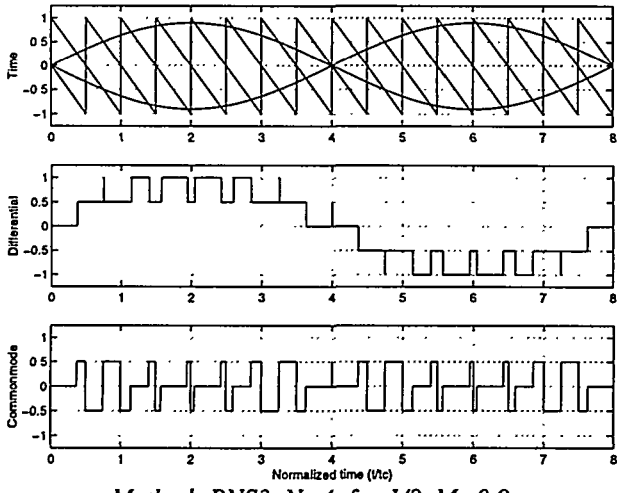
Method : BND1. N=4. f_r=1/8. M=0.9.



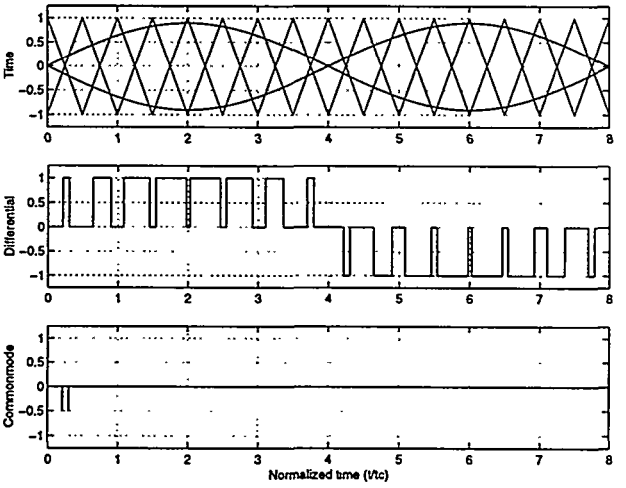
Method : BNS2. N=4. f_r =1/8. M=0.9.



Method : BND2. N=4. f_r =1/8. M=0.9.



Method: BNS3. N=4. f_r =1/8. M=0.9.



Method: BND3. N=4. f_r =1/8. M=0.9.

Fig. 2.22 Comparing time domain characteristics for Balanced PSCPWM Type 1, 2 and 3. *N=4* in all cases. Single side modulated waveforms are shown left and double sided modulated waveforms are shown right. The structure of all time domain waveforms is the same: Top: modulating signal and interleaved carriers, Mid: resulting differential output. Bottom: resulting common mode output.

Configuration	Edge	Abbreviation
Non-balanced	Single sided	NS
	Double sided	ND
Balanced (Type 1,2 and 3)	Single sided	BNS1, BNS2, BNS3
	Double sided	BND1, BND2, BND3

Table 2.3 Definition of PSCPWM methods.

All the above presented control algorithms can be realized with both single sided and double sided modulation and the possible set of PSCPWM variants are summarized in Table 2.3. The time domain characteristics of the balanced PSCPWM methods are illustrated in Fig. 2.22. Only $N = 4$ is considered since this is the most interesting case for the balanced control methods. A general characteristic is the high amount of common mode with all methods which is an inevitable drawback for all methods compared to the non-balanced configuration. A detailed analysis of the differential output requires insight into the frequency domain characteristics. This is the subject of the following section, where DFS expressions are derived for all of the above presented, novel PSCPWM pulse modulation methods.

2.6 PSCPWM analysis

This section focuses on a detailed analysis and comparison of the spectral characteristics of the proposed PSCPWM schemes defined in Table 2.3. Double Fourier series expressions will be derived for all methods. Since PSCPWM multi-level waveforms are all generated by superposition of the contributions from each switching leg, the derivation of the resulting DFS is straightforward in principle. A shown in Appendix B the derivations requires an extensive amount of trivial trigonometric manipulation. Fortunately, all pulse waveform can be represented by a compact DFS expression. The following will only present the resulting DFS expressions that are used to generate the HES.

2.6.1 DFS synthesis for NS and ND

According to (2.14) the equivalent generator voltage of the modulator and power stage for N paralleled switching legs can be written as a sum of N double Fourier series expressions:

$$F_N = \frac{1}{N}\sum_{p=1}^{N} F_{\theta_p} \tag{2.20}$$

With the control algorithm specified in (2.15) each element in the sum (2.20) is derived form the basic single sided two level DFS (NADS) with the substitution $x-\theta_p \rightarrow x$ where θ_p is defined in (2.15):

$$\begin{aligned} F_{NADS,\theta_p} &= M\cos(y) \\ &+ 2\sum_{m=1}^{\infty}\frac{1-J_0(m\pi M)\cos(m\pi)}{m\pi}\sin(mx - m(p-1)\frac{2\pi}{N}) \\ &- 2\sum_{m=1}^{\infty}\sum_{n\pm1}^{\pm\infty}\frac{J_n(m\pi M)}{m\pi}\sin(mx - m(p-1)\frac{2\pi}{N} + ny - m\pi - \frac{n\pi}{2}) \end{aligned} \tag{2.21}$$

As shown in Appendix B.3 the DFS for NS can be written in the following general form for N switching legs:

$$F_{NS,N} = M\cos(y) + 2\sum_{m\in\{N,2N,3N\ldots\}} \frac{1-J_0(m\pi M)\cos(m\pi)}{m\pi}\sin(mx) - 2\sum_{m\in\{N,2N,3N\ldots\}}\sum_{n\pm1}^{\pm\infty} \frac{J_n(m\pi M)}{m\pi}\sin(mx+ny-\frac{n\pi}{2}-m\pi) \tag{2.22}$$

For double edge modulation ND the resulting series reduces to:

$$F_{ND,N} = M\cos(y) + 2\sum_{m\in\{N,2N,3N\ldots\}} \frac{J_0(m\pi\frac{M}{2})}{\frac{m\pi}{2}}\sin(\frac{m\pi}{2})\cos(mx) + 2\sum_{m\in\{N,2N,3N\ldots\}}\sum_{n\pm1}^{\pm\infty} \frac{J_n(m\pi\frac{M}{2})}{\frac{m\pi}{2}}\sin(\frac{(m+n)\pi}{2})\cos(mx+ny) \tag{2.23}$$

The most interesting observation from the resulting DFS for both NS and ND is the similarity with the basic schemes NADS and NADD, respectively. *The PSCPWM output is constituted of a partial set of components from the scheme used in each switching leg.* PSCPWM does *not* contribute with any "new" components. This can be seen by observing the factors in the sums in (2.22) and comparing these with the original DFS expression for single sided modulation in a single switching leg (NADS).

2.6.2 Spectral characteristics

Fig. 2.24 - Fig. 2.28 shows HES-plots for NS and ND with N = 3, 4 and 8. A close investigation of the result reveals some obvious general advantages of these two PSCPWM methods:

- The differential amplitude output spectrum only contains components around multiples of $N \cdot f_c$ for both the single and double-sided case.
- PSCPWM provides an *effective* increase in sampling frequency by a factor of N.
- The maximal amplitude of the high-frequency spectrum, F_{HF}, decreases considerably with N.

This effective increase of sampling frequency is a very useful property, since it can be used effectively to reduce the switching frequency in each switching leg. The PSCPWM algorithm in effect just removes all spectral components in the original single-leg spectrum

except those around multiples of $N \cdot f_c$. These causes the resulting spectral characteristics to differ dependent upon if N is odd or even:

- With even N no harmonics of the carrier are present in the output.
- With even N the HF characteristics are very appealing at lower modulation depths where there is a close to *proportional* relationship between the Intermodulation (IM) - component amplitude and M. Thus, at $M=0$ there are no HF components at all. This resembles the characteristics for three-level methods NBDS and NBDD.
- Odd N leads to less appealing characteristics at idle, where harmonics of the carrier will be present around multiples of Nf_c

The differences between NS and ND are not surprisingly similar to the differences between NADS and NADD. Generally, the side-bands for double sided modulation are smaller and half of the IM-components are eliminated (i.e. a 'striped' nature in the HES). Consequently, ND is preferable.

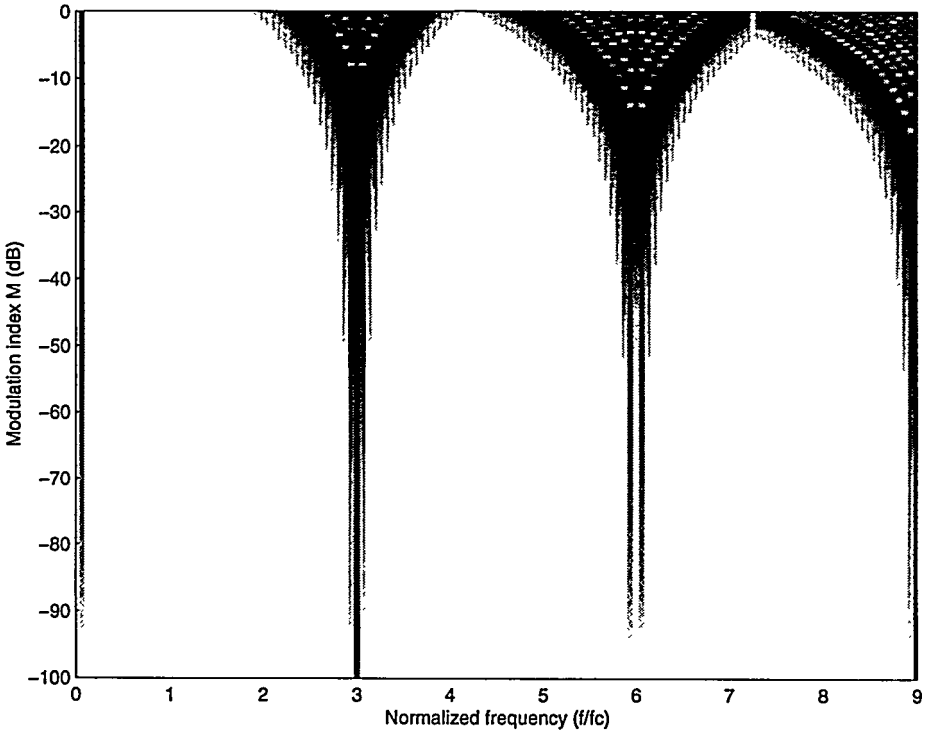


Fig. 2.23 HES-plots for *NS* with *N=3* switching legs.

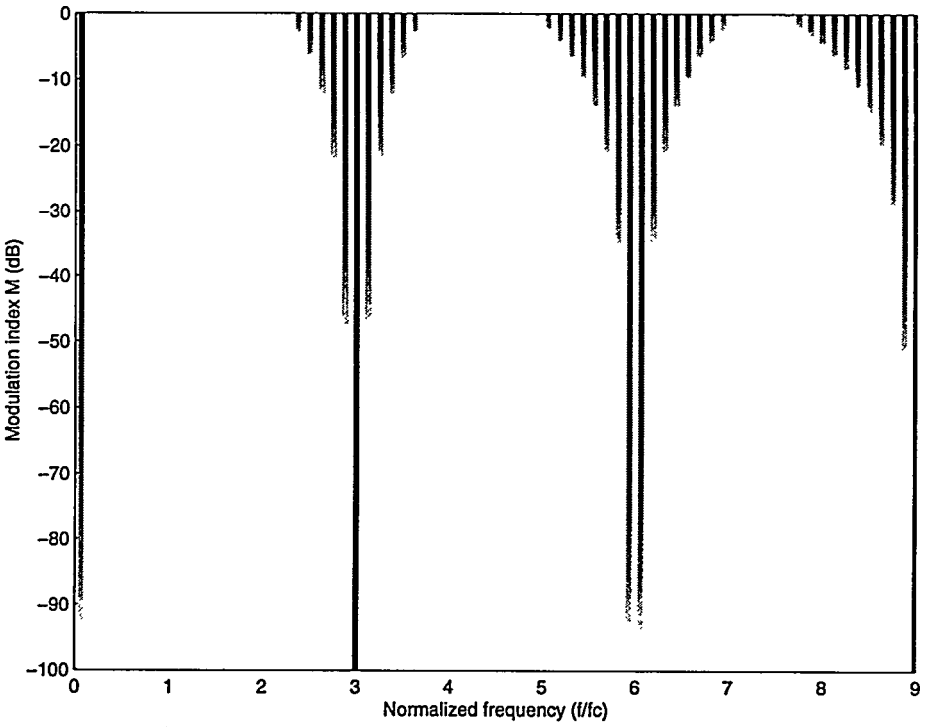


Fig. 2.24 HES-plots for *ND* with *N=3* switching legs.

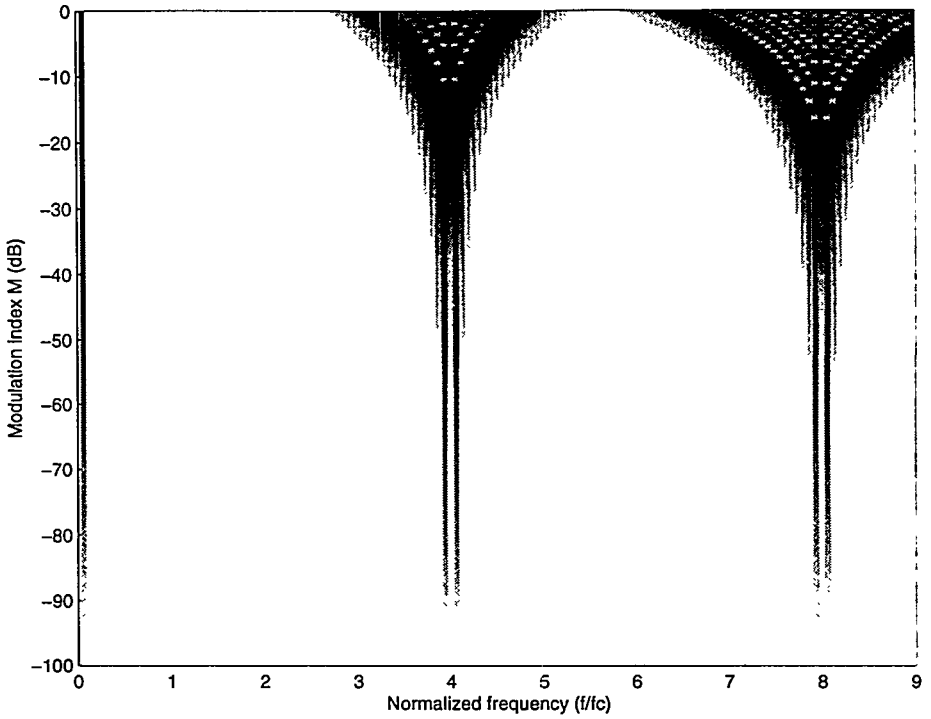


Fig. 2.25 HES-plots for *NS* with *N=4* switching legs.

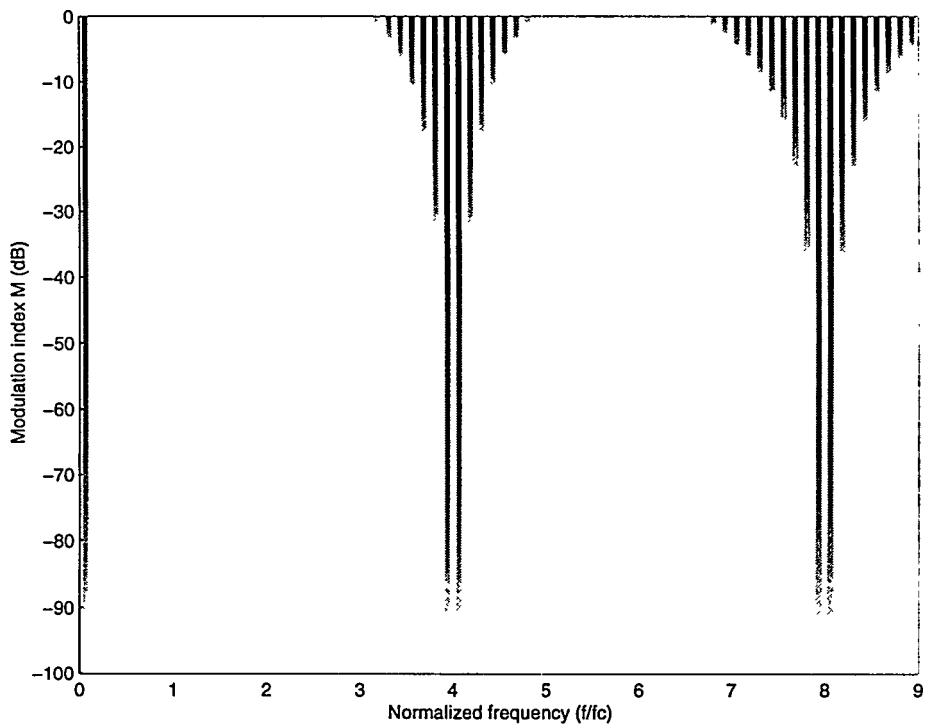


Fig. 2.26 HES-plots for *ND* with *N=4* switching legs.

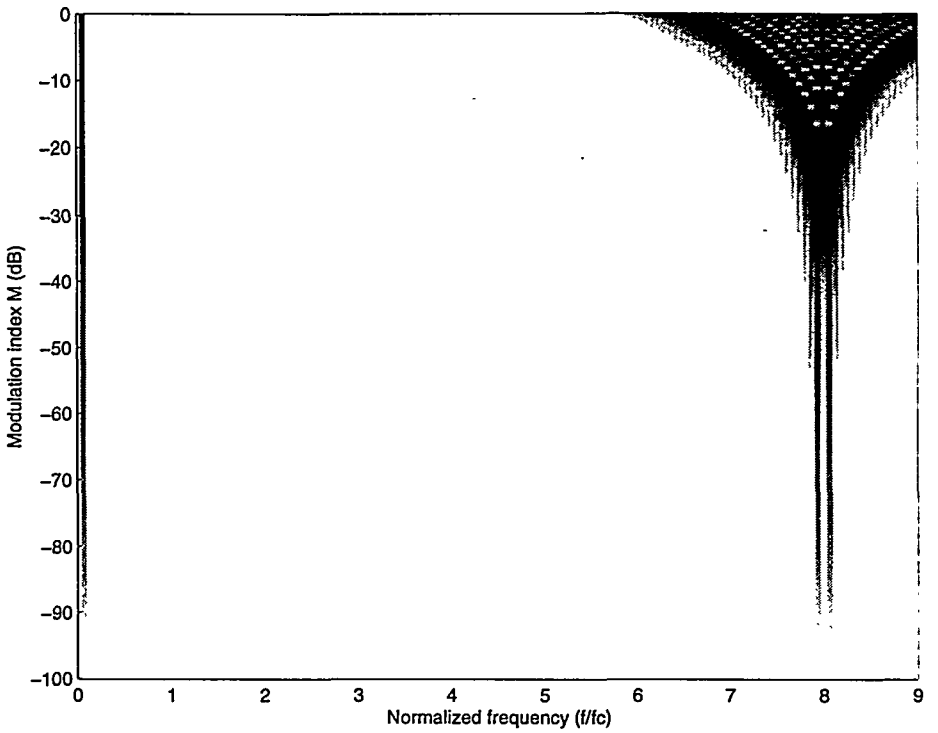


Fig. 2.27 HES-plot for *NS* with *N=8* switching legs.

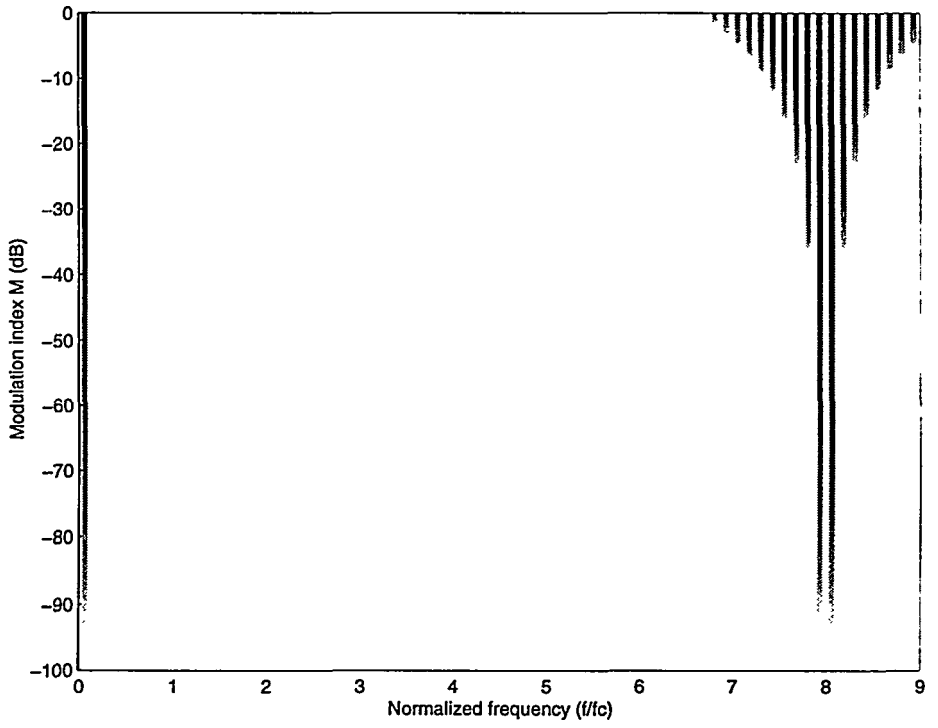


Fig. 2.28 HES-plot for *ND* with *N=8* switching legs.

2.6.3 Balanced PSCPWM type 1 (BNS1/BND1)

The control algorithm for the type 1 balanced configuration is defined above and repeated here:

$$\theta_{L,p} = (p-1)\frac{2\pi}{N_s}, \qquad p \in \{1 \ldots N_S\}$$
$$\theta_{R,p} = (p-1)\frac{2\pi}{N_s} + \frac{\pi}{N_S}, \qquad p \in \{1 \ldots N_S\} \tag{2.24}$$

The time domain characteristics for the control algorithm were shown in Fig. 2.22 for N=4. $N_s = N/2$ indicate the number of modulators on each side of the load. It should be emphasized that BNS1/BND1 is not equivalent to NBDS/NBDD in the case where N=2, corresponding to a simple H-bridge implementation. BNS1/BND1 in this specific case are new interesting modulation methods utilizing N=2 carriers, by which the H-bridge power stage can be controlled.

In the case of single sided modulation the effective signal on left side FL_{BNS1,N_s} and right side FR_{BNS1,N_s} of the load are found by superposition and normalization as:

$$FL_{BNS1,N_S} = \frac{1}{N_S}\sum_{p=1}^{N_S} F_{NADS,\theta_{L,p}} \quad and \quad FR_{BNS1,N_S} = \frac{1}{N_S}\sum_{p=1}^{N_S} F_{NADS,\theta_{R,p}} \tag{2.25}$$

The BNS1 differential and common mode output are:

$$F_{BNS1,N} = \frac{FL_{BNS1,N_S} - FR_{BNS1,N_S,\pi}}{2} \tag{2.26}$$

$$F_{BNS1,N,C} = \frac{FL_{BNS1,N_S} + FR_{BNDS1,N_S,\pi}}{2} \tag{2.27}$$

Exactly the same approach is used to derive expressions for BND1 and all balanced types in general. The details of deriving the resulting expression are show in appendix B.3 (BNS1) and appendix B.4 (BND1). The results are presented below.

BNS1 differential DFS

$$\begin{aligned} F_{BNS1,N} &= M\cos(y) \\ &+ \sum_{m\in\{N_S,2N_S,3N_S\ldots\}} \frac{1-J_0(m\pi M)\cos(m\pi)}{m\pi}\left(1-\cos\left(m\frac{\pi}{N_S}\right)\right)\sin(mx) \\ &- \sum_{m\in\{N_S,2N_S,3N_S\ldots\}} \sum_{n\pm1}^{\pm\infty} \frac{J_n(m\pi M)}{m\pi}\cos(m\pi)\left(1-\cos\left(m\frac{\pi}{N_S}\right)\cos(n\pi)\right)\sin\left(mx+ny-\frac{n\pi}{2}\right) \end{aligned} \tag{2.28}$$

BNS1 common mode DFS

$$F_{BNS1,N,C} = + \sum_{m\in\{N_S,2N_S,3N_S\ldots\}} \frac{1-J_0(m\pi M)\cos(m\pi)}{m\pi}(1+\cos(m\frac{\pi}{N_S}))\sin(mx)$$
$$- \sum_{m\in\{N_S,2N_S,3N_S\ldots\}} \sum_{n\pm1}^{\pm\infty} \frac{J_n(m\pi M)}{m\pi}(1+\cos(m\frac{\pi}{N_S})\cos(n\pi))\sin(mx+ny-m\pi-\frac{n\pi}{2})$$

(2.29)

BND1 differential DFS

$$F_{BND1,N} = M\cos(y)$$
$$+ \sum_{m\in\{N_S,2N_S,3N_S\ldots\}} \frac{J_0(m\pi\frac{M}{2})}{\frac{m\pi}{2}}\sin(\frac{m\pi}{2})(1-\cos(m\frac{\pi}{N_S}))\cos(mx)$$
$$+ \sum_{m\in\{N_S,2N_S,3N_S\ldots\}} \sum_{n\pm1}^{\pm\infty} \frac{J_n(m\pi\frac{M}{2})}{\frac{m\pi}{2}}\sin(\frac{(m+n)\pi}{2})(1-\cos(m\frac{\pi}{N_S})\cos(n\pi))\cos(mx+ny)$$

(2.30)

BND1 common mode DFS

$$F_{BND1,N,C} = \sum_{m\in\{N_S,2N_S,3N_S\ldots\}} \frac{J_0(m\pi\frac{M}{2})}{\frac{m\pi}{2}}\sin(\frac{m\pi}{2})(1+\cos(m\frac{\pi}{N_S}))\cos(mx)$$
$$+ \sum_{m\in\{N_S,2N_S,3N_S\ldots\}} \sum_{n\pm1}^{\pm\infty} \frac{J_n(m\pi\frac{M}{2})}{\frac{m\pi}{2}}\sin(\frac{(m+n)\pi}{2})(1+\cos(m\frac{\pi}{N_S})\cos(n\pi))\cos(mx+ny)$$

(2.31)

2.6.4 Spectral characteristics for Balanced PSCPWM – Type 1.

The BNS1/BND1 methods are now analyzed by the HES that is generated directly from the synthesized DFS expressions. Generally, the performance of the balanced PSCPWM methods depend on $N_s = N/2$. Consequently, BNS1/BND1 are *not* equivalent implementations of *NS/ND* on the BPSC power stage structure.

Fig. 2.29 and Fig. 2.30 shows the HES for the differential and common mode output of BNS1 with four switching legs $N = 4$. Since the carriers are the same as for NS and the modulating signal is inverted to the right side of the load, one should expect exactly the

same spectral characteristics as for NS. The main reason for the significant differences is the subtraction of modulator outputs over the load. The following general characteristics are observed for BNS1.

- Both the differential and common mode contain components around multiples of $f_c N_s = f_c N/2$.
- Although the carrier is single sided, only half of the components are present in the output spectrum (i.e. the "striped" nature of the HES).
- Common mode components are present around multiples of $N_s f_c$.
- No harmonics of the carrier are present in the output spectrum. The dynamic characteristic of the common mode output is very good since the components are close to proportional to the modulation index (i.e. they disappear at idle).

Fig. 2.31 and Fig. 2.32 shows the HES for the differential and common mode output of BND1 in the specific case where $N = 4$. The HES shown that the differential output is as desired i.e. exactly as basic double sided PSCPWM (ND). However, common mode components are generated with the first "lump" present at $f_c N_s$

A more general investigation of BND1 vs. the number of switching legss shows that the general characteristics depend significantly upon if N_s is even or odd:

- For N_s even the differential output is as for ND and there is a common mode output with the first "lump" around $N_s f_c$.
- For N_s odd (not illustrated) the differential output is *not* as ND, but contains HF-modulation components around multiples of $N_s f_c$. However, *no* common mode components are generated.

BND1 with N_s odd is a specifically interesting case in that it synthesizes a multiple level waveform from a single supply level without generating common mode. Thus, PSCPWM solves this fundamental problem that renders conventional methods as NBDS and NBDD unusable in many applications. Comparing BNS1 and BND1 leads to the clear conclusion that BND1 is superior in terms of both differential and common mode characteristics.

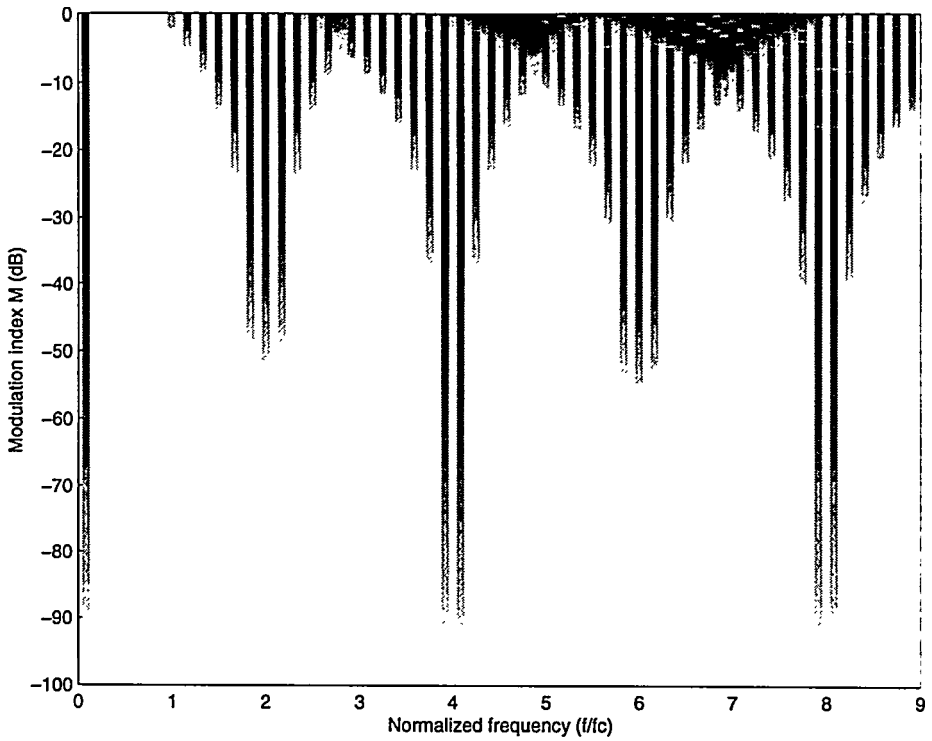


Fig. 2.29 HES-plots for BNS1 differential output with N = 4. f_r=*1/16*.

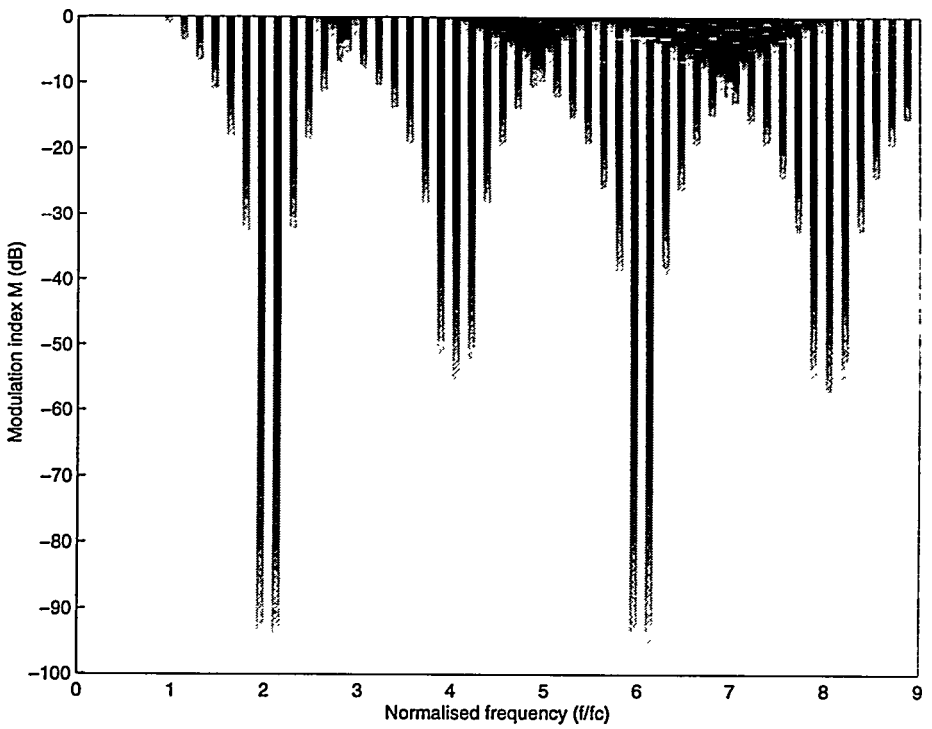


Fig. 2.30 HES-plots for BNS1 common mode output with N = 4. f_r=*1/16*.

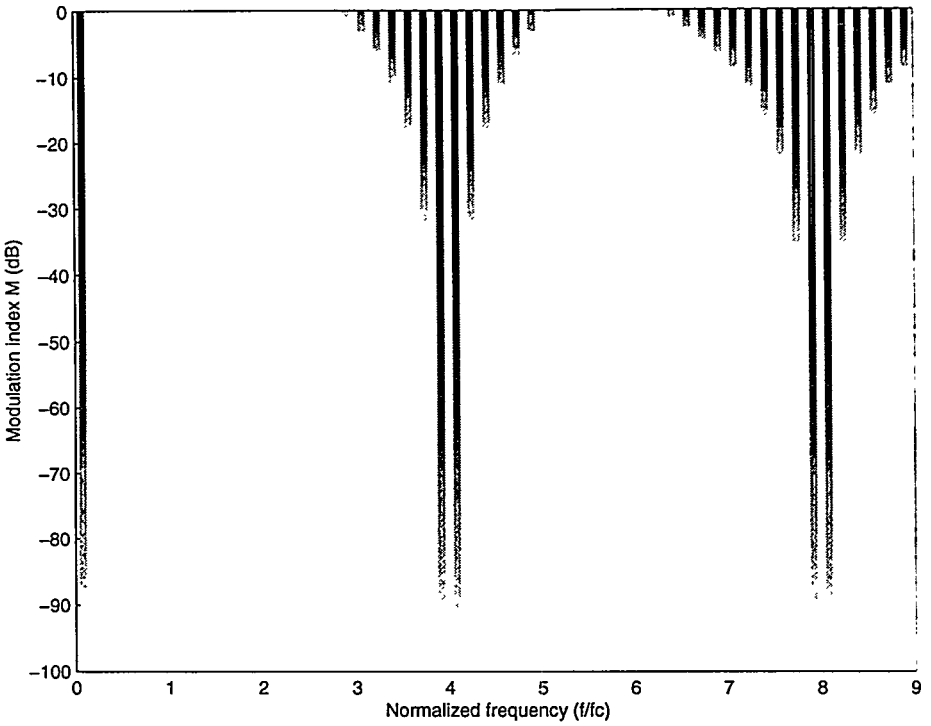


Fig. 2.31 HES-plots for BND1 differential output with N = 4. f_r=*1/16*.

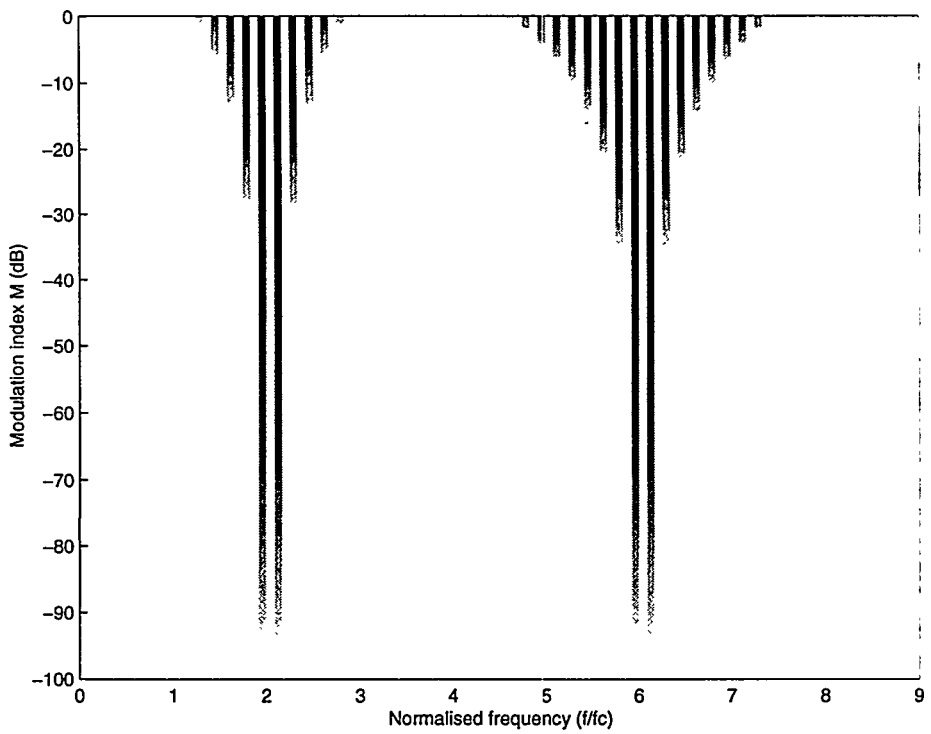


Fig. 2.32 HES-plots for BND1 common mode output with N = 4. f_r=*1/16*.

2.6.5 Balanced PSCPWM type 2 (BNS2/BND2)

The control algorithm for Balanced PSCPWM Type 2, are given in (2.18) and the time domain characteristics were illustrated in Fig. 2.22. The method requires half as many carriers as type 1. The methods should be seen as a generalization of fundamental three-level PWM methods NBDS and NBDD. For N=2, BNS2 is equivalent to NBDS and BND2 equal to NBDD. The derivation of DFS expressions for the BNS2 and BND2 are given in Appendix B.5 / Appendix B.6. The resulting expressions are presented below.

DFS for BNS2 differential output

$$
\begin{aligned}
F_{BNS2,N} &= M\cos(y) \\
&+\frac{1}{N_S}\sum_{m\in\{N_S,2N_S,3N_S,\ldots\}\wedge m\,odd}\sum_{n\pm1}^{\pm\infty}\frac{J_n(m\pi M)}{m\pi}\sin(\frac{m\pi}{2N_S})(1-\cos(n\pi))\cos(mx+ny+\frac{m\pi}{2N_S}-m\pi-\frac{n\pi}{2}) \\
&-\frac{2}{N_S}\sum_{m\notin\{N_S,2N_S,3N_S,\ldots\}\wedge m\,odd}\sum_{n\pm1}^{\pm\infty}\frac{J_n(m\pi M)}{m\pi}\frac{\cos(\frac{m\pi}{2N_S})}{\sin(\frac{m\pi}{N_S})}(\cos(n\pi)-1)\cos(mx+ny+\frac{m\pi}{2N_S}-m\pi-\frac{n\pi}{2}) \\
&+\sum_{m\in\{2N_S,4N_S,6N_S,\ldots\}}\sum_{n\pm1}^{\pm\infty}\frac{J_n(m\pi M)}{m\pi}(\cos(n\pi)-1)\sin(mx+ny+\frac{m\pi}{N_S}-m\pi-\frac{n\pi}{2})
\end{aligned}
\tag{2.32}
$$

DFS for BNS2 common mode output

$$
\begin{aligned}
F_{BNS2,N,C} &= -\frac{2}{N_S}\sum_{m\in\{N_S,2N_S,3N_S,\ldots\}\wedge m\ odd}\frac{1-J_0(m\pi M)\cos(m\pi)}{m\pi}\sin(\frac{m\pi}{2N_S})\cos(mx+\frac{m\pi}{2N_S}) \\
&-\frac{2}{N_S}\sum_{m\notin\{N_S,2N_S,3N_S,\ldots\}\wedge m\ odd}\frac{1-J_0(m\pi M)\cos(m\pi)}{m\pi}\frac{\cos(\frac{m\pi}{2N_S})}{\sin(\frac{m\pi}{N_S})}\cos(mx+\frac{m\pi}{2N_S}) \\
&+2\sum_{m\in\{2N_S,4N_S,6N_S,\ldots\}}\frac{1-J_0(m\pi M)\cos(m\pi)}{m\pi}\sin(mx+\frac{m\pi}{N_S}) \\
&+\frac{1}{N_S}\sum_{m\in\{N_S,2N_S,3N_S,\ldots\}\wedge m\ odd}\sum_{n\pm1}^{\pm\infty}\frac{J_n(m\pi M)}{m\pi}\sin(\frac{m\pi}{2N_S})(\cos(n\pi)+1)\cos(mx+ny+\frac{m\pi}{2N_S}-m\pi-\frac{n\pi}{2}) \\
&+\frac{2}{N_S}\sum_{m\notin\{N_S,2N_S,3N_S,\ldots\}\wedge m\ odd}\sum_{n\pm1}^{\pm\infty}\frac{J_n(m\pi M)}{m\pi}\frac{\cos(\frac{m\pi}{2N_S})}{\sin(\frac{m\pi}{N_S})}(\cos(n\pi)+1)\cos(mx+ny+\frac{m\pi}{2N_S}-m\pi-\frac{n\pi}{2}) \\
&-\sum_{m\in\{2N_S,4N_S,6N_S,\ldots\}}\sum_{n\pm1}^{\pm\infty}\frac{J_n(m\pi M)}{m\pi}(\cos(n\pi)+1)\sin(mx+ny+\frac{m\pi}{N_S}-m\pi-\frac{n\pi}{2})
\end{aligned}
\tag{2.33}
$$

DFS for BND2 differential output

$$F_{BND2,N} = M\cos(y) + 2(-1)^{\frac{m}{2N_S}} \sum_{m\in\{2N_S,4N_S,6N_S,\ldots\}} \sum_{n\pm1}^{\pm\infty} \frac{J_n(m\pi\frac{M}{2})}{m\pi} \sin(\frac{(m+n)\pi}{2})(1-\cos(n\pi))\cos(mx+ny+\frac{m\pi}{N_S}) \tag{2.34}$$

DFS for BND2 common mode output

$$\begin{aligned} F_{BND2,N,C} = {} & \frac{4}{N_S} \sum_{m\in\{N_S,2N_S,3N_S,\ldots\}og\ m\ odd} \frac{J_0(m\pi\frac{M}{2})}{m\pi} \sin(\frac{m\pi}{2})\sin(\frac{m\pi}{2N_S})\sin(mx+\frac{m\pi}{2N_S}) \\ & + \frac{8}{N_S} \sum_{m\in\{N_S,2N_S,3N_S,\ldots\}og\ m\ odd} \frac{J_0(m\pi\frac{M}{2})}{m\pi} \sin(\frac{m\pi}{2}) \frac{\cos(\frac{m\pi}{2N_S})}{\sin(\frac{m\pi}{N_S})} \sin(mx+\frac{m\pi}{2N_S}) \\ & + \frac{2}{N_S} \sum_{m\in\{N_S,2N_S,3N_S,\ldots\}og\ m\ odd} \sum_{n\pm1}^{\pm\infty} \frac{J_n(m\pi\frac{M}{2})}{m\pi} \sin(\frac{(m+n)\pi}{2})\sin(\frac{m\pi}{2N_S})(\cos(n\pi)+1)\sin(mx+ny+\frac{m\pi}{2N_S}) \\ & + \frac{4}{N_S} \sum_{m\in\{N_S,2N_S,3N_S,\ldots\}og\ m\ odd} \sum_{n\pm1}^{\pm\infty} \frac{J_n(m\pi\frac{M}{2})}{m\pi} \sin(\frac{(m+n)\pi}{2}) \frac{\cos(\frac{m\pi}{2N_S})}{\sin(\frac{m\pi}{N_S})} (\cos(n\pi)+1)\sin(mx+ny+\frac{m\pi}{2N_S}) \\ & + 2(-1)^{\frac{m}{2N_S}} \sum_{m\in\{2N_S,4N_S,6N_S,\ldots\}} \sum_{n\pm1}^{\pm\infty} \frac{J_n(m\pi\frac{M}{2})}{m\pi} \sin(\frac{(m+n)\pi}{2})(\cos(n\pi)+1)\cos(mx+ny+\frac{m\pi}{N_S}) \end{aligned} \tag{2.35}$$

2.6.6 Spectral characteristics for Balanced PSCPWM – Type 2

The BNS1/BND1 methods are analyzed by the HES that is generated directly from the synthesized DFS expressions. Fig. 2.33 and Fig. 2.34 show the HES plot for BNS2. It is concluded that there are components around f_c both in the differential output and the common mode. Consequently, BNS2 is inferior to all other methods. The phase interleaving over 180^0 is clearly not "sufficient" with single sided modulation. These poor spectral characteristics are general an independent of N.

The complicated DFS expressions for BND2 leads to the HES surfaces in Fig. 2.35 and Fig. 2.36. It is concluded that the differential output resembles basic double sided PSCPWM (ND), with an N-doubling of the effective sampling frequency. Since this is a general characteristic independent on N, BND2 is *superior* to BND1 in terms of the differential output although the number of carriers is halved. However, the common mode on BND2 is problematic. Independent on N there is a "lump" around f_c with full-scale amplitude.

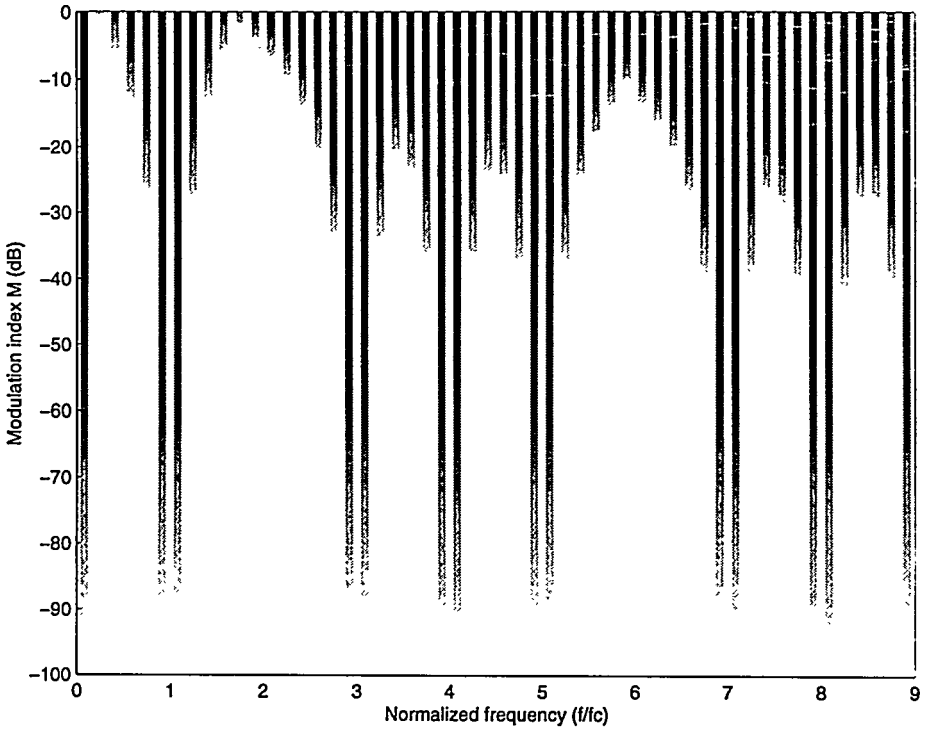


Fig. 2.33 HES-plots for BNS2 differential output with N = 4. f_r=*1/16*.

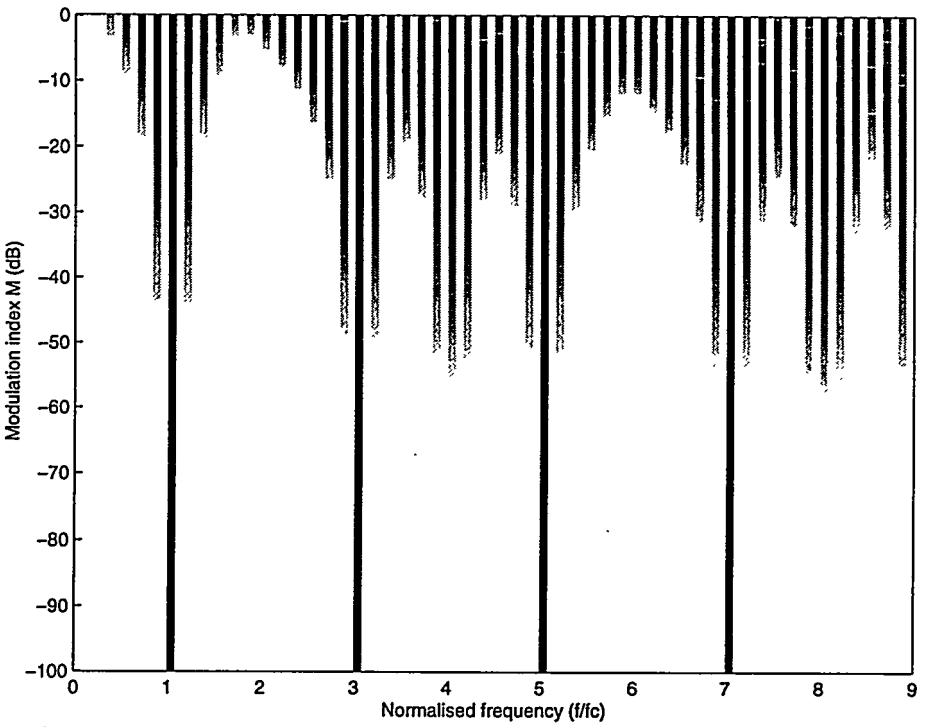


Fig. 2.34 HES-plots for BNS2 common mode output with *N = 4*. f_r=*1/16*.

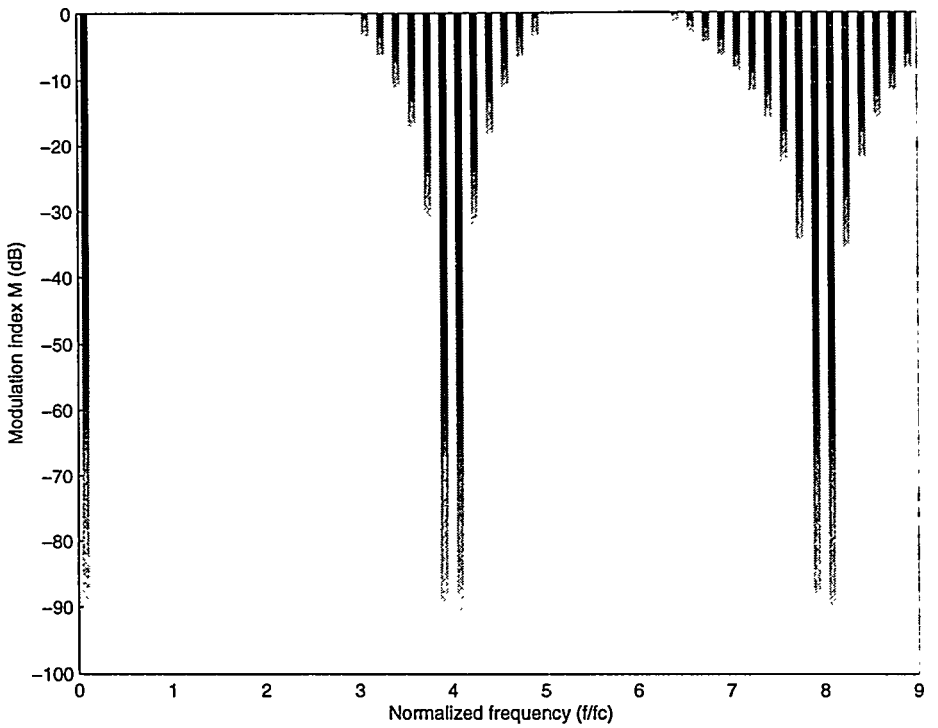


Fig. 2.35 HES-plots for BND2 differential output with N = 4. f_r=*1/16*.

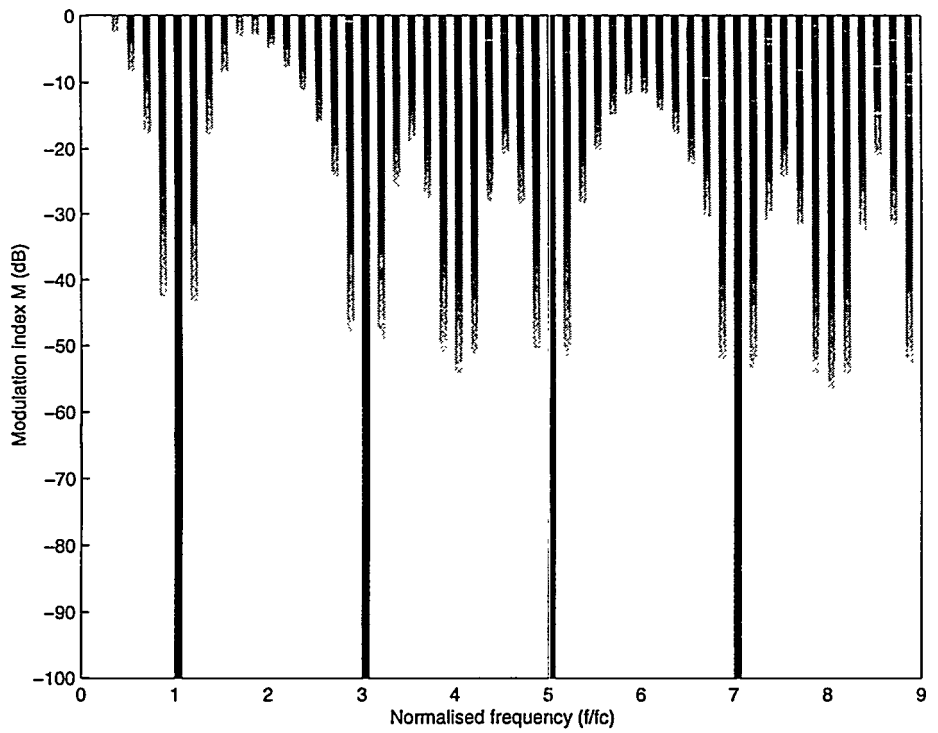


Fig. 2.36 HES-plots for BND2 common mode output with N = 4. f_r=*1/16*.

2.6.7 Balanced PSCPWM type 3 (BNS3/BND3)

The control algorithm for balanced PSCPWM type 3 was defined in (2.19), and the general time domain characteristics were shown in Fig. 2.32. The method requires half as many carriers as conventional PSCPWM. BND3/BNS3 should be seen as an alternative generalization of fundamental three-level PWM methods NBDS and NBDD, where the carriers are distributed over the complete 360° phase angle, as opposed to 180° for the Type 2 (BNS2/BND2) methods. For N=2, BNS3 is equivalent to NBDS/BNS2 and BND2 equal to NBDD/BND2. The derivations of the individual DFS expressions is significantly simpler than for type 2. Details are given in Appendix B.7 / Appendix. B.8. Only the resulting expressions are presented below.

DFS for BNS3 differential output

$$F_{BNS3,N} = M\cos(y) + \sum_{m\in\{N_S,2N_S,3N_S\ldots\}}\sum_{n\pm1}^{\pm\infty}\frac{J_n(m\pi M)}{m\pi}(\cos(m\pi)-1)\sin(mx+ny-m\pi-m\frac{n\pi}{2}) \tag{2.36}$$

DFS for BNS3 common mode output

$$F_{BNS3,N,C} = +2\sum_{m\in\{N_S,2N_S,3N_S\ldots\}}\frac{1-J_0(m\pi M)\cos(m\pi)}{m\pi}\sin(mx) - \sum_{m\in\{N_S,2N_S,3N_S\ldots\}}\sum_{n\pm1}^{\pm\infty}\frac{J_n(m\pi M)}{m\pi}(1+\cos(n\pi))\sin(mx+ny-m\pi-\frac{n\pi}{2}) \tag{2.37}$$

DFS for BND3 differential output

$$F_{BNS3,N} = M\cos(y) + 2\sum_{m\in\{N_S,2N_S,3N_S\ldots\}}\sum_{n\pm1}^{\pm\infty}\frac{J_n(\frac{m\pi M}{2})}{m\pi}\sin(\frac{(m+n)\pi}{2})(1-\cos(n\pi))\sin(mx+ny) \tag{2.38}$$

DFS for BND3 common mode output

$$F_{BNS3,N,C} = +4\sum_{m\in\{N_S,2N_S,3N_S\ldots\}}\frac{J_0(\frac{m\pi M}{2})}{m\pi}\sin(\frac{m\pi}{2})\cos(mx) + 2\sum_{m\in\{N_S,2N_S,3N_S\ldots\}}\sum_{n\pm1}^{\pm\infty}\frac{J_n(\frac{m\pi M}{2})}{m\pi}(1+\cos(n\pi))\sin(\frac{(m+n)\pi}{2})\sin(mx+ny) \tag{2.39}$$

2.6.8 Spectral characteristics for Balanced PSCPWM – Type 3

Fig. 2.37 and Fig. 2.38 shows HES-plots for BNS3 with *N=4*. The following interesting characteristics are observed for BNS3:

- The BNS3 differential output has harmonics around multiples of $N_s f_c = N/2 \cdot f_c$. The same characteristic was observed for BNS1. However, neither of the methods is as good as the fundamental single sided PSCPWM method (NS).
- BNS3 also produces a common mode output around multiples of $N_s f_c$. Note that the common mode output decreases more than proportional to the modulation index and at M=–50dB all common mode components at least 100dB below full scale.

The spectral characteristics for BND3 are illustrated by the HES plots Fig. 2.39 and Fig. 2.40 for the differential output in the cases *N=4* and *N=6*. The following is concluded:

- The BND3 differential output is dependent on $N_s = N/2$. For N_s even (Fig. 2.39) there are components around multiples of $N_s f_c$. For N_s odd (Fig. 2.40) the differential output is equivalent to the fundamental double sided PSCPWM method, *ND*.
- BND3 has *no* common mode output for N_s even. For N_s odd, the first common mode lump is around $N_s f_c$.

Again, it is interesting to observe that the output is free from common mode for N_s even. The same characteristic was observed for BND1 for N_s odd. Consequently, it is *always* possible to implement common mode free PSCPWM in the BPSC topology. The choise between the balanced control methods BND1 and BND3 will depend on N_s.

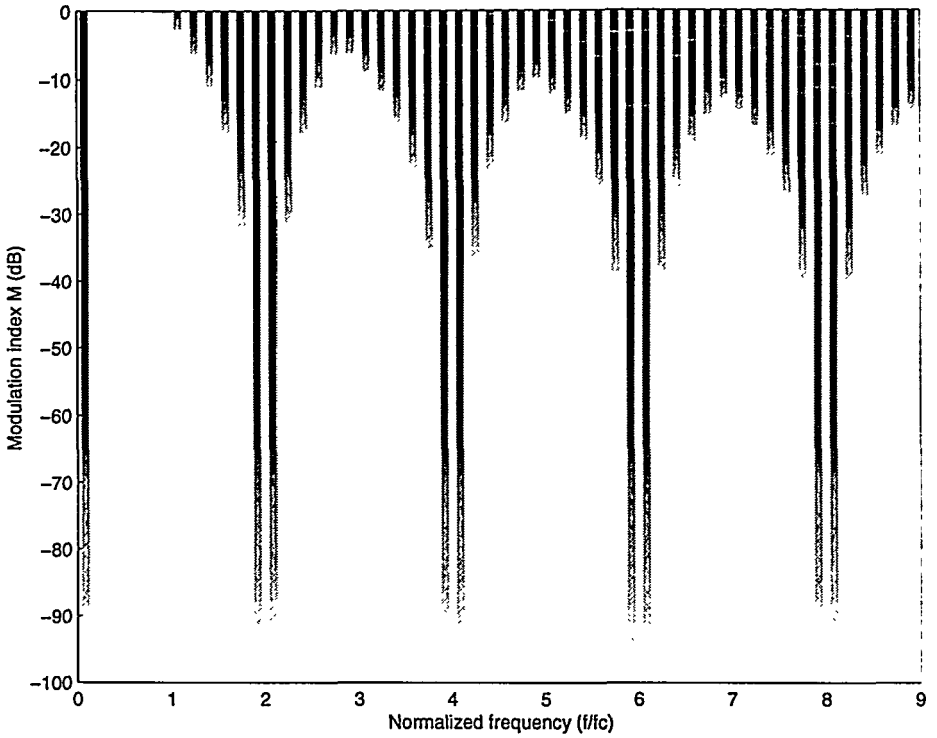


Fig. 2.37 HES-plots for BNS3 differential output with N = 4. f_r=*1/16*..

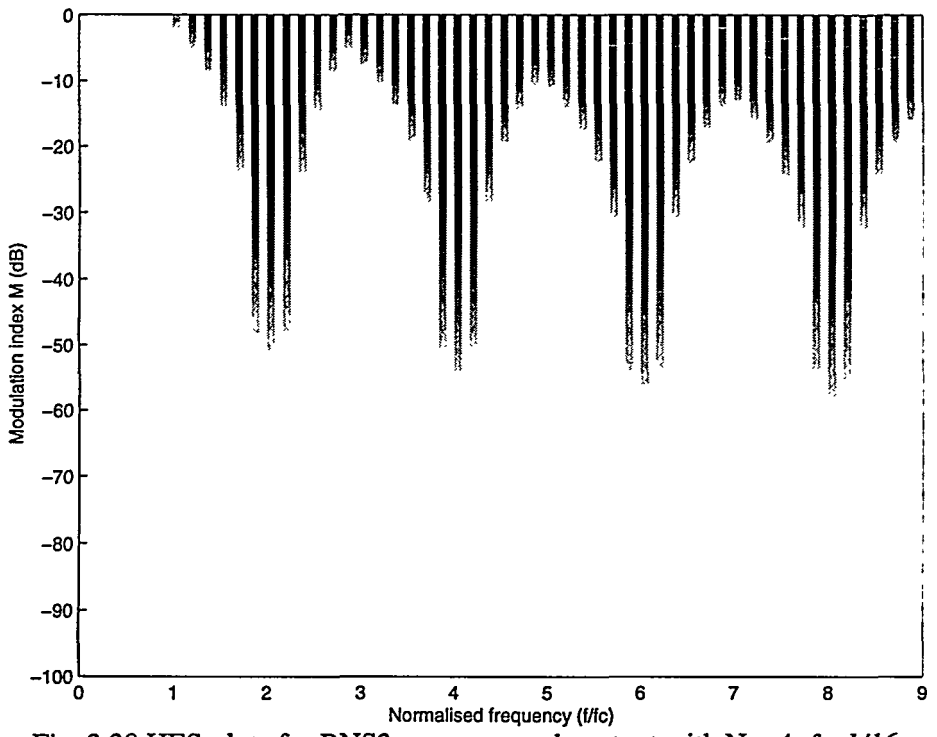


Fig. 2.38 HES-plots for BNS3 common mode output with N = 4. f_r=*1/16*.

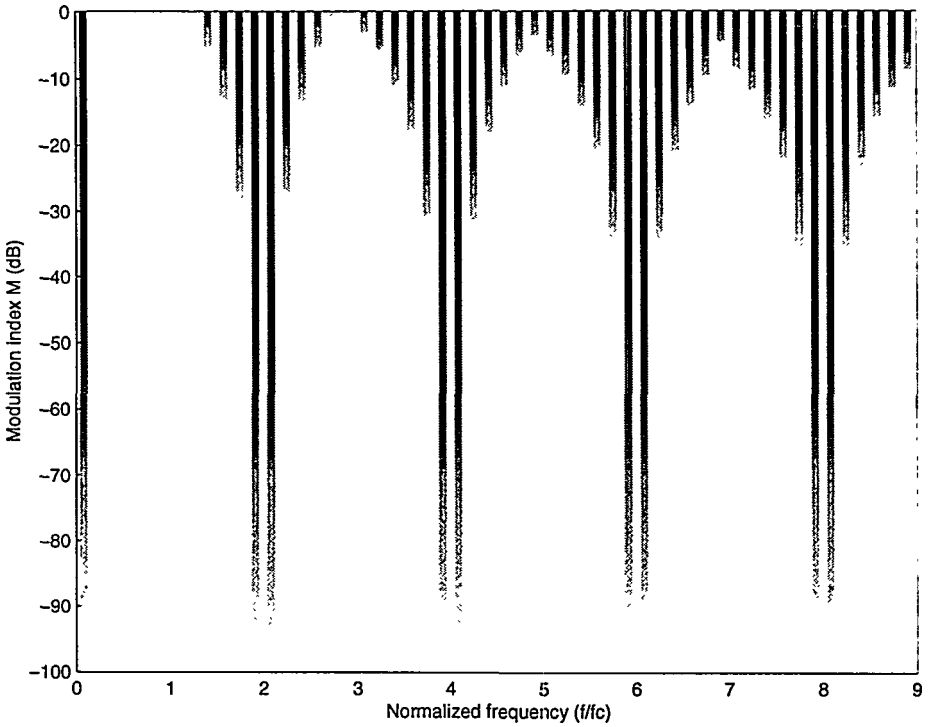


Fig. 2.39 HES-plots for BND3 differential output with N = 4. f_r=*1/16*.

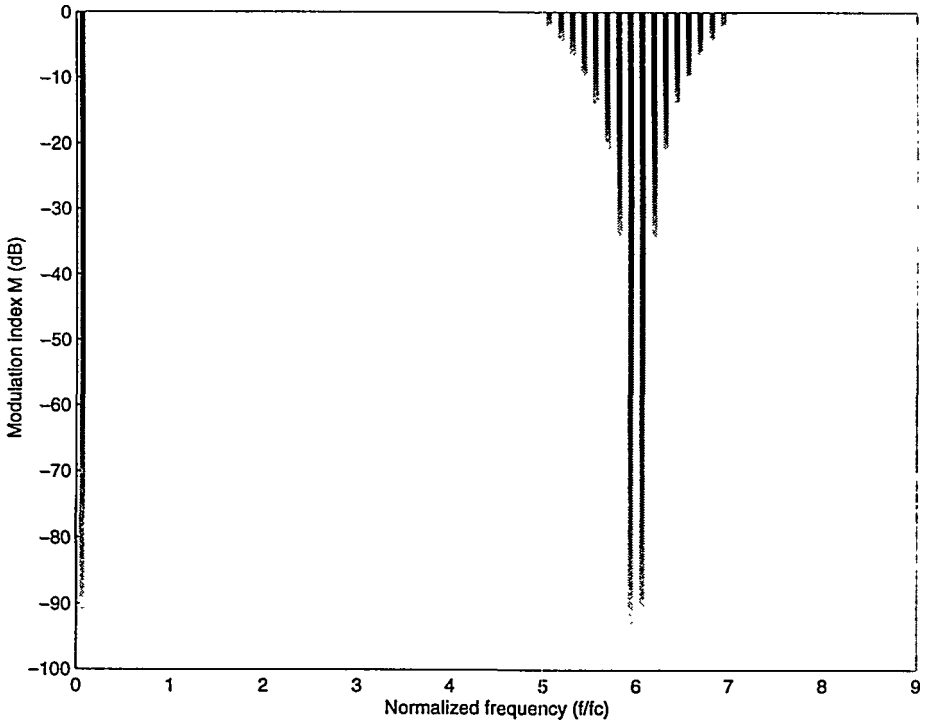


Fig. 2.40 HES-plots for BND3 differential output with *N = 6*. f_r=*1/16*.

2.7 Selection of PSCPWM method

The general characteristics of the proposed PSCPWM methods are summarized below.

	Differential		Common mode	
Method	First F_{HF} "lump"	$F_{HF}(M=0)$	First $F_{HF,C}$ "lump"	$F_{HF,C}(M=0)$
ND	Nf_c	$\approx\frac{1}{N}$ for N odd 0 for N even	---	---
NS	Nf_c	$\approx\frac{1}{N}$ for N odd 0 for N even	--.	---
BND1	Nf_c for N_s even. N_sf_c for N_s odd	0 for N_s even $\approx\frac{1}{N}$ for N_s odd	N_sf_c for N_s even --- for N_s odd	0
BNS1	N_sf_c	$\approx\frac{1}{N}$ for N_s odd 0 for N_s even	N_sf_c	0
BND2	Nf_c	0	1	≈ 1
BNS2	1	0	1	≈ 1
BND3	Nf_c for N_s odd. N_sf_c for N_s even	0	N_sf_c for N_s odd --- for N_s even	$\approx\frac{1}{N_s}$, N_s odd
BNS3	N_sf_c	0	N_sf_c	0 for N_s even $\approx\frac{1}{N_s}$, N_s odd

F_{HF} represents the HF output in the general double Fourier series. First F_{HF} "lump" indicates the first harmonic on f_c with spectral components in terms of Intermodulation (IM) components or a harmonic of the carrier. $F_{HF}(M=0)$ indicate the maximal HF-component amplitude at zero modulation.

With so many interesting methods the question arises on which method to choose for optimal power stage realization? It can in general be concluded from the investigations, that double sided modulation will be superior to single sided modulation. This excludes all single sided methods from further consideration. The choice between the remaining four methods necessitates a more detailed investigation, and will ultimately be a compromise between:

- Desired spectral characteristics (differential / common mode).
- Power supply complexity (dual supply operation or single supply operation)
- Power stage and modulator complexity.

N should be chosen as a trade-off between system complexity and spectral characteristics. Generally $N=4$ is an excellent trade-off in most applications, providing considerably improved HF spectral characteristics, lower current requirements in the individual switches at a modest increase in system complexity. It should be emphasized that the individual switches in the eight transistor BPSC power stage only handles half the current of the switches in a H-bridge.

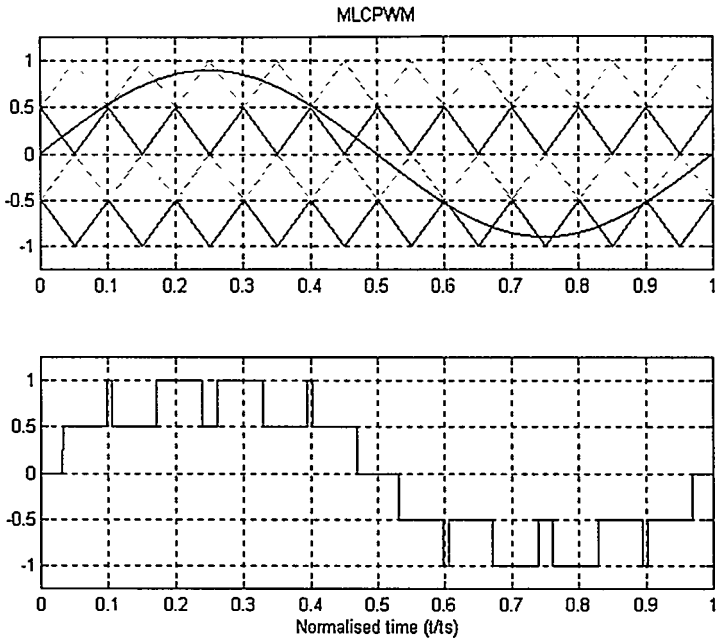


Fig. 2.41 Principle of multiple leveled Carrier PWM (MLCPWM).

Generally, the balanced power stage topology is desirable due to the single supply operation and the lower voltage requirements for the switches. However, the analysis above revealed that the optimal control algorithms (BNS, BND) for the balanced power stages do not realize the same optimal combination of characteristics as *NS* and *ND*. All double-sided balanced PSCPWM methods are investigated and compared in practice in Chapter 10.

2.8 Other Multilevel PWM methods

PSCPWM relies on an effective synthesis of a multi-level pulse waveform by superposition through summing impedance's. An alternative approach is to physically minimize the switching amplitude levels. Such direct methods are known as multi-level PWM, and have found their place in high power switching inverter systems [Ca92], [Ro95], [La96]. The foundation is generally a switching power stage with multiple power supply voltage levels and often complex control circuitry. The general drawback of such methods is the severe distortion that is introduced from diodes in the signal path. However, the methods also have certain interesting properties. In the following the most promising *physical multi-level* method, Multi-Leveled Carrier PWM (MLCPWM) is investigated in more detail to clarify the advantages and disadvantages of physical PWM methods, compared with PSCPWM.

2.8.1 Multiple Leveled Carrier PWM (MLCPWM)

The fundamental idea of MLCPWM [Ca92] is to use N carriers to achieve a N+1 level PWM signal similar to PSCPWM. The concept MLCPWM is illustrated in Fig. 2.41 with the synthesis of a five level MLCPWM signal. Four carriers are used with controlled DC offsets (successively phase shifted 180°). The carriers are compared with the modulating reference and the result is N pulse modulated signals that are added to generate the N+1 level output as show in Fig. 2.41.

MLCPWM differs from PSCPWM in terms of switching power stage realization. Fig. 2.42 shows the general power stage structure [Ca92] for direct synthesis of a physical multiple

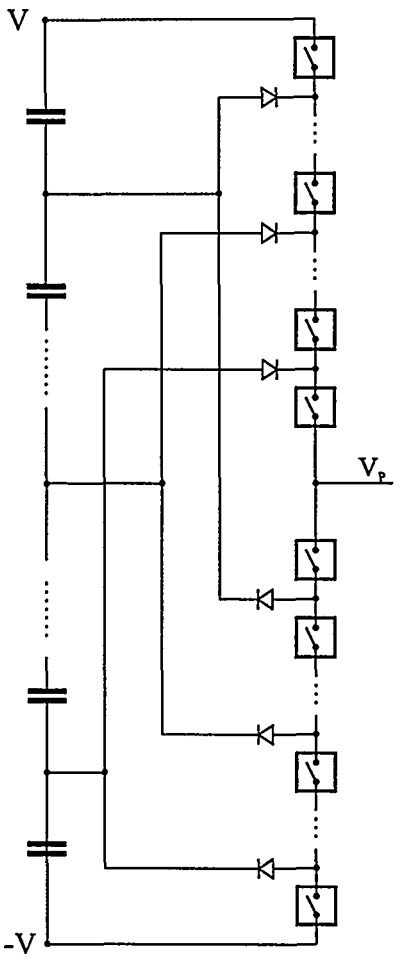


Fig. 2.42 Switching power stage for physical multi-level PWM synthesis.

level pulse waveform. The power supply is divided in *N+1* levels by separate power supplies or capacitors. The switches have to be controlled to realize the desired multi-level scheme. This control is somewhat complicated in the MLCPWM case [Ca92] and the control is dependent upon N. The interesting topologies in PMA applications are the 3-level and 4-level MLCPWM power stage topologies shown in Fig. 2.43. The topologies can be used in balanced configurations equivalent to the extension of PSC to the BPSC topology. Note, that the synthesis of a given number of levels requires the same number of transistors for both MLCPWM and PSCPWM. However, the PSC and MLC switching power stage topologies are distinctly different on a range of important parameters:

- The MLC switching power stage includes diodes in the signal path. This leads to severe distortion of the audio waveform and virtually excludes MLC from PMA implementation.
- The MLC topology does not need summing impedances to form a multi-level signal. This is an advantage of this method.
- MLCPWM requires N+1 discrete power supply levels. The power supply complexity dramatically increases with N. Recall, that PSCPWM in the balanced implementation only requires a *single* power supply level.
- Each switch in the MLC topology has to handle the full load current. The current requirements are *N* times lower in each switching leg for PSC and *N/2* times lower for the BPSC topology.
- The breakdown voltage requirements for the switches are higher for PSCPWM.
- The currents will not divide evenly in the switches, i.e. the "lower" switches will dissipate more power.

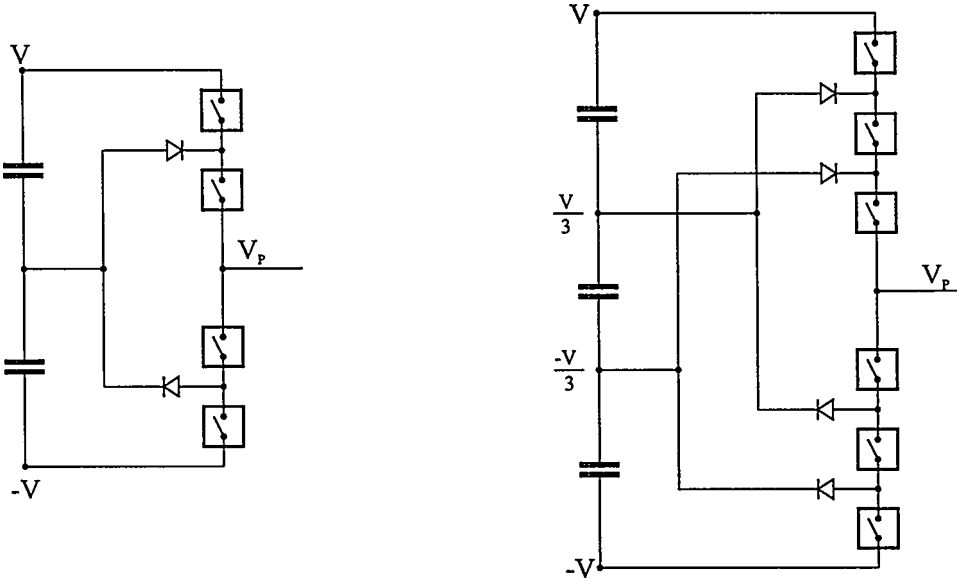


Fig. 2.43 MLCPWM power stage topologies with N=2 (left) and N=3 (right).

- Ideal MLCPWM operation requires that the voltages over the capacitors are constant. This will not be possible in practice and complex pulse amplitude distortion will be introduced.

2.8.2 MLCPWM spectral characteristics

The double Fourier series is found by superposition [Ca92]:

$$F_{MLCD,N} = M\cos(y) + 2\sum_{m=1}^{\infty}\frac{J_o\left(\frac{m(N-1)M\pi}{2}\right)}{\frac{m(N-1)\pi}{2}}\sin\left(\frac{m(N-1)\pi}{2}\right)\cos(mx) + 2\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\infty}\frac{J_n\left(\frac{m(N-1)M\pi}{2}\right)}{\frac{m(N-1)\pi}{2}}\sin\left(\frac{(m(N-1)+n)\pi}{2}\right)\cos(mx+ny) \quad (2.40)$$

Fig. 2.45 shows HES-plots for MLCPWM with $N = 3$, 4 and 8. The following is concluded on the spectral characteristics for MLCPWM:

- As for all naturally sampled schemes there are no "forward" harmonics (it is assumed that the diode forward voltage drops are zero in this idealized investigation).
- The are intermodulation components around all harmonics of the carrier.
- The amplitude of the HF component decrease linearly with N (obvious from (2.40))

Clearly, MLCPWM does not significantly improve the spectral characteristics compared with the conventional PWM methods. The only benefit of MLCPWM is the reduction in switching amplitude, but this marginal benefit comes at a very high cost. From a signal processing point of view, the proposed PSCPWM methods are without discussion superior to MLCPWM.

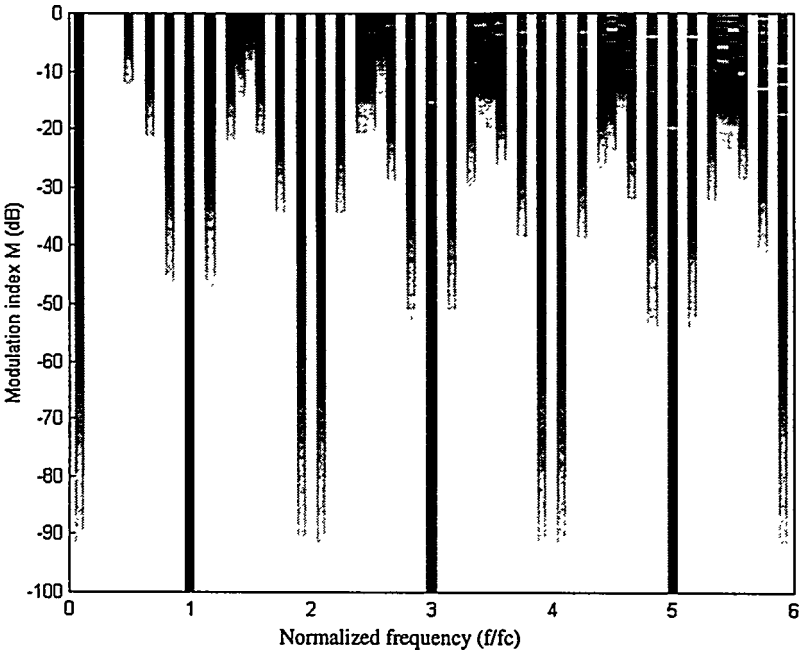


Fig. 2.44 HES-surfaces for MLCPWM for N=3.

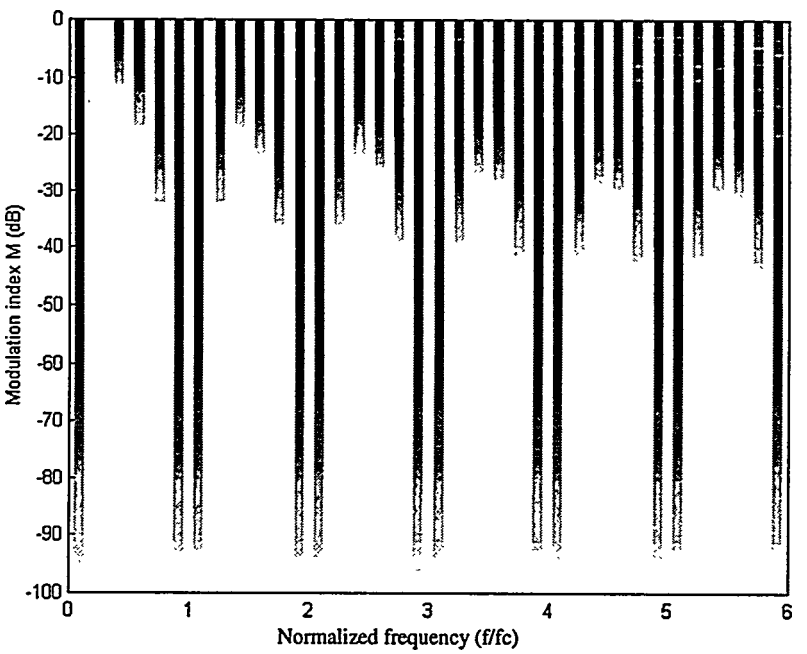


Fig. 2.45 HES-surfaces for MLCPWM for N=4.

2.9 Summary

A comprehensive investigation of analog pulse modulation methods has been carried out with the primary motivation to devise optimal modulation strategies for PMA systems. This has involved a fundamental analysis and comparison of known methods followed by investigations of new enhanced pulse modulation methods with improved characteristics.

An initial investigation of PAM, PPM, PWM and PDM concluded on the advantages of PWM. Following, the tonal behavior of the four fundamental NPWM schemes were analyzed by developing DFS expressions for the differential and common mode components of the modulated output. A visualization tool, the Harmonic Envelope Surface (HES) was introduced. The HES has been used widely throughout the investigations for spectral analysis and systematic comparison of methods. The most important conclusion of the analysis is that NPWM is totally free from harmonic distortion. In terms of modulation quality, it is possible to rank the four modulation variants form 'best' to 'worst' as NBDD, NBDS, NADD and NADS. The HF-characteristics of NBDD were shown to combine several attractive features.

The analysis was extended by the introduction of a new family of modulator and power stage structures in combination with a novel modulation principle – Phase Shifted Carrier Pulse Width Modulation (PSCPWM). As opposed to trivial paralleling similar controlled switching legs, it is possible to synthesize highly interesting multi-level modulation waveforms with a more intelligent control of the individual switching legs.

A suite of control algorithms has been defined and it has been shown that considerably improved modulator operation can be achieved. DFS expressions were derived for all methods and a detailed HES based analysis was carried out. The most important advantage of PSCPWM were proven to be a much improved synthesis of the modulating signal with:

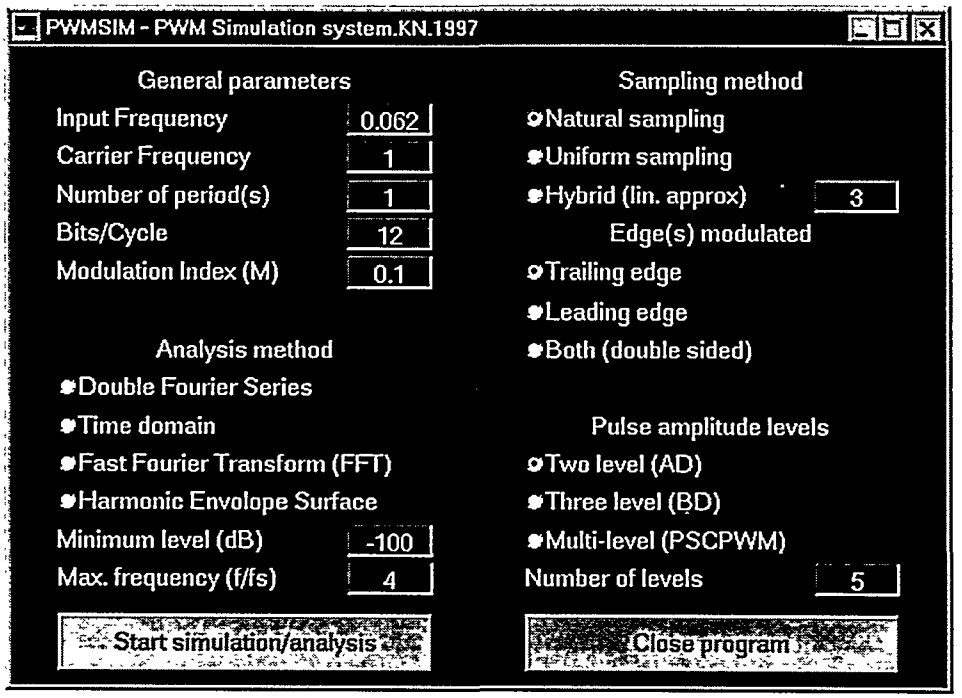
- A controllable increase in effective sampling frequency by a factor N. This can be used to reduce the switching frequency in each leg considerably.
- A reduced switching amplitude.
- A reduced current in each switching leg.

Generally, the balanced power stage topology (BPSC) is desirable due to the single supply operation and the lower voltage requirements for the switches. It was shown that by proper selection of balanced PSCPWM method, the N factor increase in sampling frequency can be realized for any N. Furthermore, several of the methods proved to have pleasant common-mode properties.

Finally, PSCPWM was compared with MLCPWM. PSCPWM was concluded to be superior on all essential parameters as HF characteristics, complexity and power stage linearity.

2.9.1 PWMSIM – GUI based toolbox for MATLAB

A GUI controlled software toolbox has been developed for MATLAB to simplify the analysis of Pulse Width Modulation methods. The GUI is shown below:



PWMSIM allow both time and frequency domain investigation of a range of PWM methods, using an analytical (DFS/HES) approach or numerical analysis.

The toolbox has been used extensively for the investigation of NPWM/UPWM/LPWM and PSCPWM methods in Chapters 2 and 3.

Part I

Chapter 3

Digital Pulse Modulation

The continuing expansion of digital techniques in the field of audio rises a question – is it possible to convert the digital encoded signals (PCM) directly to a pulse modulated signal for subsequent power amplification? The motivation is of course the topological simplification in both the digital to analog conversion stage and the subsequent power amplification stage. Intuitively, it is advantageous to keep the signal digital "as long as possible" with the accuracy and rigidity that generally follows. However, fundamental problems have persisted within digital PMAs although the field has attracted significant attention within the last decade.

The topic of this chapter is optimal digital modulator realization dedicated to digital PMAs. The known methods are reviewed to determine the optimal methods on the performance / complexity scale. Previous research is extended by a fundamental and general spectral analysis of digital pulse modulation methods. A simple digital PWM modulator design methodology is presented. The methodology can be used for systematic design of digital pulse modulators based on fundamental specifications for harmonic distortion and dynamic range.

3.1 The digital PMA paradox

Fig. 3.1 shows the basic digital PMA system. Compared to a DAC/Analog PMA system, the digital PMA offers some simplifications in that the post section of the DAC can be simplified. Furthermore, no analog pulse modulator is needed. Within the last decade, much progress on digital pulse modulation methods for digital PMA systems has been

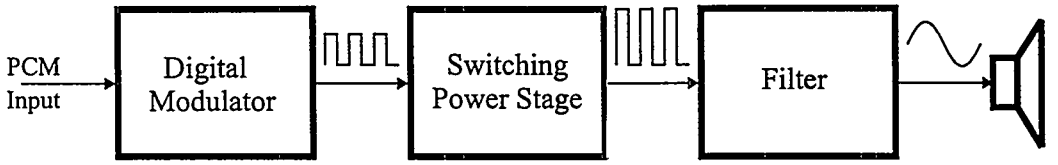


Fig. 3.1 Digital PMA topology

shown [Sa86], [Le91], [Go91], [Go91], [Sh92], [Hi94] and several methods have been developed that provide a high level of modulator performance. With the obvious topological advantages that are offered by the digital PMA, it might seem paradoxical that the topology has not already found widespread use in commercial products. The answer lies in the general misconception that the digital PMA inherently offers improved performance by keeping the signal digital and pulse modulated throughout the audio chain. The signal enters the *analog* domain at the modulator output as an analog pulse signal. Only the digital modulator is in effect *digital* with the accuracy and rigidity the follows, whereas both of the following elements are inherently analog and non-linear elements. Hence, the modulated signal is sensitive to pulse jitter and amplitude distortion. It is bound with considerable difficulty to maintain a reasonable performance level throughout the subsequent power amplification and demodulation stages. For robust power amplification, it is necessary with compensation for the distortion introduced during power amplification. The non-linear characteristic of the power stage is analyzed more closely in Chapter 4, and the important issue of optimal power conversion with inherent error correction for digital PMA systems, is the topic of Chapter 9. This chapter exclusively focuses on digital modulator realization for digital PMAs.

3.2 Digital Pulse modulation methods

The digital pulse modulator can be realized by utilizing both digital PWM and digital PDM. The properties of the two methods in digital PMA applications are discussed shortly in the following.

3.2.1 Digital PDM

Digital PDM modulators have been extensively researched as e.g. in [Na87], [Ad90], [Ha91], [Ad91], [Ri94] and found widespread use in commercial DAC's and ADC's within the last decade due to the inherent advantage of PDM on a performance/complexity scale. The digital PDM modulator topology, shown in Fig. 3.2, may be used directly as modulator in the digital PMA system in Fig. 3.1. The noise-shaping filter serves to shape the quantization noise such that the baseband performance can be maintained.

PDM has the advantage over PWM in that it can realize virtually distortion free performance over the baseband with proper selection of oversampling ratio and loop filter parameters. Another advantage is the low complexity - the modulator is realized by a linear digital filter and a quantizer. Intuitively PDM is highly "digital" by the on/off characteristic of each pulse whereas PWM codes the information into a pulse width. On the other hand, a range of problems exists with digital PDM modulators in PMA applications, although the rigidity of the digital domain allows implementation of higher order modulators. However, even with a loop filter between fourth and eighth order the resulting carrier frequency will be high. Thus, for a fourth order filter the resulting sampling frequency is 2.82MHz for reasonable audio performance [Kl97]. This leads to an average pulse switching frequency which is dependent on the audio signal but will have an average switching frequency about

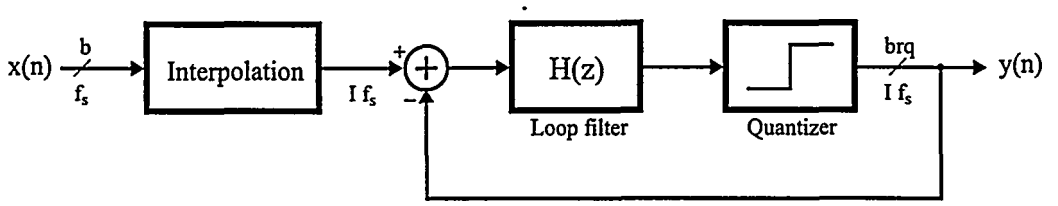


Fig. 3.2 General digital PDM modulator topology

800KHz-1MHz. Reasonable compromises between filter order and oversampling ration are 64x oversampling / fourth order filter [Kl97] or 32x oversampling / eighth order filter [Sm94]. A side-effect of higher order modulators is the limits the modulation depth which becomes a problem in PMA applications, since this increases the power supply rail voltage for a given output power. A higher power supply voltage will compromise both performance and efficiency.

There has been some activity in recent years to solve the problem of a high idling pulse activity in PDM modulators for digital PMAs. An interesting approach is presented in [Ma95] where the individual output bits of the modulator are inverted in a controlled fashion in order to minimize the resulting pulse frequency (especially at idle). By applying the pulse inversion within the loop, the distortion arising from such a modification is controlled. Some improvements over conventional PDM have been shown in [Ma95] using a higher order loop filter (7. order). However, the improvements come with an considerable increase in implementation complexity and stability issues constrains the modulation depth to below 0.5 which is very problematic with a switching power output stage. A familiar system is presented in [Ma96] where a lower carrier frequency is obtained by grouping together output pulses, which is modeled as a linear filtering, decimation and pulse width modulation process. The method attempts to emulate PWM. However, the properties and inherent limitations remain the same. To conclude on PDM, no method has yet been presented that can match previously presented results on digital pulse width modulation. Consequently, PDM and its variants will notbe considered further.

3.2.2 Digital PWM

The practical conversion of a digital PCM signal to a uniformly sampled pulse width modulated signal is remarkable simple. Fig. 3.3 shows an example system that converts the b bit represented input to a UPWM signal at the carrier rate f_c equal to the sample rate f_s of the PCM signal. The digital modulator uses a high frequency b bit counter to define the timing edges. It is essential, that the conversion from PCM to UPWM is realized without loss of information. Hence, the precision of the bit clock is critical for maintaining system performance and good long-term stability and phase noise and other elements causing jitter

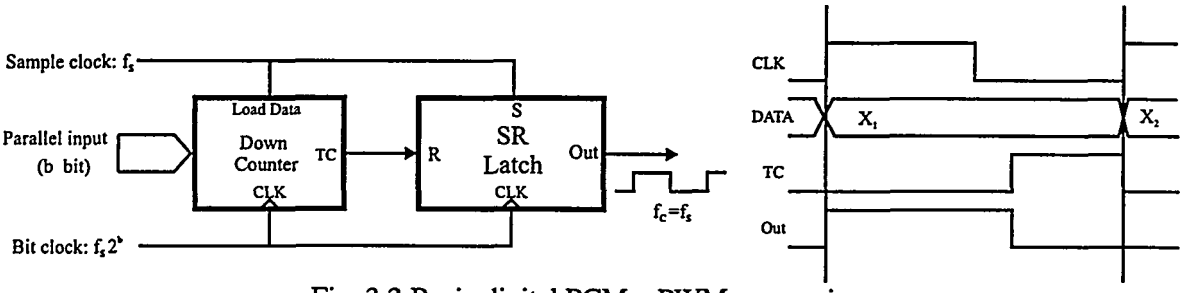


Fig. 3.3 Basic digital PCM – PWM conversion.

Sampling method	Edge	Levels	Abbreviation
Uniform sampling (UPWM)	Single sided	Two (AD)	UADS
		Three (BD)	UBDS
	Double sided	Two (AD)	UADD
		Three (BD)	UBDD

Table 3.1 Fundamental uniformly sampled PWM (UPWM) methods.

have to be controlled. The requirement for counting speed is a fundamental limitation in digital PWM systems. Since audio systems operate with 16-24 bits and sampling frequencies of at least 44.1KHz, the necessary counter speed in this direct implementation is orders of magnitude higher than what can be realized in hardware. Even with innovative circuit design to reduce the effective counter speed [Ng85], a direct implementation is not practical without certain extensions. A more fundamental problem however is the non-linearity within PCM-PWM conversion. The direct mapping of incoming digital PCM samples to a pulse width is a uniform sampling process (UPWM) that has significantly different characteristics than NPWM. Solutions to both the practical problems and inherent linearity problems within UPWM are the essential topics of the present chapter.

3.3 UPWM analysis

The topic of the following is a fundamental tonal analysis of uniformly sampled PWM. The analysis is an extension of the results that was presented on UPWM in [Ni97a]. Just as for NPWM, there are four fundamental variants of uniformly sampled PWM defined in Table. 3.1. The methods are illustrated in the time domain in Fig. 3.4 - Fig. 3.7. For coherence with the analysis methodology in chapter 2, the four variants of UPWM will be investigated in the following. The derivation of the DFS expressions is shown in detail in Appendix B.10. Only the resulting DFS expressions are given below

DFS for UADS differential output

$$\begin{aligned} F_{UADS}(t) = &-\sum_{n=1}^{\infty} \frac{J_n(n\pi Mq)}{n\pi q} \sin\left(ny - n\pi q - \frac{n\pi}{2}\right) \\ &+ \sum_{m=1}^{\infty} \frac{1 - J_0(m\pi M)\cos(m\pi)}{m\pi} \\ &- \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm\infty} \frac{J_n((nq+m)\pi M)}{(nq+m)\pi} \sin(ny + mx - \frac{n\pi}{2}) \end{aligned} \tag{3.1}$$

DFS for UBDS differential output

$$\begin{aligned} F_{UBDS}(t) = &\sum_{n=1}^{\infty} \frac{J_n(n\pi Mq)}{n\pi q} \cos(ny - n\pi q) \sin(\frac{n\pi}{2}) \\ &+ \sum_{m=1}^{\infty} \sum_{n=\pm 1}^{\pm\infty} \frac{J_n((nq+m)\pi M)}{(nq+m)\pi} \cos(ny + mx) \sin(\frac{n\pi}{2}) \end{aligned} \tag{3.2}$$

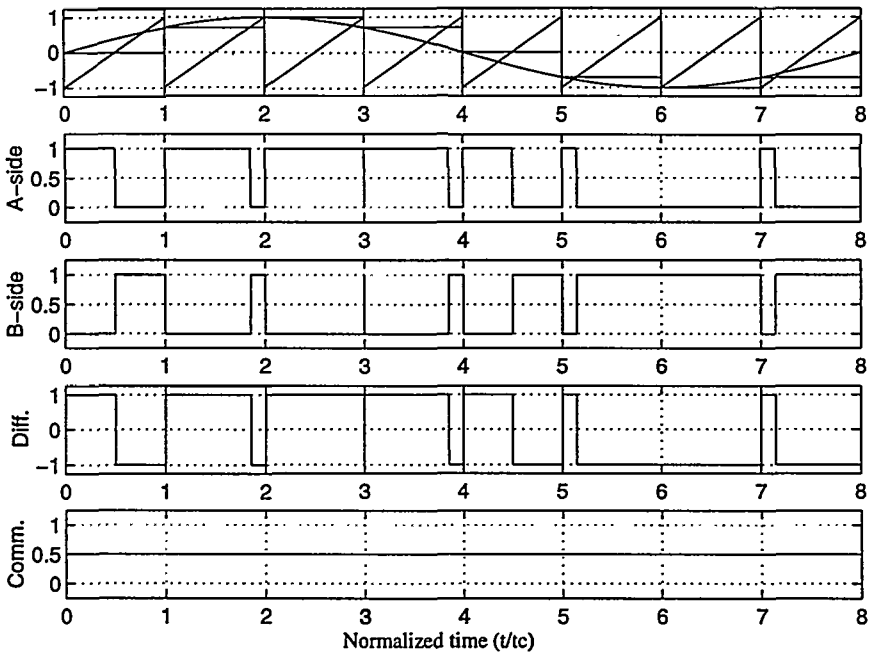


Fig. 3.4 Time domain characteristics for UADS. $f_r = \frac{1}{8}$.

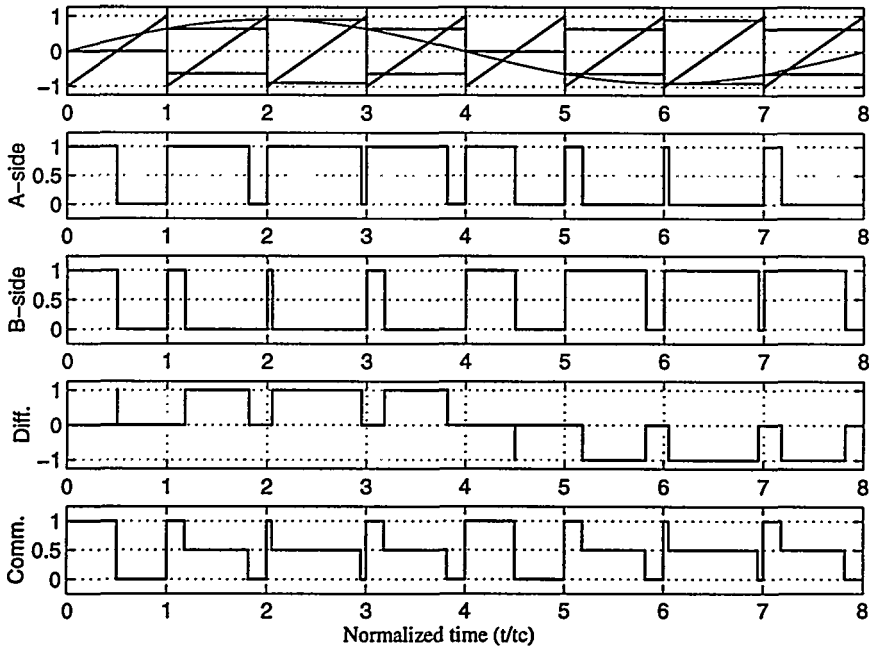


Fig. 3.5 Time domain characteristics for UBDS. $f_r = \frac{1}{8}$.

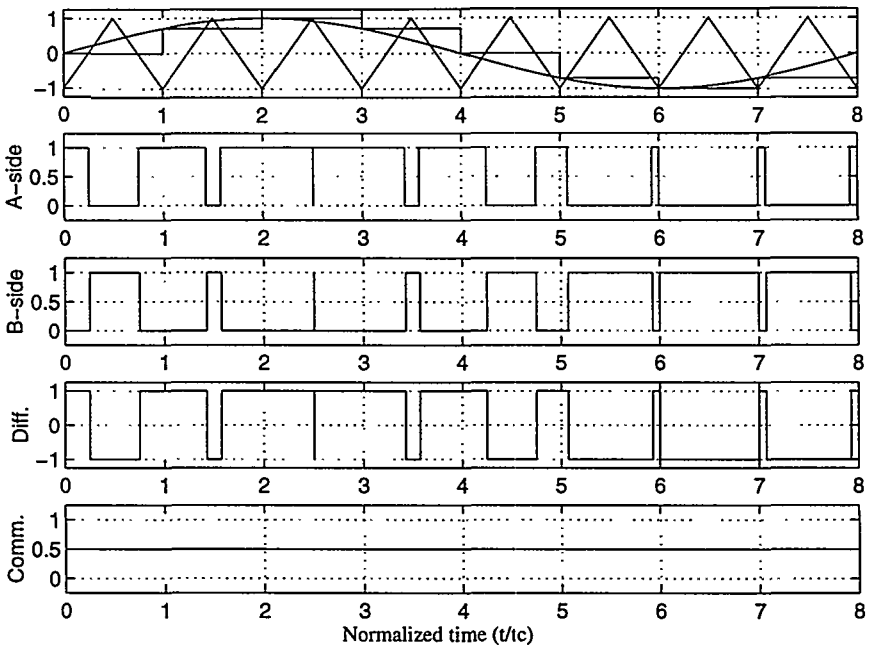


Fig. 3.6 Time domain characteristics for UADD. $f_r = \frac{1}{8}$.

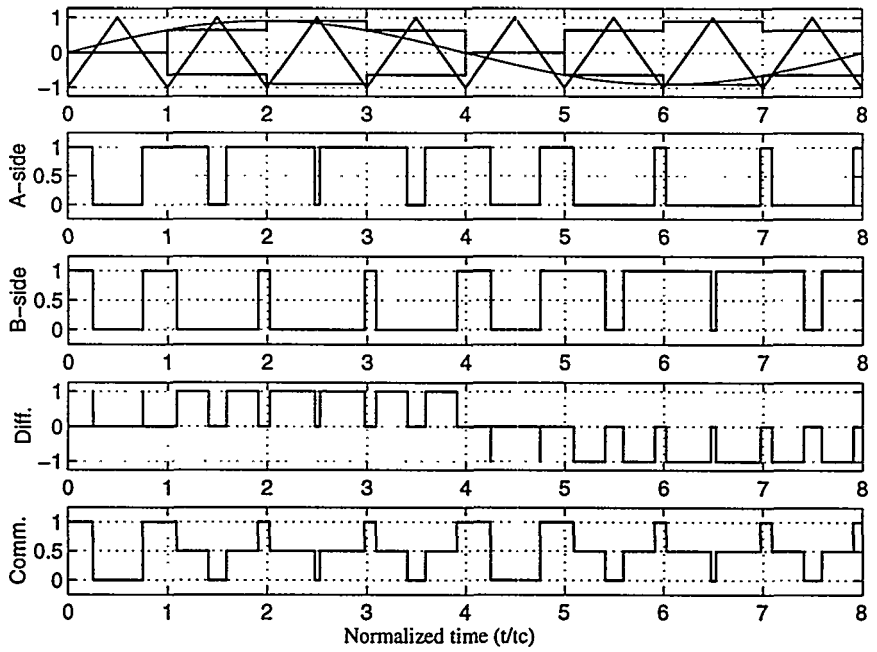


Fig. 3.7 Time domain characteristics for UBDD. $f_r = \frac{1}{8}$.

DFS for UADD differential output

$$
\begin{aligned}
F_{UADD}(t) = &\sum_{n=1}^{\infty} \frac{J_n\left(n\pi\frac{M}{2}q\right)}{n\pi q}\sin\left((q+1)\frac{n\pi}{2}\right)\cos(ny) \\
&+\sum_{m=1}^{\infty}\frac{J_0\left(m\pi\frac{M}{2}\right)}{m\pi}\cos\left(\frac{m\pi}{2}\right)\cos(mx) \\
&+\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{J_n\left((nq+m)\frac{\pi M}{2}\right)}{(nq+m)\pi}\sin\left((m+n(1+q))\frac{\pi}{2}\right)\cos(ny+mx)
\end{aligned}
\tag{3.3}
$$

DFS for UBDD differential output

$$
\begin{aligned}
F_{UBDD}(t) = &-4\sum_{n=1}^{\infty}\frac{J_n\left(n\pi q\frac{M}{2}\right)}{n\pi q}\sin((q+1)\frac{n\pi}{2})\sin(\frac{n\pi}{2})\sin\left(ny-\frac{n\pi}{2}\right) \\
&-4\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{J_n\left((nq+m)\frac{\pi M}{2}\right)}{(nq+m)\pi}\sin\left((m+n(1+q))\frac{\pi}{2}\right)\sin(\frac{n\pi}{2})\sin\left(ny+mx-\frac{n\pi}{2}\right)
\end{aligned}
\tag{3.4}
$$

3.3.1 UPWM harmonic distortion

All components within the pulse-modulated output are summarized in Table 3.2. Compared to NPWM, uniformly sampling results in both *phase and amplitude distortion of the fundamental.* Furthermore, the output contains harmonics of the input leading to a finite total harmonic distortion. A parametric analysis has been performed on these important distortion characteristics of UPWM. Fig. 3.8- Fig. 3.11 shows THD calculated as an RMS sum of the first five harmonics vs. M and $dBf_r = 20\log(f_r)$. The parameter space is chosen to represent worst-case conditions with maximal modulation and high frequencies. For all methods, THD is extremely dependent on frequency and modulation index. In the worst-case situation, none of the methods are sufficiently linear to honor the general linearity demands as e.g. THD < -80dB. For M < –20dB, all methods are sufficiently linear within the desired frequency range i.e. the linearity problems are exclusively present at high modulation index.

Method	n'th harmonic of signal	m'th harmonic of carrier frequency	IM-component $mx \pm ny$
UADS	$\frac{J_n(n\pi Mq)}{n\pi q}$	$\frac{1-J_0(m\pi M)\cos(m\pi)}{m\pi}$	$\frac{J_n((nq+m)\pi M)}{(nq+m)\pi}$
UBDS	$\frac{J_n(n\pi Mq)}{n\pi q}\sin(\frac{n\pi}{2})$		$\frac{J_n((nq+m)\pi M)}{(nq+m)\pi}\sin(\frac{n\pi}{2})$
UADD	$\frac{J_n\left(n\pi\frac{M}{2}q\right)}{n\pi q}\sin\left((q+1)\frac{n\pi}{2}\right)$	$\frac{J_0\left(m\pi\frac{M}{2}\right)}{m\pi}\cos\left(\frac{m\pi}{2}\right)$	$\frac{J_n\left((nq+m)\frac{\pi M}{2}\right)}{(nq+m)\pi}\sin\left((m+n(1+q))\frac{\pi}{2}\right)$
UBDD	$\frac{J_n\left(n\pi\frac{M}{2}q\right)}{n\pi q}\sin\left((q+1)\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{2}\right)$		$\frac{J_n\left((nq+m)\frac{\pi M}{2}\right)}{(nq+m)\pi}\sin\left((m+n(1+q))\frac{\pi}{2}\right)\sin\left(n\frac{\pi}{2}\right)$

Table 3.2 Summary of the components that constitute the UPWM DFS expressions.

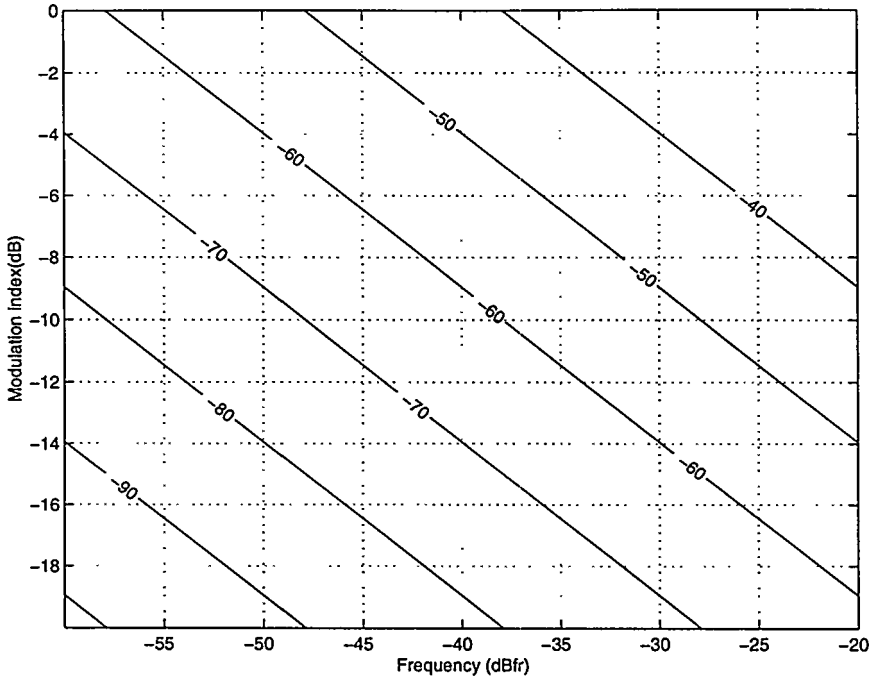


Fig. 3.8 Contour plot of THD vs. modulation index and frequency ratio dBf_r for UADS. Level curves of constant THD draw a straight line in the (M,fr)- parameter space.

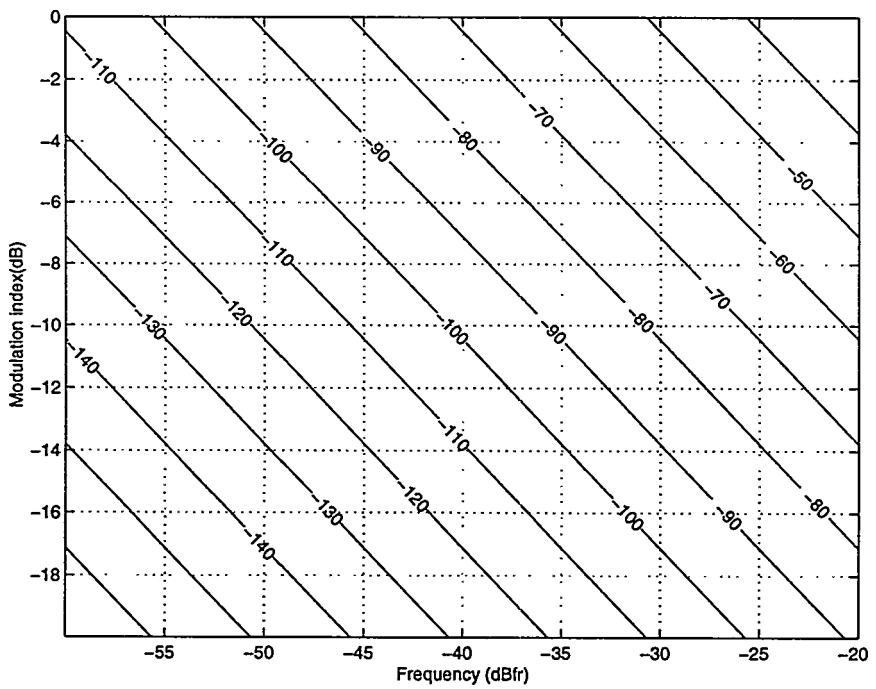


Fig. 3.9 Contour plot of THD vs. modulation index and frequency ratio dBf_r for UBDS.

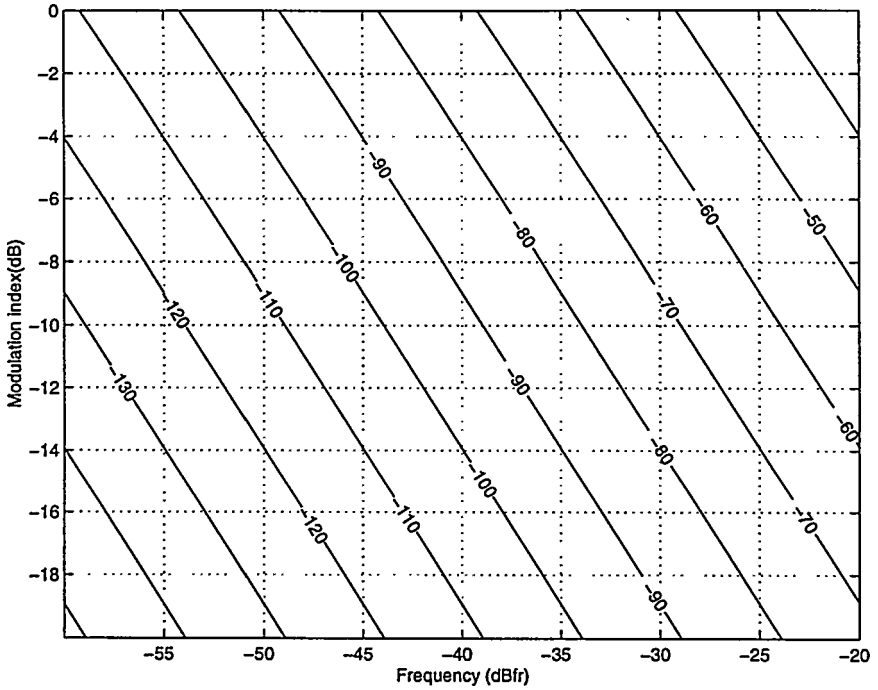


Fig. 3.10 Contour plot of THD vs. modulation index and frequency ratio dBf_r for UADD.

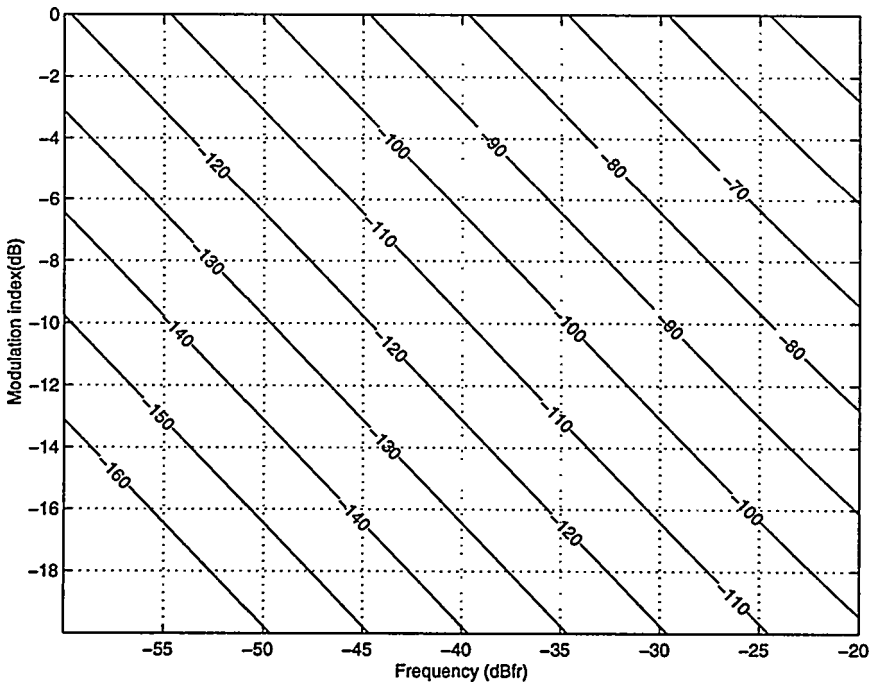


Fig. 3.11 Contour plot of THD vs. modulation index and frequency ratio dBf_r for UBDD.

The distortion characteristics of UPWM differ significantly between methods. The maximal frequency ratios corresponding for below –60dB and –80dB THD are:

	UADS	UBDS	UADD	UBDD
$f_{r,\max}$ (THD<-60dB)	-57 dBf_r	-36 dBf_r	-34 dBf_r	-29 dBf_r
$f_{r,\max}$ (THD<-80dB)	-78 dBf_r	-46 dBf_r	-44 dBf_r	-39 dBf_r

Such constraints on f_r will generally exclude UPWM from digital PMA applications where high linearity is desired. It is desirable with a much higher $f_{r,\max}$, such that the natural limitation will be the HF-characteristics as for NPWM. Only UBDD is close to honor these demands, given that up to –60dB THD can be accepted.

3.3.2 UPWM HF characteristics

Fig. 3.12 - Fig. 3.15 show the HES-plots for the four UPWM methods based on the derived DFS expressions. Comparing HES-plots for NADS and UADS it is obvious that the IM-components for uniform sampling are *lower* than for natural sampling. However, the differences are insignificant compared with the differences that were analyzed above. Other important factors to note regarding the HF spectral characteristics are:

- At lower modulation indices, the HES converges towards the natural sampling case.
- UBDD has a significant amount of components around the first harmonic of the carrier, meaning that the sampling frequency is not effectively doubled.

Except for UBDD, there are no significant differences between the HF characteristics for natural sampling methods and uniform samplings methods. The major differences lie in the distortion characteristics, which is a severe obstacle for UPWM. Note that the distortion components are also visible in the HES plots at higher modulation indices where the fundamental is smeared by harmonic components.

3.3.3 Uniformly sampled PSCPWM

It is trivial to generalize PSCPWM from natural sampling to the uniform sampling case and the generalized uniform sampling methods are defined in Table 3.3. However, the linearity problems will remain the same since PSCPWM is based on superposition of a set of individual non-linear modulator output. In addition, the multi-level effect will diminish. This has already been illustrated for UBDD that correspond to BUD2 and BUD3 with N=2. Further increasing the number of switching legs will only further worsen the harmonic cancellation.

Configuration	Edge	Abbreviation
Non-balanced	Single sided	US
	Double sided	UD
Balanced (Type 1,2 and 3)	Single sided	BUS1, BUS2, BUS3
	Double sided	BUD1, BUD2, BUD3

Table 3.3 Generalized uniformly sampled PWM. (Uniform PSCPWM).

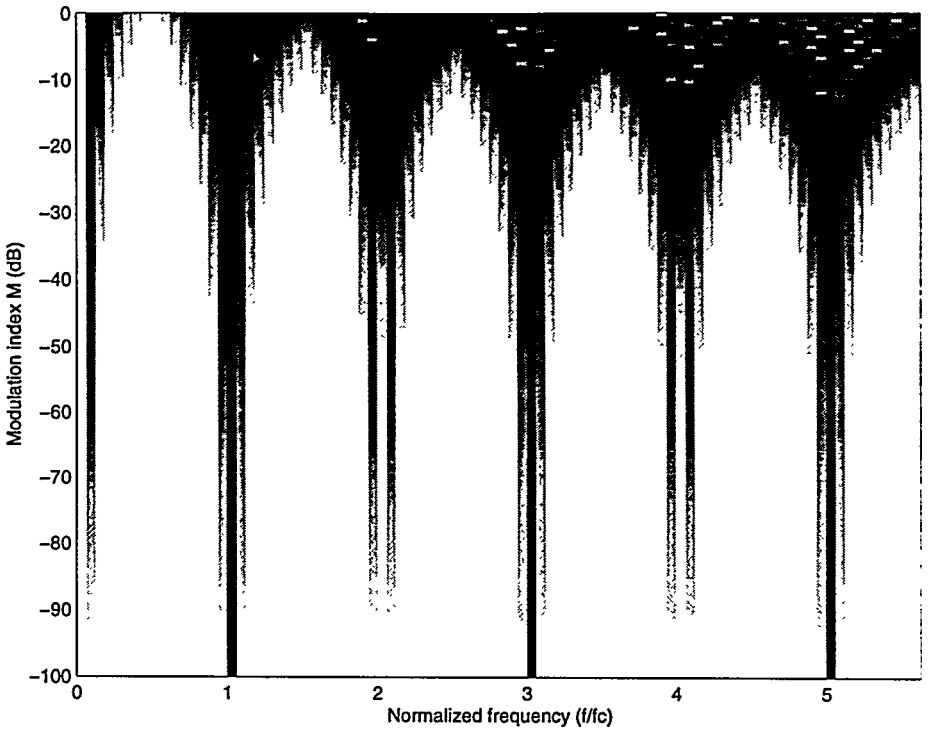


Fig. 3.12 HES-plot for UADS. $f_r = \frac{1}{16}$

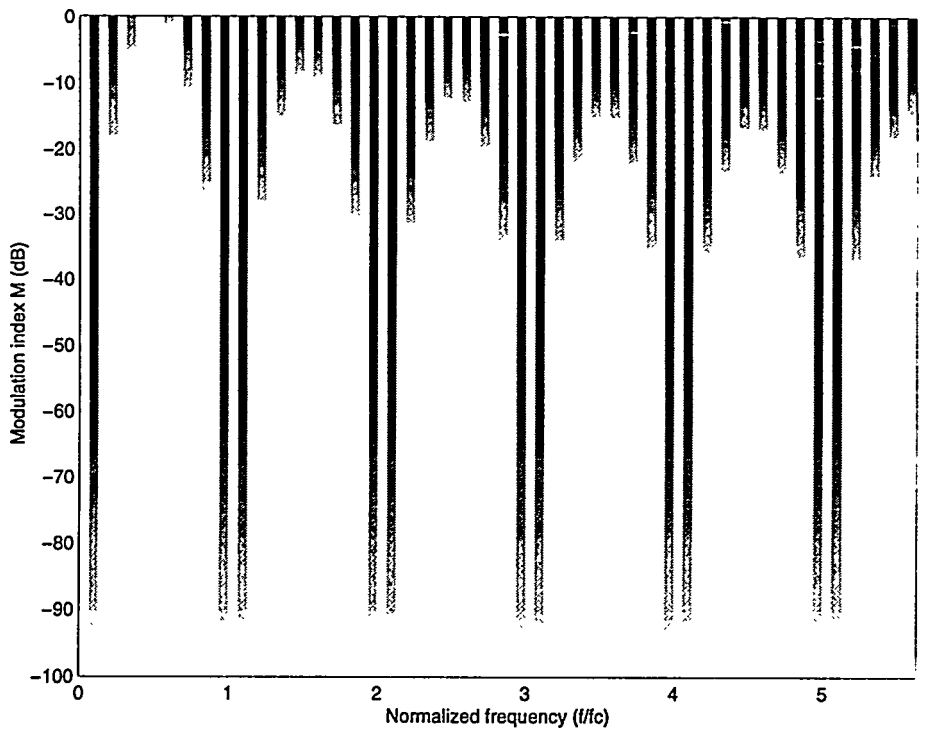


Fig. 3.13 HES-plot for UBDS. $f_r = \frac{1}{16}$.

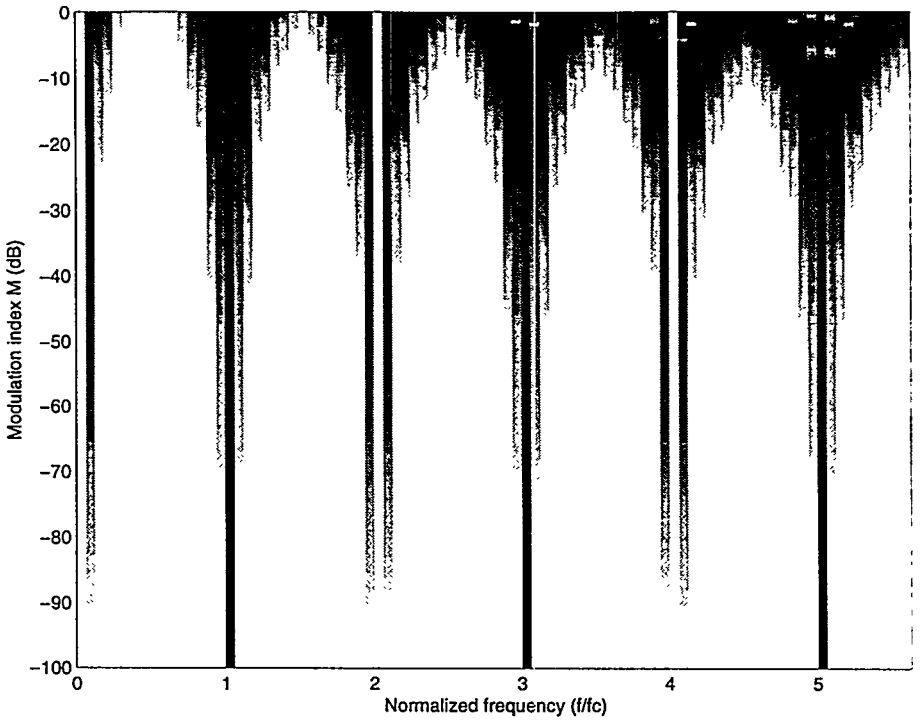


Fig. 3.14 HES-plot for UADD. $f_r = \frac{1}{16}$.

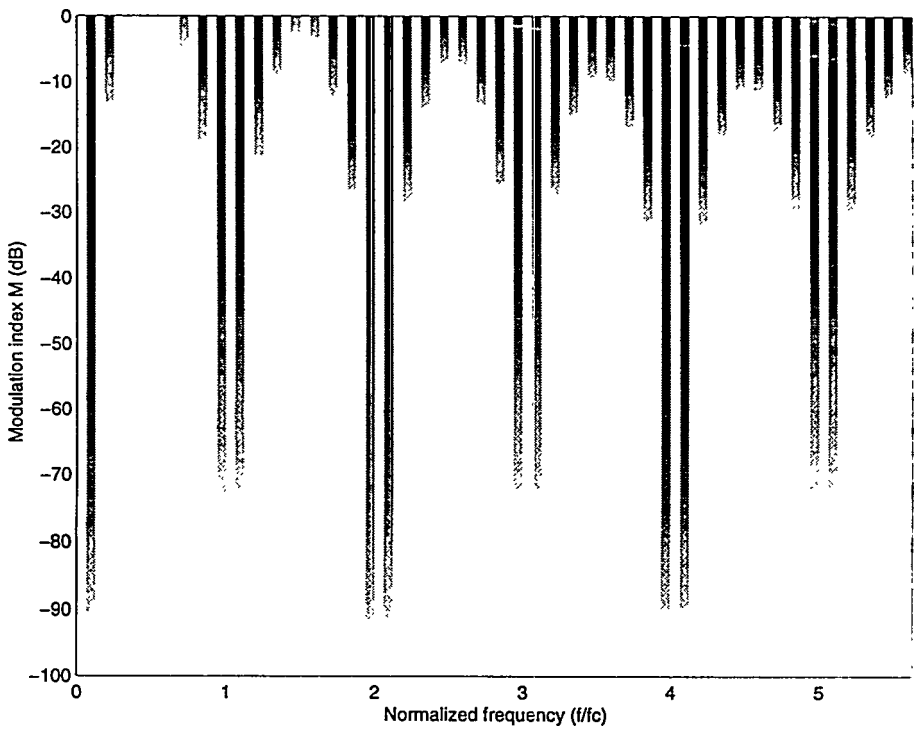


Fig. 3.15 HES-plot for UBDD. $f_r = \frac{1}{16}$.

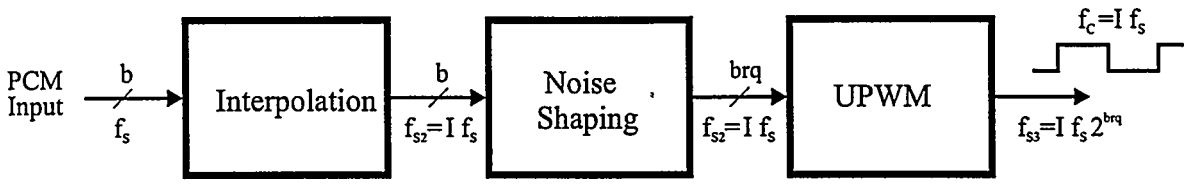


Fig. 3.16 Practical digital PCM – PWM conversion using interpolation and noise shaping.

3.4 Enhanced digital PWM methods

The inherent problems within practical PCM-UPWM conversion, has received much attention within the last decade. In the following, these methods will be reviewed shortly and a method is selected for further investigations.

3.4.1 Interpolation and noise shaping (INS) topology

Further digital signal processing in terms of interpolation and noise shaping [Go90] preceding the actual PCM-UPWM conversion stage can provide certain improvements to the digital PMA system. The topology is shown in Fig. 3.16. The interpolation has several effects:

- The interpolation improves the linearity of the conversion process by providing a considerably carrier frequency to bandwidth ratio.
- The effective oversampling of the signal opens for effective noise shaping to reduce the pulse width resolution while maintaining baseband performance.
- The increase in carrier frequency f_c by interpolation will lower the efficiency. On the other hand, demodulation will become simpler.

The interpolation factor is a compromise between modulator linearity, dynamic range and factors relating to the power conversion as efficiency and power stage linearity. Since errors in the power stage are introduced on each switching action, the carrier frequency should be minimized. Interpolation factors are much lower than e.g. in sigma-delta modulators where interpolation factors of 64x-256x are typical. For a 20KHz bandwidth digital PMA the carrier frequency should not exceed 500KHz to satisfy the requirements for efficiency and power stage performance. This corresponds to interpolation factors generally below 16x.

Noise shaping is extraordinary useful in this application, since the critical requirement for time resolution can be reduced by orders of magnitude by remarkably simple means. Previous research has shown [Go90] that re-quantization to 6-9 bits combined with 8-16 times interpolation make a reasonable compromise that enables baseband quality to be maintained with a simple noise shaper. Consequently, the well documented stability problems in noise shaping systems as e.g. sigma delta modulators [Ch90], [Ad91], [Ri94] are notably simplified in these fine re-quantizing systems.

3.4.2 Improving modulator linearity

Whereas the simple topology of Fig. 3.16 provides a realizable system with sufficient dynamic range, the constraints on interpolation factor will generally lead to linearity problems within the worst case parameter space, i.e. at high frequencies and high modulation indices. This was documented above for all four UPWM schemes. Accordingly, methods to improve UPWM linearity are desirable. The list of previous

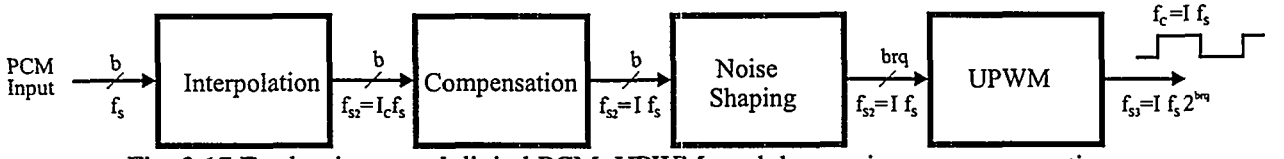


Fig. 3.17 Further improved digital PCM–UPWM modulator using precompensation.

publications that address this problem is extensive, e.g. [Le91], [Go91], [Go92], [Sh92], [Cr93], [Ha92], [Ha94], [An94], [Hi94] and [Ri97]. The methods fall into three categories, each realizing the objectives with different degrees of success:

- Precompensation based methods, where the compensation methods may be time-invariant or time-variant.
- Closed loop methods, where it is attempted to reduce the non-linearity by a feedback loop around the modulator, or alternatively both the modulator and power stage in the complete digital PWM amplifier.
- Methods using output emulation where the UPWM output is predicted or emulated such that a digital feedback loop can be applied to correct for it before the UPWM process.

3.4.3 Precompensation methods

The linearization of UPWM by precompensation is the most widely used approach in previous years. The methods can be sub-divided into three categories:

- Enhanced sampling methods as Pseudo Natural Pulse Width Modulation (PNPWM) [Go92] or Linearized Pulse Width Modulation (LPWM) [Sh92]. The general characteristic of these methods is that they attempt to emulate NPWM best possible. The motivation of course is the perfect linearity of NPWM in terms of pure harmonic distortion.
- Dynamic precompensation using time variant filters [Ha92].
- Non-linear precompensation using non-linear digital filters [Ri97].

More of these techniques have proved very successful in linearizing PWM. The first approach can be considered a hybrid-sampling scheme. The first paper to address hybrid sampling was published back in 1967 by Mananov [Ma67] who called it modulation of the third kind. Several alternative hybrid sampling schemes been presented in recent years with PWM D/A-converters and digital PMAs as specific application. The basic idea is the same - by sampling 'in between' the natural and uniform case, the harmonic distortion can be reduced, especially if the sampling approaches natural sampling. The use of such alternative sampling methods in PWM modulators were first introduced in [Le90] followed by various extensions in e.g. [Me91], [Go91], [Sa91], [Me92], [Sh92].

The general topology for these methods is shown in Fig. 3.17. The placement of the precompensation or predistortion unit deserves a comment. In theory, the predistortion might be performed directly at the input of the system or alternatively directly before the source of non-linearity, i.e. at the noise shaper output preceding the UPWM. Intuitively, the best place is directly before UPWM unit. However, the precompensation will not operate on coarse quantized data without increasing the wordlength. Accordingly, placement before the noise shaper is more appropriate. The precompensation in PNPWM [Go92] is based on polynomial interpolation combined with root-finding to approximate natural sampling. Least Squares (LS) can be used for the curve fitting, and the Newton

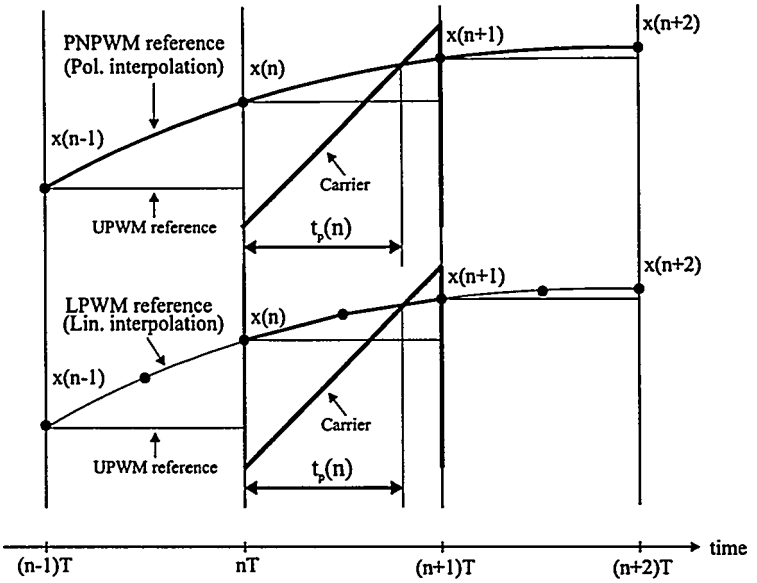


Fig. 3.18 Enhanced sampling methods

Raphson algorithm can be used to determine the crossing point. The results presented on PNPWM in previous work has been very good in terms of modulator performance, i.e. the distortion can be made arbitrarily good. However, the performance improvements come at a high computational cost. Shajaan introduces a familiar algorithm defined as LPWM [Sh92]. As opposed to PNPWM the system is based on further interpolation of the digital signal, followed by simple linear interpolation. The fundamental study of LPWM in [Sh92] showed promising performance and equally important – the method practical in terms of implementation. The two enhanced sampling methods are compared in Fig. 3.18.

LPWM analysis

The LPWM algorithm will be investigated more closely in the following. From Fig. 3.18, it is obvious how the LPWM reference, by the linear interpolation, is much closer to the NPWM (natural) reference. A new parameter is the number of samples S used in each carrier cycle to approximate the input. The principle and performance of LPWM is familiar to PNPWM but LPWM excels by being simpler in implementation. Consider trailing edge modulation where the carrier $c(t)$ is normalized to 1:

$$c(t) = 2t - 1 \tag{3.5}$$

The time is normalized such that carrier period t_c=1. The approximated reference signal $x(t)$ can be written as:

$$x(t) = (S-1)(x_{n+1} - x_n)2t + (n+1)x_n - nx_{n+1} \tag{3.6}$$

where S indicates the number of samples used in the approximation within each switching period. The pulse width is derived by setting *c(t)=x(t).* After some rearrangement, the following expression arrive:

$$t_p = \frac{(n+1)x_n - nx_{n+1} + 1}{2 - (S-1)(x_{n+1} - x_n)} \tag{3.7}$$

It is illustrative to consider three distinct cases where $S = 2$, 3 and 5. The pulse width t_p is derived from (3.7) in these three cases:

S=2 (no interpolation):

$$t_p = \frac{x_0 + 1}{2 - (x_1 - x_0)} \tag{3.8}$$

S=3 (2x interpolation):

$$t_p = \begin{cases} \dfrac{x_0 + 1}{2(x_0 - x_1) + 2} & (x_1 < 0, n = 0) \\ \dfrac{2x_1 - x_2 + 1}{2(x_1 - x_2) + 2} & (x_1 \geq 0, n = 1) \end{cases} \tag{3.9}$$

S=5 (4x interpolation):

$$t_p = \begin{cases} \dfrac{x_0 + 1}{4(x_0 - x_1) + 2} & (x_1 < -0.5, n = 0) \\ \dfrac{2x_1 - x_2 + 1}{4(x_1 - x_2) + 2} & (x_2 < 0, n = 1) \\ \dfrac{2x_2 - x_3 + 1}{4(x_2 - x_3) + 2} & (x_3 < 0.5, n = 2) \\ \dfrac{2x_3 - x_4 + 1}{4(x_3 - x_4) + 2} & (n = 3) \end{cases} \tag{3.10}$$

The complexity of the algorithm is dominated by the single division that is involved, i.e. the complexity of the algorithm is nearly independent on S. Further approximation beyond S=5 is not rational from any point of view. This will be illustrated under the more detailed analysis of LPWM later in this chapter.

3.4.4 Direct compensation methods

In [Ha92] a precompensation methods is presented that considers UPWM as a non-linear signal-dependent transfer function, where the non-linear effect can be eliminated by pre-filtering the signal with the inverse transfer function. The non-linearity causing harmonic distortion has already been identified above in terms of the first sum in the DFS expressions for the UPWM methods. By pre-filtering the input samples with the non-linear inverse transfer function:

$$H_{pre}(z) = \frac{1}{H_{UPWM,x(n)}(z)} \tag{3.11}$$

The harmonic distortion will be cancelled. Such a direct cancellation of the known non-linearity is interesting as opposed to the precompensation methods that can be categorized as *indirect* methods. Unfortunately, the computational requirements in the process are huge [Ha92] and results have only been presented in combination with high sampling frequencies and very fine quantization.

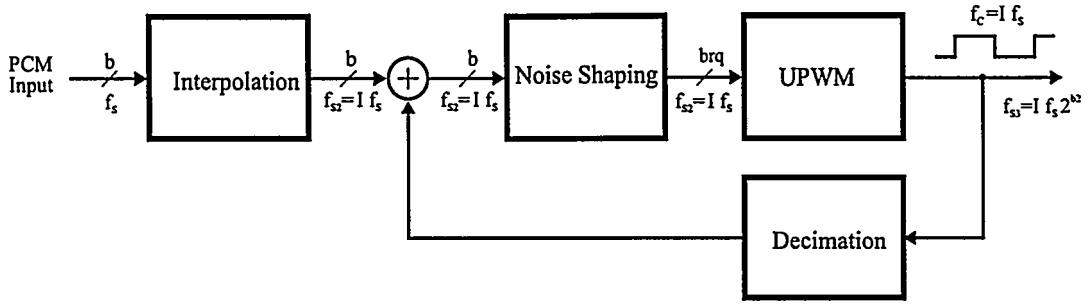


Fig. 3.19 Improving linearity by output feedback.

Another method that can be categorized as direct compensation is shown in [Ri97]. The method is based on a static non-linear precompensation to linearize the modulator, by utilizing general Hammerstein non-linear filters that are optimized for the application. Although the results given are very sparse, the method looks promising since the computational complexity is reasonably low and the distortion improvement controllable by the order of the Hammerstein non-linear filter.

3.4.5 Feedback linearization

An alternative method to compensate for the UPWM non-linearity is digital negative feedback around the digital UPWM modulator [Hi94]. The immense UPWM output frequency is a limitation in this approach since output decimation is required. Although the output is coarsely quantized to a single bit it does represent a baseband signal of very high resolution. Thus, the feedback processing has to be carried out with high precision. The direct feedback approach is severely complicated by the delay introduced by the feedback path decimation.

A more attractive approach is to *emulate* the non-linear effect of the UPWM unit in the feedback path using a non-linear filter. The method has been investigated in [An94] where the non-linear filtering is included in the feedback path of the noise shaper as shown in Fig. 3.20. The results are promising in that all negative effects of the non-linear UPWM process are effectively reduced. The main compromise in the method presented relies in the complexity of implementation and stability of the resulting modulator. With the non-linear feedback approach, stability and limited modulation index range is a concern not unlike sigma-delta modulators.

3.4.6 Method selection

As illustrated above, the field of PCM-UPWM conversion is extensively researched and various methods exist. The focus in the present research has not been on extensive research

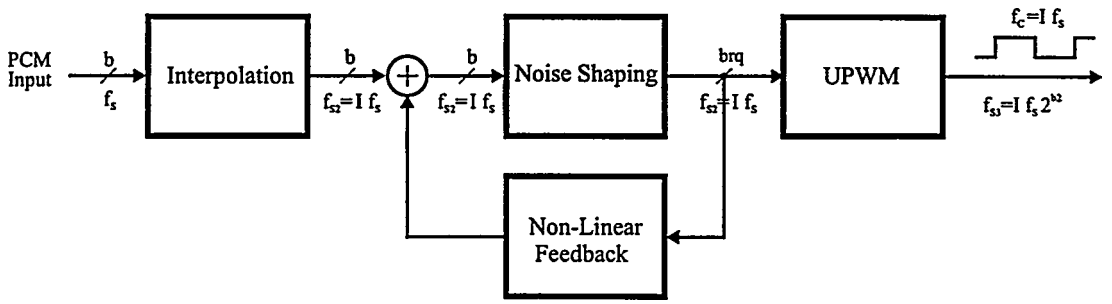


Fig. 3.20 Improving linearity by non-linear feedback.

Sampling method	Edge	Levels	Abbreviation
Hybrid sampling (LPWM)	Single sided	Two (AD)	LADS
		Three (BD)	LBDS
	Double sided	Two (AD)	LADD
		Three (BD)	LBDD

Table 3.4 Variants of LPWM

in new PCM-UPWM conversion. This would not contribute to the field in that the fundamental problems within digital PMA relate to the power conversion (the digital PMA paradox).

The choice of algorithm for digital PMA realization relies on the following simple facts:
- Effectiveness in linearization UPWM compared with the desired performance.
- Computational complexity.
- Robustness.
- Modulation depth.

Based on a combined consideration of the above parameters, the LPWM algorithm is chosen due to high performance, low computational complexity, no stability problems no constraints on modulation depth.

3.5 LPWM spectral analysis

The fundamental investigations of LPWM in [Sh92] are extended in the following with a more general and in depth analysis of the principle that covers all four fundamental LPWM variants, as defined in Table 3.4. The tonal behavior of LPWM is investigated by computer simulation, since the double Fourier integrals that arrive form this sampling approach can not be solved analytically. Distortion of lower modulation indexes can not be investigated, but since the focus is on worst-case situations this is not a severe limitation. Similarly, no HES plots are generated. The interesting properties of LPWM lie in the LF characteristics. The HF characteristics will inherently be "in-between" the natural and uniformly sampling cases. Furthermore, generation of HES surfaces requires an exhaustive set of simulations without DFS expressions.

Fig. 3.21 to Fig. 3.24 shows the simulated amplitude spectrum for the four LPWM methods for $S=1$, $S=2$, $S=3$ and $S=5$, respectively. M=0dB and $f_r = 1/16$ corresponding to the worst case combination of frequency and modulation depth. The following interesting properties are observed:
- All methods provide a significant reduction in THD in this worst case situation and the improvement increases with approximation accuracy S. E.g. for LADS the 2. and 3. harmonic are reduced 70dB and 40dB respectively with LADS, when $S = 5$.
- The HF-characteristics are in-between the naturally sampling and uniformly sampling cases. Not surprisingly, the HF-characteristics converges towards NPWM as approximation accuracy increases, i.e. the IM components increase with S.
- With sufficient approximation, LBDD provides *does* provide effective doubling of sampling frequency just as NBDD (this is not the case with UBDD)

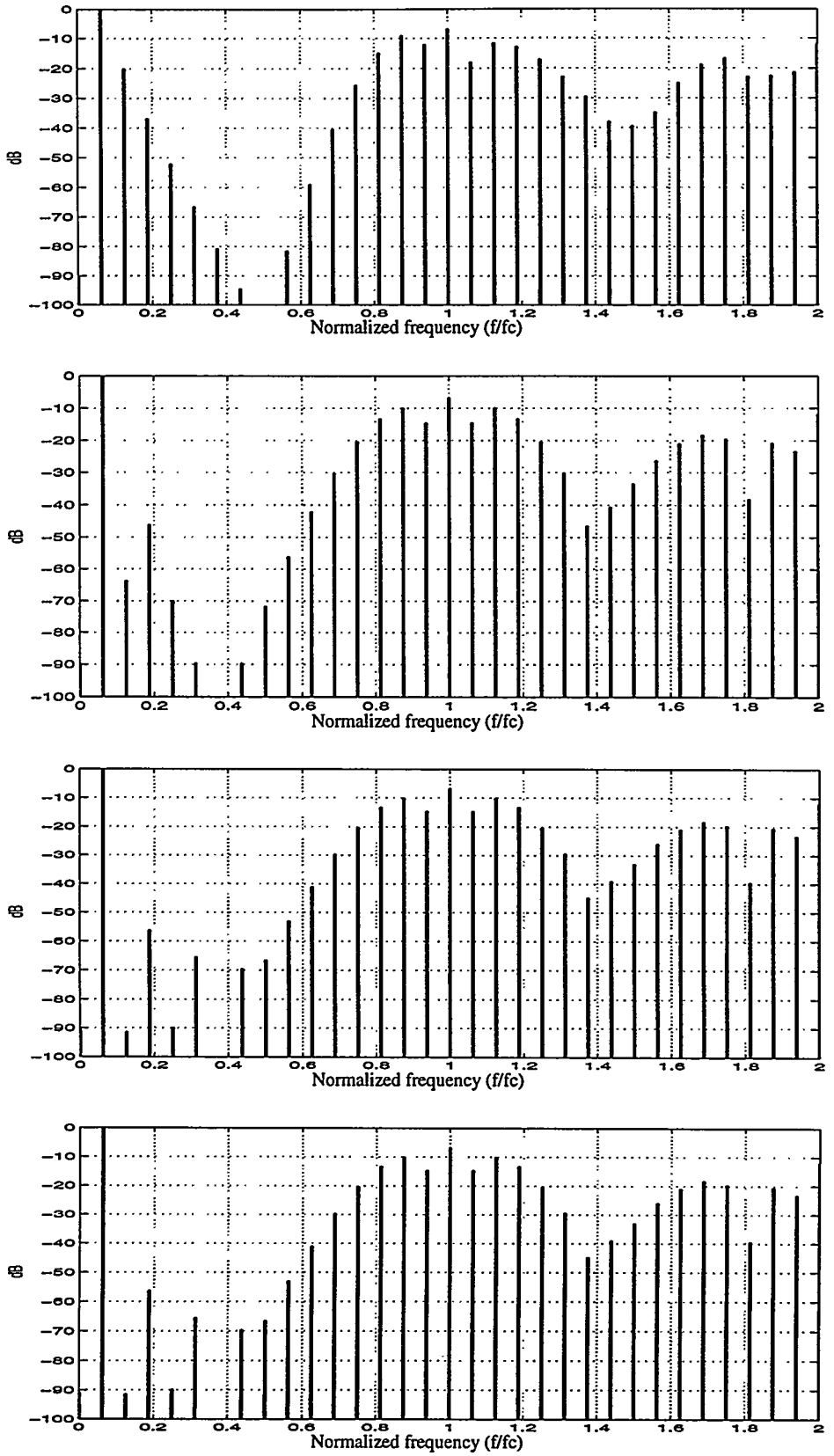


Fig. 3.21 Amplitude spectrum for **LADS**. From top to bottom S=1 (UADS), S=2, S=3 and S=5 respectively. f_r = 1/16. M = 0dB. Note the significant improvement with the approximation accuracy.

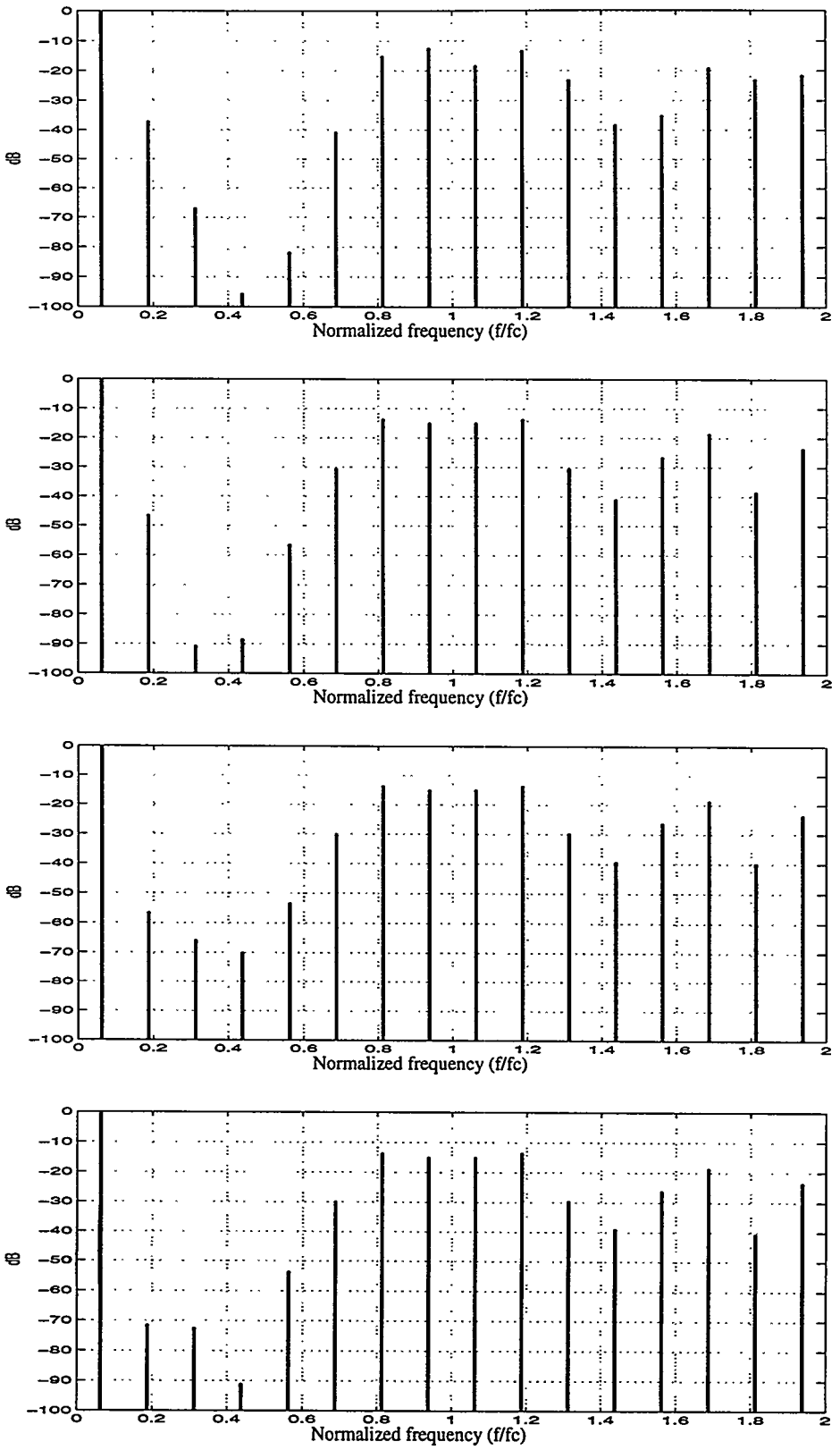


Fig. 3.22 Amplitude spectrum for **LBDS**. From top to bottom S=1 (UBDS), S=2, S=3 and S=5 respectively. f_r = 1/16. M = 0dB.

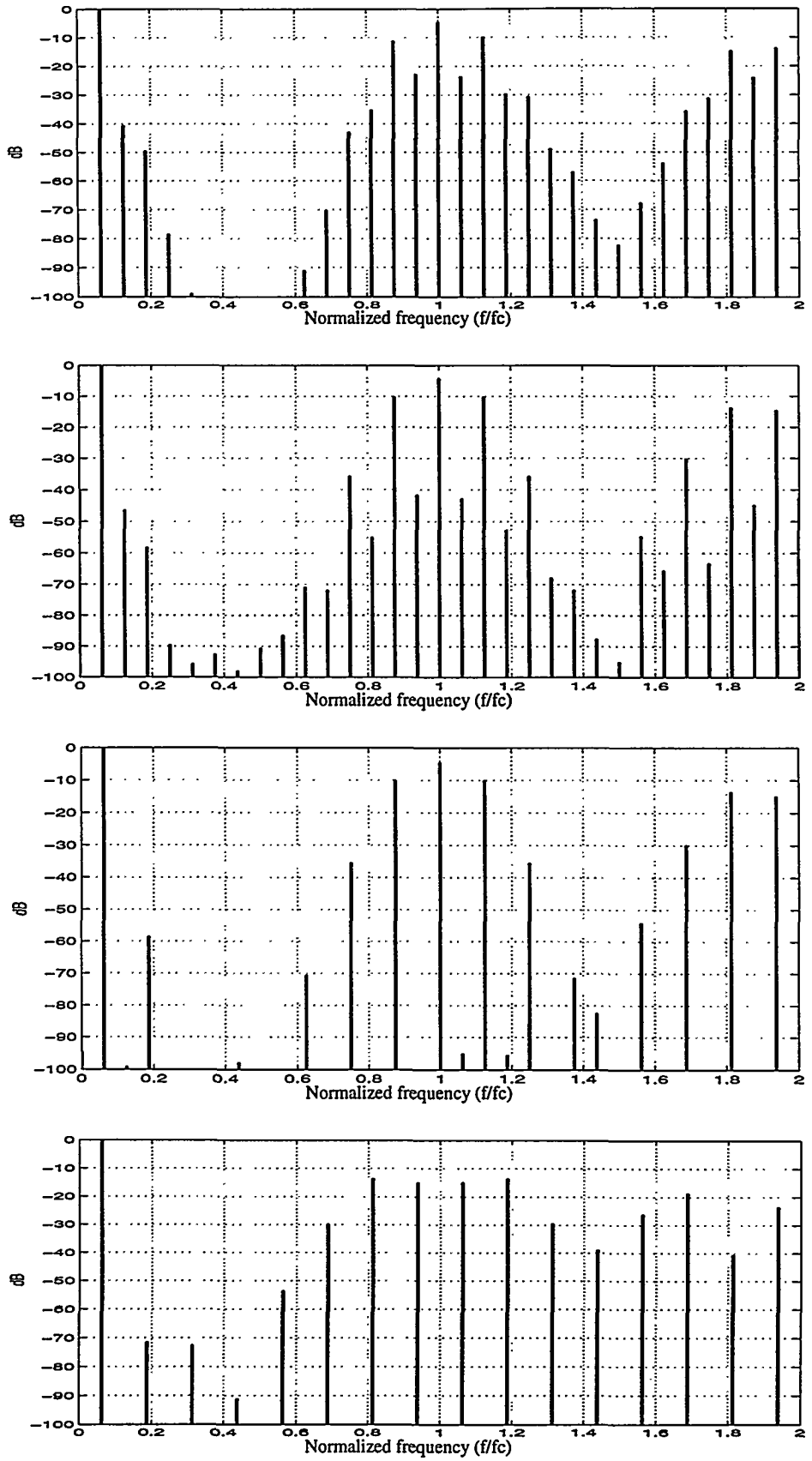


Fig. 3.23 Amplitude spectrum for **LADD**. From top to bottom S=1 (UADD), S=2, S=3 and S=5 respectively. $f_r = 1/16$. $M = 0$dB.

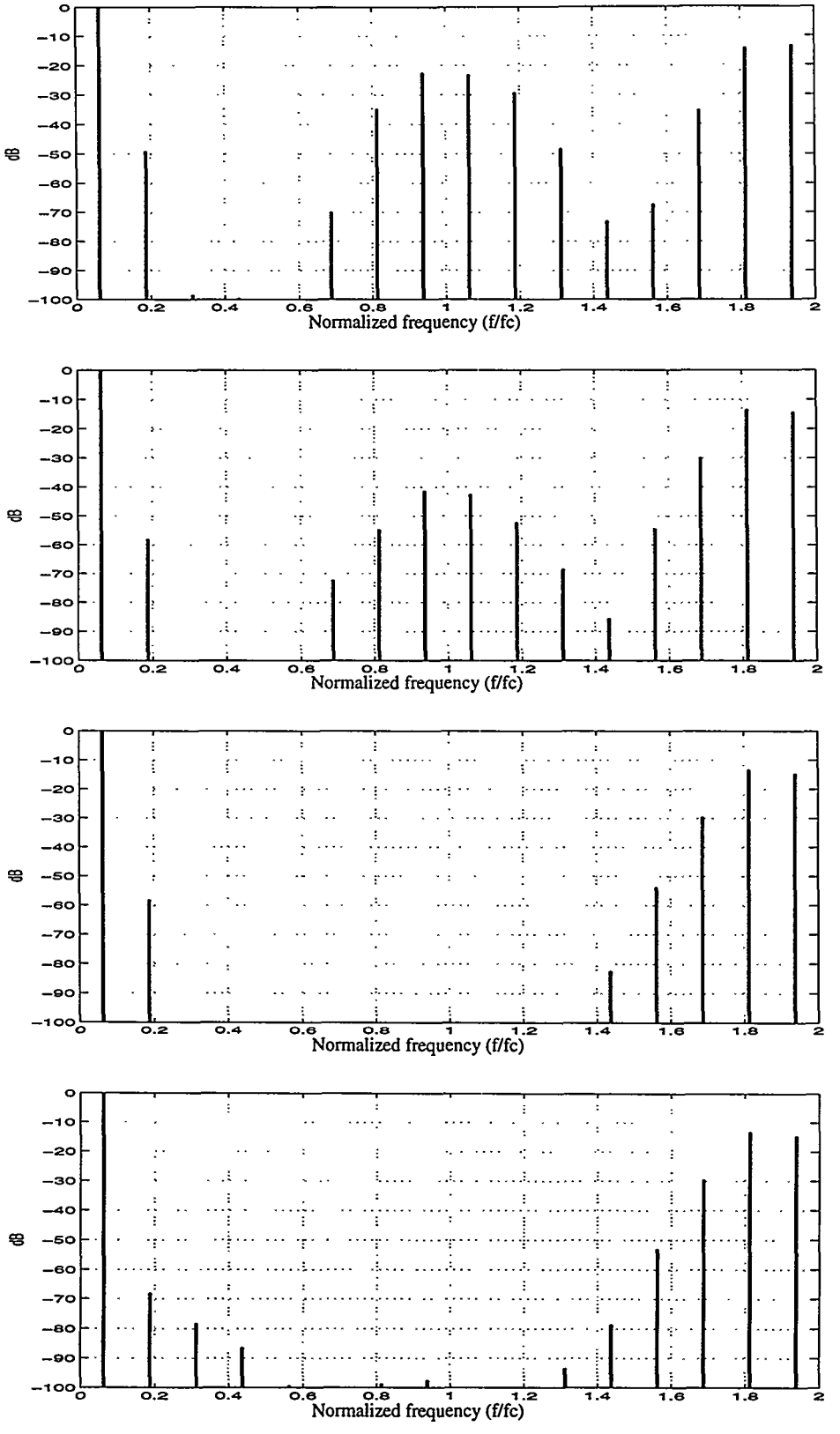


Fig. 3.24 Amplitude spectrum for **LBDD**. From top to bottom S=1 (UBDD), S=2, S=3 and S=5 respectively. f_r = 1/16. M = 0dB. Note the "morphing" transition from uniform sampling to the natural sampling like HF-spectrum as approximation accuracy increases.

3.5.1 LPWM distortion

The initial analysis above focused on the absolute worst case situation with full-scale modulation and the worst-case frequency ratio. A parametric investigation of distortion as a function of modulation index and frequency is investigated in the following. THD vs. f_r for S=2, S=3 and S=5 is shown in Fig. 3.25 to Fig. 3.29 for the four LPWM methods. It is interesting to notice that THD is close to linearly dependent on the frequency ratio f_r. A similar characteristic was found in the investigations of UPWM. The THD is seen to improve 10-15dB with each step in approximation accuracy. The approximate maximal frequencies rations where THD < -80dB at full modulation depth are summarized below.

Maximal frequency ratios $f_{r,max}$ for THD<-80dB @ M=0dB				
S	LADS	LBDS	LADD	LBDD
1	-78 dBf_r	-46 dBf_r	-44 dBf_r	-39 dBf_r
2	-42 dBf_r	-41 dBf_r	-41 dBf_r	-34 dBf_r
3	-36 dBf_r	-36 dBf_r	-35 dBf_r	-35 dBf_r
5	-31 dBf_r	-30 dBf_r	-30 dBf_r	-30 dBf_r

The frequencies are given in dB relative to the carrier frequency ($dBf_r = 20\log(f_r)$). Clearly, $f_{r,max}$ is within a range where other factors as the IM distortion and demodulation becomes more dominant such that the linearity is no longer the limiting factor within the digital modulator. Another remarkable property of LPWM is that the differences in THD between modulation schemes diminish as the approximation accuracy is increased. At S = 5 the distortion is thus nearly the same for all LPWM methods. The *nature* of the distortion however is not the same as shown from the spectral amplitude simulations in figures Fig. 3.21 to Fig. 3.24 above.

To conclude, it is possible to realize significant improvements in linearity with the simple LPWM algorithm, such that modulator linearity is no longer an obstacle in digital PMA systems. Also, the HF spectral characteristics approach the natural sampling case, and LBDD clearly has the most attractive HF-characteristics if the approximation is sufficiently good.

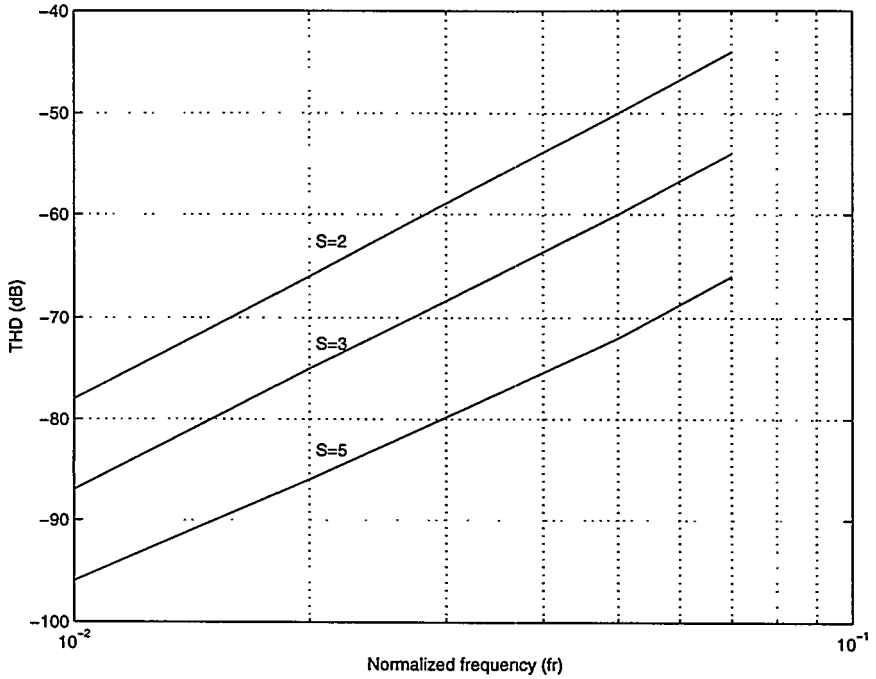


Fig. 3.25 LADS THD vs. f_r. M=0dB.

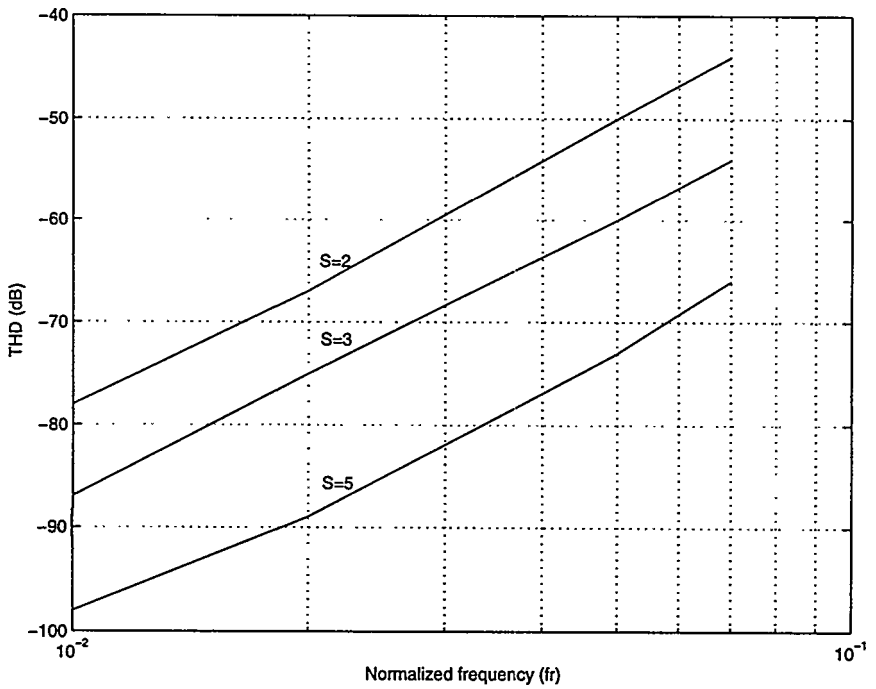


Fig. 3.26 LBDS THD vs. f_r. M=0dB.

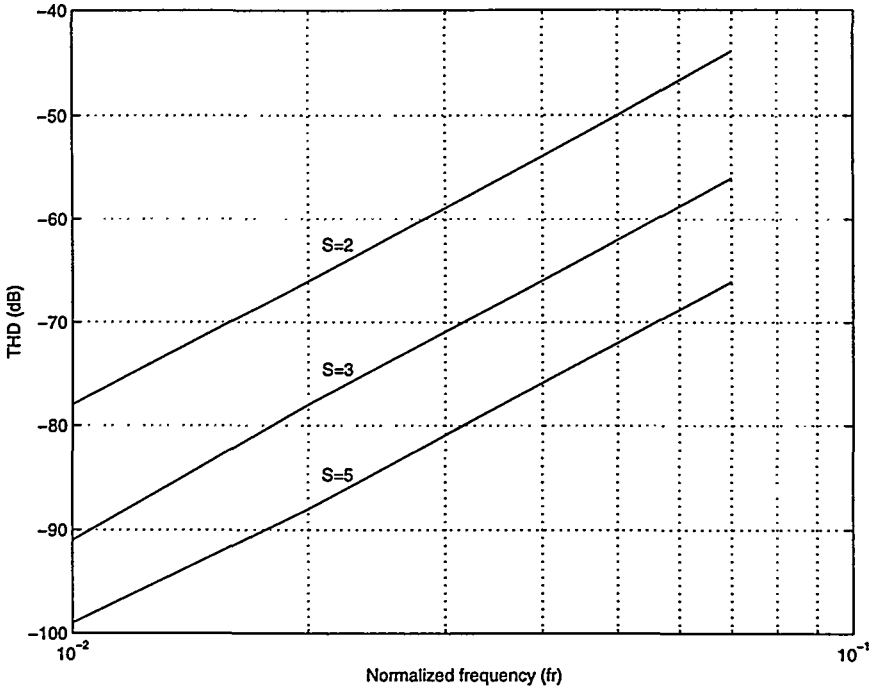


Fig. 3.27 LADD THD vs. f_r. M=0dB.

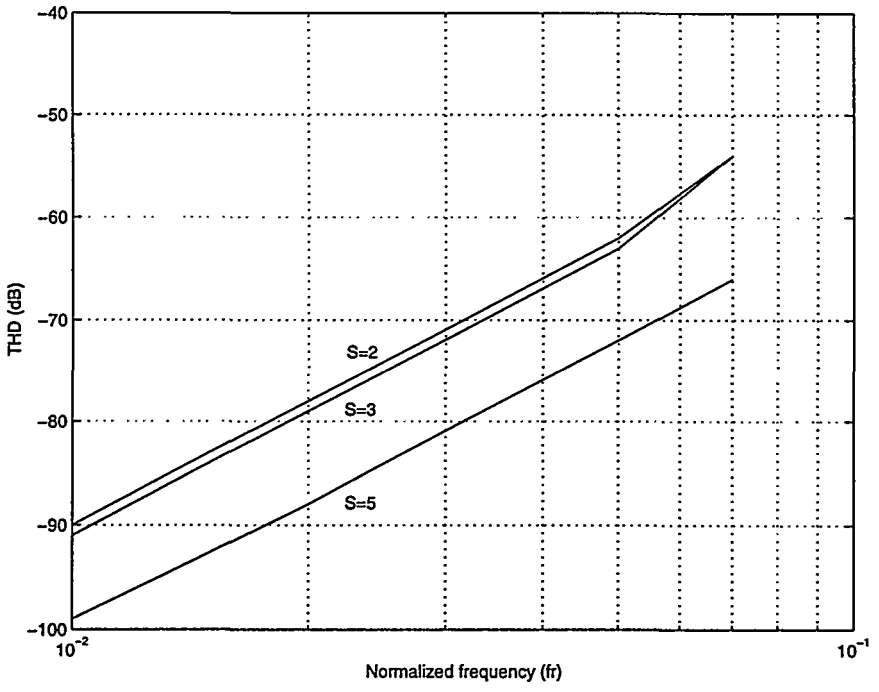


Fig. 3.28 LBDD THD vs. f_r. M=0dB.

3.6 LPWM modulator synthesis

The optimization of digital LPWM modulators dedicated to digital PMA applications will now be investigated in detail. The previous discussion has focused on the UPWM and ways to improve linearity. The focus now turns to the other elements of the digital modulator, i.e. interpolation and especially noise shaper optimization for this specific application. Finally, a simple LPWM modulator design methodology will be proposed for systematic and automated LPWM modulator synthesis for PMA applications.

3.6.1 Interpolation

Sample rate conversion is a well-known field of digital signal processing [Pr96]. There are special considerations regarding interpolation in digital LPWM modulators in that the interpolation serves three purposes:

1. To improve linearity of the modulation by providing a reasonable carrier frequency /bandwidth ratio.
2. To provide excess bandwidth for noise shaping.
3. To further improve linearity by improving the approximation of the LPWM algorithm.

It is important to differentiate between oversampling and interpolation of the input data. Since the PCM input is quantized and sampled a low rate initially, the quantization noise is concentrated in the base band. The noise cannot be removed no matter what sample interpolation rate is utilized in contrast to quantizing an *oversampled* signal where the quantization noise will be spread evenly over the band. The dynamic range of a general O times oversampled signal is [Ha91]:

$$D = 6.02b + 10\log O + 1.76 \tag{3.12}$$

A normal digital audio signal (16 bits, 44.1KHz) has a dynamic range of 98.5 dB. Every in oversampling by a factor of four increases the effective resolution by one bit. The 8x-16x interpolation required in a digital LPWM modulator is easily realized by a standard interpolation chip. Further interpolation as required by the LPWM precompensation algorithm is computationally simple and does not lead to excessive increase in total computational complexity. The wide interpolation filter band will allow for a lower order filter in the interpolation stage. In terms of practical implementation, numerous approaches exist. A particularly efficient structure that is optimally suited for 2x or 4x interpolation of an already interpolated signal, are half-band filters [Hi94]:

$$h(n) = \frac{1}{2}\frac{\sin(n\frac{\pi}{2})}{n\frac{\pi}{2}} \tag{3.13}$$

The computational advantage arises from the symmetric impulse response, where half of the coefficients are zero. Moreover, the filter order will be low in this specific application.

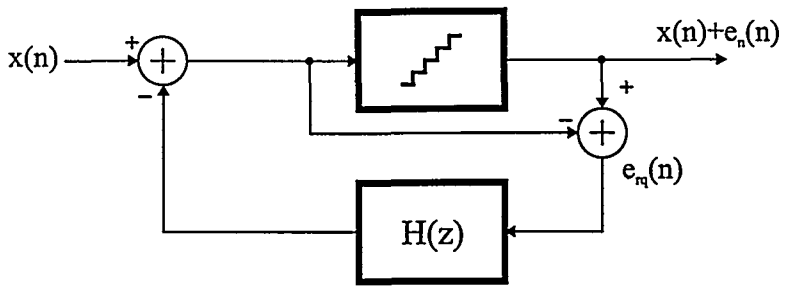


Fig. 3.29 General noise shaper topology

3.7 Noise shaping

Noise shaping is a deterministic technique to shape a signal's requantization noise by a quantizer and an error feedback loop, as shown by the general topology in Fig. 3.29. Subtracting the direct and quantized input derives the present quantization noise. Subsequently, the error signal is feedback through a linear digital filter and added to the input signal, whereby the noise shaper can spectrally shape the noise from the wide-band noise source. Noise shaping is used widely in conversion systems and has been covered extensively in the previous literature [Ge89], [Ha91], [Go92], [Hi94]. Most conversion systems use a combination of oversampling, requantization to a single or a few bits and noise shaping to secure the audio band performance. This tradeoff between resolution/accuracy and bandwidth has proven to be superior to traditional multi-bit converters in many cases. However, coarse quantization (to a single or a few bits) introduces a range of problems, mostly concerned with the complex analysis of these highly nonlinear systems. The digital PWM modulator differs from the widely used sigma delta modulators by not needing any coarse quantization. With the present speed of digital logic, quantization within the range 6-10 bits is sufficient for practical implementation.

3.7.1 Analysis

In the following, the use of noise shaping in digital PWM systems is analyzed in more detail. A general multiple bit quantizer characteristic is shown in Fig. 3.30. The quantizer rounds the to the nearest multiple of Δ. A simple approach to noise shaper modeling is to model the quantizer as an additional independent noise source. A prerequisite for this simplified model is that the noise source can be considered a wide sense stationary random process, which is independent of the input signal. The validity of this assumption is very questionable in the single bit case, but is in general a very good assumption in the case where quantization is fine [Ha91]. Before initiating the analysis of the noise shaping system, the variables of interest are summarized below:

Variable	Representation	Comment
$x(n)$	$S_x,\ \sigma_x^2$	Non-quantized input
$q(n)$	$S_q,\ \sigma_q^2$	Quantization error on input
$e_{rq}(n)$	$S_{rq},\ \sigma_{rq}^2$	Requantized noise source
$e_n(n)$	$S_n,\ \sigma_n^2$	Output error noise
$e_{nb}(n)$	$S_{nb},\ \sigma_{nb}^2$	Baseband output error noise
$e_{no}(n)$	$S_{no},\ \sigma_{no}^2$	Total output noise

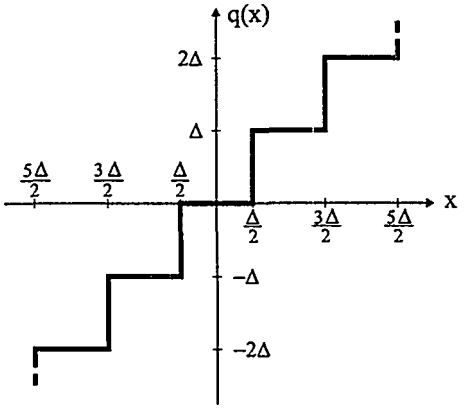


Fig. 3.30 Rounding quantizer.

From Fig. 3.29 we get can write the following z-domain expression:

$$E_{rq}(z) = X(z) + E_{rq}(z)H(z) - \big(X(z) + E_n(z)\big) = E_{rq}(z)H(z) - E_n(z) \tag{3.14}$$

The white noise source is assumed to have a Z-transform to simplify the analysis. The following simple relationship between the output error noise and the requantized noise arrives, defined as the *noise transfer function* $NTF(z)$:

$$NTF(z) = \frac{E_n(z)}{E_{rq}(z)} = 1 - H(z) \tag{3.15}$$

3.7.2 Linear modeling

To simplify the analysis of the noise shaping system, the quantizer is modeled as an additional, independent noise source as shown in Fig. 3.31. The assumption lets us treat the noise shaper as a linear system. Thus, the power spectral density (PSD) of the noise shaped noise can be written:

$$S_n(z) = |NTF(z)|^2 S_{rq}(z) \tag{3.16}$$

Subsequently, the resulting noise shaped output error power σ_n^2 can be related to the total requantized error noise power σ_{rq}^2 by a constant noise gain factor G_N, which is the squared 2-norm of noise transfer function impulse response. For a FIR NTF(z) of N-order we get:

$$G_N = \frac{\sigma_n^2}{\sigma_{rq}^2} = \sum_{n=0}^{N-1} |ntf(n)|^2 = \|ntf(n)\|_2^2 \tag{3.17}$$

G_N is defined as the *noise gain* of the noise shaper. Since:

$$ntf(n) = \begin{cases} 1 & (n = 0) \\ -h(n) & (n \in \{1,2,\ldots,N-1\} \\ 0 & (otherwise) \end{cases} \tag{3.18}$$

The following inequality holds for the noise gain:

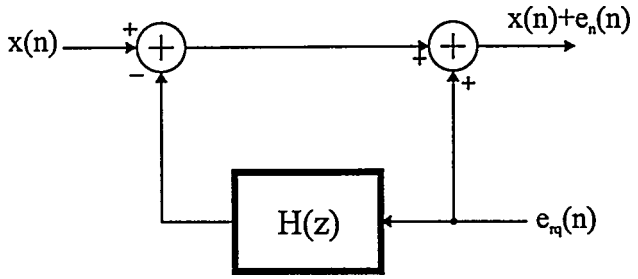


Fig. 3.31 Model of noise shaper topology

$$G_N = 1 + \sum_{n=0}^{N-1} h(n)^2 \geq 1 \tag{3.19}$$

Equality is obtained only in the trivial case where no filter is present, and the total output noise power will thus exceed the total input noise power by a constant factor corresponding to the noise gain. Parsevals theorem provides a dual expression in the frequency domain:

$$G_N = \frac{\sigma_n^2}{\sigma_{rq}^2} = \frac{1}{\pi}\int_0^{\pi} |NTF(\omega)|^2 d\omega \tag{3.20}$$

3.7.3 Noise Transfer function (NTF) filter synthesis for digital LPWM

With this basic review of fundamental noise shaping properties, the question now arises how to synthesize optimal noise shaping filters suited for digital PWM modulators? A fundamental theorem of particular interest when designing general noise shaping filters is the Gerzon/Craven *Optimal Noise Shaping theorem* [Ge89]. The theorem states that a properly scaled noise transfer function obeys:

$$\int_0^{\pi} \log|NTF(z)| d\omega \geq 0 \tag{3.21}$$

Equality is obtained if and only if $NTF(z)$ has minimum phase. Thus, with a minimum phase $NTF(z)$ plotted with linear frequency axis and logarithmic magnitude, the areas above and below the 0dB line are equal. This is a very useful property since the consequences of stopband level, passband level and transition band can be understood by simple geometric observations. The theorem clearly states that the information capacity of a channel can not be increased by processing. Thus, a noise shaper can only hope to *preserve* the information capacity.

Assuming, that all frequencies within the signal band are considered equally important, the optimal noise shaping theorem directly dictates a *flat* characteristic of the pass band as optimal. This will minimize the noise gain of the noise shaper and provide an equal distribution of the noise within the signal band. There are further arguments to support this hypothesis: The input is already quantized and the noise shaper can not influence this inherent limit on the dynamic range. Accordingly, nothing is achieved with a local attenuation beyond this limit. Any "gain" within the band will lead to a "loss" out of band which will increase the noise gain. In case of a high input resolution (e.g. 24 bits) psycho-acoustic, optimal [Wa90] or semi-optimal noise shaping could be utilized to improve the resolution further "subjective" 1-2 bits compared to the flat characteristic.

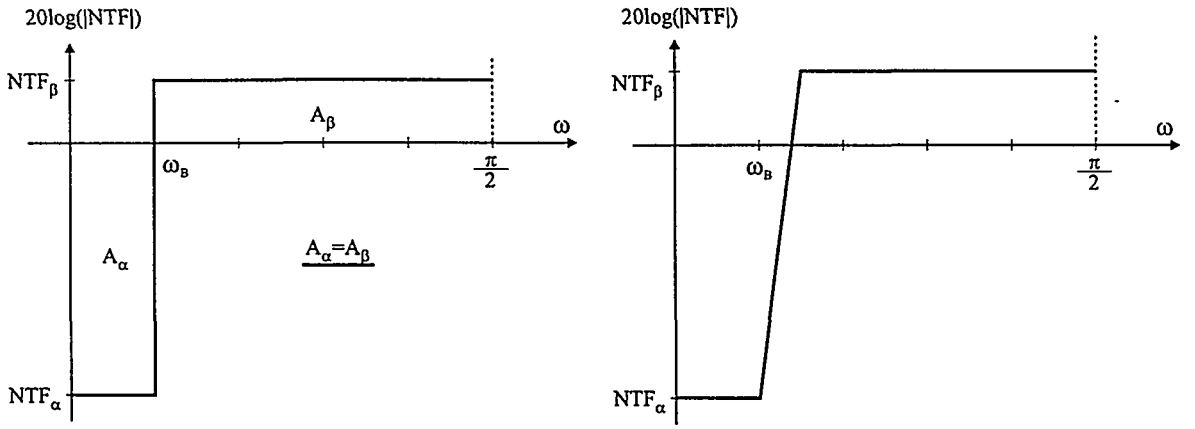


Fig. 3.32 G_N-optimal $NTF(z)$ (left) and modified optimal $NTF(z)$ prototype (right).

With this constraint on the base-band, it can be shown [Na91] that a *constant* level also in the remaining band will provide a minimum noise gain. From the perspective of minimizing the noise gain with a flat base-band characteristic, the optimal NTF the characteristic shown in Fig. 3.32 (left). If the $NTF(z)$ is minimum phase we can write:

$$\int_0^{\pi} \log|NTF(z)|d\omega = \int_0^{\omega_B} \log NTF_\alpha \, d\omega + \int_0^{\pi} \log NTF_\beta \, d\omega = 0 \tag{3.22}$$

Thus, a simple analytical relationship between the base-band attenuation and stop-band gain can be derived:

$$NTF_\beta = 2^{\left[\frac{-\omega_B}{\omega_s/2-\omega_B}\log NTF_\alpha\right]} \tag{3.23}$$

This relation could be used to determine minimum noise gain G_N for any baseband bandwidth ω_B and NTF_α. However, minimizing G_N is not the only issue when optimizing noise shaping filters. Other factors are outlined below.

Dynamic range requirements

The NTF design should be based on defined requirements for the output dynamic range D (again considering the inherent limit on this parameter). From this NTF_β can be determined directly as shown below.

NTF transition band

As shown above a minimal noise gain requires an infinitely sharp transition band. This can not be realized in practice and more important - a sharp transition band is simply not needed since the requantization is fine and the linearity requirements lead to sufficient "space" for the noise shaper operation. From the analysis of LPWM, distortion and general spectral characteristics above, the bandwidth requirements for all modulation types can be determined. The constraints on f_r due to not only linearity, but also intermodulation and demodulation will generally provide sufficient bandwidth for noise shaping. In terms of computational complexity, it is furthermore desirable with a simple filter to realize $NTF(z)$, preferably with a low order FIR or IIR filter.

Intermodulation effects
The noise shaped noise passes a non-linear element in terms of the UPWM modulator. Accordingly, there is a potential risk for intermodulation effects between any of the out of band components. This may decrease estimated performance.

It should be mentioned that various filters have been investigated in previous work [Sh92], [Go92], [Hi94], but the characteristics and focal points seem to differ. By considering the above most important design parameters, it is possible to specify a *modified optimal NTF* shape as shown in Fig. 3.32 (right).

3.7.4 NTF(z) signal band requirements

The linear noise shaper model can be used to estimate the signal band requirements with a given dynamic range specification. The dynamic range D of the modulator is defined as:

$$D = \frac{\sigma_{x,\max}^2}{\sigma_q^2 + \sigma_{nb}^2} \tag{3.24}$$

The dynamic range is normally expressed as in dB ($10\log(D)$). Assuming a rectangular distribution, we can write the noise power for a general multi-bit quantizer as:

$$\sigma^2 = \frac{\Delta^2}{12} \tag{3.25}$$

Hence, we derive for σ_q^2 and σ_{rq}^2:

$$\Delta_q = \frac{1}{2^{b-1}} \Rightarrow \sigma_q^2 = \frac{1}{12 \cdot 2^{2(b-1)}} \quad \text{and} \quad \Delta_{rq} = \frac{1}{2^{b_{rq}-1}} \Rightarrow \sigma_{rq}^2 = \frac{1}{12 \cdot 2^{2(b_{rq}-1)}} \tag{3.26}$$

The input is assumed sinusoidal with unity full-scale amplitude:

$$\sigma_{x,\max}^2 = \frac{1}{2} \tag{3.27}$$

The requantization noise power over the base-band is found from the power spectral density expression (3.16) by simple integration over the base-band:

$$\begin{aligned} \sigma_{nb}^2 &= \frac{1}{\pi}\int_0^{\frac{\pi}{L}} S_{rq}(\omega)d\omega \\ &= \frac{1}{\pi}\int_0^{\frac{\pi}{L}} \frac{1}{12 \cdot 2^{2(b_{rq}-1)}} NTF_\alpha^2 \, d\omega \\ &= \frac{NTF_\alpha^2}{12L \cdot 2^{2(b_{rq}-1)}} \end{aligned} \tag{3.28}$$

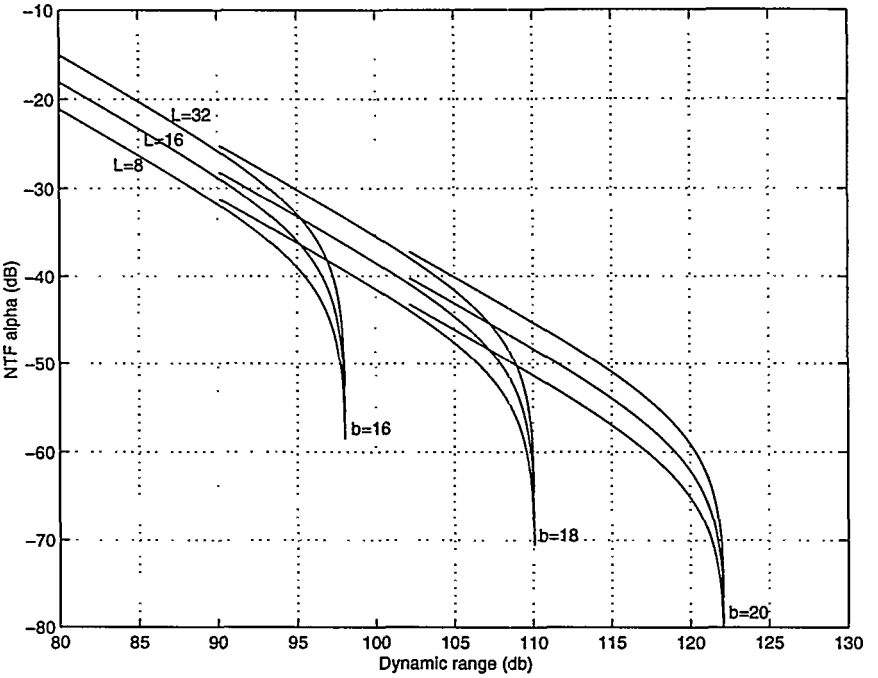


Fig. 3.33 Parametric analysis of NTF_α requirements.

From (3.24) we have:

$$D^{-1}\sigma_x^2 = \sigma_q^2 + \sigma_{nb}^2 \Leftrightarrow \frac{1}{2}D^{-1} = \frac{1}{12\cdot 2^{2(b-1)}} + \frac{NTF_\alpha^2}{12L\cdot 2^{2(b_{rq}-1)}} \tag{3.29}$$

From this, the resulting NTF passband requirements can be determined from the required signal to noise ratio from the following simple expression:

$$NTF_\alpha = 2^{(b_{rq}-1)}\sqrt{L(6D^{-1} - 2^{-2(b-1)})} \tag{3.30}$$

A parametric analysis of the base-band requirements using (3.30) is shown in Fig. 3.33. The requantized resolution is held constant at 8 bits, whereas oversampling factors are is $L \in \{8, 16, 32\}$ and the input resolution set in the range $b \in \{16, 18, 20\}$. As expected, the input resolution puts a natural limitation on the achievable dynamic range. As the desired output dynamic range approaches this limit, the NTF_α requirements increase dramatically. Well below the limit, a linear relationship between desired output dynamic range D and NTF_α is observed as predicted from theory.

3.7.5 Realizing the modified NTF(z) prototype

An inevitable constraint in designing noise shaping filters is the requirement of at least a one sample delay, i.e. $H(z)$ can be factorized in a one sample delay and a normal causal digital filter:

$$H(z) = \frac{C(z)}{D(z)} = z^{-1}\frac{c_1 + c_2 z^{-1} + c_3 z^{-1} + \ldots + c_N z^{-(N-1)}}{d_0 + d_1 z^{-1} + d_2 z^{-2} + \ldots + d_N z^{-N}} \tag{3.31}$$

We have:

$$NTF(z) = \frac{A(z)}{B(z)} = 1 - H(z) = \frac{D(z) - C(z)}{D(z)} \tag{3.32}$$

The requirement for a one-sample delay in $H(z)$ thus leads to the following normalized expression, which is causal and without delay:

$$NTF(z) = \frac{1 + a_1 z^{-1} + a_2 z^{-1} + \ldots + a_N z^{-N}}{1 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_N z^{-N}} \tag{3.33}$$

This constraint on *NTF(z)* design complicates the filter design since normal filter design packages are not directly applicable. The question arises whether to use FIR or IIR filters? In general, recursive filters can realize a given NTF prototype with a higher computational efficiency than non-recursive filters. On the other hand FIR filters are inherently stable and do not suffer from idling patterns. With the modified optimal NTF prototype, the choice of filtering approach is not essential, since both IIR and FIR filters will realize the noise shaper with a low order. The modified optimal NTF prototype can be approximated for any application using numerical optimization. In the following both FIR and IIR realizations of the optimized NTF are devised. Consider the situation where L = 9 and the NTF_α requirement is -50dB to -60dB. Both FIR and IIR approaches to NTF realization are presented below for this specific example.

FIR realization

The filter orders are only 5 and 8 in the two cases NTF_α = -50dB and NTF_α = - 60dB, respectively. The frequency response for $NTF(z)$ and zero maps of the two optimized filters are shown in Fig. 3.34. The following general characteristics are noted for FIR filter realization of the modified optimal NTF shape:

- The *modulus* of the "base-band zeros" is lower than 1, i.e. the zeros are no*t* placed on the unit circle as it is the case with most standard FIR filter design methods (e.g. Parks-McClellan).
- The *angles* of the base-band zeros are spread to minimize the base-band ripple.
- Out of band zeros a positioned to optimize the shape towards the modified optimal NTF.

The resemblance of the two filters with the modified optimal NTF prototype is obvious. The noise gains for the two filters are:

$$G_{N,FIR5} = 19.6 \quad and \quad G_{N,FIR8} = 54.3$$

The noise gain of the eighth order filter can cause intermodulation problems. The use of relatively high G_N filters as the eighth order FIR filter, requires a low noise source (i.e. fine requantization) to prevent intermodulation within the UPWM.

IIR realization

IIR filters can realize the optimized NTF prototype shape with a lower filter order. The above requirements are realized with IIR filters of only fourth and fifth order. The

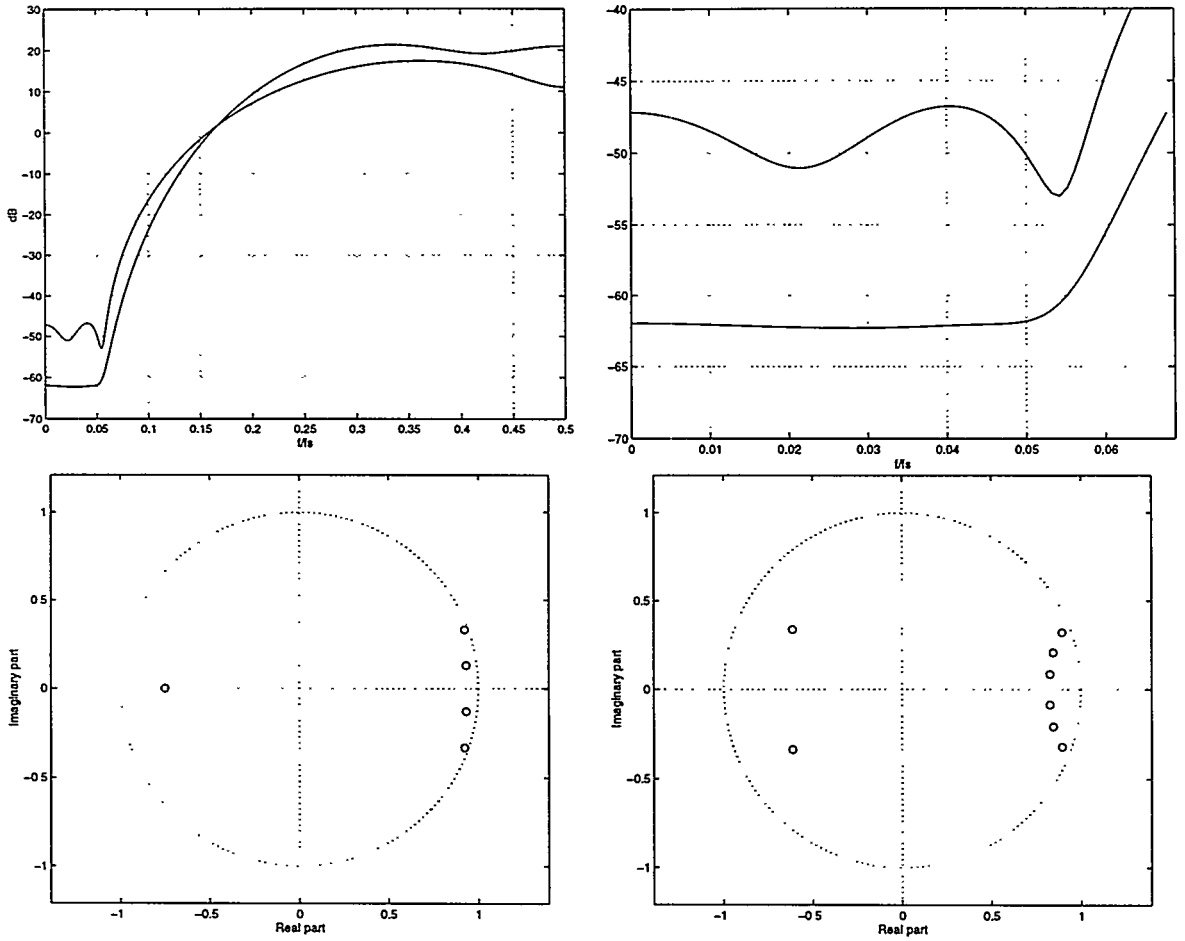


Fig. 3.34 $NTF(z)$ for the fifth and eighth order FIR filter approximating the modified NTF prototype and realizing the required NTF_α. Top - $NTF(z)$ transfer function. Bottom – Zero positions.

frequency response and pole- zero maps of the two optimized filters are shown in Fig. 3.35.

The optimized IIR have the following characteristics:

- The base-band zeros have the same characteristic as in the FIR case with modulo optimized to obtain minimal ripple (flat characteristic).
- The out-of-band poles originate from an IIR elliptic high pass filter with a stop band corresponding to the desired base-band.

Both filters realize the requirements with minimal noise gains:

$$G_{N,IIR4} = 15.2 \quad and \quad G_{N,IIR5} = 32.5$$

To conclude, even excessive requirements for NTF_α corresponding to 18-20 bits of output resolution can be realized with low order FIR and IIR filters, with typical values for L and b_{rq} in LPWM based digital PMA systems.

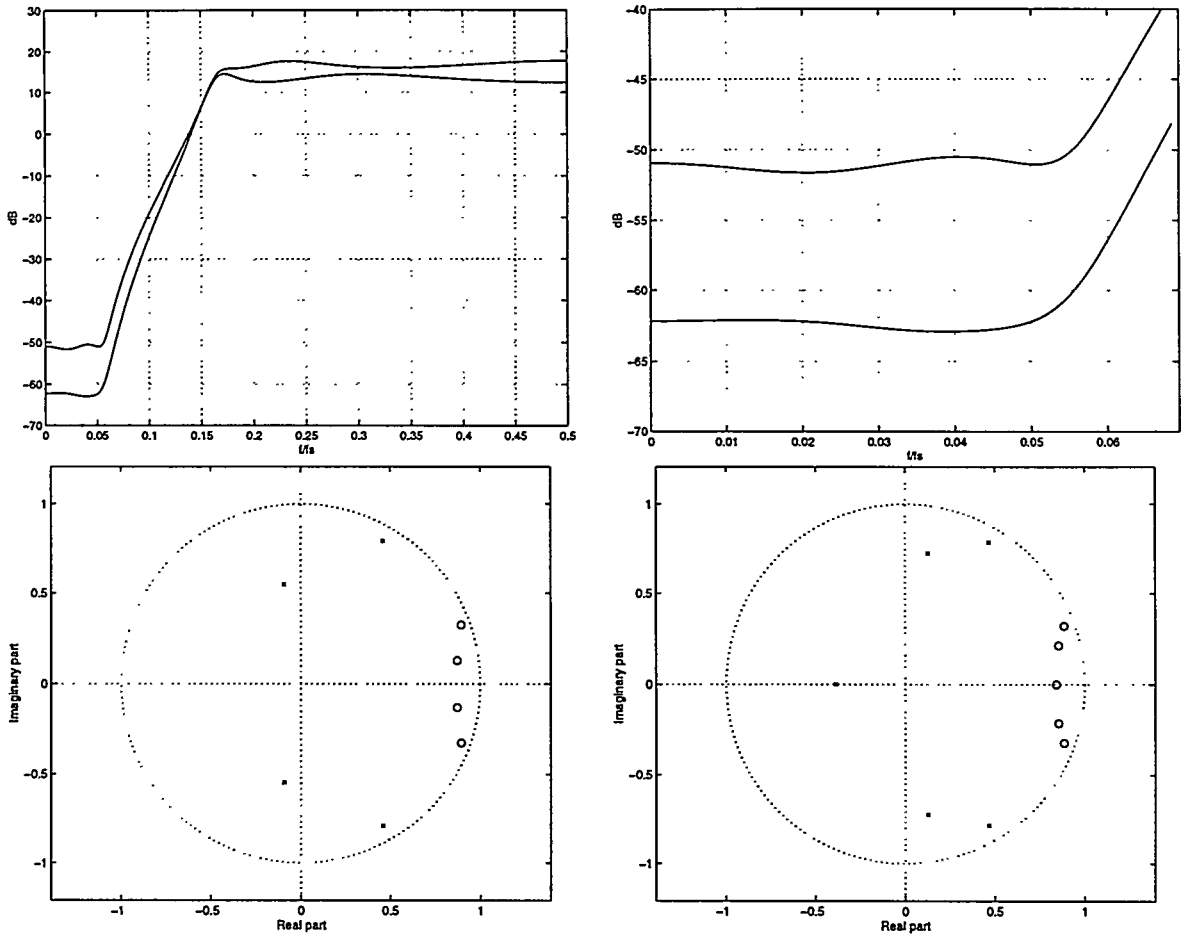


Fig. 3.35 $NTF(z)$ for the fourth and fifth order IIR filters approximating the modified NTF prototype and realizing the required NTF_α. Top - $NTF(z)$ transfer functions. Bottom – Zero positions.

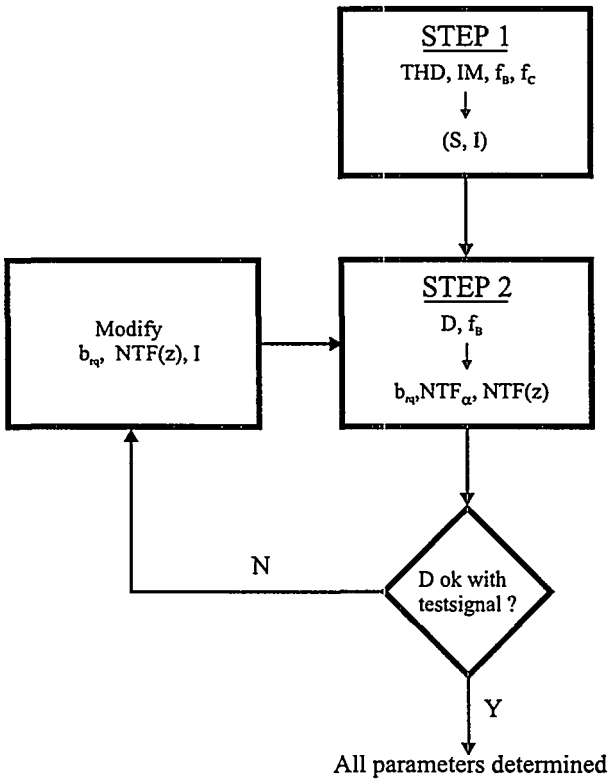


Fig. 3.36 LPWM modulator design methodology.

3.8 LPWM modulator design methodology

The optimization of the modulator involves a simultaneous optimization of a range of parameters. Besides the specific modulator parameters as the interpolation factor, the number of samples and the noise shaper resolution, it is necessary to also consider a broader range of possible sampling frequencies 44.1KHz, 48KHz and 96KHz. The target bandwidth is an important variable in active speaker systems [Ni96], and the input resolution may vary between 16-24 bits in the near future. However, the guidelines given above on individual parameter optimization can be condensed into a more systematic iterative LPWM design methodology as shown in Fig. 3.36. The foundation is a separation of the linearity and dynamic range requirements. The modulator design methodology has been used to design modulators for the digital PMA systems that have been investigated (Chapter 10).

STEP1

Based on specified requirements for bandwidth f_B, THD and IM distortion within the target bandwidth and carrier frequency (efficiency) the:

- PWM method
- Interpolation factor I
- Number of samples S

are determined. This can be carried out directly from the spectral analysis results for LPWM.

STEP2

Based on specifications for bandwidth f_B and dynamic range D the requantized resolution b_{rq}, the necessary NTF_α and the shape of $NTF(z)$ are determined. Although NTF_α is

determined directly based on the D specification according to (3.30), simulations may reveal that the intermodulation effects may reduce the dynamic range. Subsequently, further iterations on STEP2 e.g. by increasing b_{rq} may be necessary.

3.8.1 Modulator synthesis example

In the following, use of this design approach is illustrated by a typical example. A digital PWM modulator is synthesized for the full audio bandwidth. More detailed design specifications are given in the table below.

Parameter	Value
f_S	44.1KHz
f_B	20KHz
f_C	< 500KHz
THD	< 0.01% (-80dB)
IMD	< 0.01% (-80dB)
D	≥ 98dB (16bit)

STEP 1:
LADS is chosen as modulation methods due to the simple implementation. In terms of linearity, there are no significant differences between the four LPWM methods as illustrated previously (Fig. 3.25 - Fig. 3.28). The THD specification can be realized with $I=8$ and $S=3$. This leads to a carrier frequency of 352.8KHz, which obeys the specified limit. As seen from the spectral analysis of LADS the IM components will be attenuated to insignificant levels within the base-band even in the worst case with full scale at 20KHz. Note, that the effective oversampling factor with the given parameters is $L = 8.8$.

STEP 2:
Next step is to optimize the parameters for the desired dynamic range. With the given interpolation factor it is appropriate to select $b_{rq} = 8$. The required level to maintain 16 bit performance with 16 bit input is seen directly from Fig. 3.33: $NTF_\alpha \approx -50dB$.

With a higher input resolution the theoretical output dynamic range can be increased to 108dB as also seen from (3.30). With L=8.8 and the given NTF_α requirement the simple FIR NTF of fifth order is chosen. The NTF characteristics are shown in Fig. 3.34.

Verification
The practical verification of these theoretical figures is carried out by simulation with a sequence of simulations of modulator performance that covers all interesting aspects. Fig. 3.37 shows a simulation of modulator output PSD with at 1KHz with $M=0.1$. No distortion can be measured and the dynamic range is $D = 104dB$, without the quantized input applied to the modulator. Also, note the clear characteristics of the noise shaped noise. Further simulation results are shown in Fig. 3.38 to Fig. 3.40. The simulations cover the absolute worst-case situations in terms of harmonic distortion and intermodulation effects. The harmonic distortion is within the desired bounds and the IM effects are only noticeable at full scale 20KHz. However, the levels are far below the specified bounds (IMD <0.002% in Fig. 3.40). In conclusion, the modulator performance is excellent and well beyond what can be reproduced by the power conversion stage.

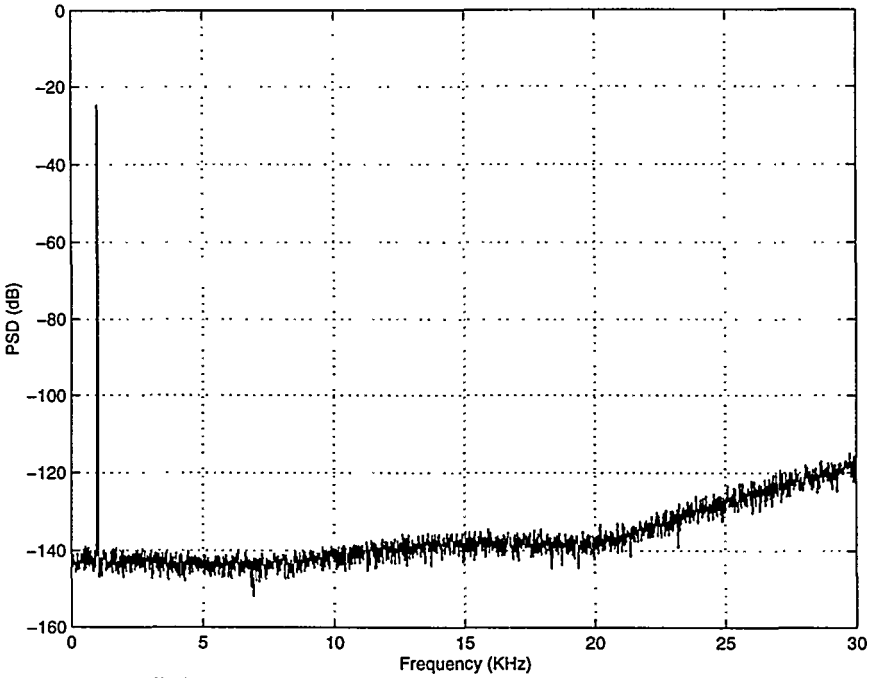


Fig. 3.37 Simulation of digital LPWM modulator output PSD (1KHZ, M=0.1). 16K samples are used in the FFT. THD<0.0001%

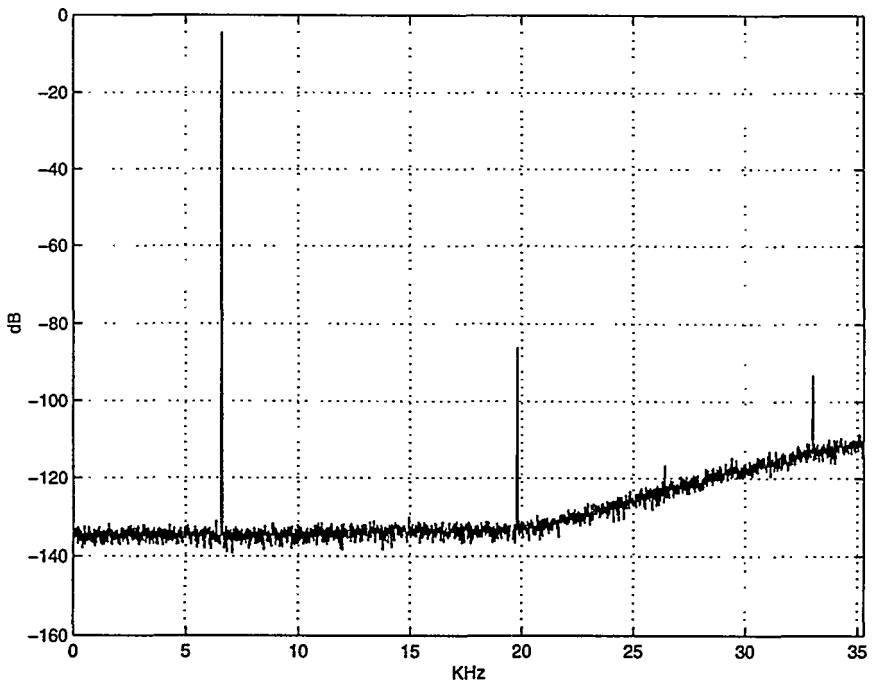


Fig. 3.38 Simulation of digital LPWM modulator output PSD (6.6KHz, M=0.9). 16K samples are used in the FFT. THD=0.009%.

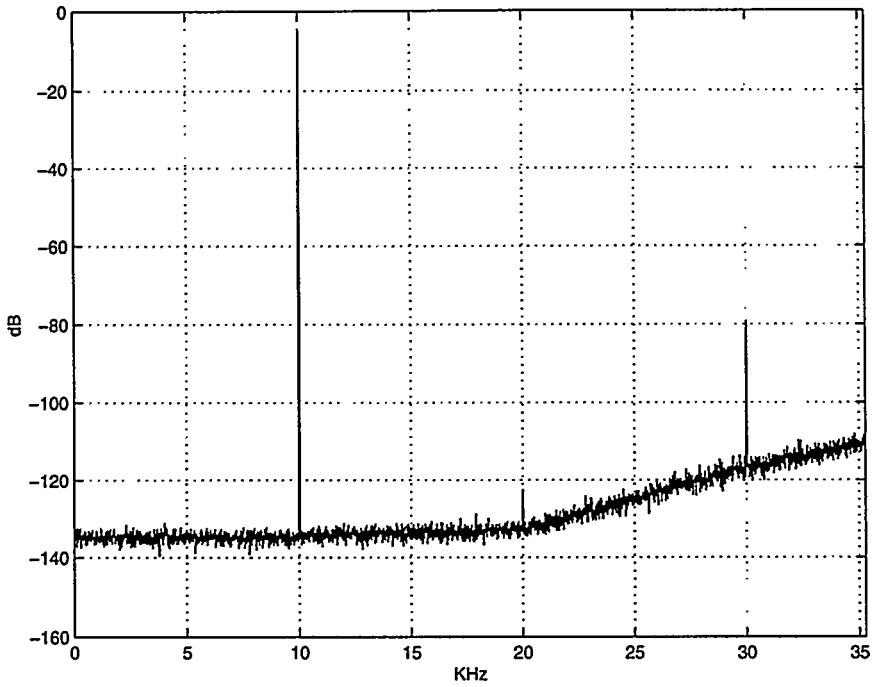


Fig. 3.39 Simulation of digital LPWM modulator output PSD (10KHZ, M=0.9). 16K samples are used in the FFT. THD<0.01%. (3. harmonic falls out of the audio band)

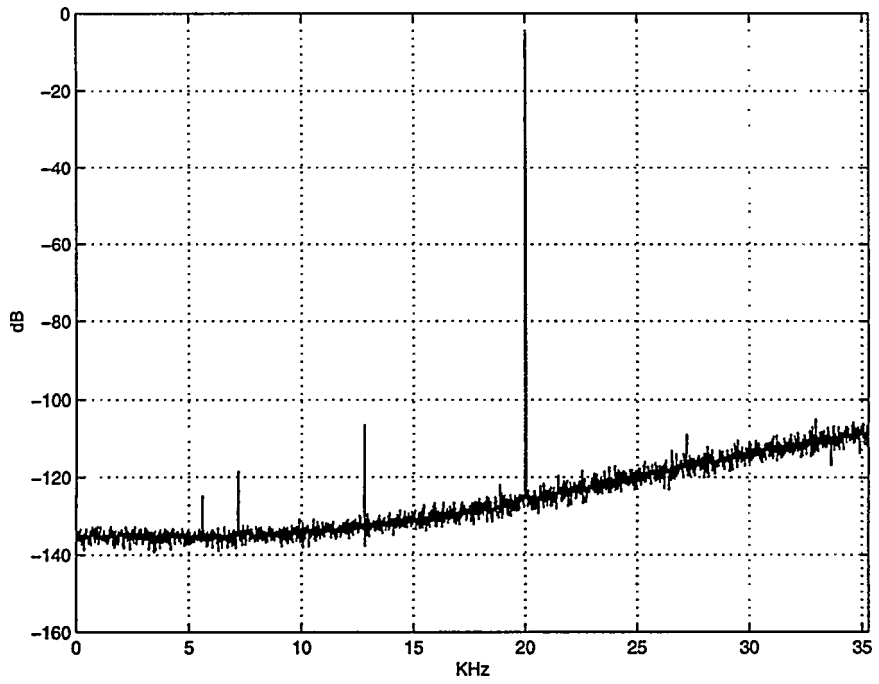


Fig. 3.40 Simulation of digital LPWM modulator output PSD (20KH, M=0.9). 16K samples are used in the FFT. The intermodulation (IMD=0.002%) is well below the specified bounds.

The resulting modulator parameters are summarized below:

Parameter	Value
S	3
I	8
f_c	352.8 kHz
L	8.8
b_{rq}	8
THD_{max}	0.01%
D	*104dB*

3.9 Summary

The chapter has focused on digital modulation methods for digital PMAs, and it was shown how digital modulator realization is significantly different from analog pulse modulation. An initial investigation of "digital" UPWM methods revealed, that digital pulse width modulation is not inherently linear as NPWM. It was concluded that the constraint on frequency ratio imposed by the UPWM non-linearity generally excludes UPWM from PMA applications.

Various enhanced digital PWM methods were addressed that overcome (at least partially) the linearity constraints within UPWM. For implementation of the digital modulator, noise shaping is required such that the HF-output is a combination of both discrete components and noise – another difference to NPWM based analog PMAs. Various methods were reviewed to find the most attractive methods on the performance / complexity scale.

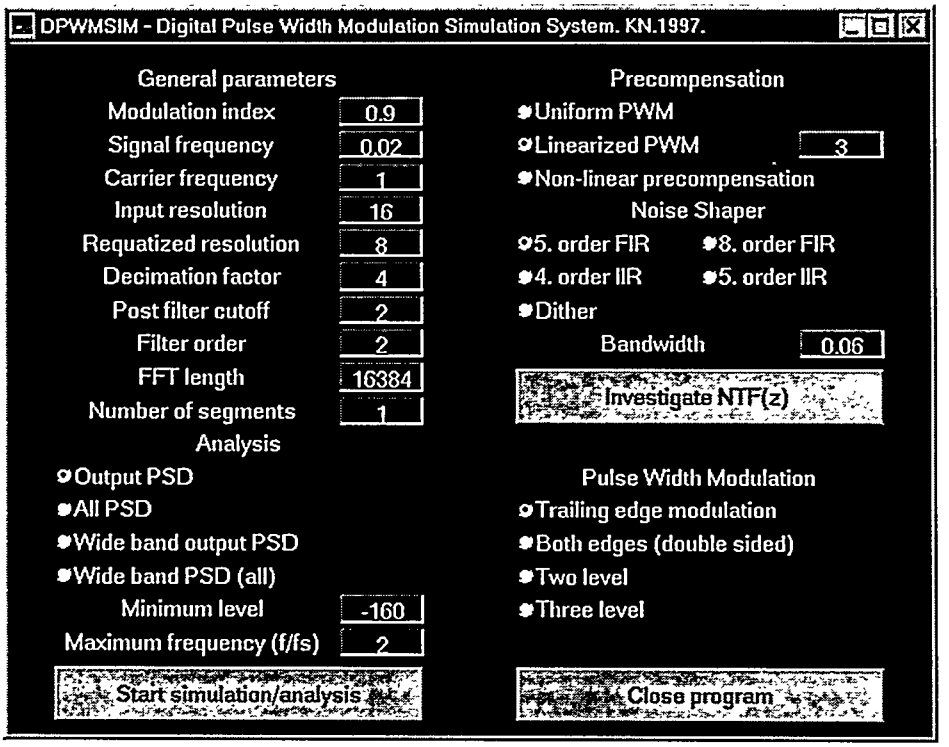
The investigations conclude with a selection of LPWM as one of the most interesting schemes. The four fundamental LPWM schemes were investigated in detail, and it was found that LPWM provides sufficient linearity to match any switching power amplification stage. An interesting conclusion was the similar distortion performance for the four fundamental LPWM methods.

Following, LPWM modulator synthesis was investigated in higher detail, with focus on optimized noise shaping. An optimal modified NTF prototype was specified for digital filter design for LPWM modulators, and methods to realize this modified optimal NTF with low order FIR and IIR filters were devised. Finally, a simple iterative LPWM modulator design methodology was devised based on a separation of linearity and dynamic range demands. A digital LPWM modulator case example verified the very high performance of digital LPWM that can be realized with modest computational complexity.

In conclusion, digital modulators for digital PMAs can be realized with a performance level that is well beyond what can be achieved by the subsequent power conversion stages. Consequently, the digital modulator will not be a limiting factor on digital PMA system performance.

3.9.1 DPWMSIM–A Digital Modulator design toolbox for MATLAB

A GUI controlled digital modulator design toolbox for MATLAB has been developed for systematic and automated LPWM modulator synthesis. The GUI window is shown below.



Based on the primary input parameter specifications the interface gives access:

- Optimal LPWM modulator design using the simple specified design methodology.
- Noise shaping filter investigation and optimization.
- Simulations of various levels of accuracy (FFT length etc.) for flexible investigations.
- Selection between PWM type.
- Various output options.

The software toolbox has been used for the simulation of the modulator example in this chapter.

Part II

Chapter 4

Error Sources

In theory, the power conversion within a switching power amplification stage has 100% efficiency, is in general perfectly linear and does not contribute with other side-effects as noise etc. In practice, the power stage has limited efficiency and can contribute with significant distortion and noise. In addition, the power conversion stage in general determines essential parameters as physical volume, complexity and cost of the complete system. Needles to say, power conversion is the heart of the PMA system.

This chapter is devoted to a very fundamental analysis of the sources of this non-ideal behavior. Essentially, the deviations from the ideal case are caused by physical limitations within the switches, the driver hardware and the filter for demodulation. Power stage topologies that will synthesize the modulation methods discussed in Chapter 3 will be introduced, and the power switching device architecture is investigated in detail to reveal the physical limitations that cause the problems. The low-level non-linear switching characteristics of the output stage are investigated based on attained knowledge on physical imitations. The pulse distortion is categorized into Pulse Timing Errors (PTE) and Pulse Amplitude Errors (PAE), and a fundamental analysis of each error source is undertaken. Finally, specific PSCPWM error sources will be addressed.

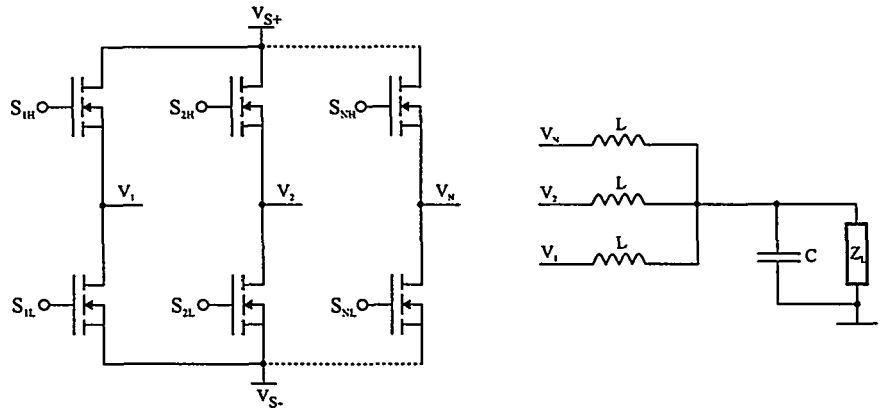


Fig. 4.1 General PSC power stage topology with N-legs (dual supply).

4.1 Power conversion

Power Conversion involves the conversion of a pulse modulated signal to a power pulse modulated signal, realized by power switching devices connected in a structure to transfer energy from a DC power source to the load. The essential concerns for the design of the power conversion stage are linearity, complexity and efficiency. The error sources within the power conversion process will be investigated for the general switching power stage topologies to synthesize PSCPWM and Balanced PSCPWM, shown in Fig. 4.1 and Fig. 4.2. The topologies will henceforth be referenced to as PSC and BPSC, respectively.

Over the years, several topologies have been used in DC/AC converter and PMA applications. The general trend has been to use a simple switching leg [At83], [At78] but bridge configurations have also been investigated [Ha91], [Ni97d], and lately the general PSCPWM method has been introduced the author [Ni97b]. As far as general DC-AC conversion is concerned, a much wider range of power conversion topologies have been presented, recently with focus on various multi-level converters [Ro95], [La95a], [La96a], [Ca92]. Despite the vital influence the power stage has on all system parameters, no fundamental analysis of the error sources within the power conversion process has been found in previous literature. Attwood [At83] discusses the effects of non-idealities in general terms, with a two-transistor output stage. Erickson and Middlebrook [Er82] also analyze distortion mechanisms in switching amplifier output stages, but the stages are based on bipolar technology. The power transistor technology has evolved over the past decade and switching devices are now clearly more ideal suited for switching power stages in audio applications. However, the fundamental sources of non-ideal behavior remain unchanged and a fundamental analysis is required.

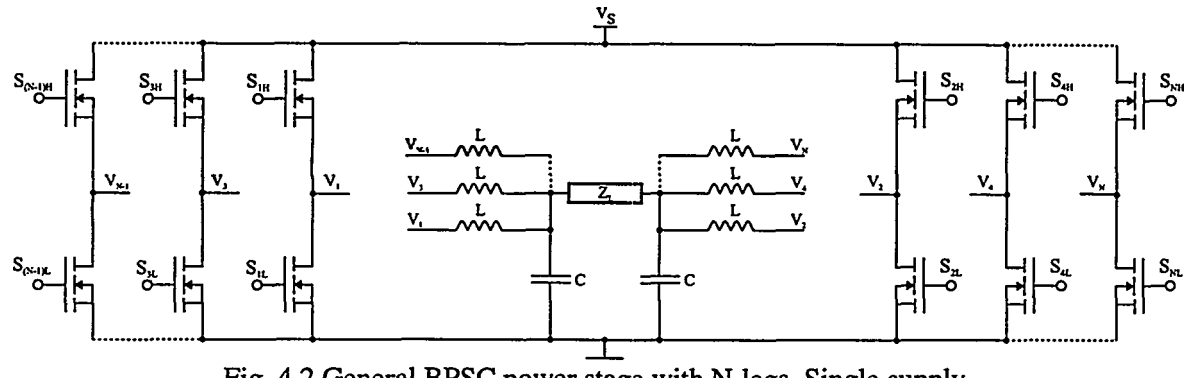


Fig. 4.2 General BPSC power stage with N-legs. Single supply.

There are additional error sources relating to the non-ideal modulation and non-ideal demodulation. The demodulation filter errors may introduce further distortion, since magnetic core materials are not ideal. In addition, the filter increases the total output impedance. Accordingly, changes in load impedance will distort the frequency response. It should be emphasized, that the non-ideal behavior of both the modulator, switching power stage and the filter for demodulation are the very reason for the extensive interest for control systems in Part III of the thesis. The investigations in this chapter thus serve as an essential foundation for the development of control systems. First, the focus turns to the fundamental components that cause the non-ideal behavior – the switches.

4.2 Switching devices

The ideal switch operates is fully shorted when ON, represents an infinite impedance when OFF and has infinitely fast transitions between states. Obviously, these requirements can never be met in practice. Within the power range of audio power amplification, Bipolar technology (BJT), MOSFET technology and IGBT (Insulated Gate Bipolar Transistor) switch technology are potential candidates for optimal switching power conversion. The choice between the devices will depend on application. However, the vertical structure DMOS Power MOSFET has the most attractive parameter set:

- The MOSFET is a majority carrier component. This minimizes the switching times.
- The resistive nature of the device when turned ON provides good linearity and a low output impedance which is specifically interesting in audio applications.
- MOSFET's are available up to 500V with good characteristics as low ON impedance and fast switching.

The BJT is a minority carrier component in which injected minority carriers recombine with majority carriers, which limits the device speed. Furthermore, the low input impedance of the BJT requires somewhat complex driver circuitry. Both factors compromise both efficiency and linearity. The IGBT, being a mixture of the BJT and the MOSFET, is preferable in comparison to the BJT since it is voltage controlled. However, the turn off characteristics of IGBTs and the diode forward drop when turned ON with compromise both efficiency and linearity, unless very high output power is required. To conclude, The MOSFET is much closer to the ideal switch than the BJT and IGBT in "lower" power applications as audio (<2KW). The following investigations on power stage synthesis and analysis will therefore exclusively based on the Power MOSFET.

4.2.1 The vertical $n^+pn^-n^+$ Power MOSFET architecture

A fundamental understanding of physics in the Power MOSFET architecture is necessary to understand the inevitable compromises between e.g. breakdown voltage, parasitic capacitance, channel ON resistance etc. that arise due the inherent physical limitations of this preferred switching device. Fig. 4.3 shows the basic N-channel Power MOSFET structure, which consists of many parallel connected cells. The device structure consists of 4 vertically arranged layers $n^+ p n^- n^+$. The large doping in the two n^+ end layers results in a low resistance (no potential barrier) between the Drain and Source metal connections and the semiconductor material. A positive voltage on the gate terminal creates an electric field in the channel region below the gate. The electric charge in the gate simply causes a conversion the *p*-region to an *n*-type region. This *surface inversion* phenomenon allows current to flow from drain to source though n-type material. This is a clear difference to the BJT, which always remains an *n-p-n* characteristic. The gate is electrically isolated by a

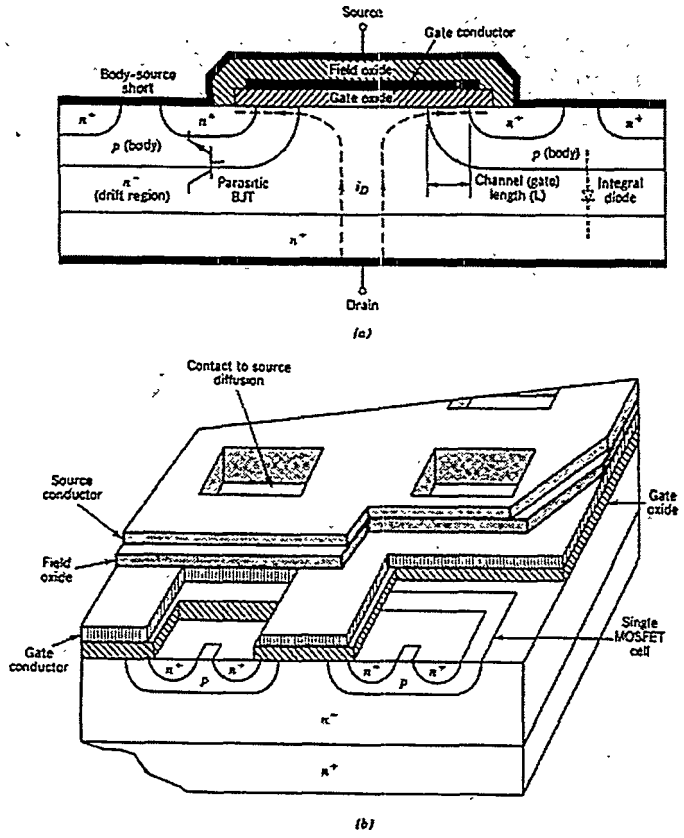


Fig. 4.3 N-channel enhancement MOSFET structure with 4 four vertically arranged layers ($n^+ p n^- n^+$).

layer of SiO_2. By virtue of this, a MOSFET is a high-input impedance voltage controlled device. Furthermore, since the device is a majority carrier switching is fast.

A byproduct of the vertical four-layer structure is a parasitic BJT caused by the *n-p-n* layers as seen from Fig. 4.3. To minimize the chance for the BJT to turn ON, the *p*-type body region is shorted to the *n*-type source region. Due to the short circuit, a parasitic diode is formed between source and drain as illustrated in Fig. 4.3. The diode is the base-collector diode of the BJT. The n^- or *drift* region determines the device breakdown voltage V_{BD}. When breakdown is reached, the voltage will appear to remain essentially constant while the current increases dramatically being limited only by the external circuit. This is known as *avalanche* mode [Mo95]. This unfortunate combination of large currents and large voltages leads to excessive power dissipation that can destroy the device, i.e. avalanche should be avoided.

Fig. 4.5 shows the four quadrant I-V characteristics of the power MOSFET. Dependent on the bias voltage V_{GS} between gate and sources the device can be considered a pure resistance over a certain current range. Fig. 4.4 shows the power diode switching characteristics. An important side effect of the intrinsic power diode is the *reverse recovery* phenomenon. During the reverse recovery time t_{rr} the reverse recovery charge Q_{rr} is swept out by the reverse current with a peak value I_{rr}. Approximate relationships between these parameters are [Mo95]:

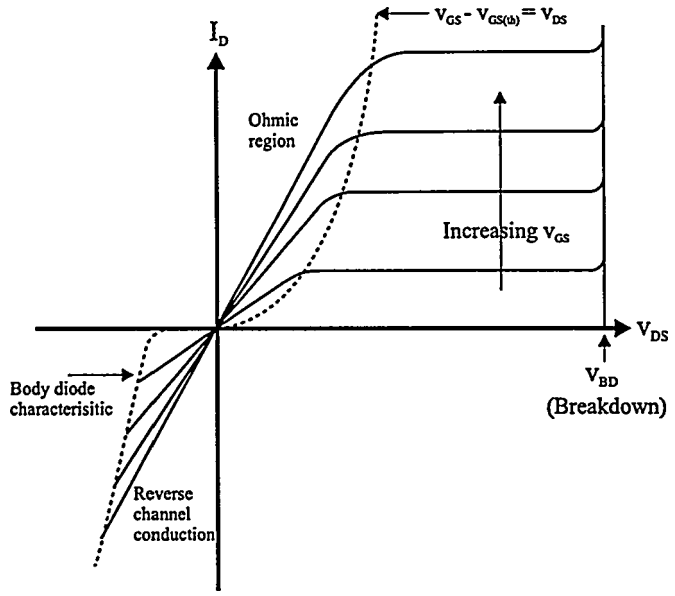


Fig. 4.5 Four quadrant N-channal Power MOSFET I-V characteristics.

$$t_{rr} \approx 2.8 \cdot 10^{-6} V_{BD} \sqrt{\frac{I_F}{di_R/dt}} \qquad I_{rr} \approx 2.8 \cdot 10^{-6} V_{BD} \sqrt{I_F di_R/dt} \tag{4.1}$$

Reverse recovery problems increase with increasing voltage, current and speed of the switching transitions. Fig. 4.6 shows circuit models for the Power MOSFET that will be used for the analysis of switching characteristics (the intrinsic body diode is not shown). C_{GD} and C_{DS} are highly dependent on the drain-source voltage.

4.3 Switching leg characteristics

The switching characteristics of a single switching leg will be analyzed in the following. The analysis is carried out under the assumption that the output current I_L and power supply level V_S are constant. The effects of reverse recovery will not be considered at this initial point. A complete switching cycle is investigated, consisting of two immediately following level shifts on the output waveform. This is not a realistic situation except at the edge of over-modulation, but it results in a fundamental understanding in the switching characteristics. Fig. 4.7 shows all essential signals during the complete cycle. The circuits diagrams on top indicated the action of the current period during the switching cycle, i.e.

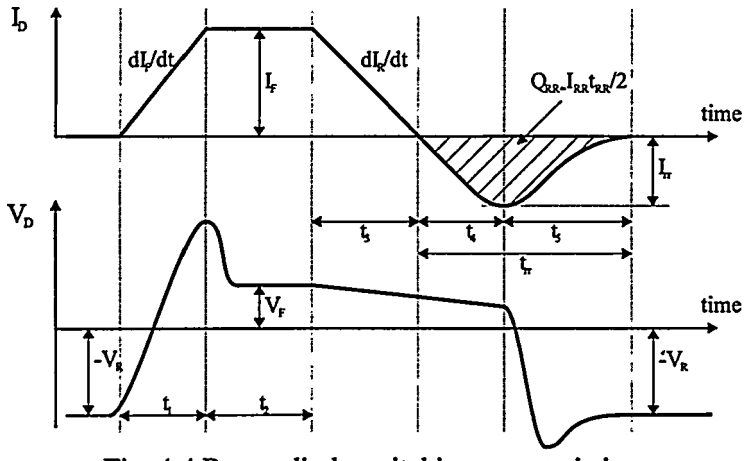


Fig. 4.4 Power diode switching caracteristics.

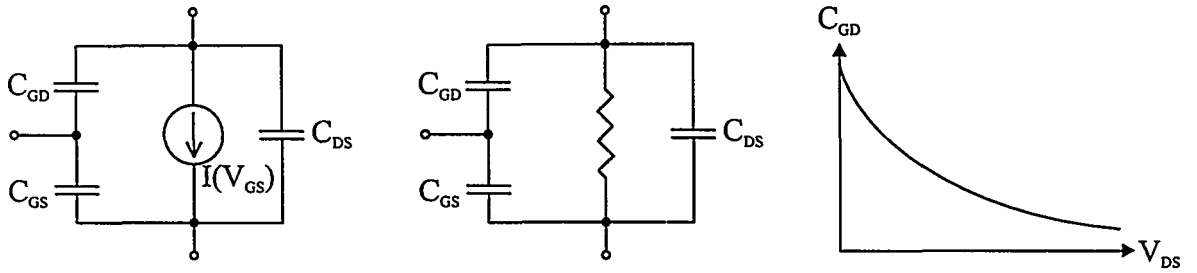


Fig. 4.6 Power MOSFET model for the analysis of switching characteristics.

the current commutation is from the fully ON "high" switch S_H to the diode in the "low" switch S_L as a consequence of the turn-off of S_H etc. A detailed description of the actions at each individual time step is given in Table 4.1. Ideally, the switching on v_p should take place at the instant that the S_H gate turn-off is initiated according to the shape of the ideal output pulse waveform. The resulting output v_p error waveforms reveals that there are several contributions to both pulse delay and pulse distortion on both the falling and rising edge. The falling transition on the output pulse is *turn-off controlled* in that the output current commutation to the diode in S_L will cause the transition. The following turn-on of S_L is a Zero Voltage Switching (ZVS) transition characterized by that the drain to source voltage of S_L is zero during the complete switching cycle. This causes a very fast switching action, where only C_{GS} has to be charged as shown in Fig. 4.7. To conclude, the turn-off of S_H and turn-on of S_L results in the following distortion on the output pulse waveform:

- A turn-off delay t_{df}, which delays the transition.
- A non-linear transition characteristic of finite duration caused by C_{GD}.

The low-high transition on is *turn-on controlled* i.e. the turn-on of S_H eventually causes the current commutation from the diode in S_L to the channel of S_H. The turn-off of S_L and turn-on of S_H results in the following distortion on the output pulse waveform v_p:

- A blanking delay t_d, that delays the transition.
- A turn-on delay t_{dr} from the initiation of the turn-on until the actual transition.
- A non-linear switching characteristic of finite duration caused by C_{GD}.

The following parameters have important influence on the switching characteristics and error sources:

- R_G strongly influences the time constants t_{dr}, t_r, t_{df} and t_f. From the perspective of minimizing distortion, R_G should be as as small as possible.
- C_{GD} is the determining parasitic capacitance on t_r and t_f, i.e. seen isolated the C_{GD} should be as small as possible.
- C_{GS} is the determining parasitic capacitance on t_{dr} and t_{df}, i.e. it should be as small as possible, again seen isolated.
- V_G, $V_{GS,th}$ and $V_{GS}(I_L)$ also influences t_{dr}, t_r, t_{df} and t_f.

Fig. 4.8 shows the switching characteristics with a negative output current. Clearly, the switching characteristics change significantly, i.e. the falling edge on v_p now becomes turn-on controlled whereas the rising edge on v_p is turn-off controlled. This dependence on current polarity causes harmonic distortion.

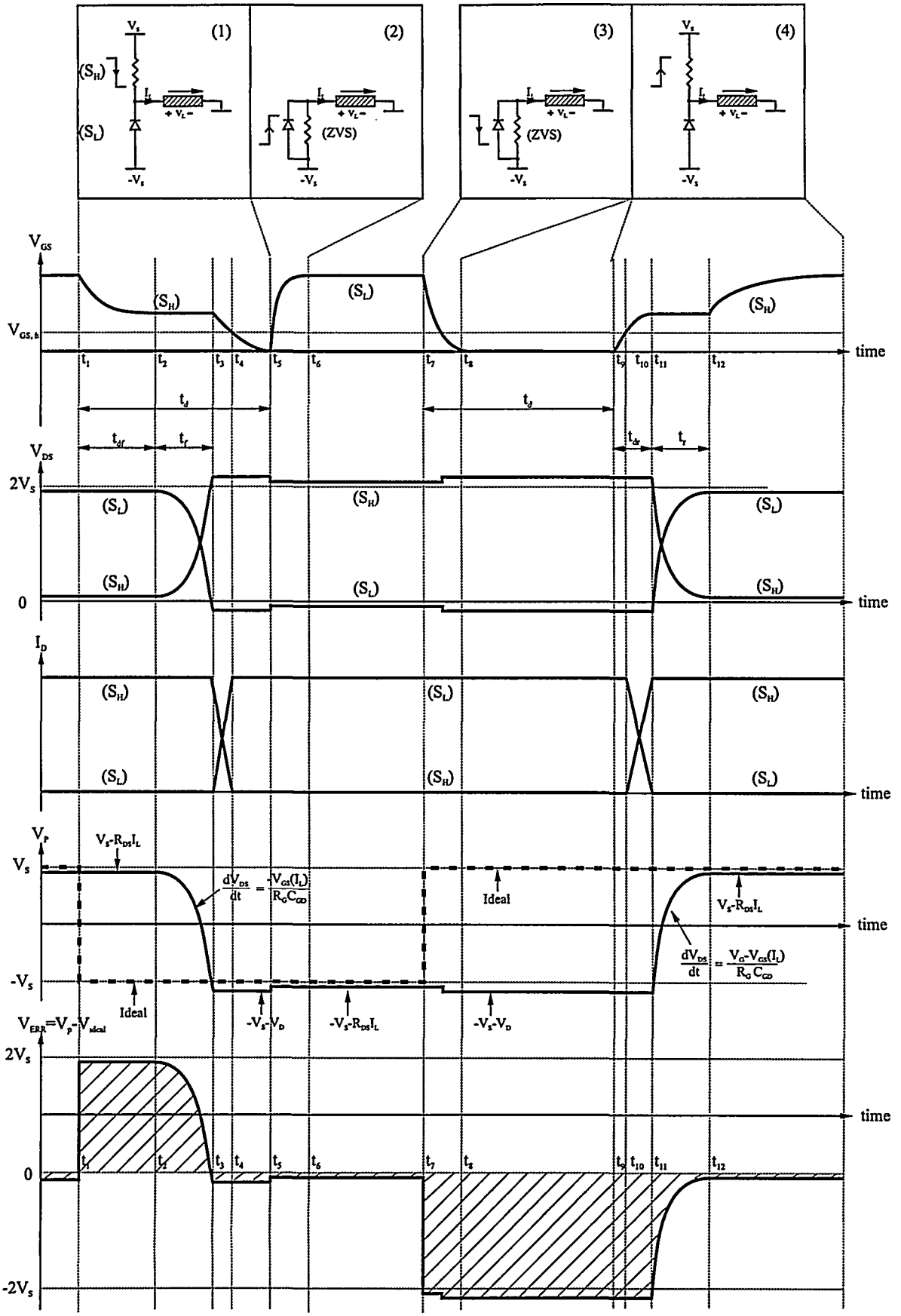


Fig. 4.7 Detailed investigated of switching characteristics in a switching leg with constant positive output current I_L. Both falling and rising transitions on the output v_p are investigated.

Time	Action
t_1	The level shift is initiated by a low level on the gate (1). The gate capacitance C_{GS} causes a turn off delay t_{df}.
t_2	v_{GS} is trapped at $v_{GS}(I_L)$ and the gate current therefore exclusively runs in C_{DG} in order to discharge the capacitor. This leads to the following dv/dt over C_{DG}, and the output pulse waveform: $$i_{G1} = -\frac{v_{GS}(I_L)}{R_G} \Rightarrow$$ $$\frac{dv_{DG1}}{dt} = \frac{dv_{DS1}}{dt} = \frac{-v_{GS}(I_L)}{R_G C_{GD}}$$
t_3	When v_p gets sufficiently low, current commutation to the diode in S_L is initiated. This holds v_p constant whereby v_{GS} is forced down towards zero.
t_4	When $v_{GS} = v_{GS,th}$, the complete load current is running in the diode in S_L.
t_5	After a blanking period t_d, the turn-on of S_L is initiated by a high gate voltage. Since the load current is already running in S_L's body diode, the switching is dramatically different from the 'normal' turn on: • Since $v_{DS} = v_{DG} = 0$ before turn-on, much less charge has to be moved. Following, the switching is much faster. • The shift only consists of moving the current inside S_L from the body diode to the channel, and is therefore not directly visible outside the MOSFET. • The Zero Voltage switching (ZVS) means that the switch will not enter the active region i.e. the switching is nearly loss-less.
t_6	The load current is running in the channel of S_L, meaning that $v_p = -R_{DS} I_L$
t_7	The high transition of the output is initiated by S_L off. Due to the current polarity, the current will shift to S_L's own body diode, i.e. the switching happens very fast and nearly loss-less, similar to the zero voltage turn on.
t_8	The load current is running in S_L's body diode, so $v_p = -V_D(I_L)$, where $-V_D(I_L)$ is the diode forward voltage.
t_9	After a blanking period t_d, the turn-on of S_H is initiated. $v_p = V_D(I_L)$
t_{10}	$v_{GS} = v_{GS,th}$, so S_H enters the active region and starts to take current. The diode of S_L holds the output voltage constant: $v_p = -V_D(I_L)$
t_{11}	The load current is now running in S_H. The gate current forces a the drain-source voltage over S_H to follow: $$i_G = \frac{V_G - v_{GS}(I_L)}{R_G} \Rightarrow$$ $$\frac{dv_{DG}}{dt} = \frac{dv_{DS}}{dt} = \frac{V_G - v_{GS}(I_L)}{R_G C_{GD}}$$
t_{12}	The switch S_H enters the ohmic region, when v_{DS} gets sufficiently low. This allows v_{GS} to increase to the asymptotic value. Accordingly, $v_p = V_S - R_{DS} I_L$

Table 4.1 Essential actions within the falling and rising transitions of v_p with a positive current.

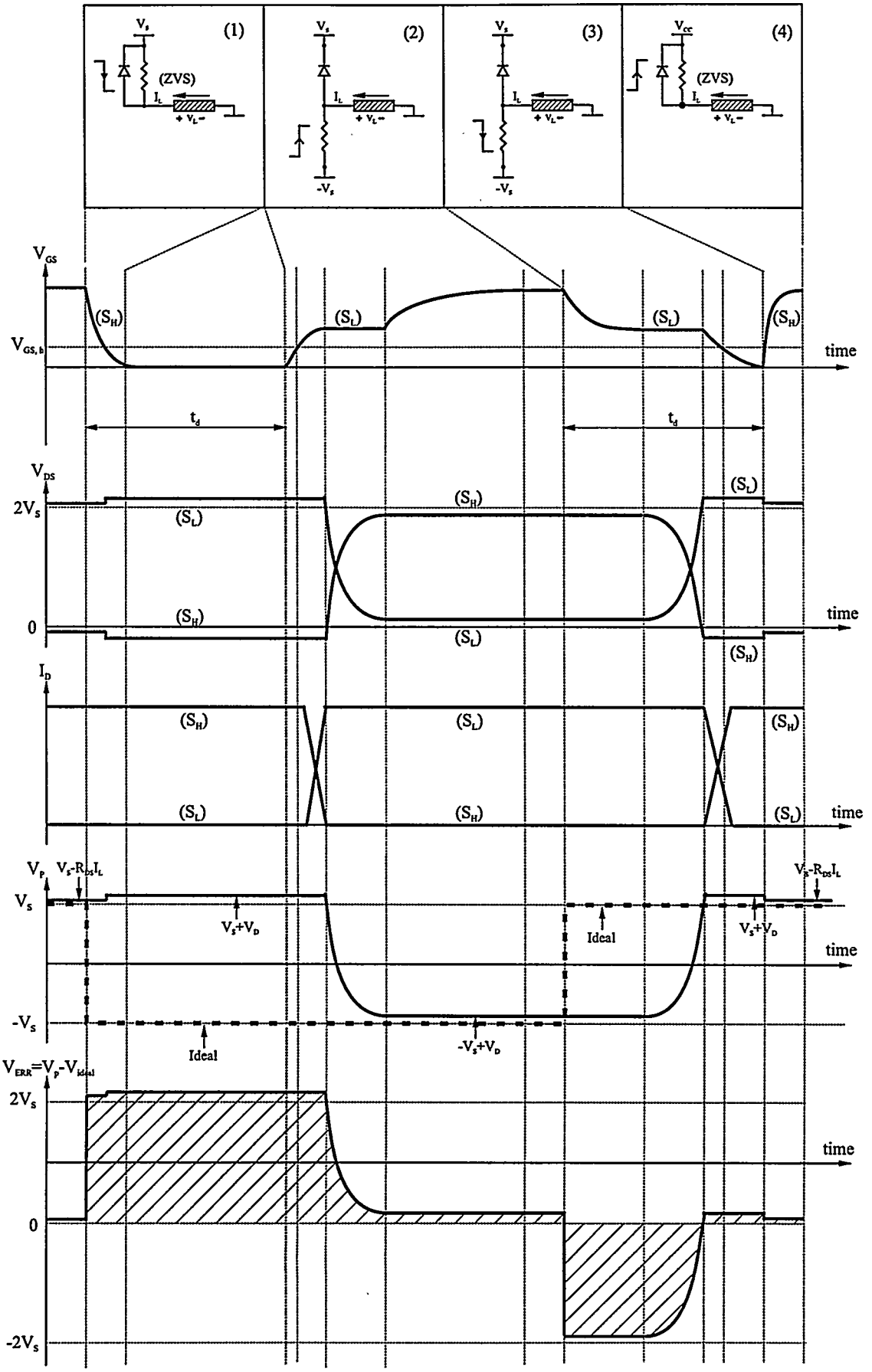


Fig. 4.8 Detailed investigated of switching characteristics in a switching leg with constant *negative* output current. Both falling and rising transitions on v_p are investigated.

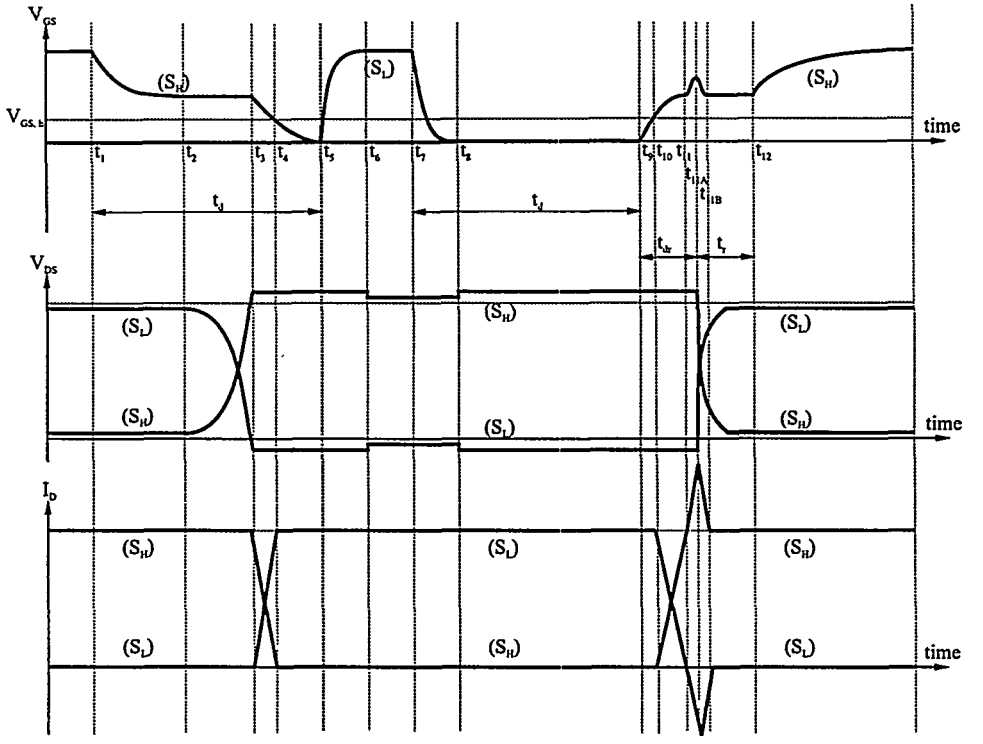


Fig. 4.9 The effects of body diode reverse recovery on the switching characteristics.

4.3.1 Reverse recovery effects

The reverse recovery effect was left out of the investigations above, since the effect can be nearly eliminated by adding anti-parallel Shottky diodes. The forward voltage of a Shottky diode is generally lower than that of the *p-n* junction of the body diode, i.e. the Shottky diode will shunt the body diode. In many applications however, reverse recovery will only marginally affect system performance. Fig. 4.9 illustrates the changes on the PWM waveform when the reverse recovery effect is considered. At t_{11} when the current in the low switch S_L approaches zero, the finite reverse recovery time of diode in S_H means that S_H will represent a finite (small) impedance in a short period after t_{11}. Since S_L is turned ON, a shoot though like current is inevitable in this period peaking at t_{11A}. A high current will help to empty the recovery charge and the duration for this high current through both switching devices will therefore in general be short. At t_{11A} all recovery charge has been pulled out of the diode in S_2 and the diode effectively shunts off within a short period causing a very high *dv/dt* on v_p. As illustrated in Fig. 4.9, the error on the output waveform will not be influenced considerably by the reverse recovery effect. A more serious concern is the trigging of resonance circuits by the high *di/dt* caused by reverse recovery. Furthermore, the high currents that shoot though the two opposing devices can will cause power loss and hence decrease the efficiency.

4.4 Categorization of error sources

The actual effect of each of these elements will be investigated in detail, both by simulation and by analytic approaches. It is expedient to divide the error sources in to pulse timing errors (PTE) and pulse amplitude errors (PAE). Pulse Timing Errors arise from:

- The turn-on and turn-off delays t_{dr} and t_{df}.
- The blanking delay t_d.

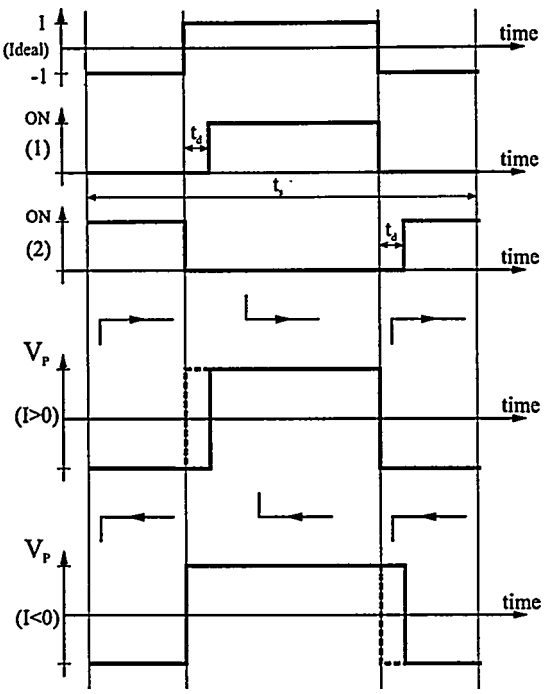


Fig. 4.10 Blanking delay effects in switching leg.

- The finite rise- and fall-times t_r and t_f.

Pulse Amplitude Errors (PAE) essentially arise from:
- Perturbations on the power supply that feeds the switching power stage.
- Finite impedance for the power switches.
- High frequency resonant transients on the resulting pulse power signals.

Since PSCPWM switching waveforms are generated by superposition of the signals in a simple switching leg, the error contributions from each different switching leg will also superpose. It is possible to estimate the errors from the investigations of a simple switching leg. Obviously, errors correlated with the modulating signal will generate distortion where as errors that are non-correlated will generate noise in the general PSC and BPSC power stages.

4.5 Pulse Timing Errors (PTE) analysis

Pulse timing errors are now subjected to a more fundamental analysis. The investigations are founded on the synthesized switching waveforms above in the switching leg. Each error source are analyzed individually.

4.5.1 Blanking effects

The turn on in a switching leg has to be delayed relative to the turn-off of the other switch in order to prevent cross conduction. Fig. 4.10 illustrates the consequences of a blanking delay t_d applied to the switching leg. The bus voltage V_s is assumed unity. The blanking delay causes an error voltage on the power stage output, which is correlated with the load current. In the case of a sinusoidal output current, this effect will cause distortion. The effective error is estimated by averaging the error signal within the switching cycle with period $t_c = f_c^{-1}$:

$$v_e = \begin{cases} \frac{-2t_d}{t_c} & (I_L > 0) \\ \frac{2t_d}{t_c} & (I_L < 0) \end{cases} \tag{4.2}$$

With a pure sinusoidal output current, this average error will be a squarewave resulting in uneven harmonic distortion. On the output, the error will be represented in a filtered version. Neglecting, that the demodulation filter will attenuate higher harmonics the Fourier components of the error signal can be expressed as:

$$A_d(m) = -2\frac{t_d}{t_c}\frac{\sin(m\frac{\pi}{2})}{m\frac{\pi}{2}} \tag{4.3}$$

With V_s assumed unity we arrive at the following general expression of total harmonic distortion vs. modulation index M and *blanking delay factor* α_d*:*

$$THD_d(M,\alpha_d) \approx \frac{\sqrt{\sum_{i=2}^{N_{max}} \left[2\alpha_d \frac{\sin(i\frac{\pi}{2})}{i\frac{\pi}{2}} \right]^2}}{M - \alpha_d \frac{4}{\pi}} \tag{4.4}$$

The blanking delay factor is defined as:

$$\alpha_d = \frac{t_d}{t_c} \tag{4.5}$$

Realistic load current

In a practical implementation of the switching leg the load current can not be considered purely sinusoidal. The load current is superposed by a ripple current with an amplitude dependent of several parameters, e.g. V_S and filter inductor size. Referring to Fig. 4.10, the general requirement for a blanking delay is that:

The current commuting to the switch at turn-on is positive referred to that specific device.

However, a low modulation depth this situation *never* occurs since the current will be *negative* relative to the device after turn-on. This is a direct consequence of the power stage switching operation and an inductive load. The condition for *blanking free* operation is:

$$\hat{I}_L < \hat{I}_T \tag{4.6}$$

where $\hat{I}_L$ and $\hat{I}_T$ represent the peak values of the output current (LF) and the ripple current. $\hat{I}_T$ will be represented by the value at zero modulation depth in the following. This is valid since the effects of the ripple current appear at low output currents. With a sinusoidal output current, the angle at which $\hat{I}_L$ will exceed the ripple component:

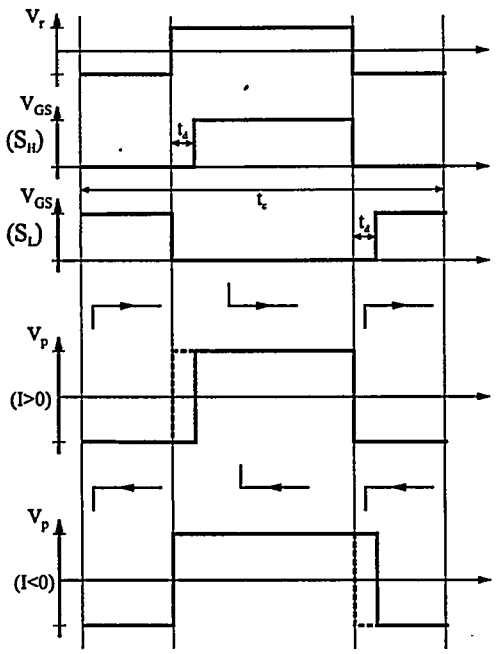


Fig. 4.11 The effects of ripple current on blanking delay error.

$$\theta = \sin\left(\frac{\hat{I}_T}{\hat{I}_L / M}\right) \tag{4.7}$$

Where the denominator represents the maximal peak output current corresponding to full modulation. Correspondingly, the *ripple current factor* is defined as:

$$\alpha_I = \frac{\hat{I}_T}{\hat{I}_L / M} \tag{4.8}$$

As opposed to error pulses during the complete period, error pulses will only be present over a fraction Δ of the period as shown in Fig. 4.11. This fraction of the period is found to be:

$$\Delta(\alpha_I) = \begin{cases} 0 & I_L \le I_T \\ \dfrac{\frac{\pi}{2} - \sin(\alpha_I)}{\frac{\pi}{2}} & I_L > \hat{I}_T \end{cases} \tag{4.9}$$

This fraction directly relates to the average error on the output as:

$$v_e(\Delta) = \begin{cases} -2\alpha_d \Delta(\alpha_I) & (\hat{I}_L > 0) \\ 2\alpha_d \Delta(\alpha_I) & (\hat{I}_L < 0) \end{cases} \tag{4.10}$$

The factor should be seen as an amplitude correction factor on the error voltage v_e. The resulting modified expression for THD can now be written:

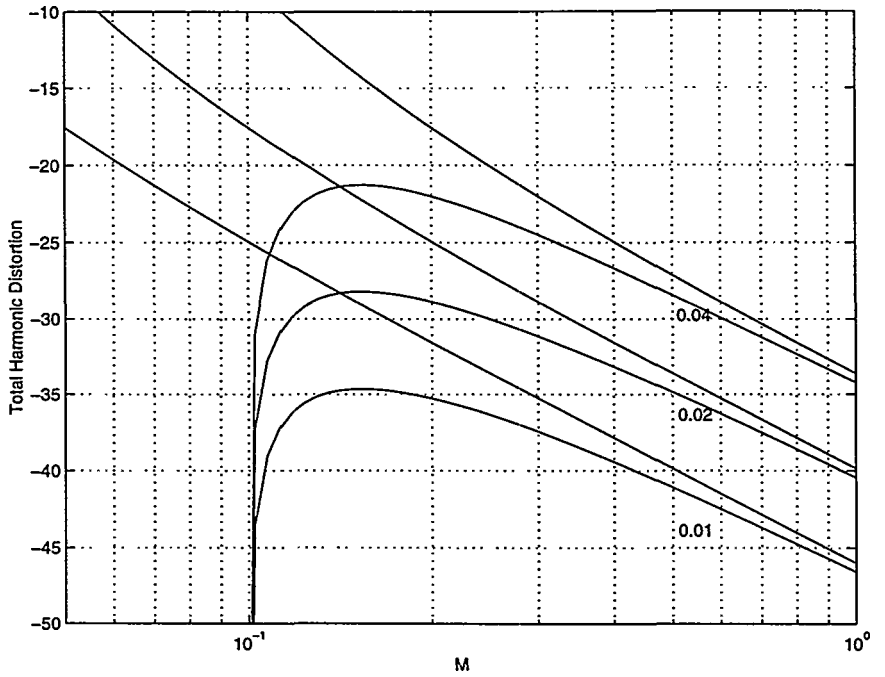


Fig. 4.12 Parametric investigation of THD vs. M and the blanking delay factor α_d with and without consideration of the ripple current. α_d = (0.01, 0.02, 0.04). The ripple current factor α_I =0.1. The ripple current dramatically changes THD at lower modulation index.

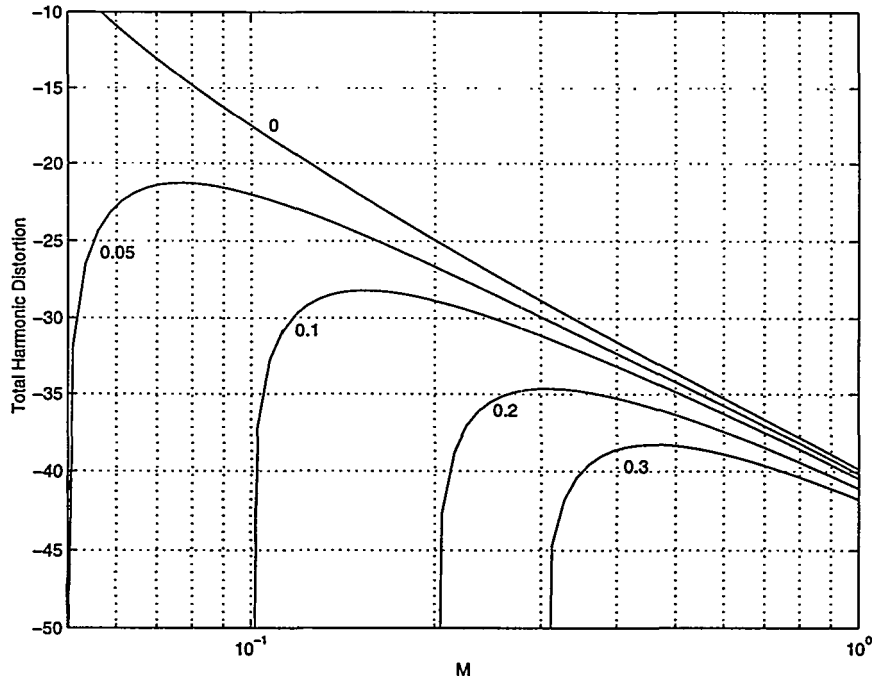


Fig. 4.13 Parametric investigation of THD vs. M and the ripple current factor α_I. α_I =(0, 0.05, 0.1, 0.2 and 0.3). The blanking delay factor is $\alpha_d = 0.02$.

$$THD_d(M,\alpha_d,\alpha_I) \approx \frac{\Delta(\alpha_I)\sqrt{\sum_{i=2}^{N_{max}}\left[2\alpha_d \frac{\sin(i\frac{\pi}{2})}{i\frac{\pi}{2}}\right]^2}}{M-\alpha_d\frac{4}{\pi}\Delta(\alpha_I)} \tag{4.11}$$

Fig. 4.12 and Fig. 4.13 shows a parametric investigation of both (4.4) and (4.11), where the two essential parameters α_d and α_I are varied within the range of practical values. Clearly, the harmonic distortion is unacceptable within the complete range of operation. From this simple analysis several facts are concluded:

- Blanking introduces a linear error as the most significant contribution. However, linear errors are generally less significant compared with non-linear errors.
- Blanking introduces significant and primarily uneven harmonic distortion, which is linearly dependent on V_S and the blanking delay factor α_d.
- The ripple current dramatically changes the effects of blanking delay. Instead of converging towards infinity, THD converges towards zero as the modulation index decreases.

In conclusion, satisfying linearity requires very low and unrealistic blanking delay factors, e.g. even with a low blanking delay factor as 0.01, THD is –35dB at M=0.15. However, a low blanking delay will compromise other factors as efficiency, i.e. compensation for the blanking delay error source is considered essential to reach the performance goals.

Generalization of blanking delay investigations

The investigations of blanking delay are now generalized to the general PSC and BPSC power stage topologies. Due to the level of errors that are generated by the blanking delay it is essential to investigate if other modulation methods and power stage topologies will be less sensitive to this specific error source.

For the simple H-bridge implementing two-level modulation, it is trivial to show that the effects of blanking will be identical to the switching leg. For a slightly more complicated modulation method as NBDD the effects of blanking are shown in Fig. 4.14. There are four states within a complete cycle. The distortion caused by blanking is not dependent upon the zero level generation or the polarity of the output pulse. The waveform causes an error voltage on the power stage output, which is correlated with the load current and there are *two* contributions to the average error in each switching cycle. However, each contribution has *half* the voltage level compared to the switching leg, i.e. the results of the error source will be the same when the error is averaged over a switching leg.

With multi-level switching topologies based on switching legs, the characteristic of the error source is the same. However, N error source generators superpose in the general PSC and BPSC switching power stages. In conclusion, the blanking delay is a universal error source for all power stages that include a switching leg. The ripple current significantly reduces the effects of the error source, however blanking delay factors below what is generally practically possible are needed for sufficiently low THD.

4.5.2 Other PAE error sources

From the detailed investigations of the switching leg characteristics, other error sources that can be categorized as PAE were observed.

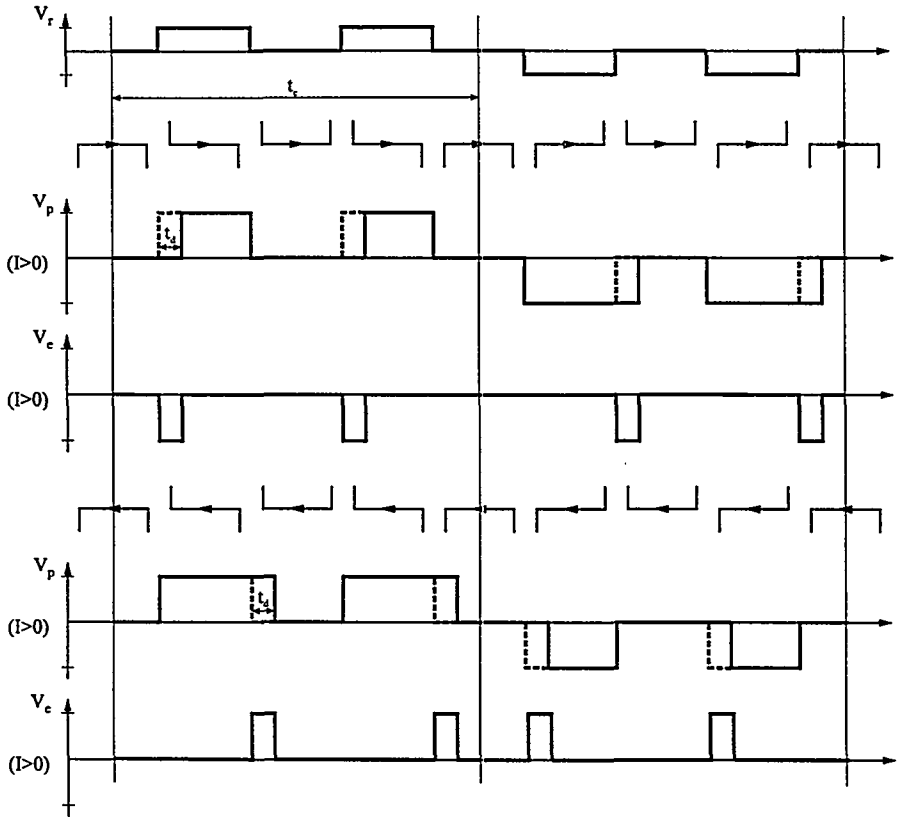


Fig. 4.14 Blanking in a bridge with NBDD PWM.

Delay distortion

The delay distortion occurs due to the inevitable delays from the initiation of a level transition by turn-off or turn-on until that output level transition is actually initiated. This is indicated by the shaded error pulses of duration t_{df} and t_{dr} referring to delay before fall and the delay before rise, respectively. We have:

$$t_{df} = \begin{cases} R_G C_{iss} \ln\left(\dfrac{V_G}{V_G - v_{GS,th} - \dfrac{I_L}{g_{fs}}}\right) & I_L > 0 \\ R_G C_{iss} \ln\dfrac{v_{GS,th} + \dfrac{I_L}{g_{fs}}}{v_{GS,th}} & I_L < 0 \end{cases} \tag{4.12}$$

$$t_{dr} = \begin{cases} R_G C_{iss} \ln\dfrac{V_G}{V_G - v_{GS,th} - \dfrac{I_L}{g_{fs}}} & I_L < 0 \\ R_G C_{iss} \ln\dfrac{v_{GS,th} + \dfrac{I_L}{g_{fs}}}{v_{GS,th}} & I_L > 0 \end{cases} \tag{4.13}$$

The two switching devices are assumed to be identical, with an input capacitance $C_{iss} = C_{GS} + C_{GD}$. The forward transconductance g_{fs} is assumed constant. The multi-

parameter dependency makes it difficult to accurately estimate the resulting differential time error:

$$\Delta t_{drf} = t_{df} - t_{dr} \tag{4.14}$$

However, with the present stage of switching technology it is possible to reduce the absolute delays to below 10ns and the differential delay to insignificant levels without compromising other aspects. This holds even for high power systems. The approach to minimize delay distortion is to minimize R_G and optimize V_G such as to cancel the delays. Generally, the transconductance of the power MOSFET is so high, that the inherent current modulation of t_{df} and t_{dr} will be negligible compared to other error sources. Consequently, delay distortion is not a limiting factor in switching output stages.

Rise-and fall times

Finite rise- and fall times can be categorized as an error source that affects pulse timing errors and pulse amplitude. The output rise and fall times will depend upon if the current is positive or negative i.e. if the transition is determined by a turn-off or turn-on:

$$t_f = \begin{cases} \dfrac{Q_{GD}}{\dfrac{v_{GS,th}+\dfrac{I_L}{g_{fs}}}{R_G}} & (I_L > 0) \\ \dfrac{Q_{GD}}{\dfrac{V_G-(v_{GS,th}+\dfrac{I_L}{g_{fs}})}{R_G}} & (I_L < 0) \end{cases} \tag{4.15}$$

$$t_r = \begin{cases} \dfrac{Q_{GD}}{\dfrac{v_{GS,th}+\dfrac{I_L}{g_{fs}}}{R_G}} & (I_L < 0) \\ \dfrac{Q_{GD}}{\dfrac{V_G-(v_{GS,th}+\dfrac{I_L}{g_{fs}})}{R_G}} & (I_L > 0) \end{cases} \tag{4.16}$$

Q_{GD} is the necessary gate charge for the drain-source voltage transition. The non-linear characteristic of C_{GD}, leads to a non-linear switching characteristic. However, assuming for simplicity that the rise and fall times are equal and that the switching characteristic is linear, the resulting pulse waveform can be interpreted as a folding between the ideal waveform with a very small pulse. Consequently, the output is shaped by the distorted as:

$$\tilde{V}_P(f) = V_P(f) \cdot H_{rs}(f) \tag{4.17}$$

Where the distorting transfer function is:

$$H_{rs}(f) = 2V_S t_{rs} \frac{\sin(\pi f t_{rs})}{\pi f t_{rs}} \tag{4.18}$$

Consider for example the typical case where $t_{rs} = 30ns$. In this case, the 3dB frequency of H_{rf} will be above 10MHz. Subsequently, under the given assumptions the influences of finite rise- and fall-times are moderate. In practice however, the effect will contribute to noise and distortion, although the effect is not dominating compared with other error sources.

4.6 Pulse Amplitude Error (PAE) analysis

Pulse Amplitude Errors (PAE) is the general designation for error sources that distorts the amplitude of the modulated pulse train. The following will present a fundamental analysis of these error sources. The methodology is again to consider a simple pulse width modulated switching leg and then generalize the results to the generalized PSC and BPSC power stages.

4.6.1 Power supply perturbations

The type of error source may have significant magnitude especially if a non-stabilized power supply is used. Assuming that f_c is much higher than the bandwidth of both the power supply $v_s(t)$ and the reference input $v_r(t)$, the average of the modulated variable v_p corresponding to the filtered output can be written as:

$$v_o(t) = \tilde{v}_p(t) = v_r(t)v_s(t) \tag{4.19}$$

The non-linear multiplying effect is exactly what causes the desired power amplification and as long as the DC power supply is constant:

$$v_s(t) = V_s \tag{4.20}$$

In this case, the operation of the switching power stage is exactly as desired, i.e. we have found our ideal and efficient multiplier (!). However, a power supply that is able to deliver e.g. several hundred watts without any error is rather utopian in that is requires a output impedance of zero over the complete target bandwidth of the power amplifier. Indeed, extreme stabilization would be required, being either a linear regulated or a switching regulator. The sensitivity to power supply voltage perturbations is:

$$S_{v_s}^{v_o} = \frac{d(v_o)}{d(v_s)}\frac{v_s}{v_o} = v_r\frac{v_s}{v_r v_s} = 1 \tag{4.21}$$

This can also be interpreted as a power supply rejection ratio (PSRR) of 0dB. Let the perturbation on the power supply be represented as an additional error:

$$v_s(t) = V_s + v_{sp}(t) \tag{4.22}$$

Consequently:

$$v_o(t) = v_r(t)V_s + v_r(t)v_{sp}(t) \tag{4.23}$$

Consider a harmonic perturbation on the power supply:

$$v_{sp}(t) = \sum_{m=0}^{M_{max}} A_m \cos(m\omega_m t) \tag{4.24}$$

Where A_m represents the harmonic amplitudes relative to V_S, that for simplicity is assumed to be unity in the following. The reference signal is defined as:

$$v_r(t) = M\cos(\omega_r t) \tag{4.25}$$

With this harmonic perturbation the resulting output will be:

$$v_o(t) = \frac{1}{2} M \sum_{m=0}^{M_{max}} A_m [\cos(\omega_r t + m\omega_m t) + \cos(\omega_r t - m\omega_m t)] \tag{4.26}$$

Clearly, any components on the perturbed power supply will directly intermodulate with the modulated signal and generate IM components with amplitude:

$$\frac{1}{2} MA_m \quad at\ \omega_r \pm \omega_m \tag{4.27}$$

Since the components are not harmonically related to the signal the IM components should be damped well (preferably 100dB or more), although one might argue that masking effects will render the components less audible. The intermodulation distortion caused by the perturbation on the power supply is found:

$$IMD(M) \approx \frac{\sqrt{2\sum_{m=1}^{M_{max}} (\frac{1}{2} MA_m)^2}}{M(1+A_0)} = \frac{\sqrt{2\sum_{m=1}^{M_{max}} A_m{}^2}}{2(1+A_0)} \tag{4.28}$$

The intermodulation distortion is exclusively determined by the components of the perturbing signal. Equally important is the Linear Distortion LD caused by a DC perturbation on the power supply in the case that $A_0 \neq 0$:

$$LD = 1 + A_0 \tag{4.29}$$

Case example

A practical example is considered to illustrate the intermodulation effects caused by power supply perturbations. The case example is targeted for the full audio bandwith. The power supply voltage is $V_S = 50V$. A pure sinusoidal perturbation is considered, i.e. only $A_1 \neq 0$. Fig. 4.15 illustrates the essential power stage signals with a 5KHz perturbation, where $A_1 = 0.5$. In this particular case, the intermodulation distortion is extreme:

$$IMD(M) = \frac{1}{\sqrt{2}} A_1 = 35\% \tag{4.30}$$

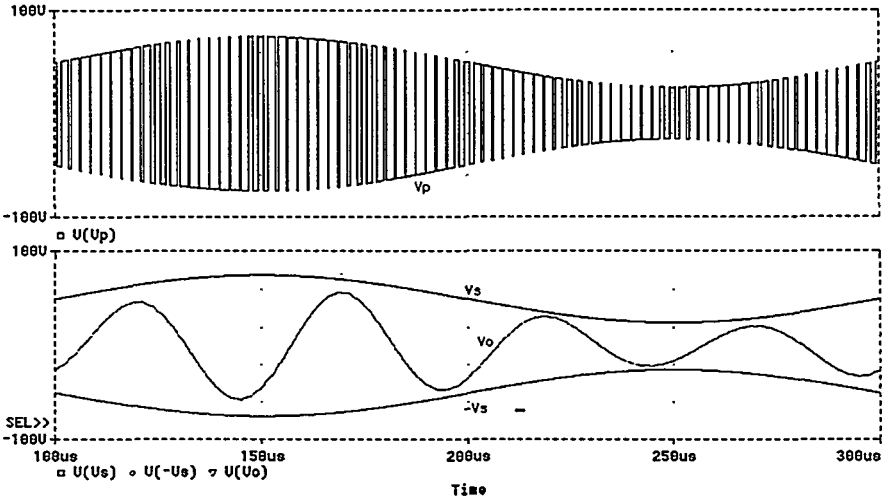


Fig. 4.15 Simulation of sinusoidal perturbation on the power supplies. $A_1 = 0.5$.

The intermodulation of the 20KHz fundamental is very clear and the resulting magnitude of intermodulation components at 15KHz and 25KHz are:

$$\frac{1}{2}MA_m = \frac{1}{2}0.9 \cdot 0.5 \cdot V_C = 11.25V \tag{4.31}$$

as expected from theory. Although perturbation on the power supply can have a significant magnitude, the case example is only illustrative and not realistic in practice.

Extensions to PSC and BPSC topologies

It is trivial to generalize the investigations above to the general N-leg PSC switching topology where errors will simply superpose. However, since each of the switching legs only contribute partially in the superposition the resulting effect will be the same as for the single switching leg.

4.6.2 PAE case example : Non-stabilized supply

The following important case example investigates PAE residing specifically from a non-stabilized power supply based on a simple mains transformer, bridge rectifier and mains capacitor. This power supply configuration excels by extreme simplicity and low cost and is desirable in most situations for general-purpose power amplification. One of the fundamental problems is that the power supply has non-linear output impedance. Due to the finite impedance of the rectifier, the effective output impedance is highly nonlinear at lower output currents, which is problematic since this is where the power amplifiers mostly operate. At higher output currents the output impedance can be estimated by:

$$R_O = R_1\left(\frac{N_1}{N_2}\right)^2 + R_2 + 2R_d \tag{4.32}$$

Where R_1, R_2 and R_d are the impedance of the primary and secondary winding, R_d the diode series resistance, and N_1 and N_2 the primary and secondary winding number. The stabilizing buffer capacitor is feed from the mains through this equivalent output impedance. Most of the music energy will be delivered from the buffer capacitor since the

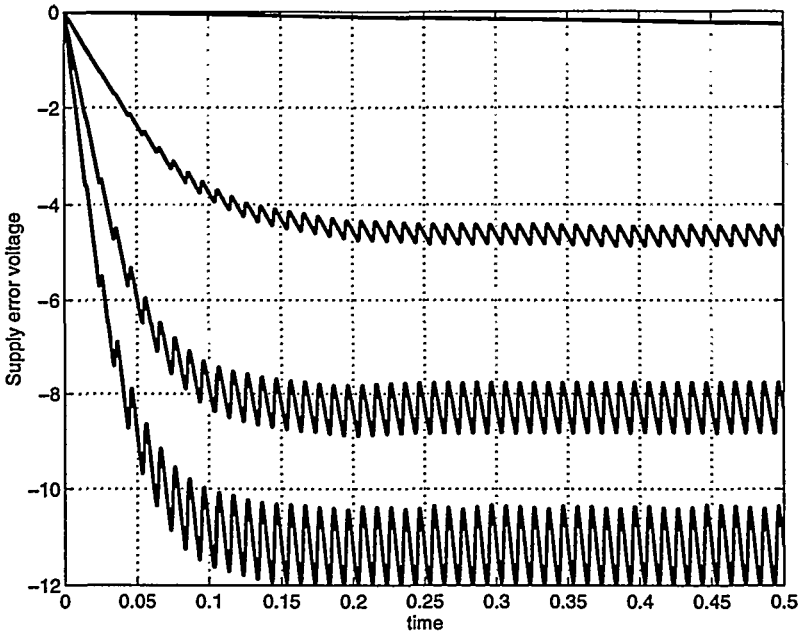


Fig. 4.16 $v_{sp}(t)$ with step DC current (10mA, 1A, 3A and 5A) from a typical 250W non-stabilized power supply.

capacitor represents the lowest impedance seen from the power amplifier. Consequently, the current drawn from the bridge and rectifier will have a significant DC component besides components related to the mains and the audio signal. The inevitable DC droop alone can be seen as a linear compression when the supply voltage is stabilized, but with normal music material the supply never stabilizes and the dynamic effects are therefore not easily analyzed.

To illustrate this severe PAE from a typical non-stabilized power supply, the transient response to a step current for a typical non-stabilized power supply (60V - 250W) is illustrated in Fig. 4.16. The current steps to 10mA, 1A, 3A and 5A. The worst error is the DC error is 11V, corresponding to a linear distortion *LD* of more than 15%. This error can be interpreted as a dynamic gain reduction in the order of several dB at high bass transients, which is clearly not acceptable. Besides the DC error, several harmonic components of twice the mains are introduced. The harmonic perturbation corresponds to several percent IMD in worst case situations. In the situation, where the PMA is feed with an audio signal, $v_{sp}(t)$ will be more complex and composed of a mixture of the mains and audio signal frequencies.

The are two approaches to minimize the magnitude of the perturbation $v_{sp}(t)$. First of all, R_O can be minimized by reducing the impedance of the transformer. However, this will increase volume and thus influence important parameters as volume and weight. Second, The buffer capacitor can be increased. This will not influence the steady state value of the power supply voltage to a constant current draw, but minimize the ripple components (and the related IM distortion). The supply ripple can simply be estimated by:

$$\Delta v_{sp,ripp} = \frac{I_{DC} \cdot t_m}{C_{buff}} \tag{4.33}$$

t_m is the time between "refresh" of the buffer capacitor, corresponding to the double of the mains frequency. Another effect of increasing the buffer capacitance is, that the time constant on the transient response will increase. However, None of these solutions are particularly elegant. On the contrary, it is desirable to minimize such costly power components. To conclude, a PMAs without error compensation can not be realized with a typical non-stabilized power supply, without severe compromises on parameters as volume, weight and cost. With a typical non-stabilized power supply, both LD the IMD are orders of magnitude higher than the acceptable distortion level.

4.6.3 Finite switch impedance effects

Another fundamental element that distorts the pulse amplitude is caused by the finite impedance of the power switch. The effects of a finite switching impedance will be analyzed for the simple switching leg and following the results will be generalized to the PSC and BPSC switching topologies.

The power MOSFET (I-V) characteristic when ON can be simplified to a resistor in parallel with a power diode. The body diode is modeled by a constant turn on voltage V_D and a dynamic resistance R_D. Correspondingly, the four quadrant (I-V) characteristic of the power MOSFET can be interpreted as a piece-wise linear function with the following (I-V) characteristic:

$$V_{DS} = \begin{cases} R_{DS(on)} I_L & (v_{DS} > -V_D) \\ -V_D + \left(R_{DS(on)} \parallel R_D\right) I_L & (v_{DS} < -V_D) \end{cases} \tag{4.34}$$

In general R_D will be considerably lower that $R_{DS(on)}$ and the diode resistance will therefore dominate the reverse channel (3. quadrant) at high currents. When possible, reverse channel conduction through the body diode should be avoided totally by simply choosing a MOSFET, which obeys:

$$R_{DS(on)} < \frac{V_D}{\hat{I}_{L,\max}} \tag{4.35}$$

It is not possible to obey this constraint in all applications with the present state of MOSFET technology. The choice of power transistor is a compromise between several other parameters, and a very low ON-resistance compromises switching speed and requires a more powerful driver circuitry. There are four switching states in the switching leg as illustrated in Fig. 4.17. Ideally, the switching output variable should only take two values:

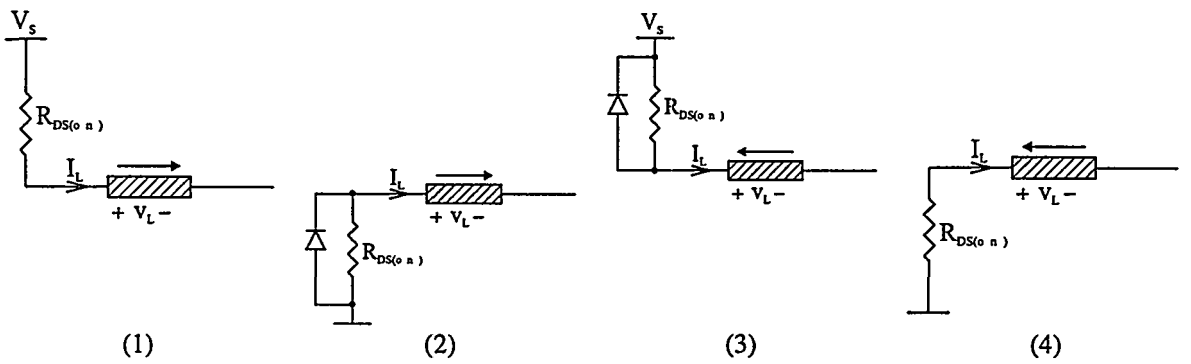


Fig. 4.17 Switching states in a switching leg.

$$v_P \in (V_S, -V_S) \tag{4.36}$$

However the actual pulse amplitude in the four states are:

State	v_p	Condition
1	$V_S - R_{DS(on)} I i_L$	$v_p > 0,\ i_L > 0$
2	$\begin{cases} -V_S - R_{DS(on)} I_L \\ -V_S - V_D - (R_{DS(on)} \parallel R_D)(I_L - \frac{V_D}{R_{DS(on)}}) \end{cases}$	$v_p < 0,\ I_L < \frac{V_D}{R_{DS(on)}}$ $v_p < 0,\ I_L \geq \frac{V_D}{R_{DS(on)}}$
3	$\begin{cases} -V_S - R_{DS(on)} I_L \\ -V_S - V_D - (R_{DS(on)} \parallel R_D)(I_L - \frac{V_D}{R_{DS(on)}}) \end{cases}$	$v_p > 0,\ I_L > \frac{-V_D}{R_{DS(on)}}$ $v_p > 0,\ I_L \leq \frac{-V_D}{R_{DS(on)}}$
4	$V_S - R_{DS(on)} I_L$	$v_p < 0,\ I_L < 0$

The finite switch impedance results in amplitude modulation. When (4.35) is obeyed, the pulse amplitude modulation can be expressed by the very simple relation:

$$v_p = v_{p,ideal} - R_{DS(on)} I_L \tag{4.37}$$

I.e. the error is linear and can be interpreted as a simple output impedance. At higher output currents where (4.35) no longer holds, the finite switch impedance will introduce both linear and non-linear distortion. The error on v_p will depend upon the polarity of the current leading to odd harmonic distortion of the modulating signal. However, the importance of this error source will be insignificant in the general case since:

- The distortion only occurs at high output levels. The non-linear error contributions will be small relative to the signal and other contributions.
- A high peak output levels, v_P the power stage will mostly be in the states 1 and 4, that are free from non-linear distortion.
- A high ON resistance is simply not desirable from any point of view.

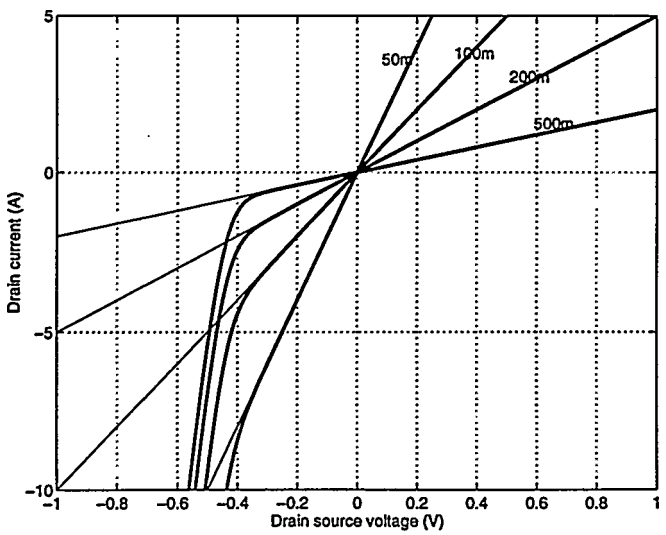


Fig. 4.18 I-V characteristic of the switch used in the simulations vs. $R_{DS(on)}$

Case example

To illustrate the effects of this error sources consider a 200W output stage case example. Parameter values are selected to f = 5KHz and M = 0.7. The I-V characteristics of the switches used in the investigations are shown in Fig. 4.18. $R_{DS(on)}$ is considered a variable parameter throughout the investigations. Fig. 4.19 shows a simulation of the power stage with a very large switch impedance, $R_{DS(on)}$= 1Ω. The high output impedance will force the switching leg into the non-linear states 2 and 3 throughout most of the complete cycle. Fig. 4.20 further illustrates the perturbations on the power stage output $v_{pp} = v_p - v_{p,ideal}$ and the filtered output $v_{op} = v_o - v_{o,ideal}$.

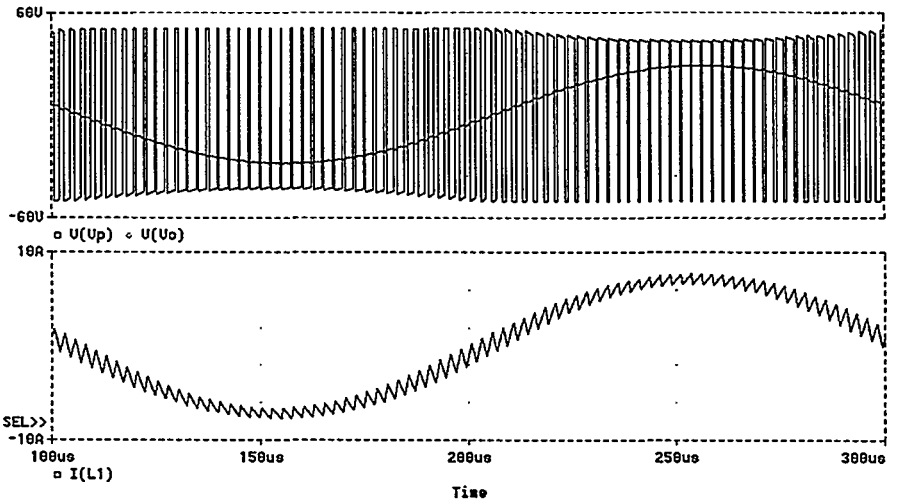


Fig. 4.19 Pulse amplitude modulation introduced by $R_{DS(on)}$= 1Ω. THD=1%.

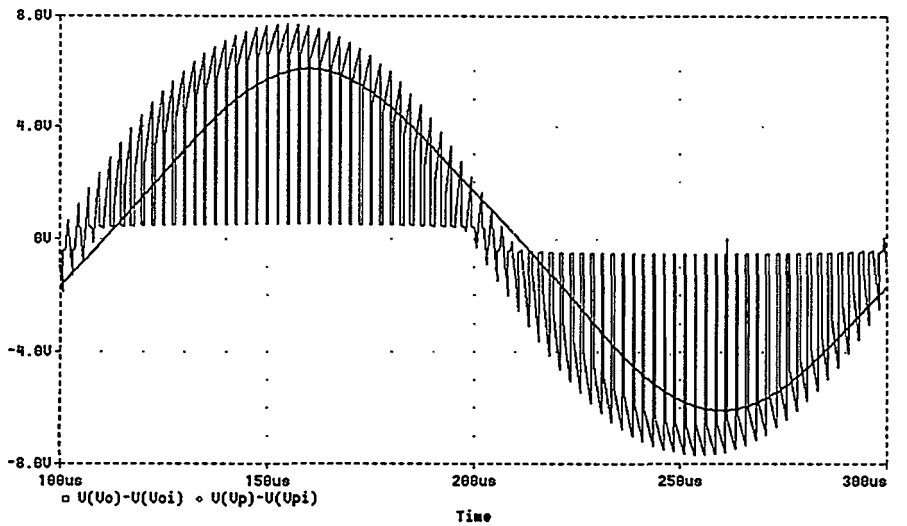


Fig. 4.20 Pulse amplitude error $v_{pp} = v_p - v_{p,ideal}$ and $v_{op} = v_o - v_{o,ideal}$. $R_{DS(on)}$= 1Ω.

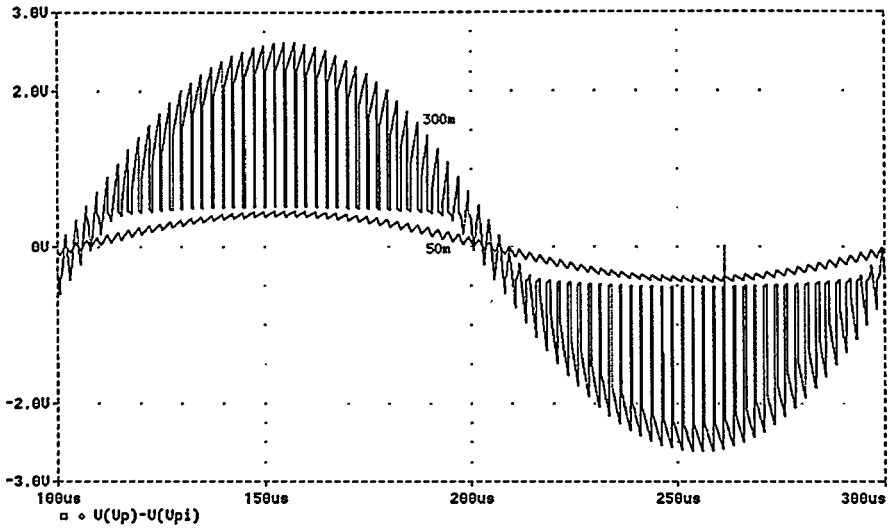


Fig. 4.21 Pulse amplitude error v_{pp} and with $R_{DS(on)}$= 50mΩ and 300mΩ.

From the filtered version of the error, $v_{op} = v_o - v_{o,ideal}$, it is clear that the distortion is mostly linear. A spectral analysis of the output waveform shows that THD=1% with $R_{DS(on)}$ = 1Ω. Such an ON impedance is not realistic however, and Fig. 4.21 illustrates the PAE effects with a lower $R_{DS(on)}$ of 50mΩ and 300mΩ. Observe, how the switching leg remains in the states 1 and 3 and the error is thus purely linear when the ON impedance is sufficiently low. Even with the unrealistic high switch impedance of 300mΩ the total harmonic distortion is only 0.25%. To conclude, the effects of the switch impedance can be made insignificant (in terms of non-linearity) with a proper selection of the switch.

Generalization to PSC and BPSC

Further generalization to the PSC and BPSC implementations is reasonably simple, i.e. the pulse amplitude errors superpose. However, the following should be noted:

- The BPSC topology doubles the output impedance.
- The paralleling of switching legs helps to prevent non-linearity to occur, since the switch can be kept in the linear range.

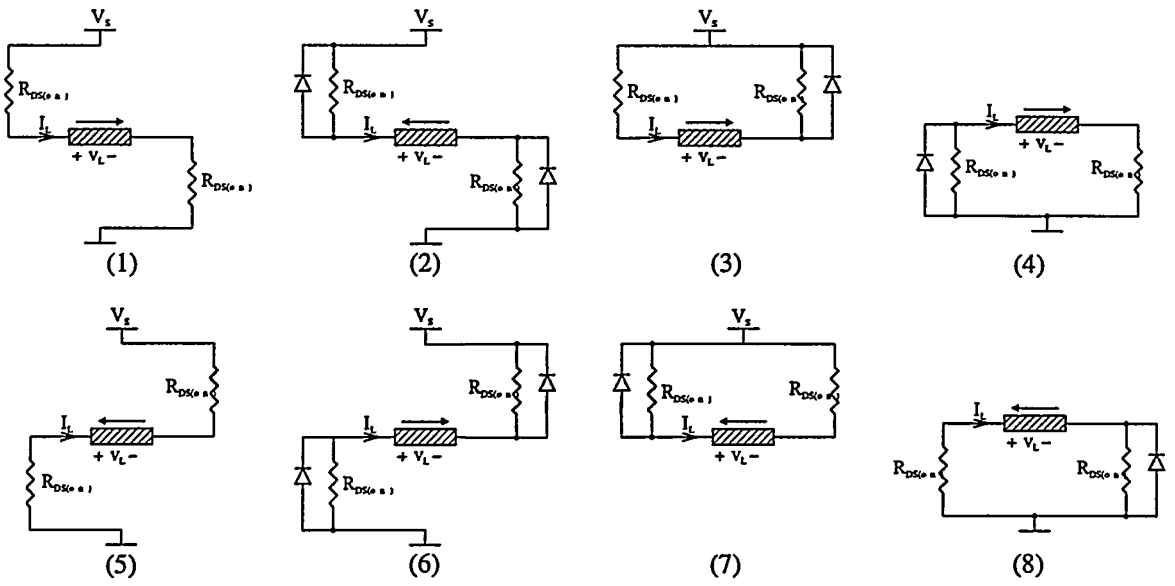


Fig. 4.22 The possible switching states for BND2 PWM with N=2 (corresponding to NBDD).

Consider e.g. a bridge implementation of BND2 in the case N=2 (corresponding to NBDD in this specific case). The switching output variable should only take three values:

$$v_L \in (V_S, 0, -V_S) \tag{4.38}$$

There are eight different switching states which are shown in Fig. 4.22. The pulse amplitude levels in the states are:

State	v_p	Current
1	$V_S - 2R_{DS(on)} i_L$	$I_L > 0$
2	$\begin{cases} -V_S - 2R_{DS(on)} I_L \\ -V_S - 2V_D - 2(R_{DS(on)} \parallel R_D)(I_L - \frac{V_D}{R_{DS(on)}}) \end{cases}$	$0 \le I_L < \frac{V_D}{R_{DS(on)}}$ $I_L \ge \frac{V_D}{R_{DS(on)}}$
3, 4	$\begin{cases} -2R_{DS(on)} I_L \\ -V_D - R_{DS(on)} I_L - (R_{DS(on)} \parallel R_D)(I_L - \frac{V_D}{R_{DS(on)}}) \end{cases}$	$0 \le I_L < \frac{V_D}{R_{DS(on)}}$ $I_L \ge \frac{V_D}{R_{DS(on)}}$
5	$-V_S - 2R_{DS(on)} I_L$	$I_L < 0$
6	$\begin{cases} V_S - 2R_{DS(on)} I_L \\ V_S + 2V_D - 2(R_{DS(on)} \parallel R_D)(I_L + \frac{V_D}{R_{DS(on)}}) \end{cases}$	$\frac{-V_D}{R_{DS(on)}} \le I_L < 0$ $I_L < \frac{-V_D}{R_{DS(on)}}$
7,8	$\begin{cases} -2R_{DS(on)} I_L \\ -V_D - R_{DS(on)} I_L - (R_{DS(on)} \parallel R_D)(I_L - \frac{V_D}{R_{DS(on)}}) \end{cases}$	$\frac{-V_D}{R_{DS(on)}} \le I_L < 0$ $I_L \le \frac{-V_D}{R_{DS(on)}}$

Clearly, the output impedance is doubled to $2R_{DS(on)}$, although the limit between linear and non-linear operation remains the same. As N increases in the PSC and BPSC topologies, the output impedance will be *reduced* as a consequence of the paralleling. Assuming that the $R_{DS(on)}$ is independent upon N, the output impedance of the switching power stage will be:

Switching leg	PSC	BPSC
$R_{DS(on)}$	$R_{DS(on)} / N$	$2R_{DS(on)} / N$

Returning to the actual BND2 case example, Fig. 4.23 illustrates the PAE effects with an ON resistance of 50mΩ and 300mΩ the each of the two switching legs. The error signal on each phase voltage is recognized from the investigations of the switching leg. The differential error has a different characteristic. The total harmonic distortion is only 0.25% with $R_{DS(on)}$= 300mΩ, exactly as for the switching leg. This verifies that the switch impedance effects are general and independent upon N. To conclude, this source of PAE will be of less significance in the PSC and BPSC power stage topologies by proper selection of the power components.

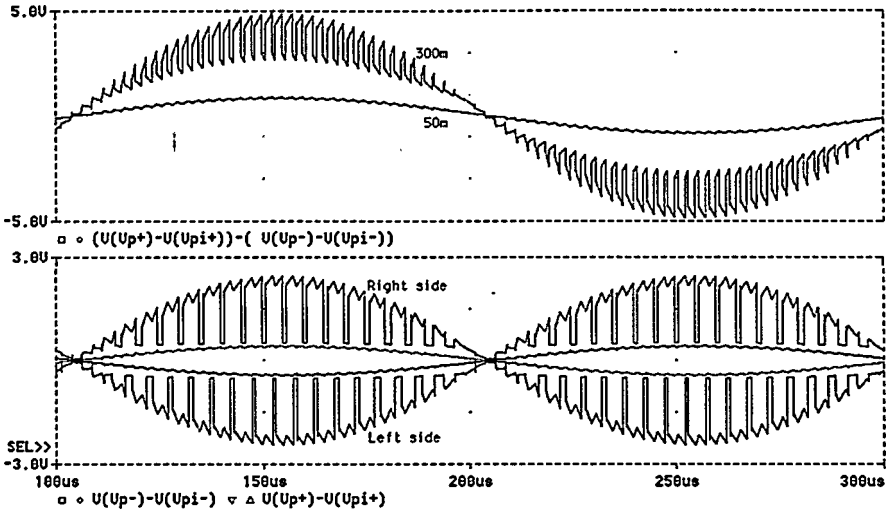


Fig. 4.23 Pulse amplitude error v_{pp} for NBDD (BND2 with two switching legs) with $R_{DS(on)}$ = 50mΩ and 300mΩ. The error on each (bottom) is recognized from the switching leg. The resulting differential error (top) is the difference between the two error sources.

4.6.4 Other contributions to PAE

Other contributions to PAE reside form the high frequency resonant action between parasitic inductance in the switching legs and the parasitic output capacitance in the individual switching legs. This error source is generally insignificant compared to other error sources, since the pulse distortion mainly affects the HF spectrum. It is very difficult to generalize on the exact effects since the resonant action depends heavily on the practical implementation. In any case, HF contributions of this kind are undesirable from any point of view and the effect should be minimized by proper design of the power stage.

4.7 Analog PMA modulator error sources

Throughout Part I, the theoretical modulator performance was analyzed isolated. In general, the modulator can be implemented with a performance level that well exceeds what can be achieved by the subsequent power amplification stage. However, this requires certain precautions in modulator design. The factors that need consideration can be summarized to:

- The inherent offset within the comparator leads to edge jitter and has to be sufficiently small.
- The speed of the comparator, especially in terms of differential delay between turn-off and turn-on.
- The carrier generator jitter and noise (especially within the target bandwidth).

PSCPWM modulator implementation introduces new concerns that require a more detailed analysis. In the following, the possible error sources will be discussed in terms of the effect on the resulting PSCPWM modulator output. Modulator error sources relate to errors on the carrier. Four categories can be defined:

- Interleave (phase) errors between carriers. The error source will be represented in degrees related to desired phase angle of the particular carrier.
- Carrier integration errors. This will lead to different amplitudes of the individual carriers. The error will be defined (in %) as the relationship between the error related to the nominal carrier amplitude.

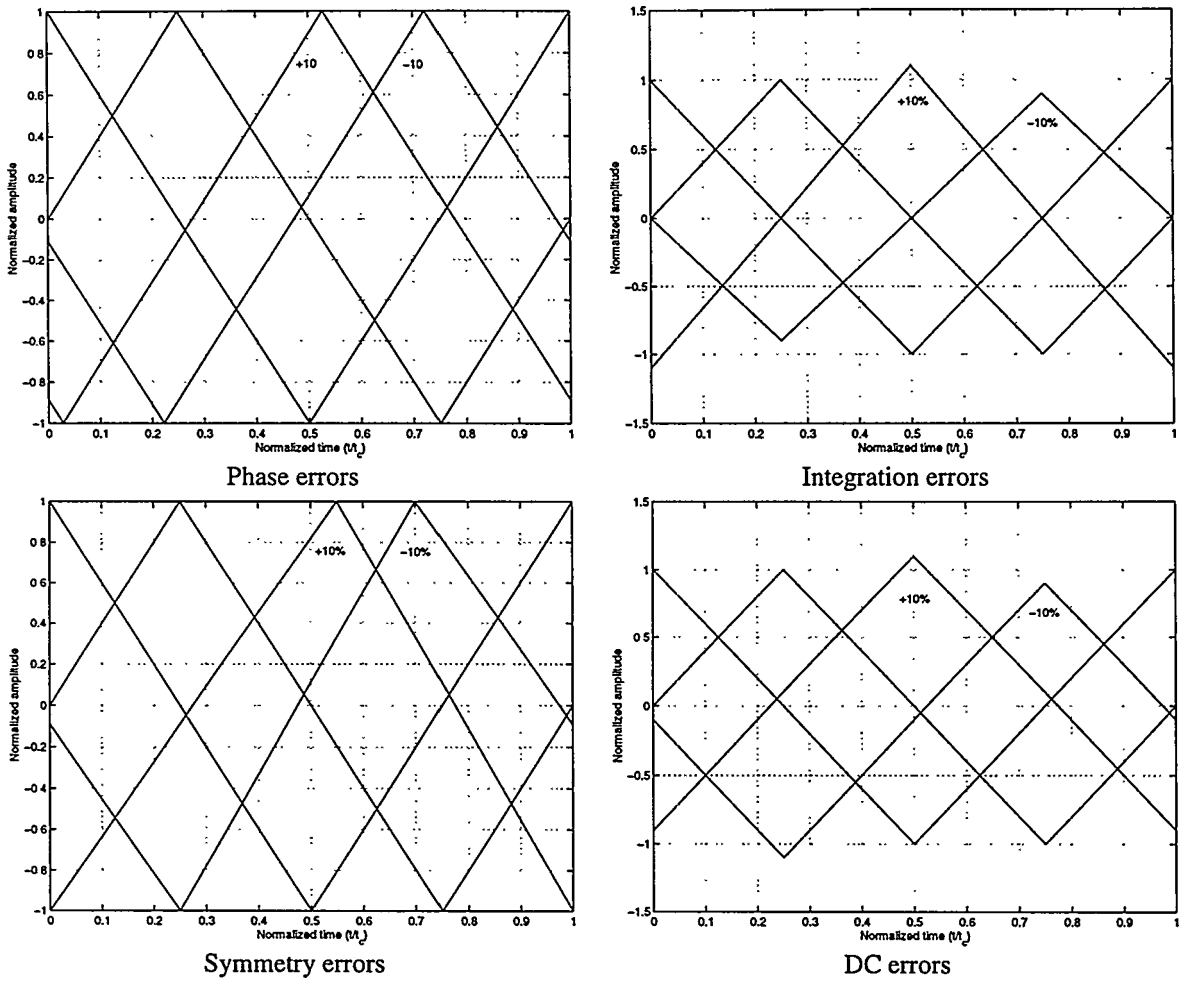


Fig. 4.24 Definition of error sources for parametric investigation (N=4).

- Carrier symmetry errors in double sided modulation. The error source is introduced if the individual carriers are not symmetrical.
- DC offset errors. The error is represented relative to the amplitude of the carrier (in %).

The origins of the errors are illustrated in Fig. 4.24. The case where N=4 is investigated more closely in the following. All errors will be analyzed in the absolute *worst-case* situation, by establishing tolerances for the individual error sources for all PSCPWM modulation methods.

The investigations lead to one fundamental conclusion: All errors sources *only* influence (i.e. degrade) the HF-characteristics and do *not influence output stage linearity*. The degradation of the HF-output means the that the harmonic cancellation of PSCPWM will not be perfect, i.e. there will be finite components around all harmonics of the carrier etc. The effects of this degradation in HF-characteristics should not be overestimated. Just 30dB of harmonic cancellation is a big improvement, that will allow for lower carrier frequency, higher control loop bandwidth, improved demodulation and all the other positive effects of PSCPWM. A complete elimination of the components is neither possible nor necessary.

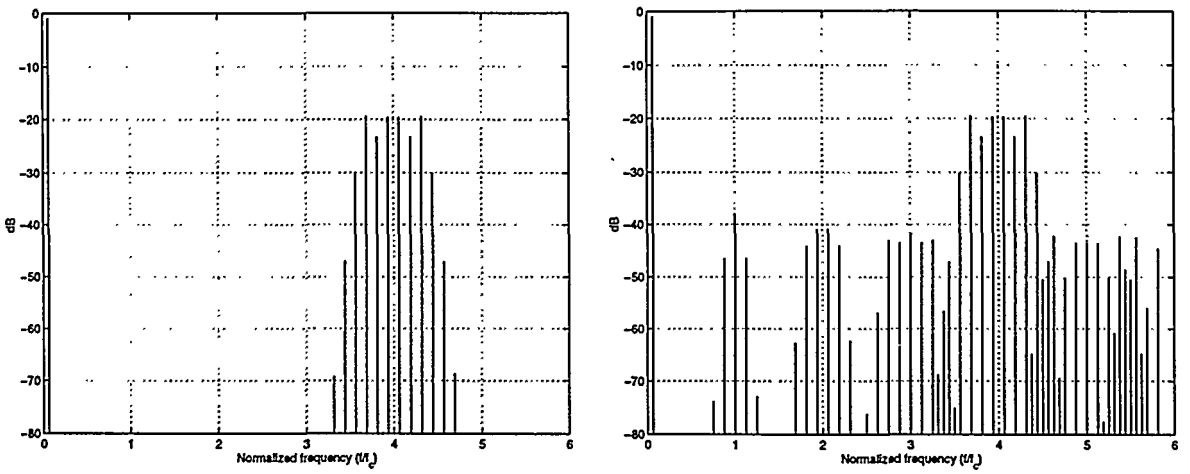


Fig. 4.25 Comparing BND1 output with ±2 degrees of phase error (worst case). The consequence of all modulator error sources is the same – imperfect harmonic elimination.

4.7.1 Parametric analysis of PSCPWM modulator error sources

To gain knowledge on the necessary tolerances to implement PSCPWM, a systematic investigation of worst-case tolerances for at least 30dB, 40dB, 50dB and 60dB of harmonic cancellation has been investigated. All investigations have been carried out at M=0.9. The investigations have been performed individually for each of the double-sided modulation schemes. The single sided modulation schemes were concluded to be sub-optimal in Chapter 2.

ND tolerance specifications (*N*=4):

Max. HF	Phase	Integration	Symmetry	DC
-30dB	4°	10%	2.5%	3%
-40dB	1.3°	3%	0.7%	1%
-50dB	0.4°	0.9%	0.2%	0.3%
-60dB	0.15°	0.3%	0.1%	0.1%

BND1 tolerance specifications (*N*=4):

Max. HF	Phase	Integration	Symmetry	DC
-30dB	4°	10%	2.5%	3%
-40dB	1.3°	3%	0.7%	1%
-50dB	0.4°	0.9%	0.2%	0.3%
-60dB	0.15°	0.3%	0.1%	0.1%

BND2 tolerance specifications (*N*=4):

Max. HF	Phase	Integration	Symmetry	DC
-30dB	7°	13%	4%	5%
-40dB	2°	4%	1.2%	3%
-50dB	0.7°	1.2%	0.4%	0.6%
-60dB	0.25°	0.4%	0.15%	0.2%

BND3 tolerance specifications (N=4):

Max. HF error	Phase	Integration	Symmetry	DC
-30dB	>10°	>10%	10%	5%
-40dB	>10°	>10%	3%	1%
-50dB	>10°	>10%	1%	0.3%
-60dB	>10°	>10%	0.3%	0.1%

From the tolerance investigations the following is concluded:

- Generally, there is a nearly proportional relationship between the specified peaks in the error HF spectrum and the tolerances, i.e. when the specification is reduced 10dB, the tolerance also tightens 10dB.
- The tolerance specifications for ND and BND1 are identical, corresponding well with that the number of carriers are the same.
- For NDB2 the errors (tolerances) can generally be doubled, corresponding to that the number of carriers is halved.
- NDB3 is extraordinary insensitive to phase and integration errors and less sensitive to symmetry errors that other methods. The tolerance to DC errors is identical to ND.

In conclusion, errors on the carrier waveform will generate a HF error spectrum around all harmonics of the carrier. However, the tolerance specifications corresponding to –30dB and –40dB can be implemented, especially in the NDB3 case. Correspondingly, PSCPWM is feasible and not inherently limited by tolerances within the modulator.

4.8 Summary

The fundamental error sources within the power amplification of a pulse modulated signal has been investigated. The essential concerns for the design of the power conversion stage are linearity, complexity and efficiency. Starting with an investigation of the switching devices, the inherent physical limitations within the switching devices were explained. Following, the switching waveforms within a simple switching leg has been investigated in detail. The error sources have been identified and it was found expedient to categorize the error sources into Pulse Amplitude Errors (PAE) and Pulse Timing Errors (PAE). Several sources of non-ideal behavior were identified. The most problematic error sources were pointed out to be the blanking effect and the intermodulation caused by perturbations on the power supply. These important error sources are fundamental and will introduce distortion with any modulation scheme and any of the considered power stage topologies.

Specific error source relating to PSCPWM modulator implementation has been addressed. It was shown that PSCPWM is feasible and not inherently limited by tolerance specifications with in the modulator and power stage.

It is bound with considerable difficulty to realize the power conversion stage with sufficient linearity for high quality PMAs. With the documented error sources, error correction systems are concluded to be vital for practical, efficient and robust implementation of the power conversion stage in both analog and digital PMA systems.

Part II

Chapter 5

Efficiency Optimization

This chapter is devoted to efficiency optimization within pulse modulation power amplifier systems. As introduced in Chapter 1 the fundamental goal of the present research is to develop amplifier solutions with significantly higher energy- and power-efficiency. A completely switched power stage has the inherent advantage of 100% efficiency in theory. Recall from chapter 4, that the efficiency will never reach this theoretical limit due to switch imperfections. In the present chapter, various contributions to efficiency degrading power loss will be analyzed theoretically. Starting with a simple switching leg, the results will be generalized to general PSC and Balanced PSC power stage topologies. Case examples are given to illustrate the efficiency and energy efficiency that can be achieved by the present state of technology within power switching devices and magnetics. The parametric dependencies and constraints in optimizing power stage efficiency will be discussed.

5.1 Efficiency in power conversion

It is bound with considerable difficulty to accurately model the power loss within power switching devices, given the existence of production spread and temperature variation in conduction and switching characteristics. One are often left with empirical tests and measurements in order to get exact results. However, reasonably accurate modeling of power loss within the PMA power stage is important, to allow optimization of system efficiency and energy efficiency. Various simplifications can make the estimation of power loss practical by relatively simple expressions. During the following investigations, the following simplifications will be made use of:

- Idealized switching characteristics, where current and voltage are assumed to have linear transition characteristics.
- The blanking time has been adjusted such as to avoid shoot-through phenomena.
- Diode reverse recovery is considered non-existent. The reverse recovery effect can contribute with significant switching losses, so the following analysis assumes that the effect is eliminated (e.g. by Shottky diodes as explained) or less significant.
- Several insignificant effects are omitted from the investigations, as the minimal contribution from diode conduction during the relatively short dead-band time.

Much progress in Power MOSFET technology has been made over the last decade. Thus, the recently introduced fifth generation provides an excellent combination of parameters. This continuos improvement of switches means that the PMA efficiency will converges towards the theoretical limit of 100% with time. Such improvements are not observed with existing linear amplification techniques, that are stuck with power loss bound to the fundamental principles.

The analysis of power loss contributions will be devided into conduction losses and switching losses. A simple switching leg will be considered first, and following the results will be generalized to N switching legs in the general PSC and BPSC switching topologies. A terminology for the following analysis of current and conduction loss characteristics are defined below:

Parameter	Comment
I_L, $\hat{I}_L$, $I_{L,AV}$, $I_{L,RMS}$	Absolute, peak, average and RMS of *signal* (LF) current running to the load.
I_D, $\hat{I}_D$, $I_{D,AV}$, $I_{D,RMS}$	Absolute, peak, average and RMS of current in the switch.
I_T, $\hat{I}_T$, $I_{T,AV}$, $I_{T,RMS}$	Absolute, peak, average and RMS of the output HF ripple current component
I_{DT}, $\hat{I}_{DT}$, $I_{D,RMS}$	Absolute, peak and RMS of HF ripple current in the switch.
I_{LN}	Output current for each individual switching leg
L_N	Inductor required in each switching leg.
$M_{\max}$	Maximal modulation index
P_O, $P_{O,\max}$	Output power, maximal output power
V_O, $\hat{V}_O$, $\hat{V}_{O,\max}$	Output voltage, Peak output voltage and maximal peak output voltage.
I_O, $\hat{I}_O$	Absolute and peak output current
V_S	Power rail voltage
R_L	Load impedance
P_S, P_C, P_D, P_{TOT}, P_Q	Switching losses, conduction losses, total semiconductor losses, total output stage losses and quiescent losses.

5.2 Conduction losses

Fig. 5.1 illustrates currents I_L and I_D (high switch S_H) in a switching leg at various modulation depths, M=0, 0.3 and 0.8. The current during the positive going period is mainly delivered by the "high switch" S_H and vice versa. Observe how the output ripple current is minimal at maximal modulation depth.

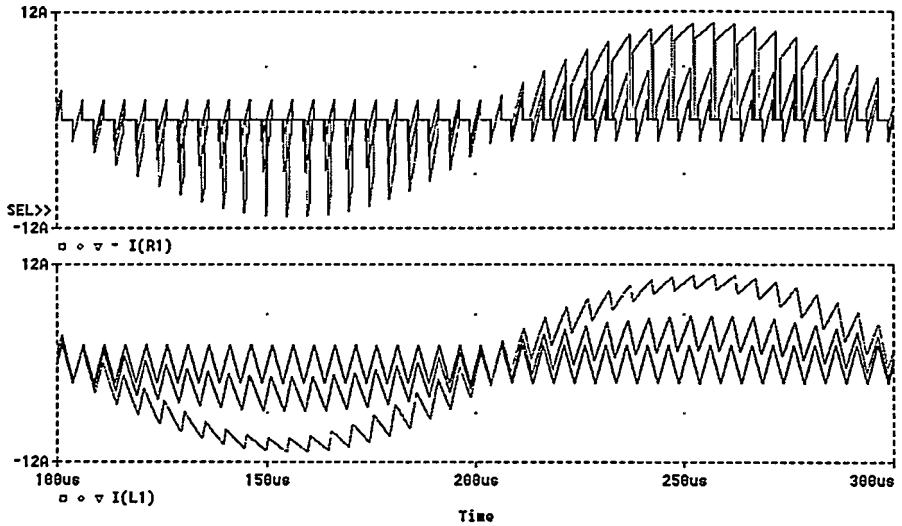


Fig. 5.1 Currents in a switching leg at three modulation depths, M = 0, 0.3, 0.8. Top – Current in "top" switch I_D. Bottom – output current = inductor current I_L.

The maximal required peak output voltage to deliver the desired power to the load is:

$$\hat{V}_{O,\max} = \sqrt{2R_L P_{O,\max}} \tag{5.1}$$

Limiting the modulation depth at $M_{\max}$ leads to the following necessary supply voltage V_S:

$$V_S = \frac{\hat{V}_O}{M_{\max}} \tag{5.2}$$

The peak output current is:

$$\hat{I}_O = \sqrt{\frac{2P_O}{R_L}} \tag{5.3}$$

It is assumed for simplicity that the signal current in the load and the output current are identical (i.e. no signal current in the filter capacitor), i.e.:

$$I_L = I_O \tag{5.4}$$

This assumption is valid as long as the frequency is well below the natural frequency of the demodulation filter. The rectified average and RMS values of the inductor current with sinusoidal modulation are:

$$I_{L,AV} = \frac{2}{\pi}\hat{I}_L \tag{5.5}$$

$$I_{L,RMS} = \frac{\hat{I}_L}{\sqrt{2}} \tag{5.6}$$

The load current is delivered from the two switches, and seen over a complete period of the modulating signal symmetry yields the same average and RMS currents in each switch. Subsequently the rectified average current and RMS current in the individual switch will be:

$$I_{D,AV} = \frac{1}{\pi}\hat{I}_L \tag{5.7}$$

$$I_{D,RMS} = \frac{\hat{I}_L}{2} \tag{5.8}$$

In the simple switching leg the ripple current magnitude is determined as:

$$\hat{I}_T = \frac{V_S}{2Lf_c} \tag{5.9}$$

This relation for $\hat{I}_T$ holds at zero modulation where the ripple current has maximal magnitude and contributes with maximal losses. However, it is assumed that $\hat{I}_T = \hat{I}_{T,\max}$ throughout the following to simplify the investigations. Furthermore, the switching voltage over the inductor is assumed to be $2V_s$ in (5.9), corresponding to a perfectly demodulated output. This simplification only marginally influences the investigations of the ripple current effects. The RMS value of the triangular ripple current is:

$$I_{T,RMS} = \frac{\hat{I}_T}{\sqrt{3}} \tag{5.10}$$

The symmetrical distribution of currents in the two switches within a complete switching cycle yields the following RMS ripple current is each switch:

$$I_{DT,RMS} = \frac{\hat{I}_T}{\sqrt{6}} \tag{5.11}$$

All essential currents have now been determined for the investigations of conduction loss within the switching leg. The semiconductor conduction loss for the switching leg is simply the sum of the two contributions:

$$\begin{aligned} P_C(I_L) &= 2R_{DS(on)}(I_{D,RMS}^2 + I_{T,RMS}^2) \\ &= 2R_{DS(on)}\left(\frac{\hat{I}_L^2}{4} + \frac{1}{12}\left(\frac{V_S}{Lf_c}\right)^2\right) \end{aligned} \tag{5.12}$$

The second contribution will generally only be of significance at quiescence. It should be emphasized, that $R_{DS(on)}$ depend strongly on the junction temperature. It is very important to consider this dependency for a reasonable estimate of conduction losses.

5.3 Switching losses

As illustrated in Chapter 4 the switching transitions for both current and voltage have a finite duration. During current or voltage switching, the switching device is in the active region leading to switching losses. The non-linear switching characteristics and multi-parameter dependency of several physical parameters makes it difficult to perform a generalized analysis. However, by simplifying the switching characteristics as shown in Fig. 5.2, the analysis can be much simplified. The scenario is repeated in every switching cycle with a positive load current. Since the switching losses are an *even* function of the load current (symmetry), only the situation with positive load currents will be considered.

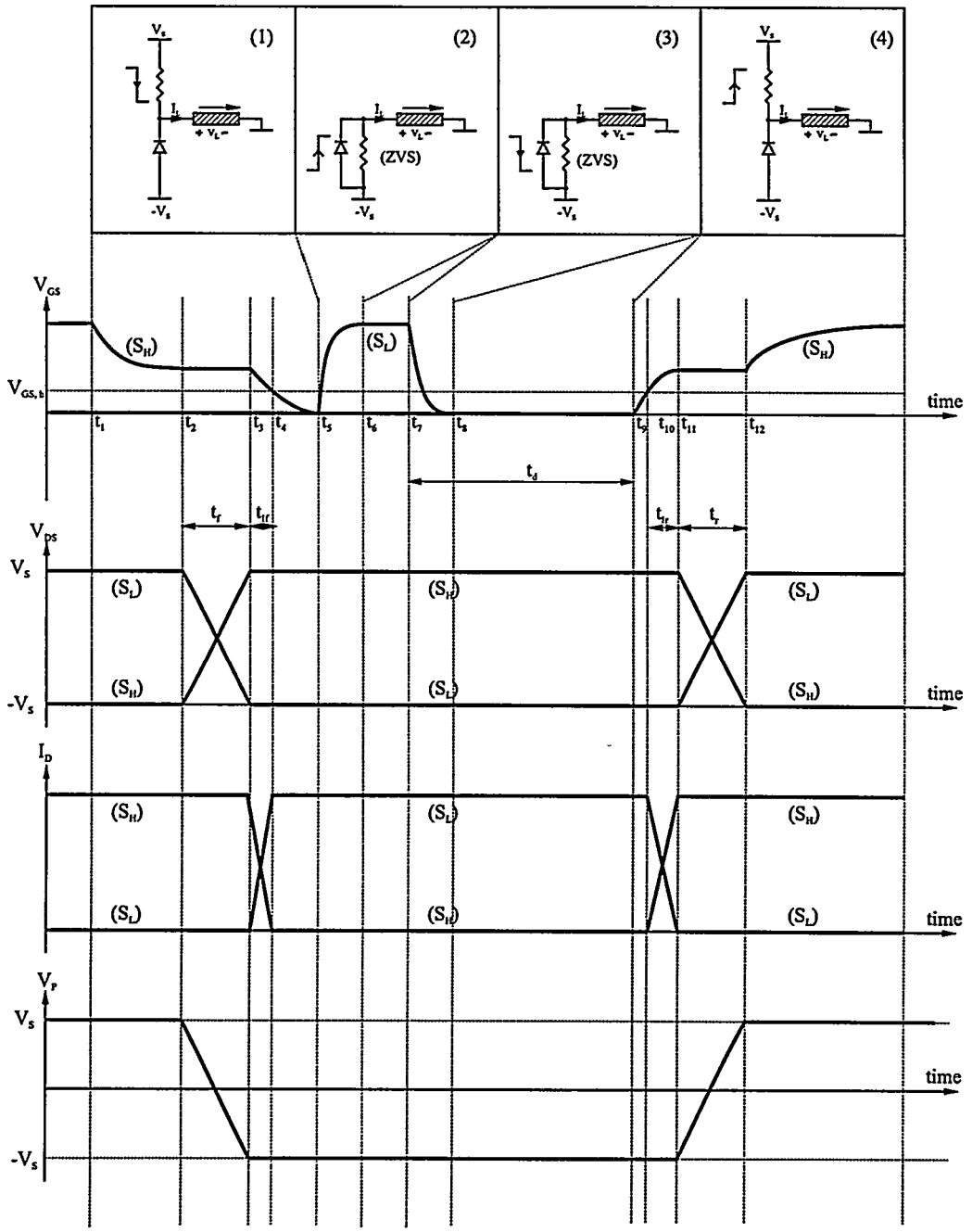


Fig. 5.2 Simplified switching characteristics for estimation of switching losses.

At lower currents where $\hat{I}_L < \hat{I}_T$, *all* switching actions will be ZVS and there will be no contributions from switches that enter the active region. For $\hat{I}_L > \hat{I}_T$, a switching cycle involves the following actions in the switching leg:

- One full turn-on.
- One full turn-off.
- One ZVS turn-on.
- One ZVS turn-off.

ZVS transitions produce negligible losses in the switching transistors. With the linear approximation, the contributions from the full turn-on and full turn-off can be derived from simple geometric relations. From Fig. 5.2, the following energy loss is introduced the falling transition $t_2 - t_4$:

$$E_{S,fall}(I_L) = \frac{1}{2} 2V_S I_L (t_f + t_{If}) \tag{5.13}$$

Note that the switching voltage over the individual devices is $2V_S$. The voltage fall and current fall times are:

$$t_f = \frac{Q_{GD}}{\frac{v_{GS,th} + \frac{I_L}{g_{fs}}}{R_G}} \tag{5.14}$$

$$t_{If} = R_G C_{iss} \ln\left(\frac{v_{GS,th} + \frac{I_L}{g_{fs}}}{v_{GS,th}}\right) \tag{5.15}$$

Similarly, the energy loss from the rising voltage and current transition $t_9 - t_{12}$ is given by:

$$E_{S,rise}(I_L) = \frac{1}{2} 2V_S I_L (t_r + t_{Ir}) \tag{5.16}$$

Where:

$$t_r = \frac{Q_{GD}}{\frac{V_G - v_{GS,th} - \frac{I_L}{g_{fs}}}{R_G}} \tag{5.17}$$

$$t_{Ir} = R_G C_{iss} \ln\left(\frac{V_G - v_{GS,th}}{V_G - v_{GS,th} - \frac{I_L}{g_{fs}}}\right) \tag{5.18}$$

By averaging over a complete period of the signal, the total switching losses arising from voltage and current transitions of finite duration are:

$$P_{S1}(I_L)=\begin{cases}0 & (\hat{I}_L<\hat{I}_T)\\ \frac{1}{2}f_c 2V_S\frac{\hat{I}_L}{\pi}(t_f+t_{If}+t_r+t_{Ir}) & (\hat{I}_T<\hat{I}_L)\end{cases} \tag{5.19}$$

In practice, the transition between states is not as sharp as indicated. Some current is necessary to provide the ZVS transition, i.e. $\hat{I}_L$ has to be somewhat lower than $\hat{I}_T$ for a full ZVS transition. A further contribution to switching losses arises from the parasitic output capacitance of the switches that are charged and discharged within each period.

$$P_{S2}=(2V_S)^2 C_{DS} f_c = 4C_{DS} f_c V_S^2 \tag{5.20}$$

The voltage dependency of C_{DS} has to be considered. A conservative but reasonable estimate of the losses can be made by using the output capacitance at 10-20% of the breakdown voltage. Each switch contributes with losses due to their output capacitance. Consequently, the total switching losses in the switching can be approximated by:

$$\begin{aligned}P_S(I_L)&=P_{S1}(I_L)+2P_{S2}\\ &=\begin{cases}8C_{DS}f_c V_S^2 & (\hat{I}_L<\hat{I}_T)\\ f_c V_S\frac{\hat{I}_L}{\pi}\tau(I_L)+8C_{DS}f_c V_S^2 & (\hat{I}_T<\hat{I}_L)\end{cases}\end{aligned} \tag{5.21}$$

Where:

$$\tau(I_L)=R_G Q_{GD}\left(\frac{1}{v_{GS,th}+\frac{I_L}{g_{fs}}}+\frac{1}{V_G-v_{GS,th}-\frac{I_L}{g_{fs}}}\right)+R_G C_{iss}\ln\left[\frac{v_{GS,th}+\frac{I_L}{g_{fs}}}{v_{GS,th}}\cdot\frac{V_G-v_{GS,th}}{V_G-v_{GS,th}-\frac{I_L}{g_{fs}}}\right] \tag{5.22}$$

The total power loss in the switching leg is the sum of conduction loss (5.12) and the total switching losses (5.21).

5.4 Demodulation filter losses

Filter inductors generally adds another significant contribution to the total power loss in PMA systems. This contribution is generally comparable to that of the switching power stage and it is important to obtain a reasonable accurate estimate of the losses. The following elements contribute to the power loss within the filter inductor(s):

- Conduction losses caused by LF current running in the finite DC resistance of the inductor.
- Conduction losses caused by the HF ripple current running in the inductor.
- Magnitic core losses due to LF induction swing
- Magnetic core losses caused by the ripple current (a HF induction swing).

It is impossible to generalize about the significance of each contribution. The typical characteristics will be illustrated by considering a specific type of inductor. Generally, single layered toroids are a good solution, that provides the highest resonance frequency, minimal volume and also a very high efficiency, by carefull design and proper selection of magnetics. Subsequently, the investigations will focus on torodial inductors. A set of parameters for the analysis are defined below.

Parameter	Description
N_L	Number of turns
A_L	Permeance (H)
$B, \hat{B}, \hat{B}_{\max}$	Induction, peak induction and maximal peak induction (T)
Φ	Magnetic flux (Wb)
$\varnothing_{cu}, l_{cu}, R_{cu}$	Winding parameters (diameter, length, resistance)
ρ_{cu}	Specific resistance of copper ($0.0155\Omega mm^2/m$)
μ_0, μ_r	Vacuum permeability (H/m), relative permeability.
d_i, d_O, h	Inner and outer diameter and height of magnetic core
A_T, l_T, V_T	Cross-sectional area, middle-length and volume of core.
P, B_r, f_r, k_f k_B	Core loss parameters
P_{cu}	Copper loss (inductor conduction loss)
P_{co}	Core loss
P_F	Total filter losses

For torodial inductors with a distributed airgab the necessary number of turns to realize a given inductance is:

$$N_L = \sqrt{\frac{L}{A_L}} \tag{5.23}$$

Where the permeance is defined as:

$$A_L = A_T \frac{\mu_0 \mu_r}{l_T} \tag{5.24}$$

By combining Amperes law:

$$N_L I_L = \frac{B l_T}{\mu_0 \mu_r} \tag{5.25}$$

And the general definition of inductance:

$$L = \frac{N \Phi}{I_L} \tag{5.26}$$

The following central relation for filter inductor design arrives:

$$B = \frac{L I_L}{A_T N_L} \tag{5.27}$$

The relation dictates the maximal allowable inductor peak current for linear operation:

$$\hat{I}_{L,\max} \leq \frac{\hat{B}_{\max} A_T N_L}{L} \tag{5.28}$$

5.4.1 Conduction losses

Conduction losses are introduced due to the finite DC impedance of any inductor. The DC impedance of the winding on a single layer toroidial inductor is:

$$R_{cu} = \frac{N_L l_V \rho_{cu}}{\left(\frac{\varnothing_{cu}}{2}\right)^2 \pi} \tag{5.29}$$

Where the average winding length is:

$$l_V = 2h + (d_O - d_I) + 4\varnothing_{cu} \tag{5.30}$$

For a single layer winding the maximal winding diameter is:

$$\varnothing_{cu,\max} = \frac{d_I \pi}{N_L} \tag{5.31}$$

The resulting conduction losses will be a superposition of the two contributions:

$$P_{cu}(I_L) = R_{cu}(I_{L,RMS}^2 + I_{T,RMS}^2) \tag{5.32}$$

5.4.2 Core losses

Due to the magnetic hysteresis power dissipation within the core material will exist. By a reasonable choice of core material, core losses are only significant in the idle situation. The core losses can be expressed as the sum of the two contributions:

$$P_{co}(I_L) = PV_T \left[\left(\frac{f_B}{f_r}\right)^{k_f} \left(\frac{B(I_L)}{B_r}\right)^{k_B} + \left(\frac{f_c}{f_r}\right)^{k_f} \left(\frac{B(I_T)}{B_r}\right)^{k_B} \right] \tag{5.33}$$

The simple expression is based on the assumption that the HF current is a sinusoidal current with amplitude $\hat{I}_T$ and frequency f_c. This is a valid assumption, since higher frequency components have considerably lower amplitude. The HF contribution can be made negligible by a suitable choice of core material. In (5.33) it is furthermore assumed that the HF induction swing is *constant* although the average induction swing is lower at high output levels. The resulting filter losses for the switching leg is the sum of the conduction loss and core loss:

$$P_F(I_L) = P_{cu}(I_L) + P_{co}(I_L) \tag{5.34}$$

5.5 Generalization to BPSC and PSC

The PSC switching power stage topology is realized by N parallel coupled switching legs. In the balanced configuration for the BPSC topology, there are N/2 parallel-coupled switching legs driving each end of the load. Correspondingly, the output current for each individual switching leg, I_{LN}, is related to the total output current I_O as:

Switching leg	PSC	BPSC
$I_{LN} = I_O$	$I_{LN} = I_O / N$	$I_{LN} = 2I_O / N$

Due to the paralleling of switching legs and balanced drive in BPSC, the required inductance in each individual switching leg, L_N, is dependent upon the number of switching legs. The paralleling of N switching legs in PSC corresponds to a paralleling of N inductors. Similarly, the balanced drive in BPSC corresponds to a series coupling of two sets of N/2 inductors. Correspondingly, the inductor L_N required for each switching leg for the general PSC and BPSC switching topologies are:

Switching leg	PSC	BPSC
$L_N = L$	$L_N = L \cdot N$	$L_N = L \cdot N / 4$

The voltage swing over the inductors, corresponding to the necessary breakdown voltage depends on power stage topology as:

Switching leg	PSC	BPSC
$2V_S$	$2V_S$	V_S

With these definitions, the general expressions for *total* semiconductor loss and filter loss in an N-leg PSC or BPSC output stage is:

$$P_D(I_O) = N \cdot [P_S(I_{LN}) + P_C(I_{LN})] \tag{5.35}$$

$$P_F(I_O) = N \cdot [P_{cu}(I_{LN}) + P_{co}(I_{LN})] \tag{5.36}$$

These expressions are general with the relationships that have been established between I_O and I_{LN} above.

5.6 Case example

A case example is considered to illustrate the efficiency level that can be achieved by a switching power stage, using the present state of technology. The synthesis of a 200W power stage is considered. The general parameters are summarized below:

Parameter	Description
$P_{O,\max}$	200W
R_L	4Ω
f_B	20KHz
f_O	$2f_B$
Q_O	$\frac{1}{\sqrt{3}}$
V_S	44V ($M_{\max}$=0.9)

f_B, f_O and Q_O represent the PMA target bandwidth, the filter natural frequency and the filter Q, respectively. The optimization is carried output using the Power Stage Optimization Tool (PSOT) that has been developed to automate PSC and BPSC power stage design. The MATLAB toolbox is described more closely at the end of this chapter. The following topologies will be optimized for this specific application:

- PSC with N=1. (i.e. a simple switching leg).
- BPSC with N=2. (i.e. a H-bridge).
- BPSC with N=4.

The power stages will be implemented with realistic switching devices and filter core materials. Throughout the investigations, it will be assumed that the junction temperature is 120°. This causes the ON impedance to be 50-60% higher than the nominal value.

5.6.1 Implementation with a simple switching leg

In this simplest possible realization the voltage requirements for the two switches is $2V_S$=88V. The power stage implementation is investigated using 100V MOSFET technology although the derating factor is low. An appropriate switch for the application is a 50mΩ/100V MOSFET type. The gate driver parameters are set at (V_G=12V, R_G=5Ω) as a compromise between losses and noise. The filter core material is low μ_r iron power with good HF characteristics. Fig. 5.3 shows the distribution and total semiconductor losses vs. output power and Fig. 5.4 shows the efficiency of the switching leg, filter and the total system efficiency. The results are summarized below.

Parameter	Description
f_c	300KHz
L_N	27 μH
$\hat{I}_{LN} = \hat{I}_O$	10A
P_Q	1W
$P_{TOT,\max}$	13.5W
Efficiency	93.5%
Energy efficiency	32%

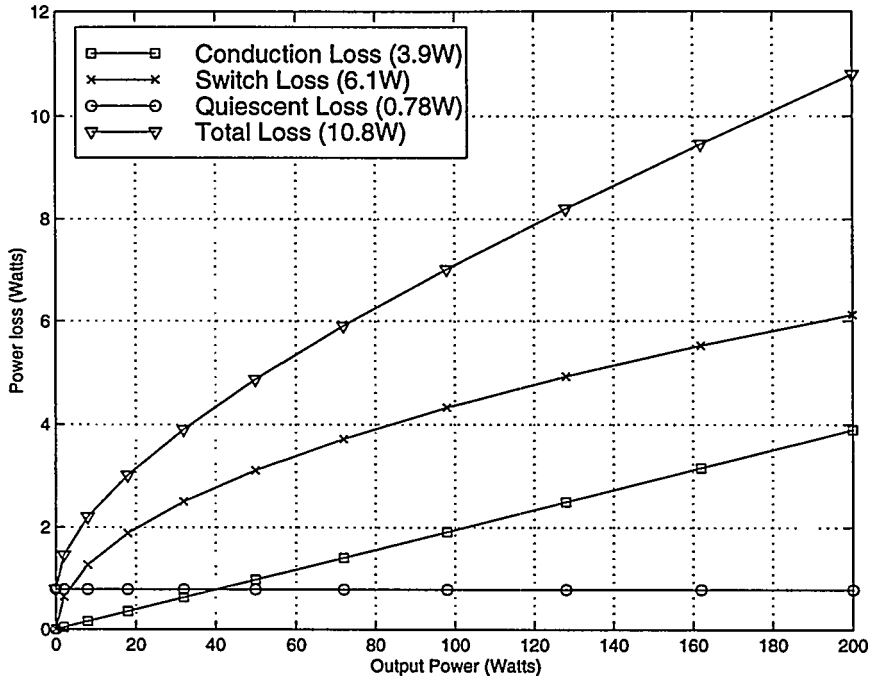


Fig. 5.3 Semiconductor losses in a switching leg implementation of the case example.

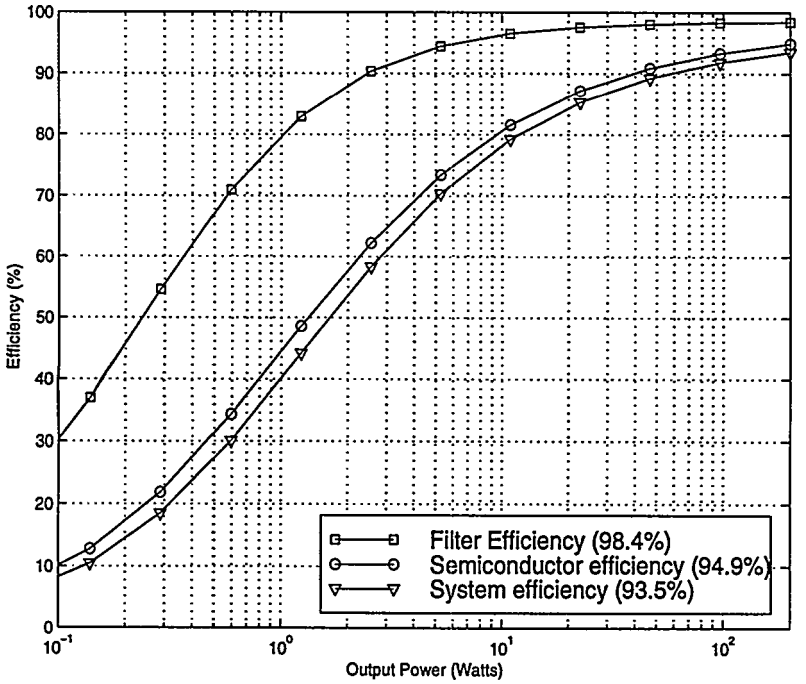


Fig. 5.4 Efficiency of the switching power stage, the filter and complete system in a switching leg realization of the power stage case example.

The energy efficiency is calculated directly from the system power dissipation as defined in chapter 1 with the specified time distribution of relative output levels. The average output power from the amplifier is thus $P_{O,AV} = 350mW$ under the given assumptions (Table 1.1), whereas the average power dissipation over time is calculated to $P_{TOT,AV} = 1.1W$. Clearly, the given realization provides a dramatic improvement in energy efficiency of more that an order of magnitude compared to conventional amplifier principles. The main reason is the optimization towards minimal power loss of only 1W at quiescence. It should be remembered however, that the losses of the other elements as driver circuitry are not included.

5.6.2 BPSC realization (N=2)

The BPSC topology with N=2 corresponds to the conventional H-bridge. The four switches all handle the same current as the switching leg for a given output, i.e. the conduction losses will inevitably increase. However, rich compensation is provided by the reduced voltage requirements for each individual switch, which is halved to $V_S = 44V$. For comparison with the switching leg, the losses in the bridge configuration have been investigated with the same parameters (i.e. components) as above. Fig. 5.5 shows the semiconductor losses in each of the two switching legs. Whereas the conduction losses in each leg are unchanged, the switching losses are approximately reduced by 50% in each leg. With four switches the switching losses remain *unchanged* whereas the conduction loss *doubles* causing the total efficiency to reduce to 91.7%. However, the lower voltage requirement means that 60V technology becomes a feasible alternative. The efficiency can be improved by a better compromise between ON-resistance and parasitic capacitance, e.g. a 25mΩ/60V. This will lead to system efficiency above 93% as for the simple switching leg. The efficiency the four transistor output stage configuration closely resemble what is achieved above by the switching leg.

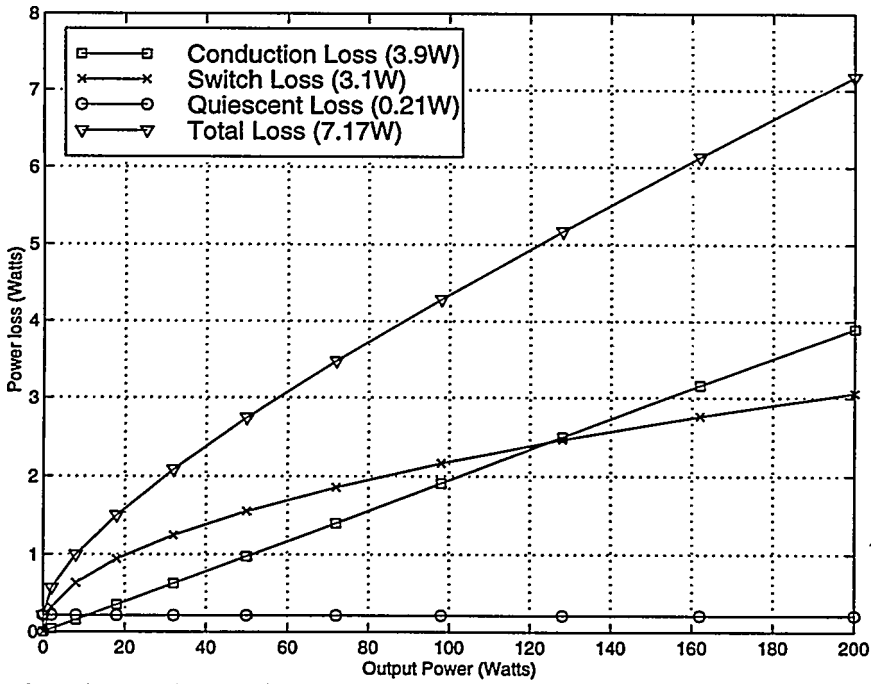


Fig. 5.5 Semiconductor losses in each of the two switching legs for the BPSC (N=2) implementation of the case example.

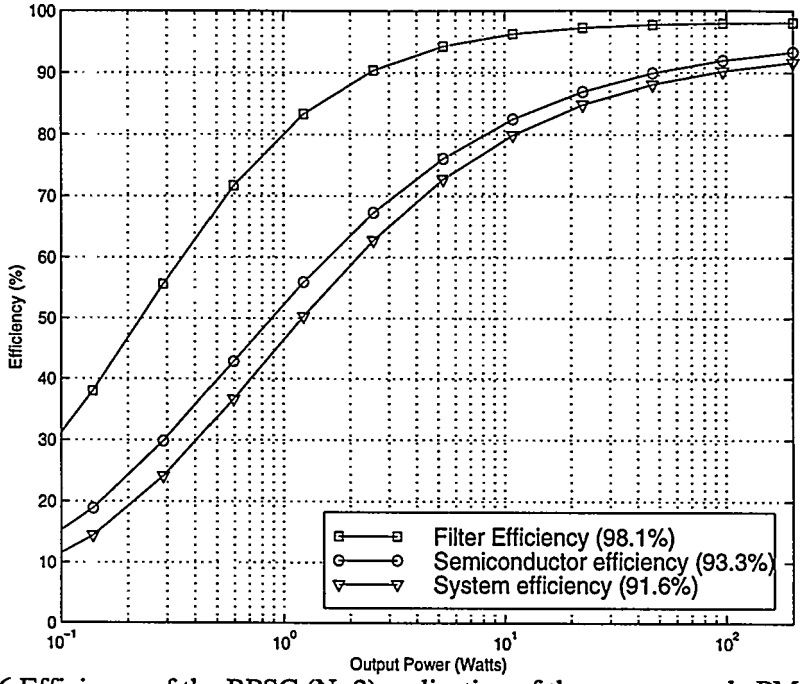


Fig. 5.6 Efficiency of the BPSC (N=2) realization of the case example PMA.

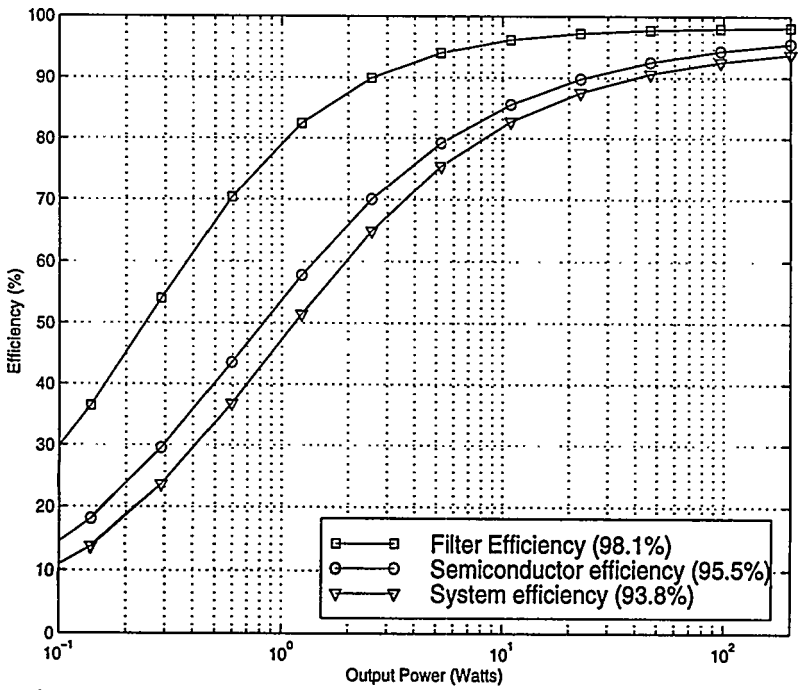


Fig. 5.7 Efficiency of the BPSC (N=2) realization of the PMA case example with optimized 60V switches.

Parameter	Description
f_c	300KHz
L_N	13.5 μH
$\hat{I}_{LN,\max} = \hat{I}_{O,\max}$	10A
P_Q	0.8W
$P_{TOT,\max}$	13.1W
Efficiency	93.6%
Energy efficiency	40%

The improvement in energy efficiency is caused by the reduced switching voltage for the parasitic output capacitance of the switches. Halving the voltage reduces the individual contributions by a factor of four in each switch.

5.6.3 BPSC realization (N=4)

The BPSC topology with *N=4* significantly changes the power loss in the individual switching legs. The peak current in each switching leg and filter inductor is *halved*, compared to both the simple switching leg and the bridge considered previously. The voltage requirement for each switch is 44V with the given specifications, independent upon N. This renders the use of 60V possible and the application of a 25mΩ/60V switch is considered.

Another essential issue of BPSC power stage optimization is the carrier frequency, which can be reduced as a consequence of the improved synthesis of the modulating signal. The carrier frequency throughout this case example is halved to 150KHz, corresponding to an effective sampling frequency of 600KHz. Fig. 5.8 shows the semiconductor losses in each of the four switching legs. Looking at the individual switching leg, switching losses are *halved* and conduction losses reduced by a *factor of four* compared with the single leg realization. The maximal power dissipation of each switch barely 600mW at the maximal output power of 200W (!). Fig. 5.9 shows the system efficiency vs. output power. Clearly, PSCPWM provides improved efficiency at higher output levels. The efficiency of 96% is extremely high for a full bandwidth, high power PMA. Essential parameters for The BPSC realization of the 200W power stage are summarized below.

Parameter	Description
f_c	150KHz
L_N	27 μH
$\hat{I}_{LN,\max} = \hat{I}_{O,\max}/2$	5A
P_Q	1.1W
$P_{TOT,\max}$	8.3W
Efficiency	96%
Energy efficiency	32%

It is important to emphasize a fundamental property of PSCPWM. Under the assumption that the switch and inductor resistance to not change with N the conduction losses in both filter and switching power stage will be *inversely proportional to N.*

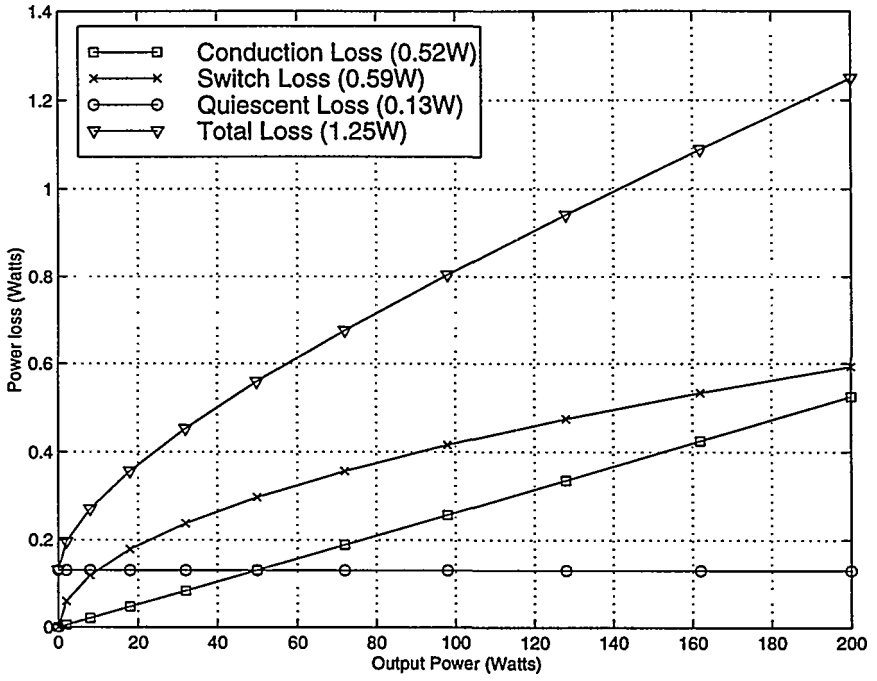


Fig. 5.8 Semiconductor loss in a single switching leg with a BPSC realization (N=4).

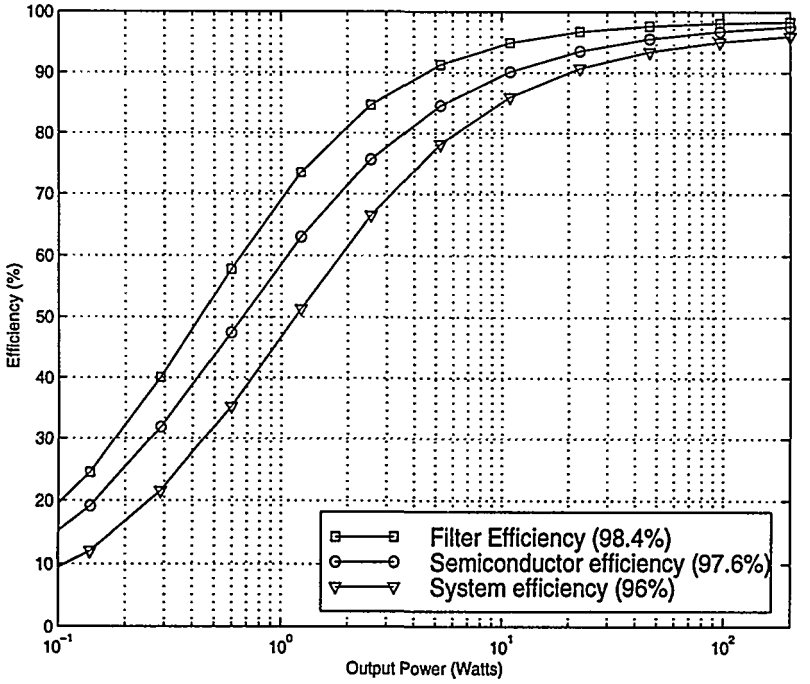


Fig. 5.9 System efficiency in a BPSC realization *(N=4)*. The excellent efficiency is achieved by a low carrier frequency minimizing switching losses and the reduced conduction losses achieved by dividing current.

5.6.4 BPSC in high power realizations

Balanced PSCPWM realized with the BPSC power stage has shown to provide both improved modulation and higher efficiency. The true potential of PSCPWM becomes apparent in higher power systems, where it gets problematic or even impossible to implement the power conversion stage with a bridge or a switching leg. PSCPWM is a very elegant solution in this case. This will be demonstrated by considering an 800W power stage, suitable for e.g. general-purpose professional power amplification. Besides the wider power range, the fundamental parameters from above are left unchanged. With $N = 4$ the following is achieved with the BPSC 800W power stage:

Parameter	Description
V_S	88V
f_c	150KHz
L_N	27 μH
$\hat{I}_{LN,\max}$	10A
P_Q	4W
$P_{TOT,\max}$	43W
Efficiency	95%
Energy efficiency	35%

Fig. 5.10 shows the power loss in a single switching leg with 50mΩ/100V MOSFET technology. The stress of each individual switching leg is minimal.

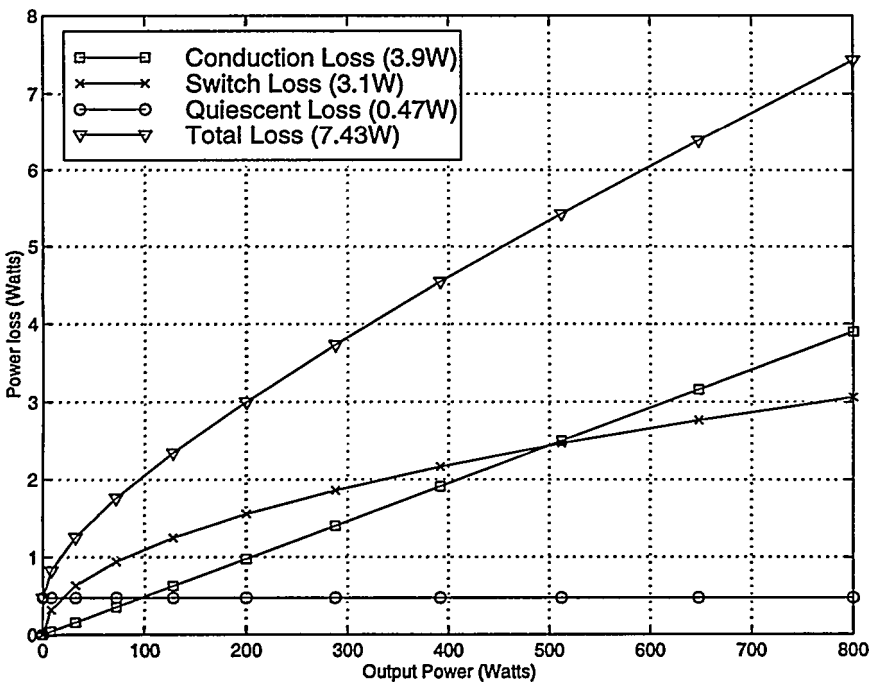


Fig. 5.10 Semiconductor loss in one of the switching legs in a 800W BPSC (N=4) case example. The stress of each individual switching leg is minimal even at full load.

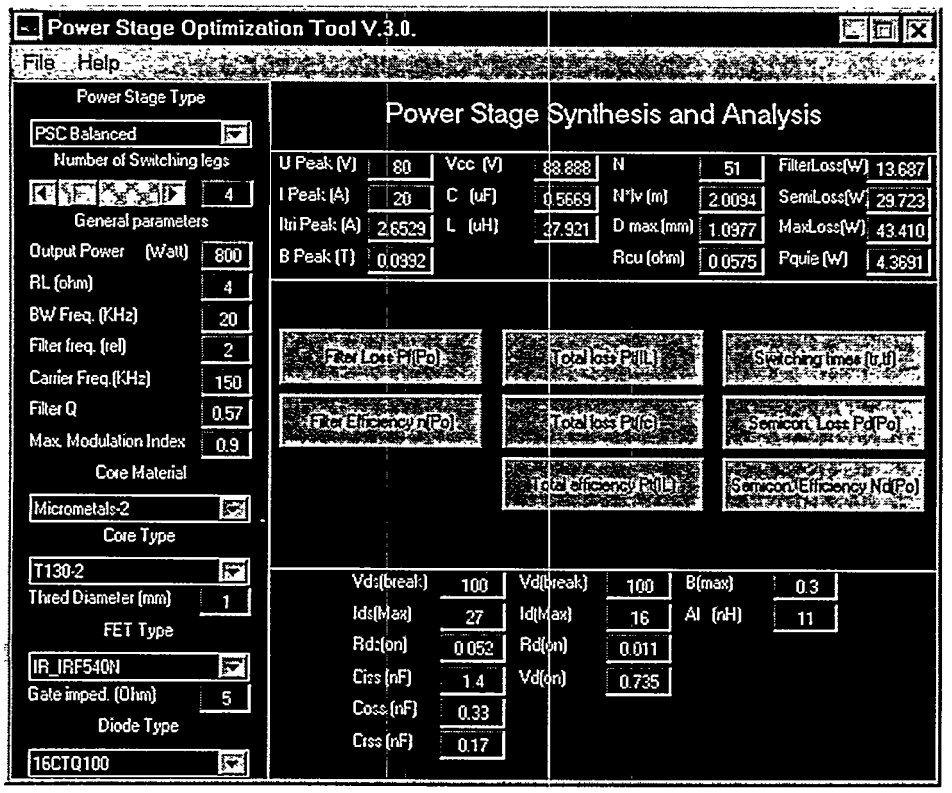
5.7 Summary

This chapter was devoted to efficiency optimization in the switching power stage of PMA systems. The contributions to power dissipation within output stages has been investigated and general analytical expression for power dissipation in PSC and BPSC switching power stages has been derived. The increasing number of power components in the general PSC and BPSC topologies was shown not to compromise efficiency. On the contrary, improvements in efficiency are generally possible. It is important to emphasize a fundamental property of PSCPWM. Under the assumption that the parasitic MOSFET and inductor resistance does not change with N, the conduction losses in both filter and switching power stage will be *inversely proportional to N.* Furthermore, switching losses are reduced as a consequence of the lower switching frequency and lower current in each switching leg.

Case examples has been investigated, showing the excellent efficiency and energy efficiency that can be achieved by the present state of technology within the field of power switching devices and magnetics. To conclude, in practical PMA applications within the range of a few hundred watts of output power, the heat sink will virtually be eliminated. Furthermore, the energy efficiency can be improved by an order of magnitude.

5.7.1 PSOT – A MATLAB toolbox for power stage optimization

Power stage optimization is a tedious process since the various loss contributions depend on a range of parameters. A power stage optimization toolbox has been developed for MATLAB [Ch98], [Fr98] for swift and automated power stage synthesis of the general PSC and BPSC topologies. The toolbox is GUI controlled with push button access to all essential functions. The GUI is shown below.



The "shap-shot" corresponds to the 800W BPSC realization that was considered in the chapter. Controllable parameters on the GUI are:

- Topology (PSC, BPSC)
- Number of switching legs
- General parameters as Output power, Load impedance, ...
- Core material (selected from a library)
- MOSFET (selected from a library)

Based on these input specifications the output panels provide all interesting parameters. The push buttons provides access to various parametric investigations of power stage loss and efficiency.

Part III

Chapter 6

Robust Linear Control

Recall from Chapter 4, that there are significant difficulties in maintaining modulator performance throughout the power conversion stage. It is essential to reduce the sensitivity to the diverse non-ideal effects, in order to improve performance and make system design practical. Obviously, the fundamental design goal must be a perfect reproduction of the amplified reference such that demodulated output is proportional to the input, within the bandwidth on interest. This should be achieved independent on any non-ideal effects within the fundamental elements of the PMA, i.e. the modulator, switching power stage and filter.

This chapter is devoted to the application of robust linear feedback control methods to analog PMA systems. This introduces a wide range of new aspects to PMA design as the selection of control variables, control configurations, parameter optimization, i.e. control systems introduce various new degrees of design freedom. This newfound freedom adds flexibility to the system optimization, and one question comes to mind: Is there an optimal control topology specifically for PMA systems? Unfortunately, this proves to be a very difficult question to answer, simply because optimal performance is not a well-defined concept, given that perfect reproduction of the reference can never be reached anyway. The task of control system design is to achieve best compromises and tradeoffs between performance criteria, complexity, bandwidth, efficiency etc. Due to the degrees of freedom, there will been and wide set of seemingly indifferent configurations and parameter sets that will yield comparable results.

Specific objectives for the application of linear control to PMAs are:

- Minimization of all effects of non-linear behavior in terms of distortion, noise and intermodulation within the complete operating range of the power amplifier.
- Stabilization of frequency response and the amplifier gain.
- Simplified power supply design leading to a lower system complexity.
- Improved efficiency. The power stage can be optimized isolated for efficiency with much less focus on open loop linearity performance with efficient control.
- Improved robustness. The control system should provide a natural correction of variations due to spread in production, aging, temperature variations etc.

Applying feedback control also introduces the potential problem of instability, which can have serious effects as loudspeaker and amplifier failure. Nevertheless, control systems is considered an essential aspect of PMA system design.

A simple methodology for robust control system design will be developed in this chapter, founded on initial studies of the control object or plant. Three different control structures are defined and controller synthesis methods for the structures presented. Case examples are presented to evaluate the robust control methods.

6.1 Terminology

Consider the one degree of freedom system in Fig. 6.1, where r is the reference input, n is the forward path noise referred to the output and d represents the disturbance noise that is introduced in the output measurement. The compensator C manipulates u such that the output y has the desired characteristics. A represents the *plant* to be controlled and the B compensator serves to manipulate the output feedback. From the system block diagram the closed loop response are easily derived. The output is a superposition of three contributions:

$$y = \frac{CA}{1+CAB} r + \frac{1}{1+CAB} n + \frac{CAB}{1+CAB} d \tag{6.1}$$

The following general terminology will be used throughout the following:

Parameter	Definition	Description
L	CAB	Loop transfer function
H	$\frac{CA}{1+CAB}$	Closed loop transfer function
S	$\frac{1}{1+CAB}$	Sensitivity function
T	$\frac{CAB}{1+CAB}$	Complementary sensitivity function

The term sensitivity is very natural since S represents the sensitivity reduction afforded by feedback. Assuming at this point that an error source within the plant can be modeled by an additive parameter ε, the sensitivity of A to ε is:

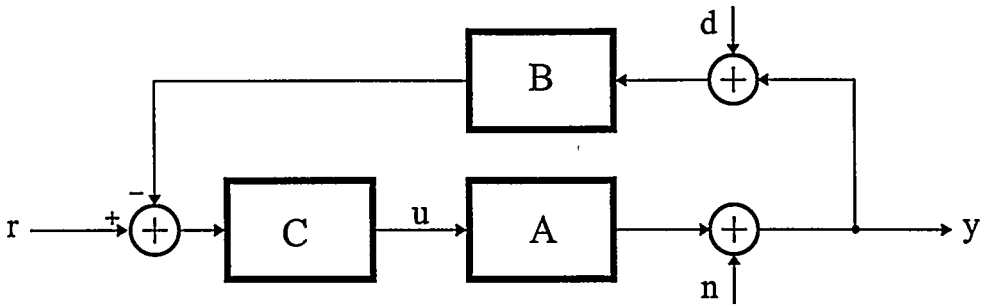


Fig. 6.1 One degree of freedom feedback control system.

$$S_{\varepsilon}^{A} = \frac{\frac{dA}{A}}{\frac{d\varepsilon}{\varepsilon}} = \frac{\varepsilon}{A}\frac{dA}{d\varepsilon} \tag{6.2}$$

without control. For the system controlled by the loop the sensitivity is accordingly:

$$S_{\varepsilon}^{H} = \frac{\frac{dH}{H}}{\frac{d\varepsilon}{\varepsilon}} = \frac{\varepsilon}{H}\frac{dH}{d\varepsilon} = \frac{\varepsilon}{H}\frac{\partial H}{\partial A}\frac{dA}{d\varepsilon} \tag{6.3}$$

By partial differentiation combined with trivial reductions S_{ε}^{H} is reduced to:

$$S_{\varepsilon}^{H_{cl}} = \frac{\varepsilon}{A}\frac{dA}{d\varepsilon}\frac{1}{1+CAB} = \frac{1}{1+CAB}S_{\varepsilon}^{A} \tag{6.4}$$

The loop thus reduces the sensitivity towards any error by the factor $1+CAB$ exactly corresponding to the sensitivity function S. Note the fundamental relation between sensitivity and complementary sensitivity:

$$S+T=1 \tag{6.5}$$

Since the optimal values of both S and T are zero (corresponding to total noise immunity), (6.5) adds a fundamental constraint on the controller optimization, since the ideal case can never be reached in practice.

6.1.1 Evaluating control system performance

Control system performance can be evaluated in both time and frequency domain. Here the focus will be on frequency domain performance with the established maximal peak or infinity norm of the sensitivity function:

$$\|S\|_{\infty} = \max_{\omega}|S| \quad \forall\omega \tag{6.6}$$

The sensitivity to all disturbance inputs are reduced corresponding to the sensitivity function S, the following parameter:

$$S_M = \max_{\omega}|S| \qquad \forall\omega \ \textit{within PMA target bandwidth} \tag{6.7}$$

is an important performance parameter. The maximal peaks criteria are closely related to the gain and phase margins:

$$G_m = \frac{1}{|L(j\omega_{180})|} \qquad P_m = L(j\omega_u) + 180^o \tag{6.8}$$

Where ω_{180} is the phase crossover frequency, i.e. point where L crosses the negative real axis between –1 and 0. ω_u is the gain crossover frequency or the unity gain frequency where $|L|$ first crosses 1. The margins are related to $\|S\|_\infty$ as [Sk96]:

$$G_m \geq \frac{\|S\|_\infty}{\|S\|_\infty - 1} \qquad P_m \geq 2\arcsin(\frac{1}{2\|S\|_\infty}) \geq \frac{1}{\|S\|_\infty}(rad) \tag{6.9}$$

A $\|S\|_\infty$ specification makes specifications on gain and phase margins unnecessary. The relationship between important values of $\|S\|_\infty$ and the minimum gain and phase margins are:

$\|S\|_\infty$	$\min(P_m)$	$\min(G_m)$ (deg)
1	∞	60°
1.5	3	40°
2	2	30°
3	1.5	20°

$\|S\|_\infty < 1$ indicates that the system never reaches phase crossover corresponding to excellent stability.

Besides the quality of the loop response, the speed in terms of *bandwidth* is also a very important in understanding the benefits and tradeoffs involved when applying feedback control. The literature gives several definitions of bandwith of a control system. The following exclusively uses the *gain crossover* frequency or *unity gain frequency* f_u to define the bandwidth of the PMA system.

6.1.2 Control system representation and optimization

In practice, the controller design may be carried out by shaping of transfer functions, either loop transfer functions or closed loop transfer functions. For true Multiple Input Multiple Output (MIMO) systems, the Glover McFarlane H_∞ [Sk96] optimal control is a widely used. The method is an extension of classical loop shaping where optimization is used to make an initial loop-shaping design more robust. Shaping of closed loop transfer functions is based on objectives for S and/or T to reach the desired specifications. An alternative and widely used method is the signal-based approaches, as the widely used Linear Quadratic Gaussian (LQG) control method. In addition, there are numerical optimization methods with direct multi-objective optimization, where it is attempted to directly optimize the true objectives of the controller. Throughout Part III of this thesis, classical loop shaping has been found most appropriate to realize the performance objectives. The PMA should be considered a Single Input Single Output (SISO) system with one primary input and output. The sensitivity function S is shaped in terms of bandwidth and slope using classical methods. The system representation used throughout the analysis is the "classical" transfer function. State space representation, often used to represent MIMO systems, does

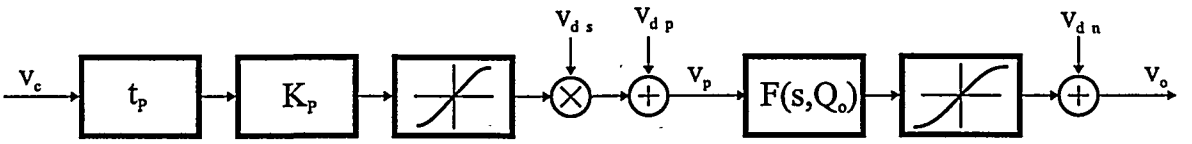


Fig. 6.2 Non-linear model.

not provide any additional advantages in PMA systems, again due to the inherent SISO character with multiple disturbances.

6.2 Robust control system design for PMAs

Control system design generally involves an iterative process of steps in terms of plant modeling, control structure design, controller synthesis, control system analysis in terms of performance and robustness and finally non-linear simulation. A control system is *robust* if it is insensitive to differences between the actual system and the model of the system that was used to design the controller. The following investigates various aspects of robust controller design specifically for PMAs.

6.2.1 System model

All control problems starts with a detailed investigation on the *plant* on which the control system is applied. Fig. 6.2 shows a model of the PMA plant consisting of the non-linear modulator, power stage and demodulation filter. The first block represents the inevitable delay t_P throughout the system that arises due to propagation delays within the fundamental elements. The Laplace transform is:

$$e^{-t_P s} \tag{6.10}$$

The time delay is critical since it causes a frequency dependent phase shift, i.e. the order of the plant is inherently infinite (!). The following block represents the equivalent gain K_P from the modulator input v_c to the fundamental component of the switching power stage output $\tilde{v}_p$, i.e. the relationship between the input to output amplitude relationship:

$$K_P = \frac{\tilde{v}_p}{v_c} \tag{6.11}$$

In practice, both the modulator and specifically the power stage will behave as dynamic-nonlinear systems as shown in Chapter 4. The non-linearity is reasonably low below clipping but rises rapidly when over modulation occurs, i.e. the power stage block has a limiting characteristic. Thus, over-modulation reduces the effective gain of the system. Non-linearity and noise within the power conversion process are modeled as additional disturbance v_{dn} input referred to the output. The disturbance input v_{ds} represents the perturbation on the power supply that will multiply with the modulating signal as shown in Chapter 4.

The disturbance input v_{dp} represents the HF power output, constituted by harmonics of the carrier and IM-components between the carrier and modulating signal. As widely illustrated in Chapter 3, this noise generator varies considerably with modulation method. The level of noise is can be significant, e.g. the signal to noise ratio on the switching power stage output is best case *unity* e.g. with NBDD PWM and the preferred PSCPWM

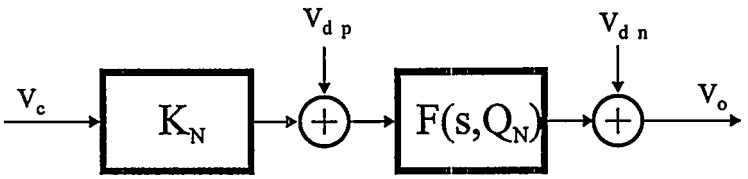


Fig. 6.3 Simplified linear model.

schemes, but in general *negative* (!). Fortunately, the noise energy is concentrated well beyond the target frequency range with a proper selection of carrier frequency. Still, v_{dp} generally influences control system performance since measured variables for feedback control, are superposed by components of this HF generator. This may compromise the performance of the control system. The filter $F(s,Q_o)$ is assumed of second order filter throughout the following:

$$F(s,Q_o)=\frac{\omega_o^2}{s^2+\frac{\omega_o}{Q_o}s+\omega_o^2} \tag{6.12}$$

Q_o depends on the load impedance, which is a variable "external" parameter.

6.2.2 Uncertainty and robustness

Independent on the level of modeling *uncertainty* will always exist on certain parameters, due to external parameter variations, non-linearity and changes in operating conditions as e.g. temperature. Furthermore, the measurement of control variables may be compromised by sensor imperfections etc. The different sources of model uncertainty may be grouped into the two main classes, parametric uncertainty referring to uncertainties in a known model (component tolerances etc.) and neglected dynamics referring to missing information. This missing information may be due to deliberate ignorance or a lack of understanding of the physics. Any model will have this source of uncertainty, especially at higher frequencies. It is advantageous to simplify the model in Fig. 6.2 to the nominal model in Fig. 6.3, and treat all other non-ideal elements as model uncertainty. This simplification of the plant leads to much simplified controller design. Two concepts are essential in combination with the nominal model:

The Nominal Stability (*NS*) criterion
A control system obeys *NS* if the nominal system is stable:

$$NS \overset{def}{\Leftrightarrow} \textit{Nominal system stable} \tag{6.13}$$

The Nominal Performance (*NP*) criterion
A control system obeys *NP* if the system satisfies the desired performance specifications. In the most general form *NP* can be defined as:

$$NP \overset{def}{\Leftrightarrow} \left\|\omega_p S\right\|_\infty < 1 \tag{6.14}$$

Where ω_P is a performance weight that represents the desired performance. The definition of *NP* can equally be based on a separation of the stability characteristics and the

performance within the target frequency band, i.e. direct specifications on S_M and $\|S\|_\infty$ as e.g.:

$$NP \overset{def}{\Leftrightarrow} \|S\|_\infty < 1 \quad \text{and} \quad S_M \leq S_{\max} \tag{6.15}$$

This separation will be used widely throughout the investigation of various control structures. A control system is *robust* if it is insensitive to differences between the actual system and the model of the system that was used to synthesize the controller. The approach to robust control systems design is simply to define an Uncertainty Set (*US*) and following secure that the controller when designed obeys Robust Performance (*RS*) and Robust Stability (*RP*) for all plants within this *US*. The exact definition of the important concepts of *US, RS, RP* are given in the following.

Uncertainty Set (*US*)
The Uncertainty Set (*US*) is a mathematical description of the tolerances and uncertainties within the plant, such that the nominal plant and the *US* together represent the physical plant best possible in all situations.

The Robust Stability (*RS*) Criterion
If the system remains stable for all perturbed plants within the *US*, the system is said to obey the Robust Stability (*RS*) criterion:

$$RS \overset{def}{\Leftrightarrow} System\ stable \forall L_p \tag{6.16}$$

L_p indicates the complete as of perturbed loop transfer functions within the defined uncertainty set.

The Robust performance (*RP*) Criterion
If *RS* is satisfied, the system is said to obey Robust Performance (*RP*) if the defined performance specifications for perturbed plants are met for *all* plants within the *US*. This can be expressed by a performance weight as:

$$RP \overset{def}{\Leftrightarrow} \|\omega_p S_p\|_\infty < 1 \tag{6.17}$$

Or alternatively:

$$RP \overset{def}{\Leftrightarrow} \|S_p\|_\infty < 1 \quad \text{and} \quad S_{M,p} \leq S_{\max} \tag{6.18}$$

S_p represents the complete as of perturbed sensitivity functions within the defined *US*.

6.2.3 Defining the Uncertainty Set (*US*)

The definition of the *US* is considered in the following. The propagation delay through fundamental blocks may vary widely. However, by appropriate design it will typically be in the area $t_P = 100ns$. A worst case perturbation of $t_P = 200ns$ is defined to include slow

switching and ZVS switching in the power stage. Subsequently, the uncertainty on t_P is defined as:

$$t_P \leq 200ns \tag{6.19}$$

Perturbations on the power supply influence the effective gain K_P. The perturbations on K_P may be significant due to e.g. tolerance on the mains voltage, DC errors on non-stabilized power supplies etc. K_P is also affected (reduced) if the output stage is clipping or the filter enters saturation. This source of uncertainty can be controlled by bounding the input. The uncertainty on K_P is defined as a multiplicative uncertainty:

$$K_P = K_{PN} r_K, \quad 0.5 \leq r_K \leq 1.5 \tag{6.20}$$

This uncertainty on K_P will allow large-scale perturbations on the power supply and mains voltage etc. Nevertheless, perturbations in this range will be present in many applications (worst-case). Another important parametric uncertainty is the filter Q that depends on the load applied to the system. This uncertainty is equally represented as a multiplicative uncertainty:

$$Q_0 = r_Q Q_{oN}, \qquad r_Q \leq 4 \tag{6.21}$$

r_Q is specified from practical experience on the range of typical loudspeaker loads.

The non-linearity caused by both the power stage and filter generates harmonic distortion components, which are modeled as disturbance input as long as the power stage is not directly clipping and the filter is not saturating. Similar, the power supply perturbation generates disturbance input in terms of intermodulation components. Other uncertainties cover tolerances on filter components, uncertainties within the controller, in terms of tolerances on components and neglected high frequency dynamics. Furthermore, there will be limitations in terms of the dynamic range of controller elements. Finally, the HF-components will introduce noise on control variables and functions. Not all these effects can be well predicted from theory, but has to be supported by non-linear simulation and practical investigations. The three defined uncertainties are by far the most important and the robustness investigations henceforth will be based on this defined *US*.

6.3 Control system design methodology

It is appropriate to have consistent approach for design, verification and comparison of control systems for PMAs. In the following, such a generalized methodology for control system design is presented, followed the presentation of a step-wise controller synthesis methodology that will be used widely throughout the thesis to design and evaluate various control systems. The block diagram in Fig. 6.4 illustrates the concept of the design methodology. The initial STEP A involves an investigation of the plant disturbances in terms of distortion, noise, intermodulation etc. This is the foundation for the selection of an appropriate control topology, and the definition of appropriate performance specifications. It should be emphasized that the performance of the plant may vary widely dependent upon e.g.:

- Power range.
- Bandwidth (e.g. required carrier frequency).

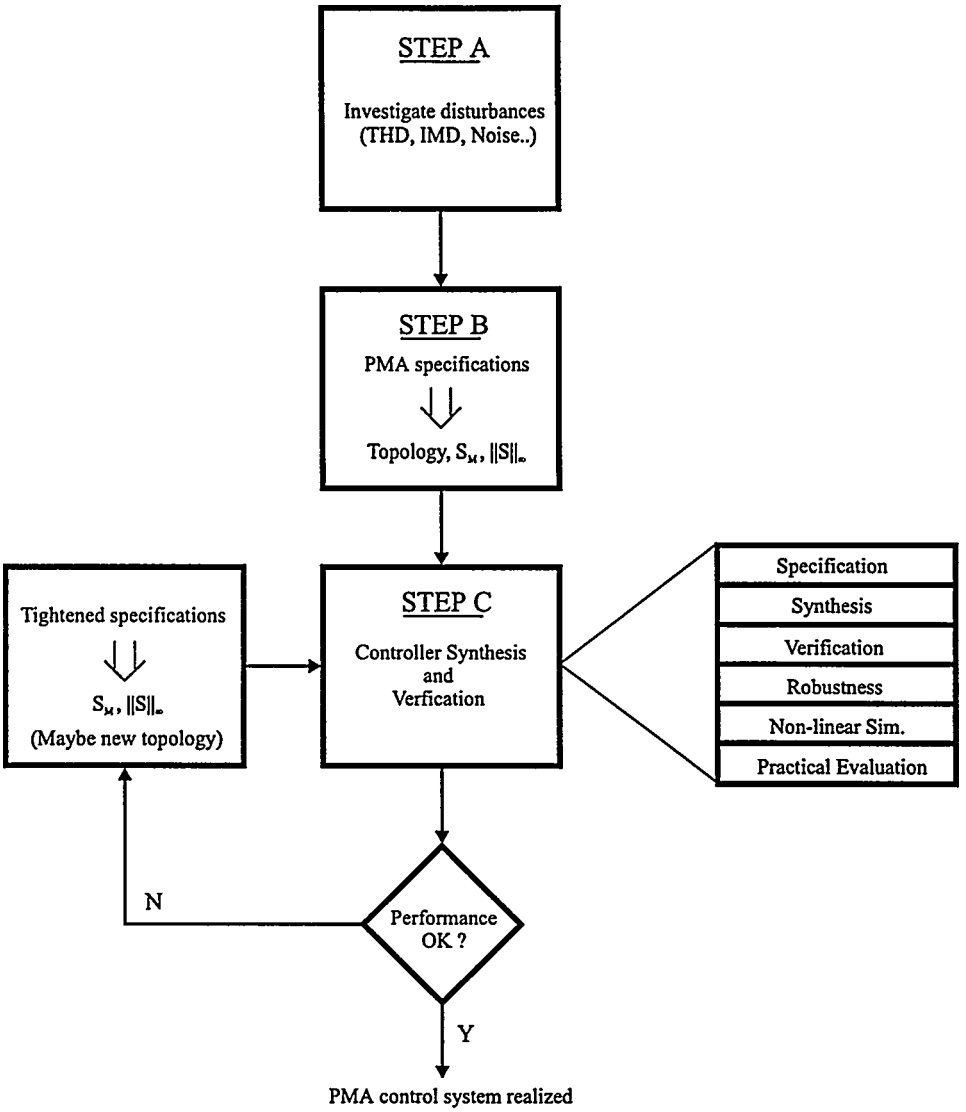


Fig. 6.4 General PMA control system design methodology

- Implementation technology (discrete, integrated).
- The power supply (stabilized, non-stabilized).
- Demodulation filter implementation (linearity etc.)

In STEP B, the desired PMA specifications, combined with the studies of the plant, lead to a selection of an appropriate control topology from the set of control topologies that are presented throughout the subsequent sections and chapters (Part III). STEP B also involves the determination of appropriate performance specifications $(S_M, \|S\|_\infty)$ as input specifications to the actual controller design process. Based on the input specifications, the controller is synthesized and the resulting system subjected to an evaluation process evaluation. This can be carried out effectively using a six-step synthesis and verification methodology that is discussed in more detail below. In the case, that the resulting prototype does not realize the expected performance, STEP C is repeated with modified specifications or e.g. by investigating a more powerful control topology.

6.3.1 Generalized controller synthesis and verification

A general approach to controller synthesis based on primary input specifications $(S_M, \|S\|_\infty)$ is specified in the following. This involves a six-step process of controller synthesis combined with linear and non-linear evaluation.

STEP 1 – Design specifications
The fundamental system parameters are specified. This covers:

- The amplifier bandwidth f_b.
- The nominal gain K_{PN}.
- The desired system gain K.
- The demodulation filter nominal Q, Q_{oN}.
- The demodulation filter natural frequency, f_o.
- Performance specifications $(S_M, \|S\|_\infty)$, possibly combined with shape of S, bandwidth limitations or other specific requirements.

STEP 2 – Synthesis of the nominal system
The nominal controller is synthesized. This covers the synthesis of the individual sub-controllers to reach the desired performance and stability goals, based on simple loop shaping in the frequency domain. This step is not necessary a simple process, given the design freedom that exists in controller design. Subsequently, general frequency normalized loop shaping methods will be presented for all considered topologies to *automate* the controller synthesis. Generalized controllers will be developed for each of the considered control topologies to meet generalized performance and stability goals that will be defined below.

STEP 3 – Verification of the nominal system
Verification of the system can be performed in the frequency domain and time domain. This may involve frequency domain investigations of loop transfer functions, closed loop transfer functions, sensitivity functions, and controller signal transfer functions. Time domain investigations may include stability investigations in terms of transient response and overload. The *NS* and *NP* criteria are verified.

STEP 4 – Robustness properties
The robustness of the controller is verified by investigating the effects of uncertainties on performance *RP* and stability *RS*.

STEP 5 – Low level verification using non-linear simulation
A non-linear simulation of the system is carried out in the time domain using PSPICE to verify controller performance at a low cycle-cycle level with actual disturbances. The non-linear simulation is a very powerful method to verify the functionality and performance of the controlled PMA at a very low circuit level. The non-linear simulations generally includes:

- A fundamental functional verification.
- Correction of Pulse Timing Errors (PTE).
- Correction of Pulse Amplitude Errors (PAE).
- Stability and robustness investigations.
- Carrier frequency optimization.

Other important factors as limiting effects, compensator non-idealities and the effects of switching noise may successfully be investigated using a non-linear simulation model.

STEP 6 – Implementation and practical verification
The control system is implemented in hardware, to verify the expected improvements offered by the control system.

6.3.2 Generalized performance considerations

The following generalized performance criteria are defined for PMA systems:

$$NP \overset{def}{\Leftrightarrow} \|S\|_\infty \leq 1.5 \quad \wedge \quad S_M < S_{\max} \tag{6.22}$$

$$RP \overset{def}{\Leftrightarrow} \|S_p\|_\infty \leq 3 \quad \forall L_p \quad \wedge \quad S_M < S_{\max} \tag{6.23}$$

The argumentation for these generalized performance criteria is as follows:
The limit on the nominal plant $\|S\|_\infty < 1.5\,(3.5dB)$ corresponds to 'good' stability properties, and generally this limit is sufficient to also obey *RP* within the defined *US*. Perturbed plants will exhibit higher $\|S\|_\infty$ in worst-case situation. The constraint on perturbed plants $\|S_p\|_\infty \leq 3\,(9.5dB)$ is important to have a good safety margin to instability. Both (6.22) and (6.23) constrains the degrees of freedom in loop shaping. Performance specifications for the sensitivity function within the target frequency band generally involve the maximum specification $S_M < S_{\max}$, possibly combined with a desired frequency shape. Since THD on most plants will be independent on frequency, it is generally appropriate with a constant maximum specification within the target frequency band. $S_{\max}$ is simply determined as a the *relationship between the desired closed loop disturbance and the observed disturbance* levels within the plant. Other effects as severe intermodulation caused by e.g. a non-stabilized power supply may necessitate a lower sensitivity to errors at lower frequency where the errors from the power supply will dominate due to larger signal levels.

6.3.3 General loop shaping constraints

The loop shaping involves explicitly shaping the magnitude of the loop transfer functions such that the performance objectives for the sensitivity function are realized. Besides the already discussed constraint, there are several other limitations to consider in the loop shaping process.

Loop bandwidth limitations
Due to carrier frequency limitations and the general difficulties of wide band control, the bandwidth of the control system will be constrained. As a compromise between efficiency and performance the general limitation for bandwidth limit is (normalized to the target bandwidth f_b):

$$f_u \leq 10 \tag{6.24}$$

Higher bandwidths may be realized in e.g. dedicated applications, where the PMA target bandwidth is low. In the general case however, the (6.24) is a suitable constraint since it will represent a reasonable compromise between loop performance and carrier frequency.

Slope limitations
Further constraints exists on the slope of the loop transfer function:

$$N_L = \frac{d(\ln|L|)}{d(\ln(\omega))} \tag{6.25}$$

To obey *NS*, N_L has to be lower than -2 around the unity gain point. For *RS* and *RP* to hold, the slope has to be lower. Generally, a slope of $N_L = -1.5$ at the unity gain point is appropriate.

Switching Noise and Slew Rate Instability (SRI)
Another essential constraint is the HF disturbance source v_{dp} that will superpose all control variables. Of particular importance is the HF residual superposing the modulating signal $v_{c,dp}$. The transfer function from v_{dp} to the modulator input is:

$$\frac{v_c}{v_{dp}} = \frac{L(s)}{K_{PN}} \tag{6.26}$$

The HF residual may spoil the modulator function by introducing *Slew Rate Instability (SRI)*, when the slew-rate of the HF residual on the modulating signal exceeds the slew-rate of the carrier:

$$SR_{\hat{v}_{c,dp}} < SR_{carrier} \tag{6.27}$$

This kind of instability should be prevented since a PMA operating under SRI is unreliable. It is desirable to minimize both the amplitude and slew-rate of $v_{c,dp}$ such that (6.26) holds with a reasonable margin. This can be carried out by:

- Carrier frequency tuning.
- Choosing modulation methods with attractive HF-characteristics as NBDD or PSCPWM. In Chapter 2, it has been shown that PSCPWM yields an apparent sampling frequency $f_s = N \cdot f_c$.
- Applying tuned circuits to the control system (notch filters) to eliminate the component that causes Slew-Rate Instability.

Generally, the effect of the HF residual on the modulating signal is a slightly degraded performance, although theory suggests that a switching residual should not effect performance. Modulating the carrier frequency itself does generate components within the target frequency band for any of the considered modulation schemes in Chapter 2. Note that optimizing for minimal HF residual will compromise the control bandwidth.

Other considerations
For optimal control system design, further practical considerations are necessary:

- The controller should be simple in implementation with standard components, low tolerances etc.
- Control signals should be well conditioned throughout the control structure, such that no controller signals are buried in noise.

- The bandwidth requirements for the controllers should be as low as possible. It can be bound with considerable difficulty to realize wide-bandwidth controller with e.g. high gain at high frequencies.

Clearly, controllers for PMA systems are constrained by a broad range of limitations.

6.3.4 Definition of linear control structures

Control structure design involves the selection of controlled outputs, measured and manipulated variables, control structure (or topology) and controller type. The controlled output is simply the amplifier output v_o. Three output stage variables are considered as measured variables for the controller:

- The power stage output v_p.
- The filter inductor current i_L
- The PMA output v_o.

The control configuration or topology refers to the restrictions imposed on the overall linear controller by decomposing it into a set of local controllers (sub-controllers, units, elements and blocks) with predetermined links. Three linear control topologies are investigated in the following:

Voltage Feedback Control - Topology 1 (VFC1): This is the "obvious" structure where the output voltage v_o is the only measured variable. The controller is subdivided in three elements, a forward path compensator $C(s)$, a feedback path compensator $B(s)$, including attenuation in order to provide the desired closed loop gain and an initial reference shaper $R(s)$ to stabilize the high frequency dynamics. The topology will in the following be referenced to as Voltage Feedback Control – type 1 (VFC1).

Voltage Feedback Control Topology 2 (VFC2): The structure also only uses a single measured variable, which is the "local" switching power stage output v_p. The controller is subdivided in three elements similar to topology 1. The topology will in the following be reference to as Voltage Feedback Control – type 2 (VFC2).

Current – Voltage Feedback Control Topology (CVFC): The control structure uses two measured variables, i_L and v_O. The multivariable controller is subdivided in five elements, two forward path compensators $C_C(s)$ and $C_V(s)$, and two feedback path compensators $B_C(s)$ and $B_V(s)$. Finally, a pre-compensator $R(s)$ serves to stabilize the high frequency dynamics. The topology will be referenced to as the Current Voltage Feedback Control (CVFC) topology.

A comprehensive study of previous work including the patent literature three decades back clearly illustrates the lack of fundamental research in control system for PMA systems. The methods applied previously are related to VFC1 or VFC2 in terms of feedback source, e.g. control topologies related to VFC2 are very well known in various configurations [At78], [At83], [Pa88], [Ha91], [Ha97]. Control configurations related to VFC1 has also been investigated previously in various configurations in e.g. [Pa88], [Ni97d]. CVFC is a new improved control topology that has been developed in the present work in [An95], [An97] and [Ni98a].

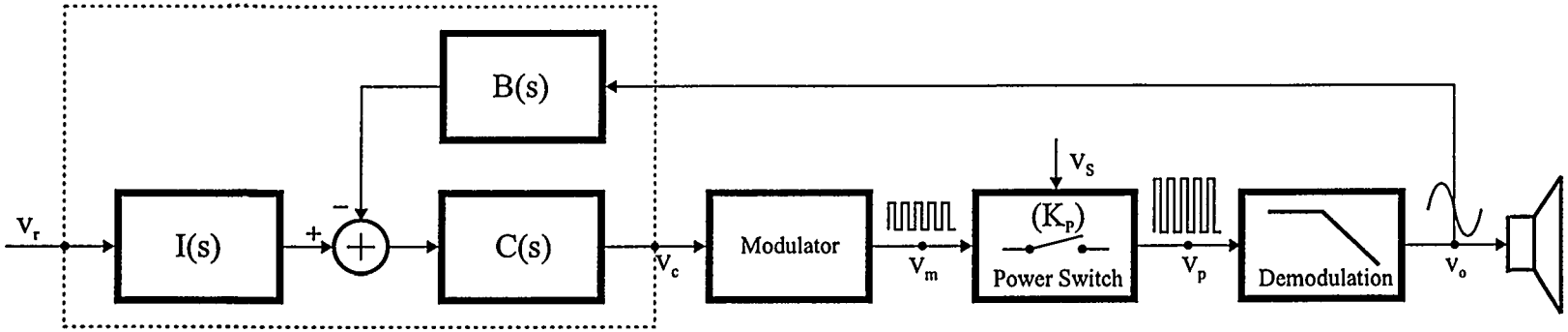


Fig. 6.5 Definition of the VFC1 Topology with three sub-controllers *B(s)*, *C(s)* and *R(s)*.

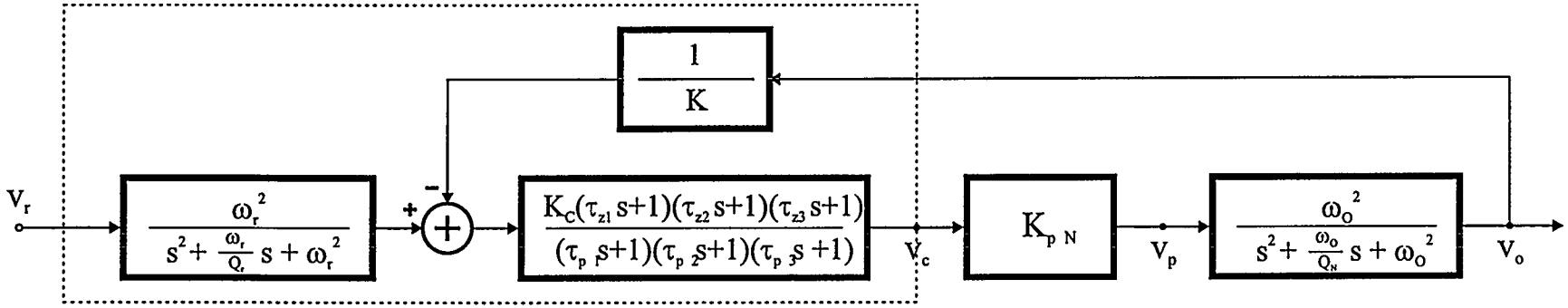


Fig. 6.6 VFC1 linear model with compensators defined.

6.4 Voltage Feedback Control Topology 1 (VFC1)

The VFC1 topology is defined in Fig. 6.5 and Fig. 6.6 shows a linear model for the system with the compensators defined. A general frequency normalized loop shaping approach will be presented in the following, corresponding to automation of STEP 2 in the general methodology for controller synthesis and verification, that was specified above. The degrees of freedom are minimized to simplify the controller design and minimize the requirements for tedious iterations. Fundamentally, the only input specification is S_M or alternatively the loop bandwidth f_u. Again, it should be emphasized that no unique controller exists for any application. The presented control structure and controller synthesis method excels by providing pleasant stability and performance characteristics in the general case with very simple controller blocks. Independent of the primary input specification, the proposed approach to VFC1 controller design leads to a system where the generalized stability and performance criteria *(NS, NP, RS, RP)* are obeyed within the defined *US*.

The system feedback path determines the system gain within the target bandwidth. This locks the shape of *B(s)* in the desired target frequency range. Since the B-compensator is positioned in the feedback path, where noise and distortion are not under control by the loop, it is appropriate to keep the compensator as simple as possible:

$$B(s) = \frac{1}{K} \tag{6.28}$$

The task of the compensator is to shape the loop to realize the desired stability and performance characteristics. This can be carried out with compensators of varying complexity. The compromise lies in the complexity of the controller and the bandwidth requirements to reach the stability and performance goals. It will become apparent, that the proposed compensator with has three nominator and denominator roots is a good compromise between these two issues:

$$C(s) = K_C \frac{(\tau_{z1}s+1)(\tau_{z2}s+1)(\tau_{z3}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)} \tag{6.29}$$

The specific purpose of the individual roots will be explain below where generalized loop synthesis is explained.

The reference filter serves to optimize the input to the PMA system, e.g. remove excess noise at high frequencies etc. Furthermore, *R(s)* determines the system response. An appropriate reference filter is of second order:

$$R(s) = \frac{\omega_r^2}{s^2 + \frac{\omega_r}{Q_r}s + \omega_r^2} \tag{6.30}$$

Obviously, a second order active filter will provide a much more well defined system response than the open loop response which is inherently determined by the passive demodulation filter. This stabilized system response is just one of the advantages afforded by VFC1.

Parameter	Value	Comment
$f_{p1}=\frac{1}{2\pi\tau_{p1}}$	$\frac{1}{20}f_u$	Optimized compensator LF-pole frequency
$f_{p2}=\frac{1}{2\pi\tau_{p2}}$	$\frac{1}{20}f_u$	Optimized compensator LF-pole frequency
$f_{p3}=\frac{1}{2\pi\tau_{p3}}$	$3f_u$	Optimized compensator HF-pole frequency
f_{z1}, f_{z2}	2	Cancellation zeros frequencies
$f_{z3}=\frac{1}{2\pi\tau_{z3}}$	$\frac{1}{3}f_u$	Optimized compensator HF-zero
f_o	2	Post filter natural frequency
Q_{oN}	$\frac{1}{\sqrt{3}}$	Nominal demodulation filter Q (Bessel)
f_r	$\frac{1}{2}f_u$	Reference filter natural frequency
Q_r	$\frac{1}{\sqrt{3}}$	Reference filter Q (Bessel).

Table 6.1 Proposed general parameters for VFC1.

6.4.1 Loop shaping

With all elements of the control loop defined, the resulting loop transfer function can be written:

$$L(s)=\frac{K_C K_{PN}}{K}\frac{(\tau_{z1}s+1)(\tau_{z2}s+1)(\tau_{z3}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)}\frac{\omega_o^2}{s^2+\frac{\omega_o}{Q_{oN}}s+\omega_o^2} \tag{6.31}$$

The loop transfer function is shaped to realize an average slope of approximately $N_L=-1.5$ beyond the target frequency band. This will guarantee *NS* and *NP*. With the loop slope defined, performance specifications as $S_M < S_{\max}$ and bandwidth specifications will be dual, by the following simple relation:

$$\begin{aligned} f_u &= S_{\max}^{-\frac{1}{N_L}} f_b \\ &\approx S_{\max}^{-\frac{2}{3}} f_b \end{aligned} \tag{6.32}$$

A specification on f_u thus renders a specification on S_M superfluous and vice versa. Following, the proposed VFC1 loop shaping approach will be based on one primary specification – the bandwidth of the controller f_u. This dramatically reduces the complexity the loop synthesis since the degrees of freedom is reduced to this single parameter. Table 6.1 defines general parameter relationships for VFC1, controlled by the bandwidth specification f_u. The two poles at low frequency $s=-\tau_{p1}^{-1}$, $s=-\tau_{p2}^{-1}$ initiate a second order characteristic within the amplifier signal band. The two zeros $s=-\tau_{z1}^{-1}$, $s=-\tau_{z2}^{-1}$ exclusively serve to cancel the demodulation filter poles. The zero-pole pair

$s=-\tau_{p3}^{-1}, s=-\tau_{z3}^{-1}$ provides the desired loop slope. With all roots in the loop transfer function specified, the necessary compensator DC gain K_C is derived:

$$\begin{aligned} &|L(j\omega_u)|=1 \;\Leftrightarrow \\ &\left|\frac{K_C K_{PN}}{K}\frac{(\tau_{z1}j\omega_u)(\tau_{z2}j\omega_u)(\tau_{z3}j\omega_u)}{(\tau_{p1}j\omega_u)(\tau_{p2}j\omega_u)}\frac{\omega_o^2}{\omega_u^2}\right|=1 \;\Leftrightarrow \\ &K_C=\frac{K}{K_{PN}}\frac{\omega_u}{\omega_o^2}\frac{\tau_{p1}}{\tau_{z1}}\frac{\tau_{p2}}{\tau_{z2}}\frac{1}{\tau_{z3}} \end{aligned} \tag{6.33}$$

All parameters for the VFC1 system are now defined. The system transfer function $H_T(s)$ is derived from the linear system model in Fig. 6.6:

$$\begin{aligned} H_T(s) &= R(s)H(s) \\ &= R(s)\frac{C(s)A(s)F(s)}{1+C(s)A(s)F(s)B(s)} \\ &\cong \begin{cases} K & (f<f_r) \\ \dfrac{K_C K_{PN}}{K}\dfrac{\tau_{z1}\tau_{z2}\tau_{z3}}{\tau_{p1}\tau_{p2}\tau_{p3}}\dfrac{\omega_u^2}{s^2}\dfrac{\omega_r^2}{s^2} & (f\geq f_u) \end{cases} \end{aligned} \tag{6.34}$$

The reference input filter $R(s)$ will determine the system response with the given parameters.

6.4.2 VFC1 Case example synthesis

The characteristics of the VFC1 control topology will now be demonstrated in higher detail by a case example. It will be shown that the proposed control structure and controller realization obeys the generalized stability and performance criteria *NS*, *RS*, *NP* and *RS* within the defined *US*. The controller synthesis will follow the six steps approach that has been defined.

STEP 1: Specification

The desired gain is $K=26dB$ and the equivalent nominal gain of the plant is assumed to be $K_{PN}=26dB$. It is assumed that an initial study of the plant has lead to the following performance specification $S_M<-20dB$. No further performance specifications within the target bandwidth are assumed necessary to realize the desired closed loop system performance. The parameter specifications are summarized in the table below:

Parameter	Value
K	26dB
K_N	26dB
S_{max}	-20dB

Step 2: Synthesis
The performance specification will be realized with a reasonably margin by a bandwidth specification of $f_u = 8$. All parameters of the control system are now defined. The actual synthesis of the individual sub-controllers is extremely simple and follows directly from the parameter assignment in Table 6.1.

Step 3: Verification
With all sub-controllers defined, the functional verification of the system is carried out. Fig. 6.7 shows Bode plots for each component in the loop and the resulting loop transfer function with the specified parameters. Note, that the bandwidth is as specified. The performance specifications are found from the sensitivity function shown in Fig. 6.8:

$$\|S\|_\infty = 1.5, \quad S_M = -26dB \tag{6.35}$$

Hence, both *NS* and *NP* are satisfied as claimed.

Fig. 6.9 shows the resulting closed loop response with/without reference input filter. The system gain is forced to 26dB within the target bandwidth as desired. Clearly, the total system response is determined by $R(s)$. With the selected parameters for $R(s)$, the bandwidth is approximately 3 and the frequency response $\pm 0.1dB$ within the target bandwidth. Another important advantage of the reference filter is that control signals are well conditioned throughout the system, independent of what is applied at the input. This is easily verified by investigating input to control signal transfer functions.

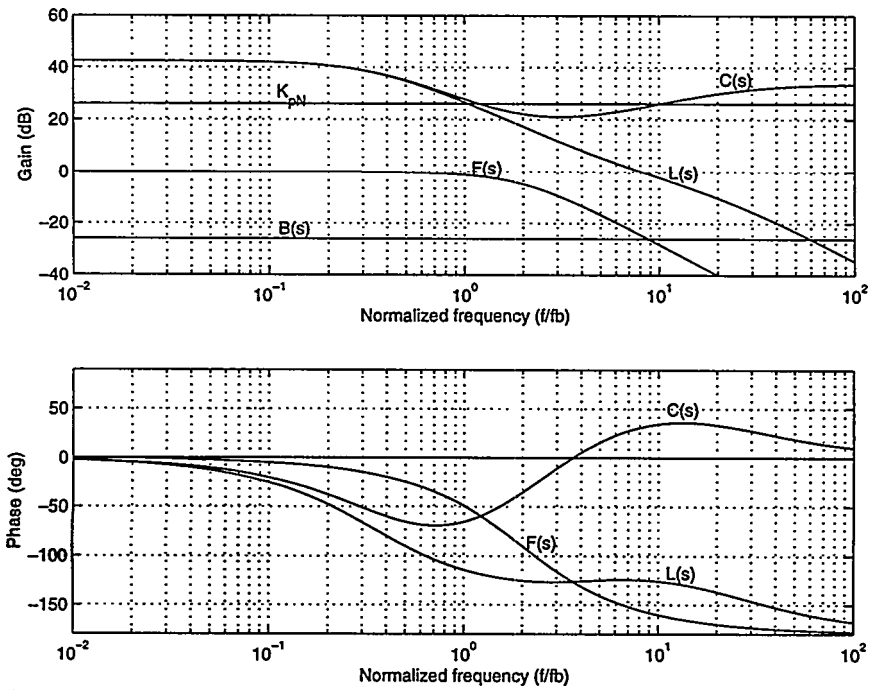


Fig. 6.7 VFC1 case example. Bode plots for loop components and resulting loop transfer function.

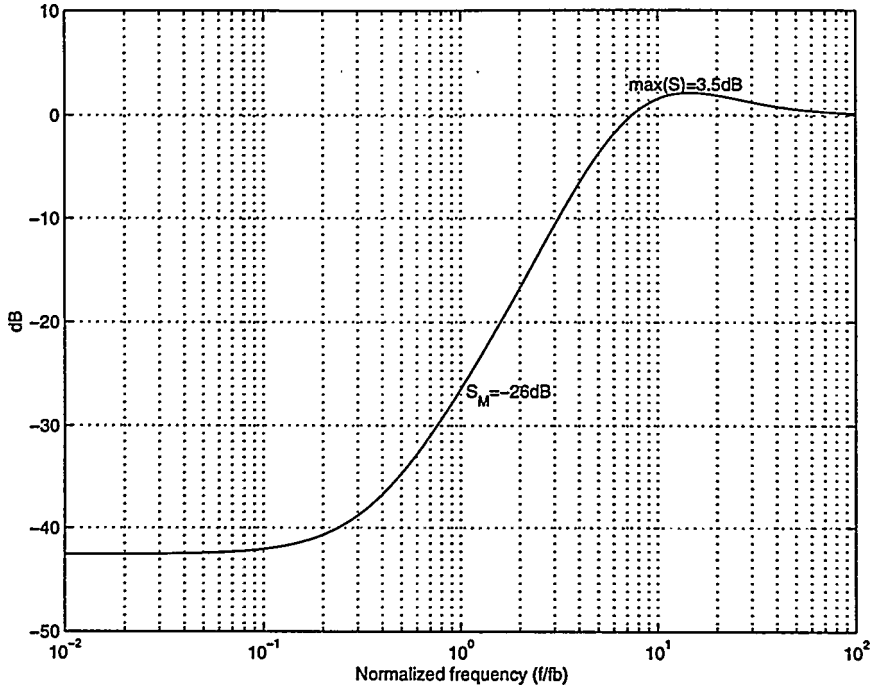


Fig. 6.8 VFC1 case example. Sensitivity function for the control system. *NS* and *NP* are verified.

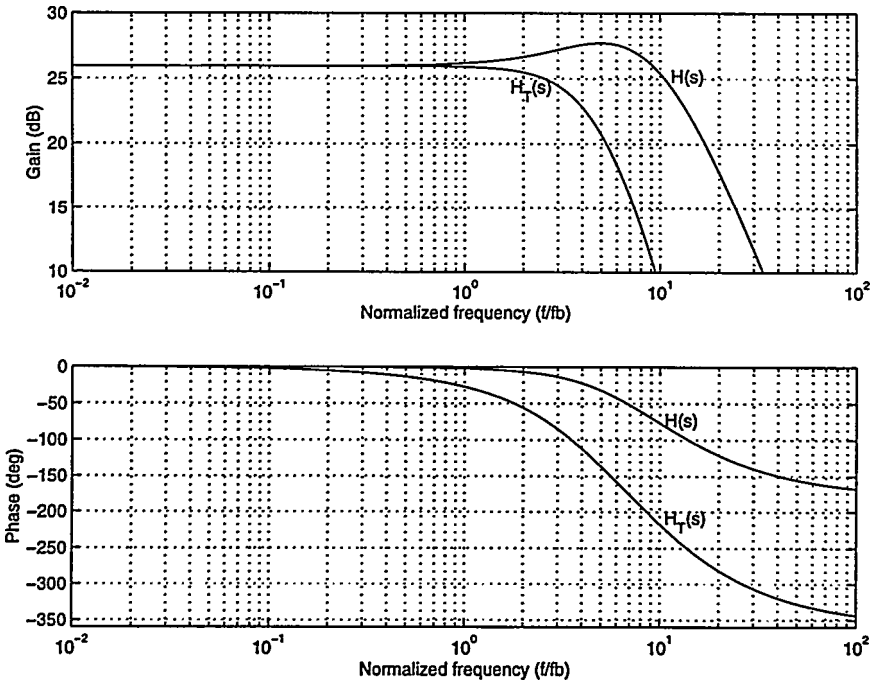


Fig. 6.9 VFC1 case example. Bode plots for closed loop transfer function $H(s)$ and system transfer function $H_T(s)$.

Step 4: Robustness properties

The robustness of the proposed system is now investigated within the defined uncertainty set. The set of perturbed loop transfer functions can be written:

$$L_p(s,r_K,r_Q,t_P)=\frac{K_C r_K K_{pN}}{K}\frac{(\tau_{z1}s+1)(\tau_{z2}s+1)(\tau_{z3}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)}\frac{\omega_o^2}{s^2+\frac{\omega_o}{r_Q Q_{oN}}s+\omega_o^2}e^{-t_p s} \tag{6.36}$$

Fig. 6.10 shows the sensitivity function for the *worst-case* perturbed system within the *US*, corresponding to the loop transfer function $L_p(s,0.5,4,200ns)$. For the worst case plant we have:

$$\|S\|_\infty = 8.6dB\,, \quad S_M = -22dB \tag{6.37}$$

Clearly, the worst-case perturbed system obeys *RS* and *RP*. This verifies the proposed design method for VFC1 will always lead to a robust control system. The worst-case perturbed system always refers to the perturbed system with maximal $\|S\|_\infty$ within the US.

In the general case, a 3-dimensional parametric search is necessary to find the worst case perturbed system. Indeed, it can be illustrative to plot the complete set of perturbed systems, $L_p(s,r_K,r_Q,t_p)$, as a filled 'area' within the (frequency, $|S|$) - space in the general case. However, in reasonably simple systems as VFC1 it is straightforward to determine the worst case situation and check for *RS* and *RP*. Uncertainty on the plant will also affect the system response, although the control system will attempt to minimize such effects. The system response for the nominal model and the worst-case perturbed system are compared in Fig. 6.11. Clearly, the VFC1 system response nearly unaffected within the target frequency band, i.e. VFC1 provides excellent suppression of all perturbations.

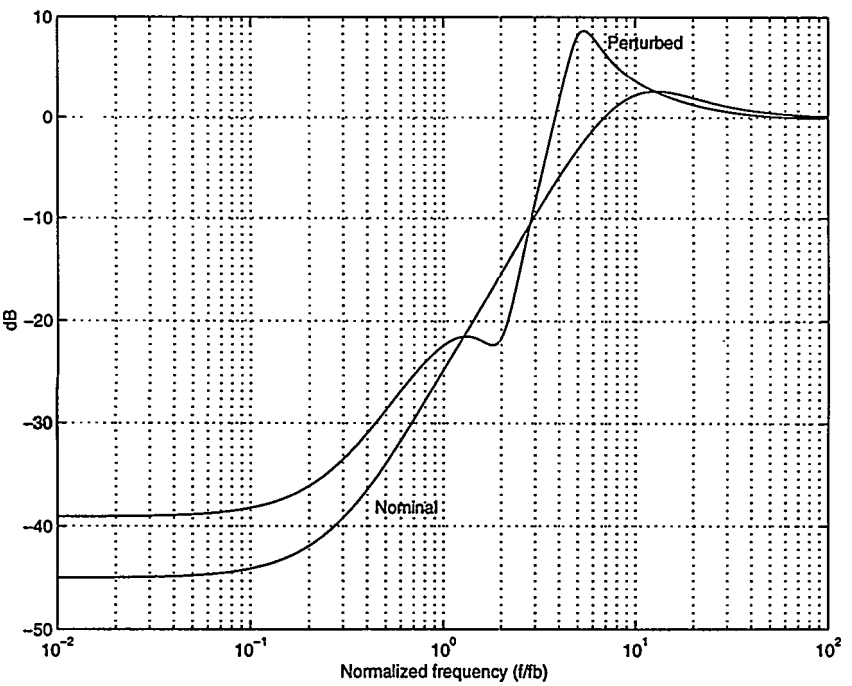


Fig. 6.10 VFC1 case example. Sensitivity function of perturbed system (worst-case).

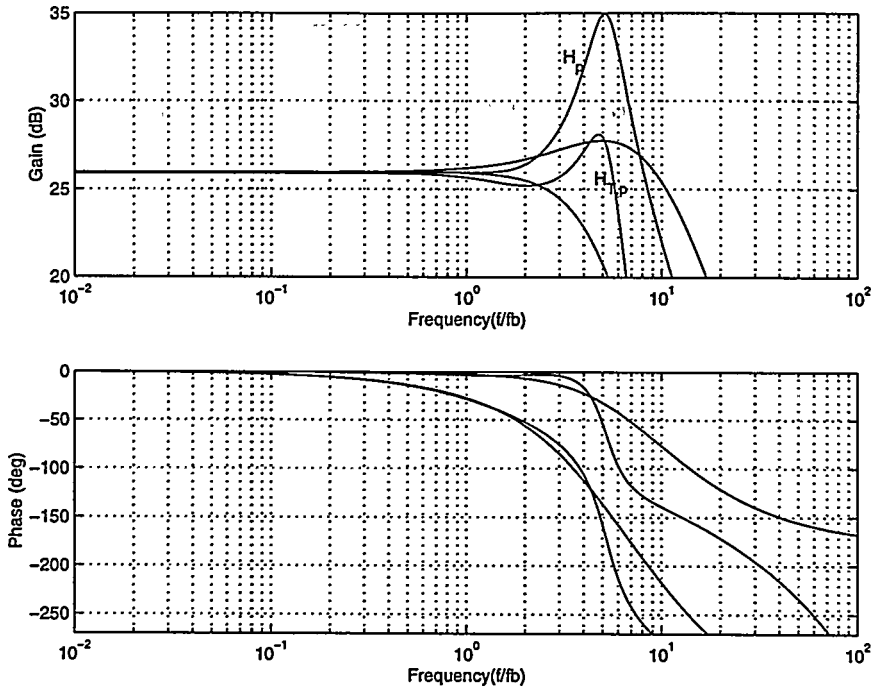


Fig. 6.11 Comparison of closed loop transfer function $H(s)$ and system transfer function $H_T(s)$ with worst-case perturbed versions $H_p(s)$ and $H_{T,p}(s)$ respectively.

STEP 5: Non-linear simulation

The low-level non-linear simulation includes a power stage model including the most important non-linear and limiting effects. The investigations will be based on NADD PWM (see Chapter 2 for spectral characteristics). NADD is not the optimal modulation scheme but it is appropriate to illustrate the limitations caused by the HF-disturbance v_{dp} using NADD. The power stage parameters are summarized below:

Parameter	Value
V_S	50V
V_T	2.5V

V_T is the amplitude of the carrier. To prevent Slew Rate Instability with double-sided modulation as NADD, the maximal amplitude of the switching fundamental at the modulator input is:

$$v_{c,dp} < \frac{2V_T}{\pi} = 1.6V \tag{6.38}$$

Where $v_{c,dp}$ indicates the amplitude of the carrier component that will superpose the control signal v_c. If the amplitude of the carrier residual at the modulator input exceeds this limit, SRI will occur and destroy the modulator performance. Since the amplitude of the power stage "noise generator" at idle operation is:

$$\hat{v}_{dp} = V_S \frac{4}{\pi} = 63.6V \tag{6.39}$$

The HF residual at the modulator input is:

$$v_{c,dp} = |L(j\omega_c)| \frac{\hat{v}_{dp}}{K_{PN}} \tag{6.40}$$

The maximal carrier frequency do prevent SRI is determined from:

$$|L(j\omega_c)| < \frac{K_{PN}}{\hat{v}_p} v_{c,dp} \approx 0.5 \tag{6.41}$$

Solving for $f_{c,\max}$ yields a maximal carrier frequency of 280KHz to prevent Slew Rate Instability (SRI). To obey the Nyquist criteria the constraint on switching frequency is 320KHz, with the given loop bandwidth of 160KHz ($f_u = 8$). Subsequently, a carrier frequency of $f_c = 400KHZ$ is selected for the following non-linear simulations. This will yields a 6dB margin to SRI. The HF residual on that superposed the modulating signal is calculated to be:

$$v_{dp} = |L(j\omega_c)| \frac{\hat{v}_p}{K_{PN}} \approx 0.75V \tag{6.42}$$

Fig. 6.12 shows as a functional simulation of the VFC1 based system at idle. This verifies the functional performance, and illustrates how all controller signals are superposed by carrier related components. The modulator input is superposed by a carrier frequency component of 0.75V as determined from theory above.

Correction of PTE

The general correction capability toward PTE is investigated by a non-linear simulation of the system with the blanking delay t_D varying within the range 0ns - 100ns. Fig. 6.13 shows the controller signal and the resulting output in the two extremes t_D=10ns and t_D=100ns. Both linear and non-linear errors are considerably reduced when applying the VFC1 system, i.e. the outputs are indistinguishable in the time domain. Note how the control system pre-distorts the modulating signal. Fig. 6.15 shows the parametric simulation of the resulting THD vs. t_D with and without VFC1. The improvement is about 25dB corresponding well with theory. The sensitivity function at the third harmonic (15KHz) is about 30dB, whereas the fifth harmonic is only suppressed by 22dB by the sensitivity function.

Correction of PAE

The correction effect towards pulse amplitude error is investigated by a non-linear simulation with a severe pulse amplitude error. The power supply is superposed by a 50Vpp, 5KHz perturbation. The 50Vpp correspond exactly to the ±50% perturbation of K_P within a single cycle of the perturbing signal. This exact range was defined as the worst case perturbation in the Uncertainty Set. Fig. 6.14 shows the results of the simulation. Although the error is well beyond any practical situation, it illustrates the powerful control offered by VFC1.

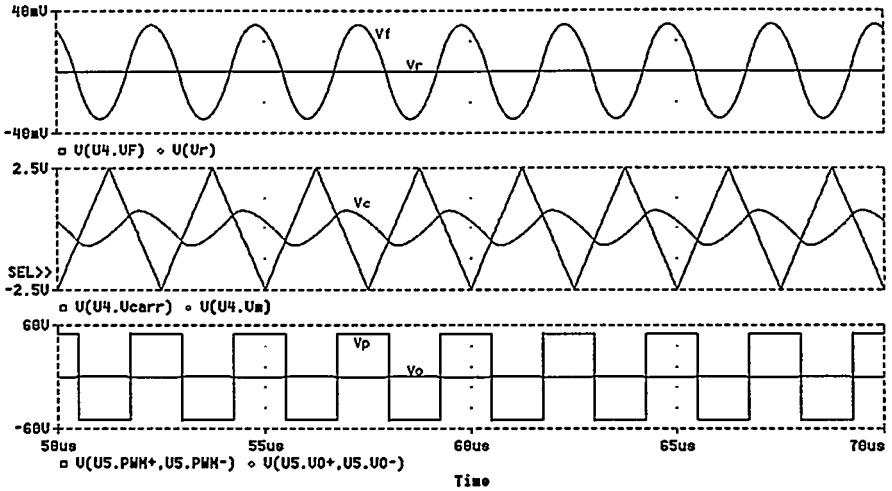


Fig. 6.12 Functional simulation of VFC1 case example. Top – Reference v_r and feedback signal v_f. Mid – Controller signal v_c and carrier. Bottom – Power output v_p and v_o.

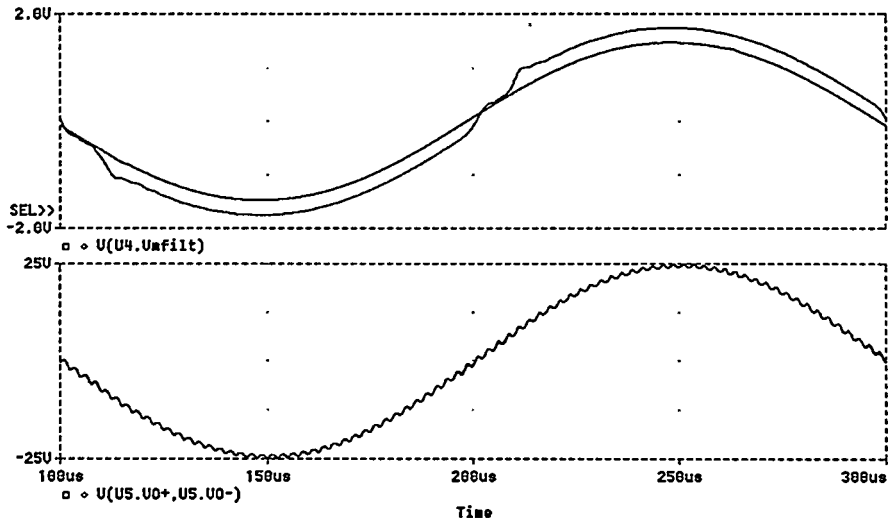


Fig. 6.13 Simulation of PTE. v_c (filtered with a 200KHz brick-wall) illustrates how the controller applies and anti-distorted signal to the modulator. t_D = 10ns and 100ns in the two cases.

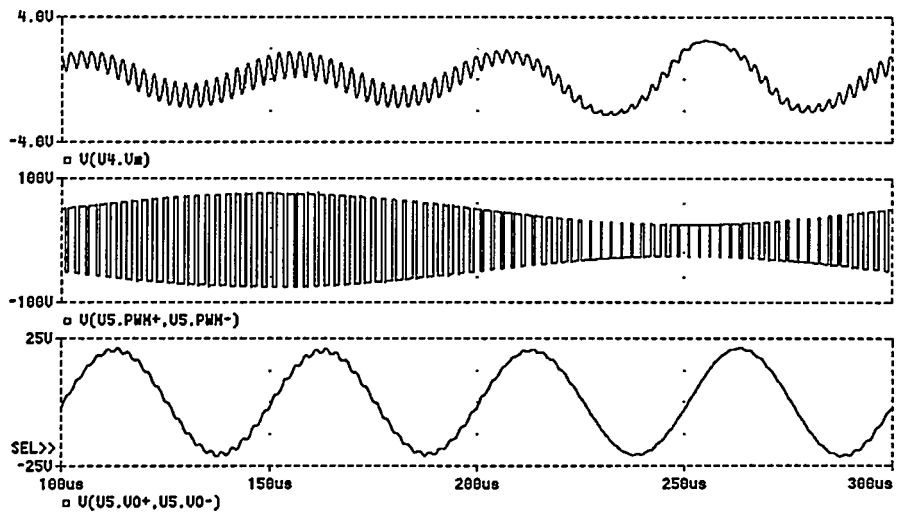


Fig. 6.14 Simulation of PAE. A 50Vpp 5KHz signal is superposed on the power supply. No visible intermodulation distortion is "visible" in the time domain output. PSRR=25dB with VFC1.

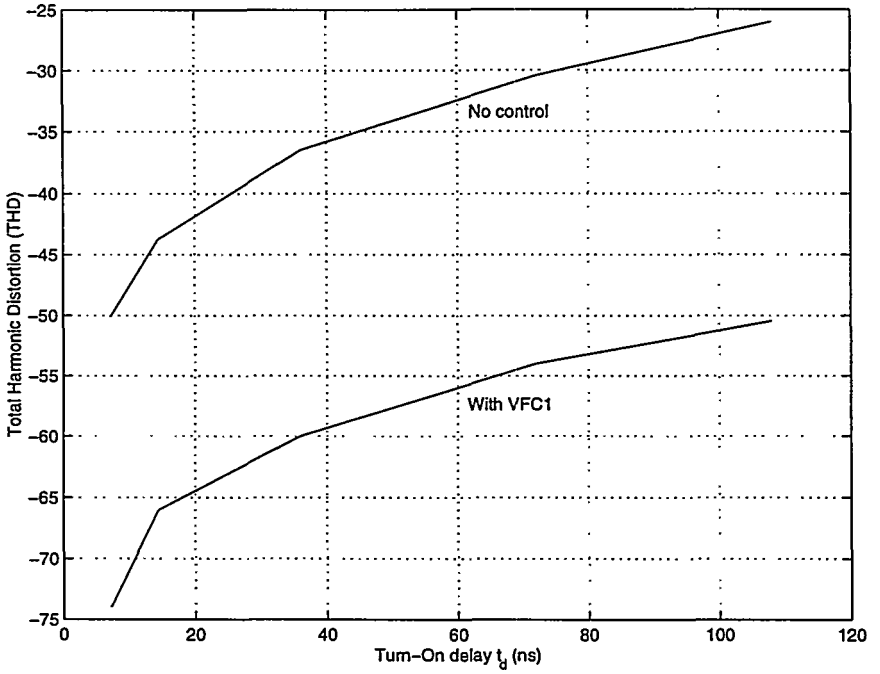


Fig. 6.15 Simulation of PTE error correction for VFC1 case example. THD is investigated vs. t_d at 5KHz with VFC1 and without control. The improvement in THD is about 25dB.

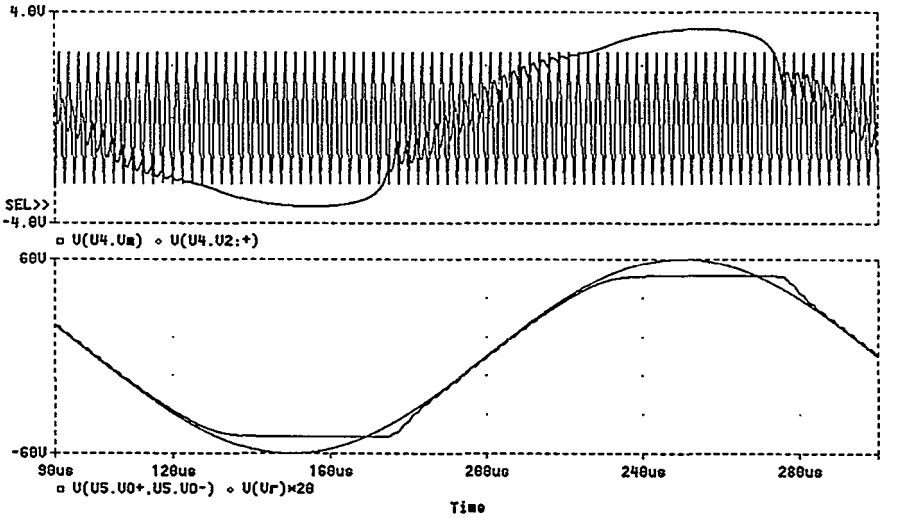


Fig. 6.16 Simulation of VFC1 case example with 20% overload.

With the proposed VFC1 system, the severe perturbation on the power supply is barely noticeable on the resulting time domain output. A closer investigation of the spectral content shows that the intermodulation components are less than 50mV with the controller, corresponding to a reduction in intermodulation distortion of more than 25dB compared to the open loop case. This corresponds to the expected performance, i.e. the sensitivity function is –25dB at 20KHz.

Stability

Fig. 6.16 shows a simulation with 20% overload showing that the system can be overloaded without problems. A limitation is inserted at the controller output to limit the

control signal at overload situations where large errors are generated. Note however, that there will be a finite time to recover from overload, dependent upon limitation circuitry on the modulating signal.

To conclude, the proposed VFC1 control structure and loop shaping approach offers significant improvements to the PMA system with simple means. It has been shown, that that the control design approach is stable and robust. However, there are a inherent constraints bound to the topology:

- Wide-band control requires a very high compensator gain at high frequencies. This requires a wide bandwidth controller, which is difficult to implement in sufficient quality.
- Loop shaping is constrained especially at higher frequencies to bandwidth and slope constraints. The requirements for robustness constrain the slope of the loop transfer function. Efficiency and open loop linearity will limits the bandwidth.
- System stability and performance is sensitive to load variations. However, with careful controller design as above, *RS* and *RP* can be guaranteed within the defined *US*.

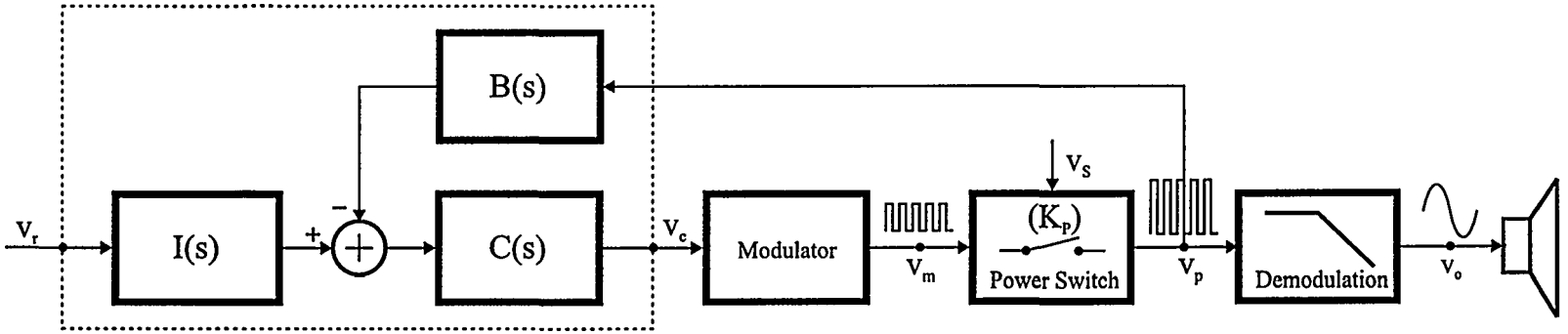


Fig. 6.17 The Voltage Feedback Control Topology 2 (VFC2).

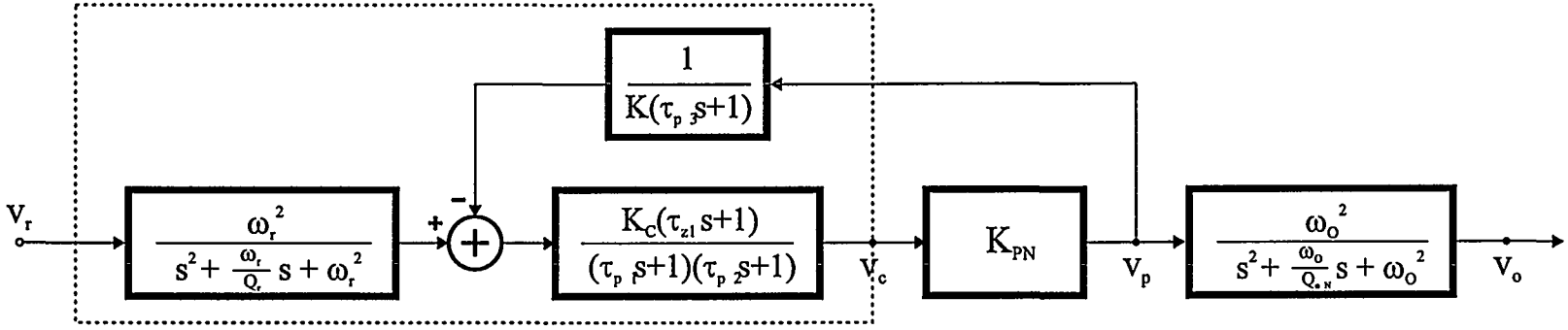


Fig. 6.18 VFC2 linear model with compensators defined.

6.5 Voltage Feedback Control Topology 2 (VFC2)

The VFC2 topology is defined in Fig. 6.5, and Fig. 6.6 shows a linear model for the system with proposed compensators defined. The controller is subdivided in three elements, a forward path compensator $C(s)$, a feedback path compensator $B(s)$, including attenuation in order to provide the desired closed loop gain and an initial reference shaper $R(s)$ to stabilize the high frequency dynamics. The main difference compared to VFC1 is the feedback source and the simpler compensator. As for VFC1, a general frequency normalized loop shaping approach is devised for VFC2. Independent of the primary input specification f_u or S_M, the synthesized controller will obey the stability and performance criteria *(NS, NP, RS, RP)*.

The feedback path compensator *B(s)* determines the closed loop gain and to filter the components from v_p:

$$B(s) = \frac{1}{K}\frac{1}{(\tau_{p3}s+1)} \tag{6.43}$$

The filtering reduces the bandwidth requirements for the feedback compensator. The following general compensator is proposed:

$$C(s) = K_C \frac{(\tau_{z1}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)} \tag{6.44}$$

The reference filter is a second order filter just as for VFC1.

6.5.1 Loop shaping

The resulting loop transfer function for VFC2 is simple:

$$L(s) = \frac{K_C K_{PN}}{K}\frac{\tau_{z1}s+1}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)} \tag{6.45}$$

To secure *NS* an *NP* the target is again a slope of $N_L = -1.5$. The desired slope is realized by the general parameter values in Table 6.2. Obviously, two of the compensator zeros for VFC1 are not required to VFC2 to compensate for the second order output filter. Otherwise, the remaining zeros and poles closely resemble VFC1, only $s = -\tau_{p3}^{-1}$ is now realized in the feedback path. Some noticeable differences between VFC1 and VFC2 should be noted. The zero-pole pair ($s = -\tau_{p3}^{-1}, s = -\tau_{z3}^{-1}$) differs slightly from VFC1, causing a slightly steeper slope. Since the control does not enclose the filter, the control system is not affected by uncertainty; i.e. the space of uncertainties is now only 2-dimensional. This renders a steeper slope possible, without compromising *RS* and *RP*. Another difference is the optimized input and output filter parameters, which differ significantly between VFC1 and VFC2. Again, this is related to the fact that VFC1 does not control the output filter, such that perturbations on the load will affect the system response. For a reasonable system response within the defined *US*, it is necessary to increase the natural frequency of the filter.

Parameter	Value	Comment
$f_{p1}=\frac{1}{2\pi\tau_{p1}}$	$\frac{1}{20}f_u$	Optimized compensator LF-pole frequency
$f_{p2}=\frac{1}{2\pi\tau_{p2}}$	$\frac{1}{20}f_u$	Optimized compensator LF-pole frequency
$f_{p3}=\frac{1}{2\pi\tau_{p3}}$	$2f_u$	Optimized feedback path compensator B(s) HF-pole frequency
$f_{z1}=\frac{1}{2\pi\tau_{z1}}$	$\frac{1}{2}f_u$	Optimized compensator HF-zero
f_0	3	Post filter natural frequency
Q_{oN}	$\frac{1}{\sqrt{3}}$	Nominal post filter Q (Bessel)
f_r	5	Reference filter natural frequency
Q_r	$\frac{1}{\sqrt{3}}$	Reference filter Q (Bessel).

Table 6.2 Proposed general parameters for VFC2.

The compensator DC gain K_C is determined as:

$$|L(j\omega_u)|=1 \quad \Rightarrow \quad K_C=\frac{K}{K_{PN}}\frac{\tau_{p1}}{\tau_{z1}}\tau_{p2}\omega_u \tag{6.46}$$

The closed loop system transfer function is:

$$\begin{aligned} H(s) &= R(s)H(s)F(s) \\ &= R(s)F(s)\frac{C(s)A(s)}{1+C(s)A(s)B(s)} \\ &\cong \begin{cases} K & (f<f_b) \\ \frac{K_C K_{PN}}{K}\frac{\tau_{z1}}{\tau_{p1}\tau_{p2}}\frac{\omega_f^2}{s^2}\frac{\omega_r^2}{s^2} & (f\geq f_u) \end{cases} \end{aligned} \tag{6.47}$$

The resulting system response is $H_T(s)=R(s)H(s)F(s)$.

6.5.2 VFC2 case example

A case example is used to demonstrate the special properties of VFC2, especially in terms of differences to VFC1.

STEP 1: Specification.
Parameter specifications are the same as for the VFC1 case example in order to enable a direct comparison of the two topologies. The parameter specifications are given below:

Parameter	Value
K	26dB
K_P	26dB
S_{max}	-20dB

STEP 2: Synthesis
A bandwidth of $f_u = 8$ will realize the performance specification $S_M < S_{max}$. The synthesis of the individual controllers follows directly from the general VFC2 parameters Table 6.2.

STEP 3: Verification – VFC2
Fig. 6.19 shows Bode plots for each component in the loop and the resulting loop transfer function with the specified parameters. Clearly, the resulting loop characteristic closely resembles that of VFC1. The compensator differs significantly for the two topologies; i.e. the VFC2 compensator has a much more pleasant characteristic. The proposed parameters yields the following performance parameters (Fig. 6.22):

$$\|S\|_\infty = 1.5, \quad S_M = -29dB \tag{6.48}$$

Hence, both *NS* and *NP* are satisfied. The improvement in S_M compared with VFC1 is realized by the steeper loop slope, made possible by the insensitivity to load perturbations. Fig. 6.20 shows the closed loop response, the response with *R(s)* and the resulting system response $H_T(s) = R(s)H(s)F(s)$. The resulting response is dominated by the output filter, which has the lowest natural frequency. The control loop forces a system gain of 26dB as desired, the bandwidth is approximately 2.5 and the frequency response is $\pm 0.3dB$ within the target bandwith.

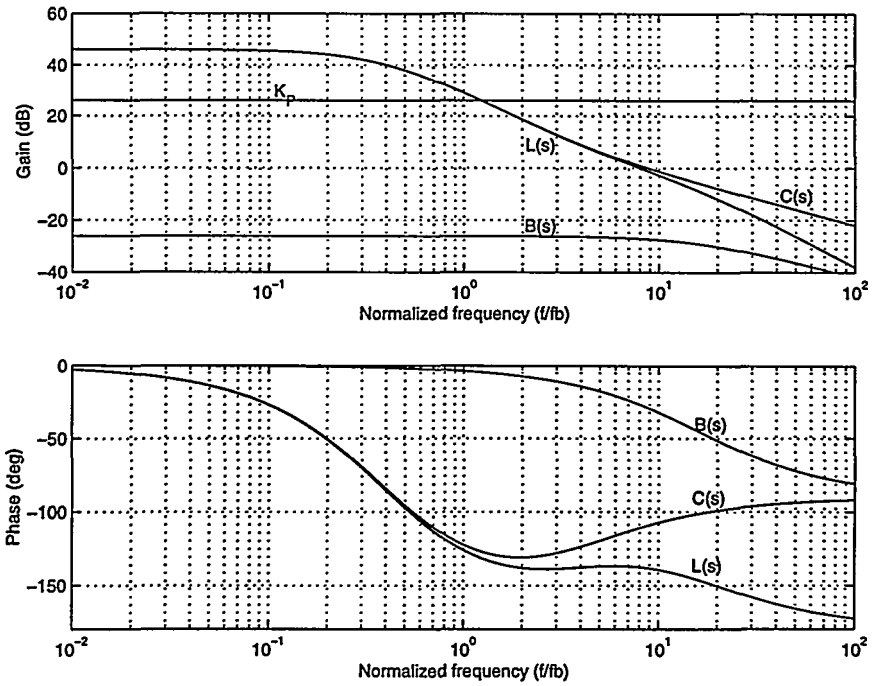


Fig. 6.19 VFC2 case example. Bode plots for loop components and resulting loop transfer function.

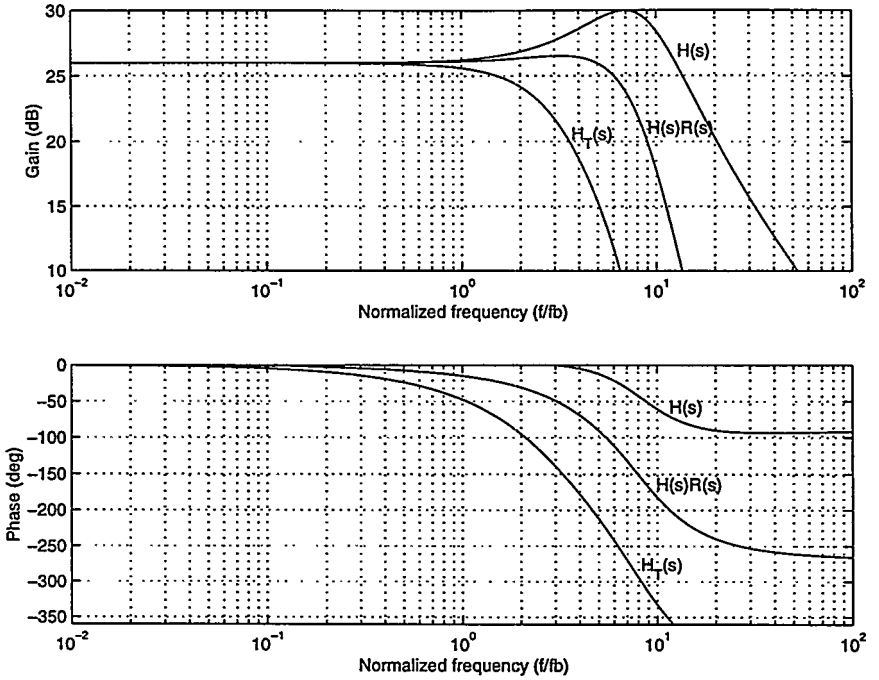


Fig. 6.20 VFC2 case example. Bode plots for closed loop system $H(s)$, $H(s)R(s)$ and resulting system transfer function $H_T(s) = R(s)H(s)F(s)$.

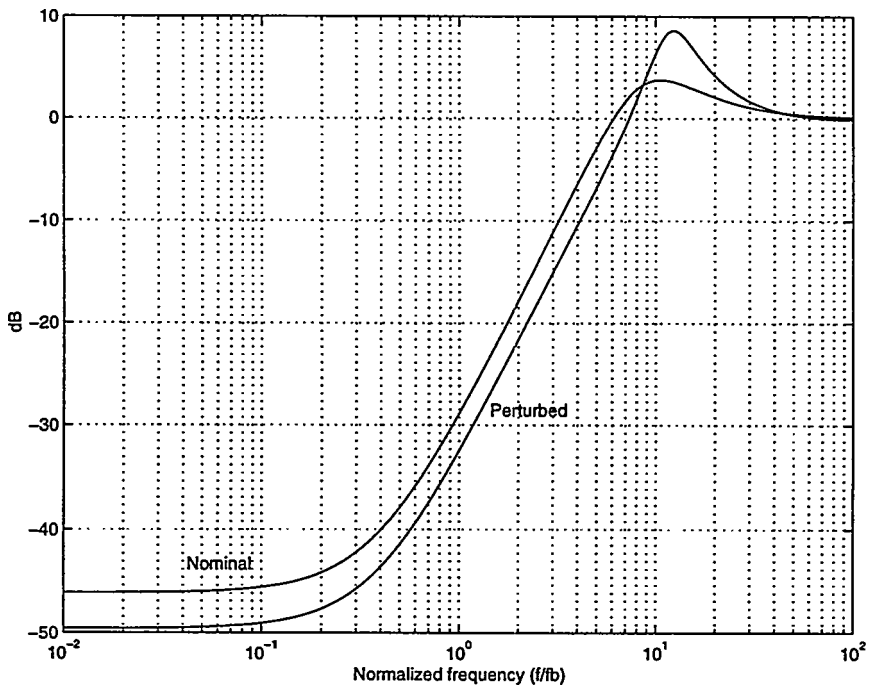


Fig. 6.21 VFC2 robustness investigation. Sensitivity function for nominal and perturbed sensitivity function $S_p(s,1.5,4,200ns)$, corresponding to the worst case situation.

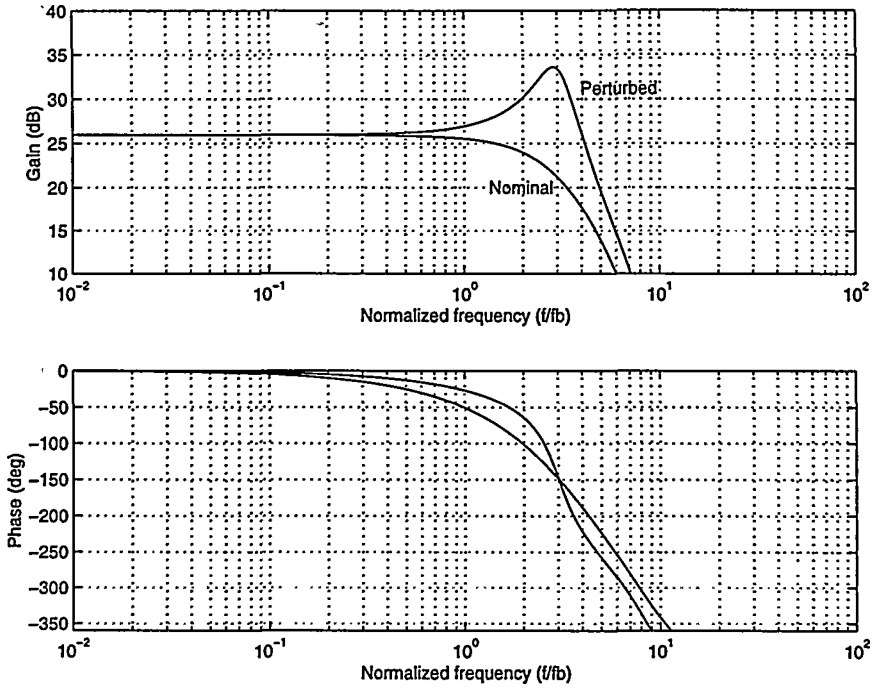


Fig. 6.22 VFC2 robustness. Closed loop response for $H_T(s)$ and $H_{T,p}(s,1.5,4,200ns)$.

STEP 4: Robustness

The perturbed loop transfers within the *US* are:

$$L_p(s,r_K,r_Q,t_P)=\frac{K_C r_K K_{PN}}{K}\frac{(\tau_{z1}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)}e^{-t_P s} \tag{6.49}$$

Fig. 6.21 shows the sensitivity function for the worst-case perturbed sensitivity function $S_p(s,1.5,4,200ns)$, compared with the nominal system. The performance specifications in for this worst-case system are:

$$\|S_p\|_\infty = 2.7, \quad S_{M,p} = -32dB \tag{6.50}$$

RS and *RP* hold within the defined *US*. Note, that the worst case plant within the US occurs when K_P is maximal, as opposed to VFC1 where the worst-case plant is with a minimal K_P. The difference is explained by the r_Q-perturbation, that does not affect VFC2 but severly affects the robustness and stability characteristics of VFC1.

However, since the output filter is not controlled, perturbations on the filter Q will affect system response more seriously for VFC2. This is illustrated in Fig. 6.22. The peaking caused by $r_Q = 4$ will directly affect the system response, such that the frequency response is now $\pm 0.5dB$. If the filter natural frequency is lower, the influence on system response will worsen. Obviously, for a reasonable system response within the *US*, it is essential with a natural frequency of the output filter of at least $f_o = 3$. Consequently, demodulation is compromised with VFC2.

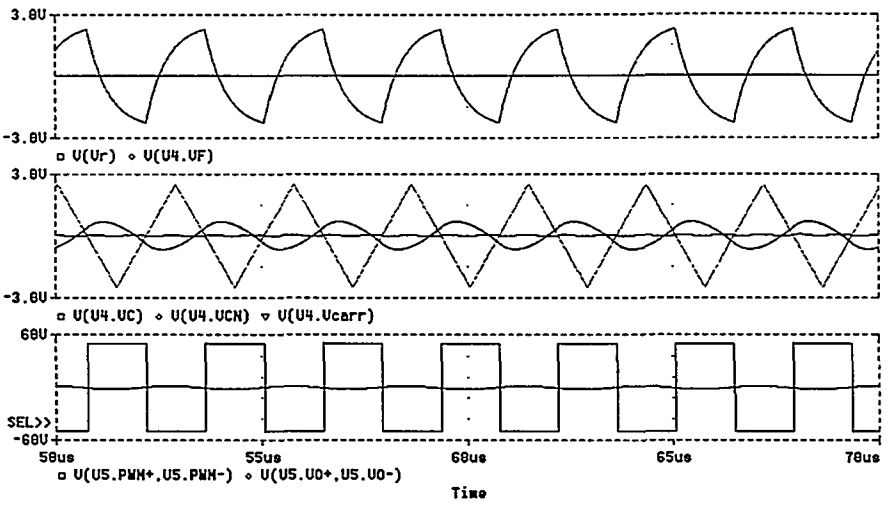


Fig. 6.23 Functional simulation of VFC2 based PMA at idle. Top – Feedback v_f and reference v_r. Mid – Carrier and compensator output v_c. Bottom – Power stage outputs v_p and v_o.

STEP 5: Non-linear simulation

Parameters for the non-linear simulation are the same as for VFC1 for a coherent comparison of the system characteristics. Since the loop transfer functions are similar, the resulting HF residual at the modulator will be the same. Fig. 6.23 shows the functional simulation of the VFC2 based system at idle. The system is stable, and all control signals are as expected. The first order filtering and attenuation of the feedback signal leaves a significant residual of HF-components superposed on v_f. The C-compensator following attenuates this residual, such that the v_p related noise has a 0.75V peak magnitude as expected from theory.

Error Correction, Stability and Overload

The correction of PTE and PAE has been investigated for VFC2. The performance is slightly better that for VFC1, corresponding the difference in sensitivity function. The stability and overload characteristics also resemble the characteristics for VFC1.

In conclusion, the VFC1 topology offers the simplest possible controller for PMA systems. The extremely noisy feedback source is not a severe problem with appropriate compensator design that utilizes filtering in the feedback path. The compensator design is simplified especially e.g. in terms of the high frequency gain requirements. Furthermore, it is simple to realize an extremely robust design within the specified *US*, with minimal performance compromises. On the other hand, the output filter is not controlled, and this limits the use in general purpose applications. In dedicated applications however, the simple topology has is a possible solution if the open loop performance is reasonably good.

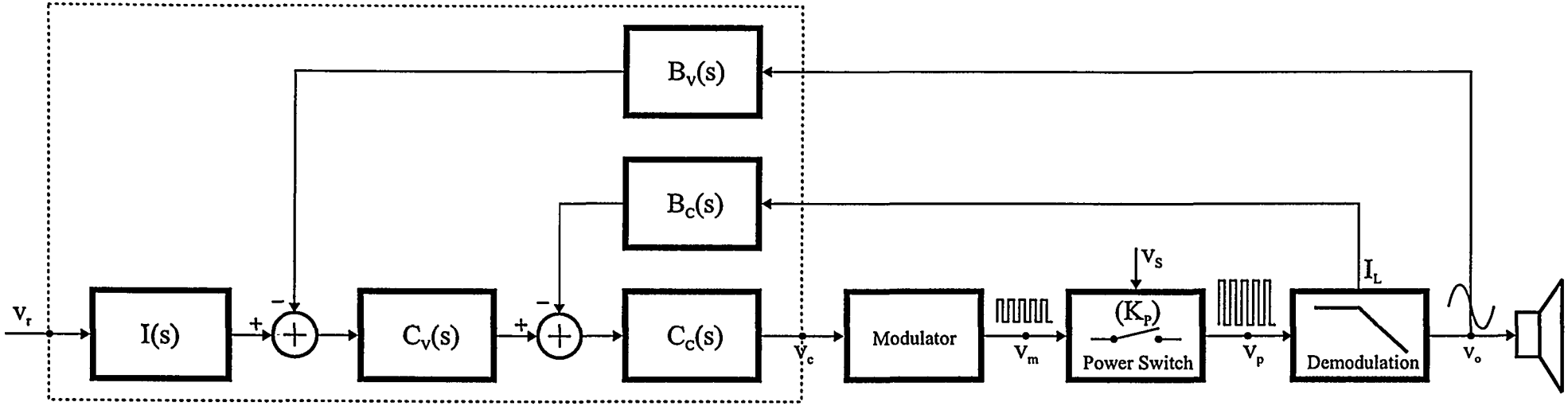


Fig. 6.24 The CVFC Topology with five general sub-controllers

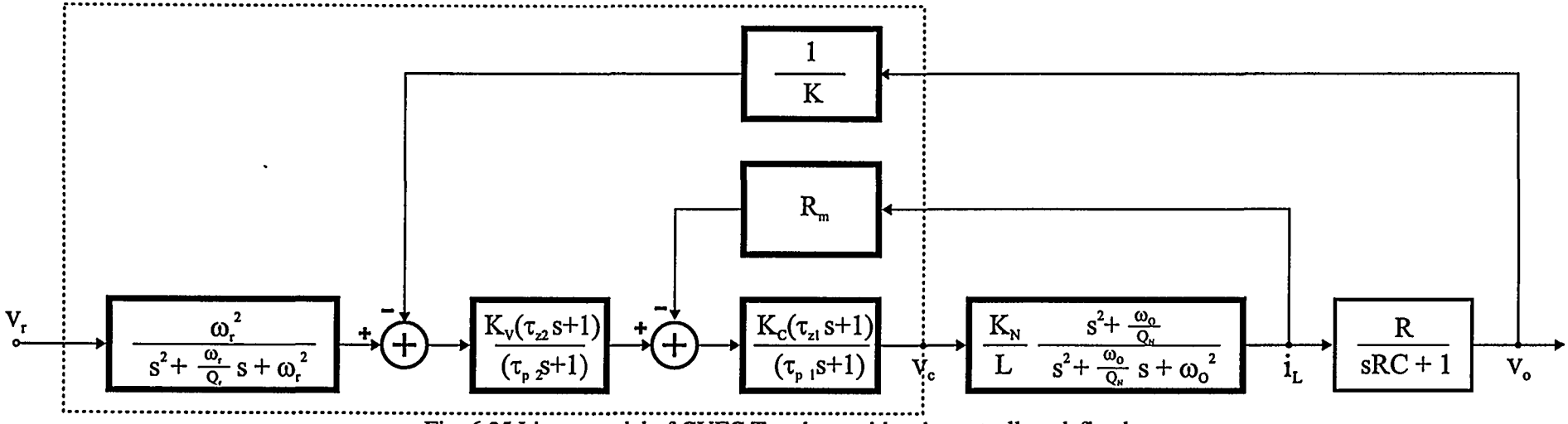


Fig. 6.25 Linear model of CVFC Topology with sub-controllers defined.

6.6 Current Voltage Feedback Control Topology (CVFC)

A more complex control topology is presented in the following that utilizes a combination of current and voltage feedback in the attempt to overcome the shortcomings of VFC1 and VFC2. The CVFC topology is shown in Fig. 6.24. It should be mentioned that current – voltage control is one of the most widely used methods within the power electronics industry in motor control and inverter applications. Some of the prominent qualities in these applications cover excellent control over the load and good stability characteristics. However, PMAs systems differ in the requirements for bandwidth, linearity and noise to e.g. motor controllers and general power conversion systems, where the design objectives are significantly different. This section is devoted to the dedication of current/voltage feedback to realize the control objectives best possible. Obviously, the application of a more complex controller structure is only justifiable as long as this offers notable advantages.

Generally, multiple loop controller optimization is more complicated due to the increasing number of sub-controllers to optimize. For the CVFC topology, it is expedient to separate the synthesis of the current and the voltage loop. The current loop is optimized individually to realize certain design objectives. Following, the voltage loop is synthesized based on the improved plant that the current loop provides. The linear model of the proposed CVFC topology is shown in Fig. 6.25. The multivariable controller is subdivided in five elements, two forward path compensators $C_C(s)$ and $C_V(s)$, and two feedback path compensators $B_C(s)$ and $B_V(s)$. Finally, a pre-compensator $R(s)$ serves to stabilize the high frequency dynamics.

The following presents a fundamental analysis of the CVFC topology, based on compensator characteristics as they are defined in Fig. 6.25. Following, loop shaping methods to reach the *(NS, NP, RS, RP)* criteria within the defined *US* will be addressed.

6.6.1 Current loop analysis

$B_c(s)$ is very simple. The current measured over an equivalent measurement resistance is feed directly back to the difference point, i.e.:

$$B_C(s) = R_m \quad (\Omega) \tag{6.51}$$

To derive the filter inductor current, it is appropriate to represent the filter by its fundamental components L, C and R. The impedance seen by the switching output stage is:

$$Z_O(s) = sL + \frac{R}{1+sRC} = \frac{s^2LRC + sL + R}{sRC+1} \tag{6.52}$$

Subsequently, the transconductance from the current loop compensator to the switching power stage output current (= inductor current) is:

$$G_O(s)=\frac{K_{PN}}{Z_O(s)}=K_{PN}\frac{sRC+1}{s^2LRC+sL+R}$$
$$=\frac{K_{PN}}{L}\frac{s+\frac{\omega_0}{Q_{oN}}}{s^2+\frac{\omega_0}{Q_{oN}}s+{\omega_0}^2} \tag{6.53}$$

Where:

$$\omega_0=\frac{1}{\sqrt{LC}} \qquad Q_{oN}=R\sqrt{\frac{C}{L}}=RC\omega_0 \tag{6.54}$$

(6.53) show the clear first order characteristic of the transconductance, i.e. the current loop can be considered as a first order system. The following simple compensator is proposed to optimize the characteristics of the current loop:

$$C_C(s)=K_C\frac{\tau_{z1}s+1}{\tau_{p1}s+1} \tag{6.55}$$

The resulting current loop transfer function can now be written:

$$L_C(s)=C_C(s)Z_O(s)B_C(s)$$
$$=K_C\frac{\tau_{z1}s+1}{\tau_{p1}s+1}\cdot\frac{K_{PN}}{L}\frac{s+\frac{\omega_0}{Q_{oN}}}{s^2+\frac{\omega_0}{Q_{oN}}s+{\omega_o}^2}\cdot R_m \tag{6.56}$$

The compensator gain K_C is determined from the current loop bandwidth f_{uc} as:

$$\left|L_C(j\omega_{uc})\right|=1 \Rightarrow$$
$$\left|K_C\frac{\tau_{z1}}{\tau_{p1}}\frac{K_{PN}}{L}R_m\frac{1}{j\omega_{uc}}\right|=1 \Rightarrow \tag{6.57}$$
$$K_C=\frac{L}{K_{PN}}\frac{\tau_{p1}}{\tau_{z1}}\frac{\omega_{uc}}{R_m}$$

The closed loop transconductance of the current loop is now derived:

$$G_C(s)=\frac{C(s)Z_O(s)}{1+C(s)Z_O(s)R_m}=\frac{1}{R_m}\frac{1}{1+\frac{1}{L_C(s)}}$$
$$\cong\frac{1}{R_m}\frac{1}{1+\tau_{uc}s} \tag{6.58}$$

The current loop can be approximated by a constant transconductance over the current loop bandwith, and a first order characteristic beyond that bandwidth.

6.6.2 The voltage analysis

The characteristics of the voltage loop are strongly influenced by constant transconductance characteristics of the current loop. Appropriate compensators are:

$$B_V(s) = \frac{1}{K} \tag{6.59}$$

$$C_V(s) = K_V \frac{\tau_{z2}s+1}{\tau_{p2}s+1} \tag{6.60}$$

The "current generator" $G_C(s)$ drives the parallel impedance of the filter capacitor and load:

$$Z_{RC}(s) = \frac{R}{sRC+1} \tag{6.61}$$

All contributions in the voltage loop are now defined and the resulting loop transfer function is:

$$L_V(s) = K_V \frac{\tau_{z2}s+1}{\tau_{p2}s+1}\frac{1}{R_m}\frac{1}{s\tau_{uc}+1}\frac{R}{sRC+1}\frac{1}{K} \tag{6.62}$$

In (6.62) the approximate expression for the closed current loop transconductance (6.58) is used. The control object consisting of the closed current loop and the filter is essentially a first order system within the bandwidth of the current loop, under the assumption that the bandwidth of the current loop is designed sufficiently wide. Subsequently, the voltage loop optimization differs considerably from VFC1 in terms of compensator characteristics. The voltage loop compensator gain to realized the specified bandwidth is found:

$$\begin{aligned} &|L_V(j\omega_{uv})| = 1 \;\Rightarrow \\ &\left|\frac{K_V}{K}\frac{\tau_{z2}}{\tau_{p2}}\frac{1}{R_m}\frac{1}{\omega_{uv}C}\right| = 1 \;\Rightarrow \\ &K_V = K\frac{\tau_{p2}}{\tau_{z2}}R_m\omega_{uv}C \end{aligned} \tag{6.63}$$

The resulting voltage loop transfer function is:

$$H_V(s) = K\frac{L_V(s)}{1+L_V(s)} \cong K\frac{1}{s\tau_{uv}+1}\frac{1}{s\tau_{uc}+1} \tag{6.64}$$

6.6.3 Current and voltage loop shaping

A general loop shaping approach is presented for the CVFC topology, such that the criteria for stability and robustness *(NS, NP, RS and RP)* are obeyed within defined *US*. The current loop is shaped for a to realize a first order characteristic beyond the target bandwidth, with a slope that approaches $N_L = -1$. Similar, the voltage loop is shaped towards a first order characteristic within the bandwidth of the current loop. To minimize

Parameter	Value	Comment
f_{uv}	$f_{uv}=\frac{f_{uc}}{2}$	Bandwidth of voltage loop
$f_{p1}=\frac{1}{\tau_{p1}}$	$\frac{1}{10}f_o$	Current loop compensator pole
$f_{z1}=\frac{1}{\tau_{z1}}$	f_o	Current loop compensator zero
$f_{p2}=\frac{1}{\tau_{p2}}$	$\frac{1}{20}f_{uv}$	Voltage loop compensator pole
$f_{z2}=\frac{1}{\tau_{z2}}$	$\frac{1}{2}f_{uv}$	Voltage loop compensator zero
f_o	1	Post filter natural frequency
Q_N	$\frac{1}{\sqrt{3}}$	Nominal post filter Q (Bessel characteristic)
f_r	$\frac{1}{2}f_{uc}$	Reference filter R(s) frequency
Q_r	$\frac{1}{\sqrt{3}}$	Reference filter R(s) Q (Bessel characteristic).

Table 6.3 Proposed general parameter values for the CVFC topology.

the degrees of freedom, the relationship between the current loop bandwidth and voltage loop bandwidth is a locked at a factor two. It is necessary with a sufficiently wide current loop to secure sufficient compensation for the voltage loop within the defined *US*. On the other hand, it is desirable to maximize the voltage loop bandwidth as much as possible relative to the current loop to secure maximal compensation, and the proposed factor of two will prove to be a good compromise. The proposed general current loop and voltage parameters that define the loop shaping are specified in Table 6.3. Note, that the demodulation filter natural frequency is specified low ($f_o=1$) for the CVFC topology, compared with $f_o=2$ for VFC1 and $f_o=3$ for VCF2. This is made possible by the excellent control over the load that is offered by the topology. The advantages of the CVFC topology become apparent with the following case example, where CVFC synthesis and verification is illustrated in more detail.

6.6.4 CVFC Case example

STEP 1: Specification

It is assumed that the fundamental parameters are as specified for the other topologies. However, it is assumed that the plant requires a more effective control to suppress the error sources, and that this can be achieved with a more tight $S_{\max}$. A fundamental advantage of the dual loop topology is that the compromise between bandwidth and performance is significantly different. The input parameter specifications for the loop synthesis are:

Parameter	Value
K	26dB
K_{PN}	26dB
$S_{\max}$	-30dB
R_m	0.3

STEP 2: Synthesis
The performance requirements can be realized by $f_{uc} = 8$, corresponding to a voltage loop bandwidth of $f_{uv} = 4$. With an approximate first order characteristic in each loop, the expected maximal sensitivity functions are:

$$S_{M,c} = -18dB \quad \text{and} \quad S_{M,v} = -12dB$$

Corresponding to: $S_M = S_{M,c}S_{M,v} = -30dB$ in the nominal case. With the current loop bandwidth determined, the synthesis of the individual controllers is trivial from the general parameter assignments in Table 6.3.

STEP3: Verification
Fig. 6.26 - Fig. 6.27 shows Bode plots for the current and voltage loop. The loop bandwidths are as specified.

With the specified parameters, the current loop is compensated to a near first order characteristic. A steeper slope is possible without compromising nominal stability, but this will compromise the robustness of the dual loop system. Note however, that the current loop slope is slightly steeper that expected since the zero in $C_C(s)$ and the two poles and one zero in $G_O(s)$ do not cancel perfectly. The performance parameters for the optimized current loop are found to:

$$\|S_C\|_\infty = 1 \quad S_{M,c} = -22dB \quad \textit{(Current loop)} \tag{6.65}$$

$$\|S_V\|_\infty = 1.3 \quad S_{M,c} = -13dB \quad \textit{(Voltage loop)} \tag{6.66}$$

Thus, the effective sensitivity function is:

$$S_M = -35dB \tag{6.67}$$

Consequently, the criteria for *NS* and *NP* are satisfied by a considerable margin. Clearly, the dual loop topology is superior in terms of nominal performance compared with VFC1 and VFC2, although the bandwidth requirements for the three topologies are the same.

Fig. 6.29 shows the perfectly flat frequency response of the dual loop controlled system. The 3dB bandwidth of the dual loop system is 6.5, notwithstanding that the demodulation filter natural frequency (and thereby the open loop system) is as low as $f_o = 1$. This clearly illustrates one of the advantages of feedback control from the global output – high bandwidth and perfect frequency response can be combined with optimal demodulation. The complete system response is controlled by the input filter response.

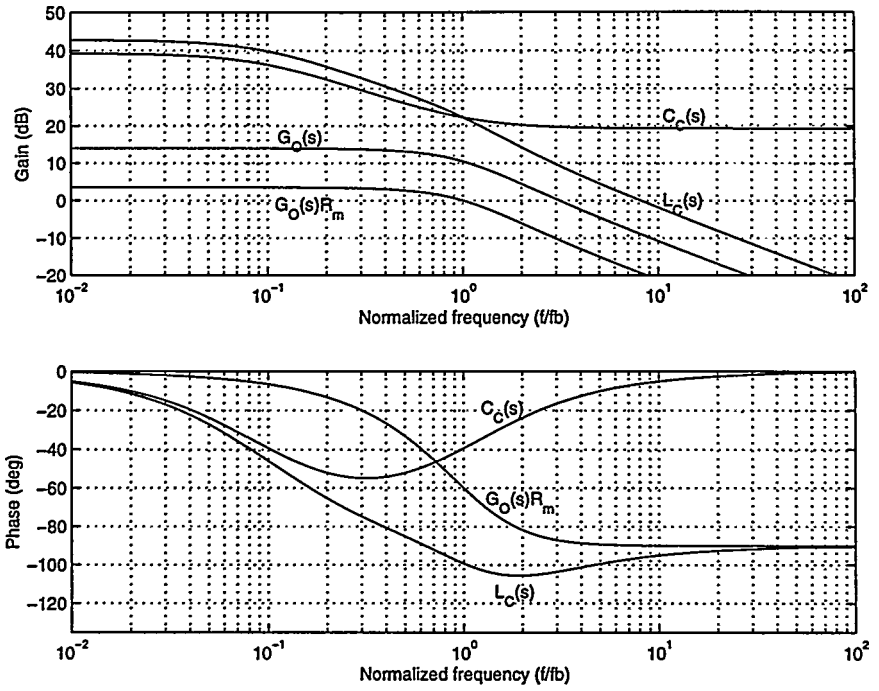


Fig. 6.26 CVFC case example. Bode plot of current loop components and the resulting current loop transfer function $L_C(s)$.

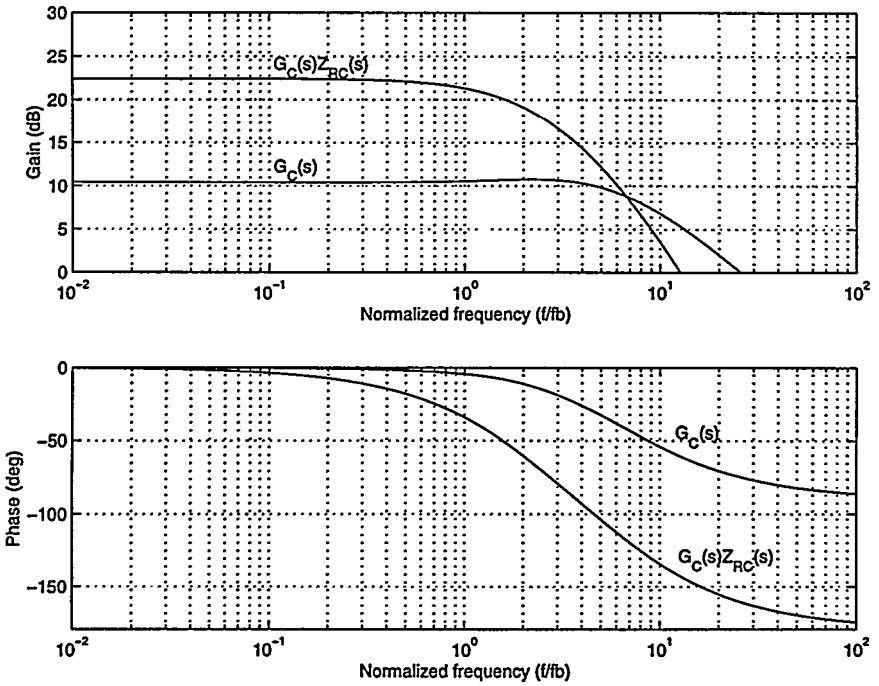


Fig. 6.27 CVFC case example. Bode plots of closed current loop transconductance $G_C(s)$.

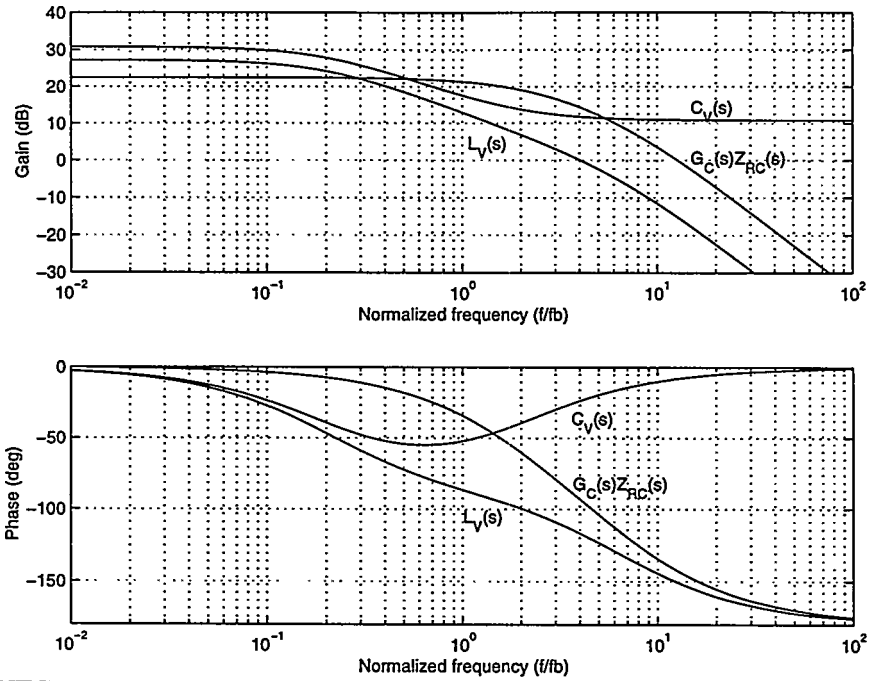


Fig. 6.28 CVFC case example. Bode plot of voltage loop components and the resulting loop transfer function $L_V(s)$.

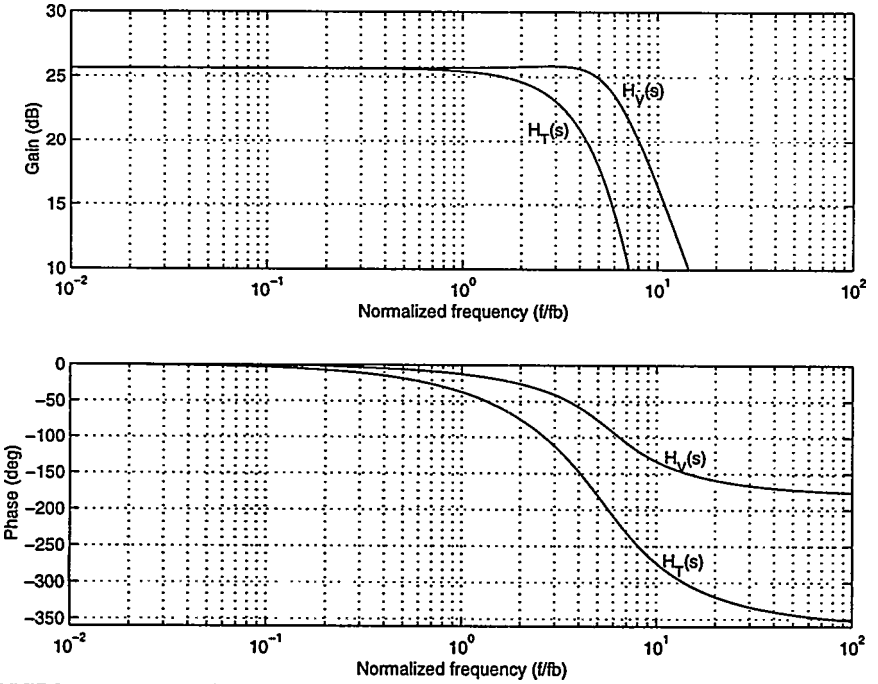


Fig. 6.29 CVFC case example. Bode plot of system transfer function w/o reference input filter.

STEP 4: Robustness properties

It is a more involved task to verify robustness for multi-loop systems, since the influence of perturbations within a given loop on the other loops of the system will be more difficult to evaluate. Any perturbations on the plant will directly influence the current loop performance whereas the voltage loop is partially "protected" from uncertainty since the current loop will attempt to suppress undesirable effects caused by parameter variations. The set of perturbed transfer functions within the *US* can be expressed as:

$$L_{C,p}(s,r_K,r_Q,t_P) = K_C \frac{\tau_{z1}s+1}{\tau_{p1}s+1} \cdot \frac{r_K K_{PN}}{L} \frac{s+\frac{\omega_0}{r_Q Q_0}}{s^2+\frac{\omega_0}{r_Q Q_0}s+{\omega_0}^2} \cdot R_m \cdot e^{-t_P s} \tag{6.68}$$

$$L_{V,p}(s,r_K,r_Q,t_P) \cong K_V \frac{\tau_{z2}s+1}{\tau_{p2}s+1} \frac{1}{R_m} \frac{1}{sr_K\tau_{uc}+1} \frac{r_Q R}{sr_Q RC+1} \frac{1}{K} \tag{6.69}$$

Fig. 6.30 shows the sensitivity functions corresponding to the worst-case plants within the uncertainty set, corresponding to $S_{C,p}(s,0.5,4,200ns)$ and $S_{V,p}(s,0.5,4,200ns)$. The perturbed sensitivity functions are compared with the nominal case. The following performance specifications are realized:

$$\left\|S_{C,p}\right\|_\infty = 0dB \quad S_{M,c} = -18dB \tag{6.70}$$

$$\left\|S_{V,p}\right\|_\infty = 9dB \quad S_{M,v} = -17dB \tag{6.71}$$

RS and *RP* are satisfied.

That $\left\|S_{V,p}\right\|_\infty$ is close to the specified limit for *RP* only emphasizes that the specified parameters for CVFC are close to optimal. Fig. 6.30 shows how r_Q affect both loops simultaneously. Increasing r_Q decreases the current loop gain and increases the voltage loop gain, and vice versa. Due to these proportional relationships, the resulting sensitivity function within the target frequency band will *only change marginally* with r_Q, which is an interesting property for the CVFC topology.

Physically, this should be interpreted as:
Increasing the load impedance (r_Q) will increase the loop gain correspondingly, since a higher load impedance results in a lower current output to the load. Accordingly, the current loop gain is inversely proportional to the load impedance and equally inversely proportional to r_Q. On the other hand, increasing the load impedance will increase the voltage produced by a given current in the load, i.e. the voltage loop gain increases with the load impedance.

Fig. 6.31 compares the resulting system transfer functions with the nominal and the perturbed system. The frequency response is only affected marginally within the target frequency band, in that the system perturbation causes the system peak slightly at the

bandwidth limit (0.3dB). Furthermore, the increasing voltage loop gain causes the system gain to converge towards the desired 26dB. The response is concluded to be excellent even in this worst case situation. The CVFC topology is sensitive to uncertainties on K_P, since K_P variations directly influence the current loop bandwidth. This is a drawback compared with the single loop control methods that there shown to be perfectly robust towards wide perturbations on K_P. On the other hand, the CVFC-topology excels by a remarkable robustness towards to other parameters within the *US*. The proposed CVFC will leave the system response and performance nearly unaffected, even with significant perturbations on the load. This special feature will be demonstrated by investigating the limiting case $r_Q \to \infty$, corresponding to an open load. Fig. 6.32 shows the sensitivity functions corresponding to the perturbed system and Fig. 6.33 shows the resulting system response. The performance parameters are:

$$\left\|S_{C,p}\right\|_\infty = 1 \quad and \quad \left\|S_{V,p}\right\|_\infty = 1.66 \tag{6.72}$$

RP and *RS* are obeyed by significant margins and the system response is nearly unaffected by this extreme perturbation.

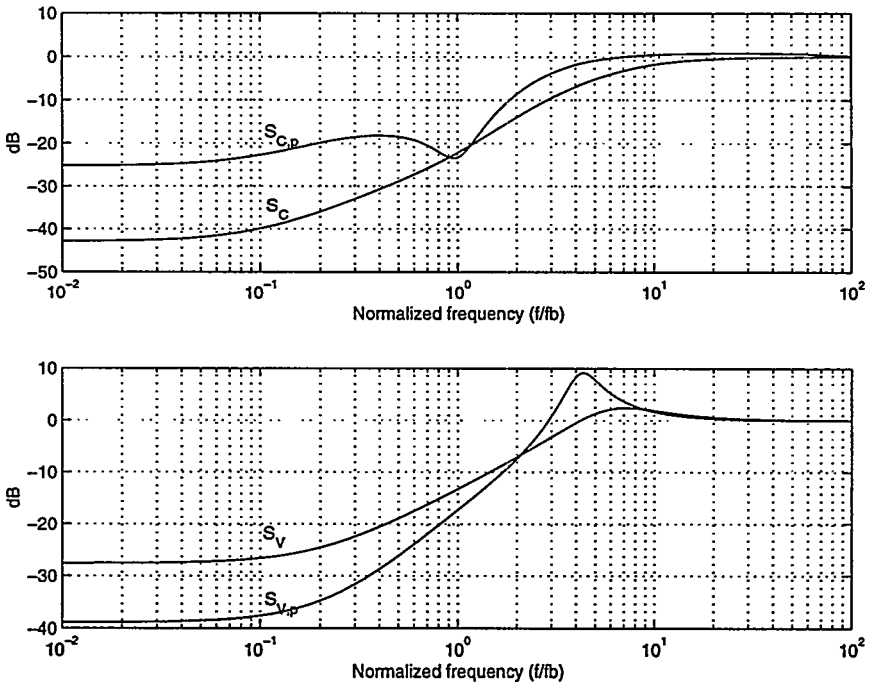


Fig. 6.30 Robustness investigation for CVFC case example. The sensitivity functions corresponding the worst-case perturbations, $S_{C,p}(s,0.5,4,200ns)$ and $S_{V,p}(s,0.5,4,200ns)$, are compared with the sensitivity functions for the nominal system.

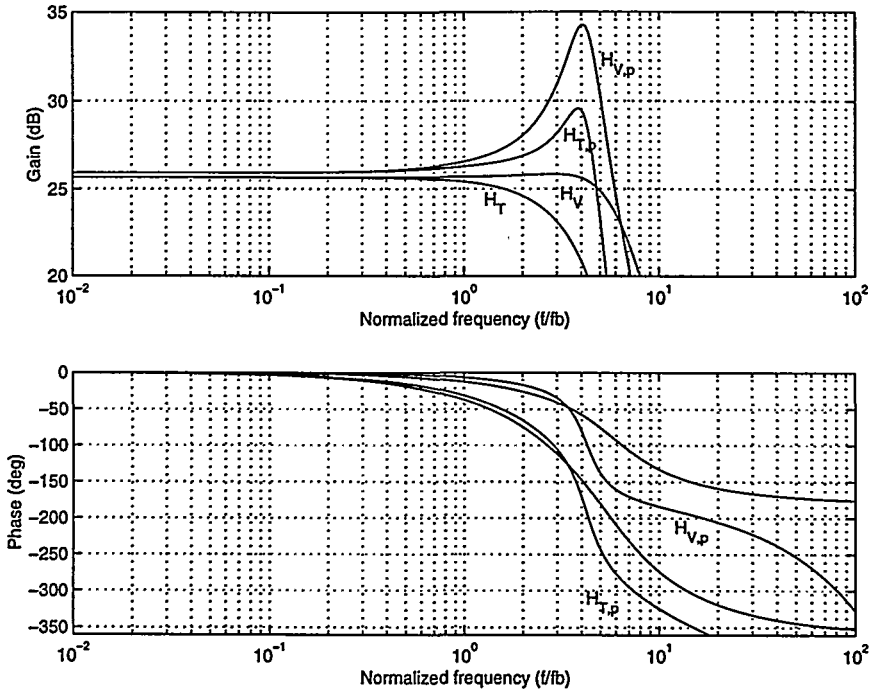


Fig. 6.31 Robustness investigation for CVFC case example. System transfer functions for the nominal system and the perturbed system compared.

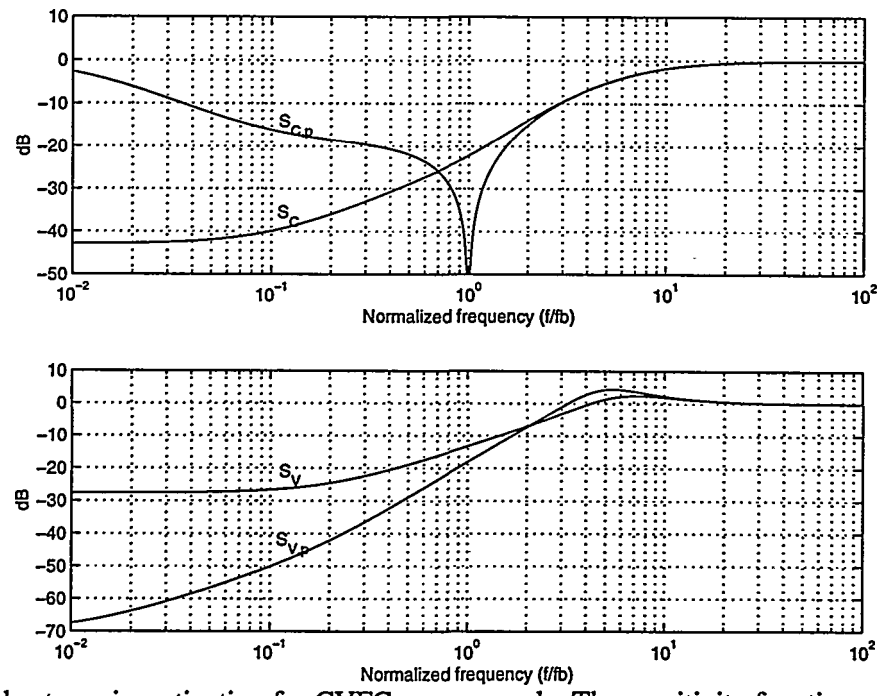


Fig. 6.32 Robustness investigation for CVFC case example. The sensitivity functions are illustrated in the limiting case $r_Q \to \infty$ are compared with the function for the nominal system.

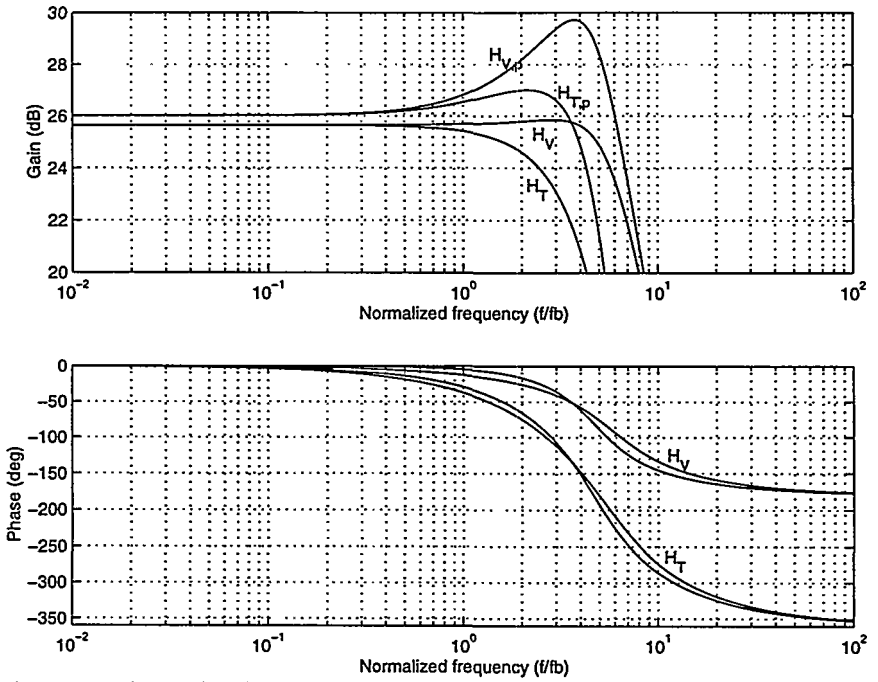


Fig. 6.33 Robustness investigation for CVFC case example. The system transfer function is investigated in the limiting case $r_Q \rightarrow \infty$ are compared with the response for the nominal system.

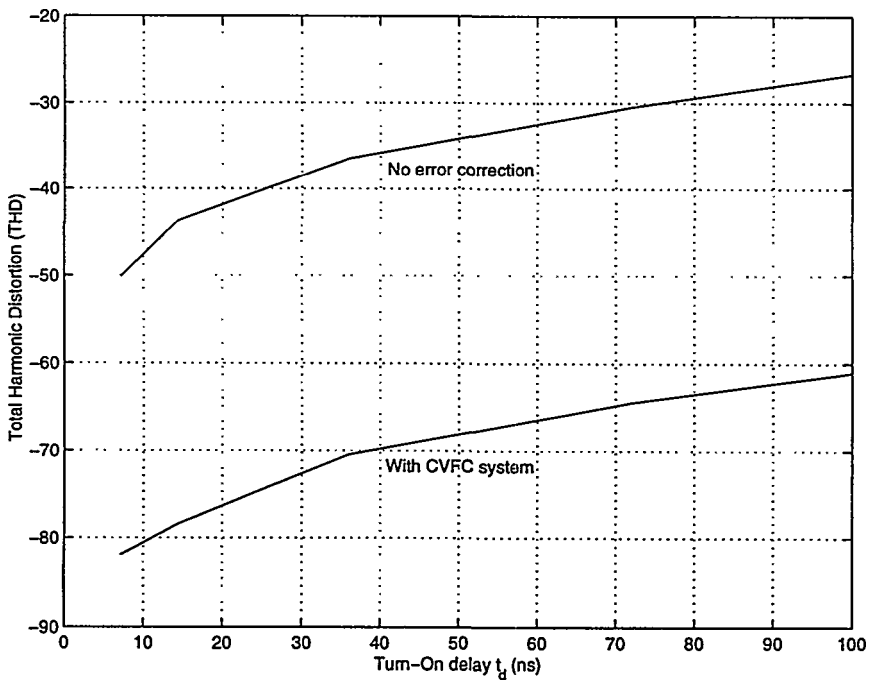


Fig. 6.34 Parametric investigation of THD vs. t_D in the worst-case situation (f=5KHz, M=0.5)

STEP 5: Non-Linear simulation

The non-linear system simulation is based on the same power stage as for VFC1. Furthermore, NADD PWM and a carrier frequency of $f_c = 400KHz$ is used for comparison. Recall for the investigations for VFC1, that the maximal amplitude of the carrier component to prevent SRI with the given parameters is:

$$v_{c,dp} < \frac{2V_T}{\pi} = 1.6V \tag{6.73}$$

This can be related to the current loop transfer function with the equation:

$$|L(j\omega_c)| < \frac{K_{PN}}{\hat{v}_p} v_{c,dp} \approx 0.5 \tag{6.74}$$

For the synthesized current loop $|L(j\omega_c)| = -8db$, and the CVFC system is clearly much closer to the SRI limit, although there is still a reasonable margin. The explanation is that the current loop is a *first order system* with less attenuation of HF components that the inherent second order systems VFC1 and VFC2.

Fig. 6.35 shows as a functional simulation at idle, verifying that the dual loop system is stable. As predicted, the HF content on the modulating signal is higher than for VFC1 and VFC2. The modulator input is superposed by harmonics of the carrier component from the current feedback. The higher order harmonics are significantly more visible than for VFC1 and VFC2. The fundamental is found to:

$$v_{c,dp} = 1.1 \tag{6.75}$$

I.e. there is a reasonable margin to SRI in the nominal case, as expected from the theoretical investigations above. However, with a worst-case $r_K = 1.5$ perturbation the system will be on the edge of SRI. It is possible to modify the current loop to have a second order characteristic at higher frequencies for further attenuation of the HF-components with only marginal influences on stability and robustness. Other solutions include the use of tuned circuits and of course – use of improved modulation methods as NBDD PWM.

Correction of PTE

Fig. 6.36 shows the controller signal and the resulting output in the two extremes t_d=10ns and t_d=100ns. Both linear and non-linear errors are considerably reduced i.e. the outputs are indistinguishable in the time domain. The distortion is reduced from nearly THD=5% in the open loop case to only THD=0.09% in this worst-case situation, or about 34dB as expected. The correction is primarily performed by the current loop as seen from the current loop compensator output signal which has significant pre-distortion in the case t_d=100ns in order to compensate the power stage non-linearity. The voltage loop controller output on the other hand is only marginally affected by the non-linearity, i.e. the voltage loop is operating on an *already much improved plant*. Fig. 6.34 shows a parametric simulation of the resulting THD vs. t_d with and without control. The improvement is about 34dB independent upon the level of non-linearity, corresponding well with theory.

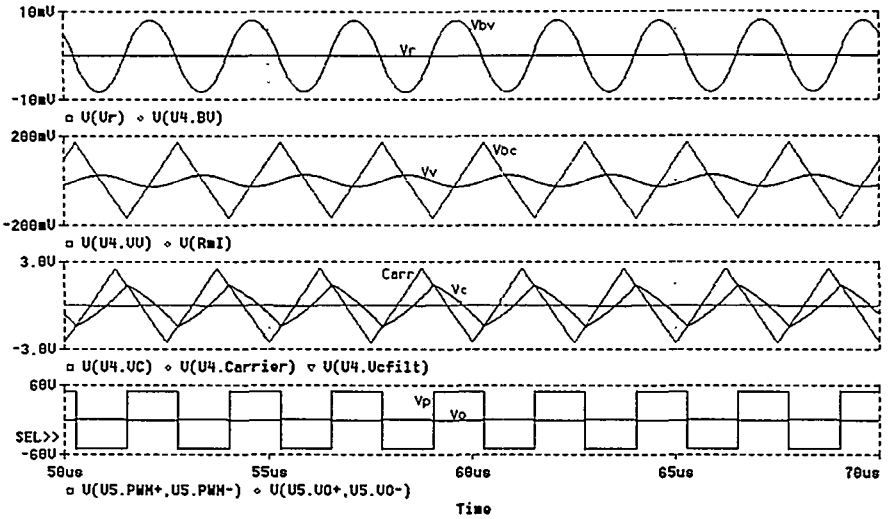


Fig. 6.35 Functional simulation of CVFC system. Top – voltage feedback v_{bv} and reference v_r, Mid1 – Current feedback v_{bc} and voltage loop compensator v_v, Mid2 – Carrier and compensator v_c. Bottom – resulting power stage signals v_p and v_o.

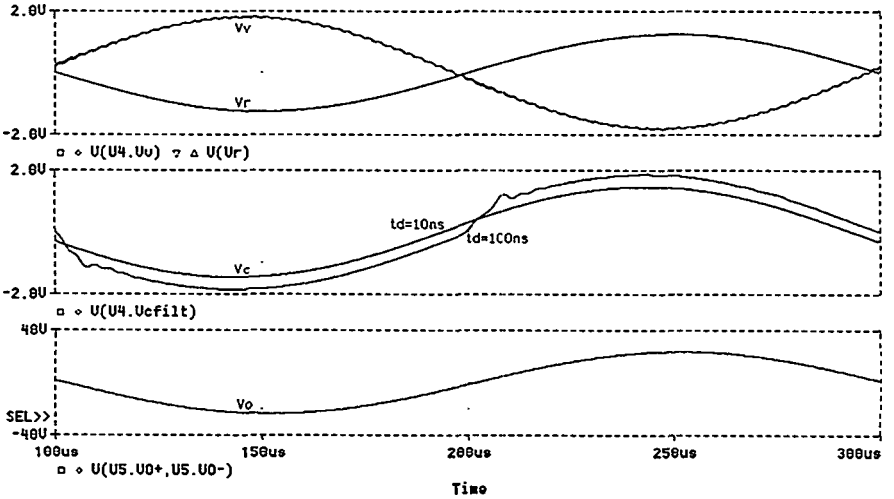


Fig. 6.36 Simulation of CVFC system with PTE. Note the predistortion on the current compensator output = the modulator input.

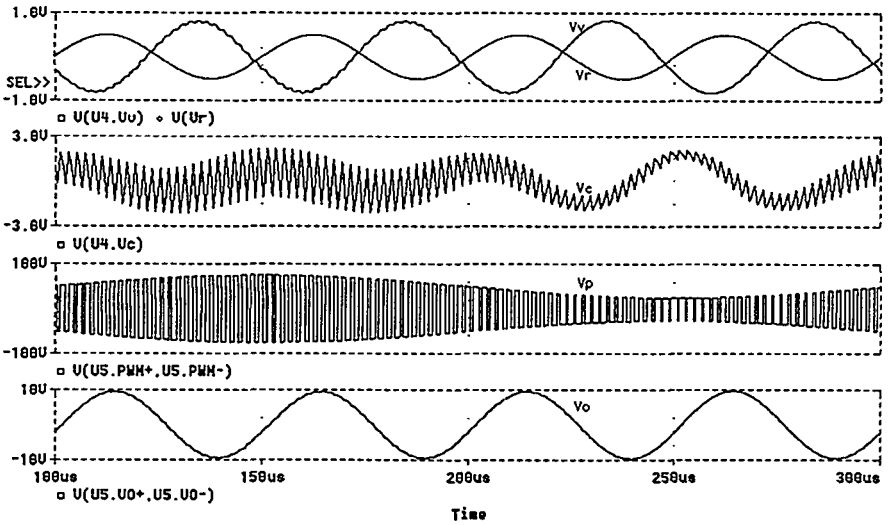


Fig. 6.37 Simulation of CVFC system with PAE. (50Vpp/5KHz perturbation on the power supply).

Correction of PAE
Fig. 6.37 shows the controller signals and resulting outputs with a severe perturbation on the power supply of a 5KHZ, 50Vpp component. The signal frequency is 20KHz and the modulation index M=0.2 in the simulation. Clearly, the current loop apparently is the "working" loop in terms of suppression of the error. With the CVFC topology, IM-distortion components at 15KHz and 25KHz are reduced around 30dB corresponding to theory. The resulting IM-distortion is not visible in the time domain.

6.7 Summary

The chapter has been devoted the application of robust linear control to PMA systems, in order to reduce the sensitivity to error sources and hence stabilize and improve performance compared to non-controlled systems. An initial study of the *plant* to be controlled revealed that there are significant complications and numerous parameters to consider when optimizing control systems of PMAs. The complications especially cover the power stage HF-noise source (that depends on the modulation method), the necessary demodulation filter and the constraints on bandwidth, that are dictated by limitations on carrier frequency. The plant *uncertainties* were investigated and general stability and performance criteria were defined based on a defined Uncertainty Set.

A simple framework for the general design and verification of robust control systems for PMAs was presented. Based on initial plant studies and the specification of desired performance, the design methodology involves a six step process of synthesis and performance evaluation at various levels.

Three linear control methods VFC1, VFC2 and CVFC have been defined and simple approaches to robust control system design were presented. The proposed loop shaping method reduces the degrees of freedom to a single performance parameter such that the controller synthesis is trivial.

The three topologies proved to have different characteristics, in terms of controller complexity, performance, bandwidth requirements, robustness and the stabilization of closed loop frequency response. Al topologies have their advantages and drawbacks:

The VFC1 topology proved advantageous in several specific aspects. The control system will attack all error generated in modulator, switching power stage *and* filter. A further advantage is the excellent frequency response, stable against load variations within reasonable limits. On the other hand, a range of problematic issues can also be identified. The reduction of sensitivity is constrained at high frequencies, and the controller has to realize a high gain at high frequencies with requires wide-band controller components.

VFC2 it is the simplest possible topology. The system is furthermore highly robust to uncertainty within the Uncertainty Set, since the filter is not included within the loop. On the other hand there are also drawbacks, i.e. the filter is not controlled so both demodulation and system response are compromised.

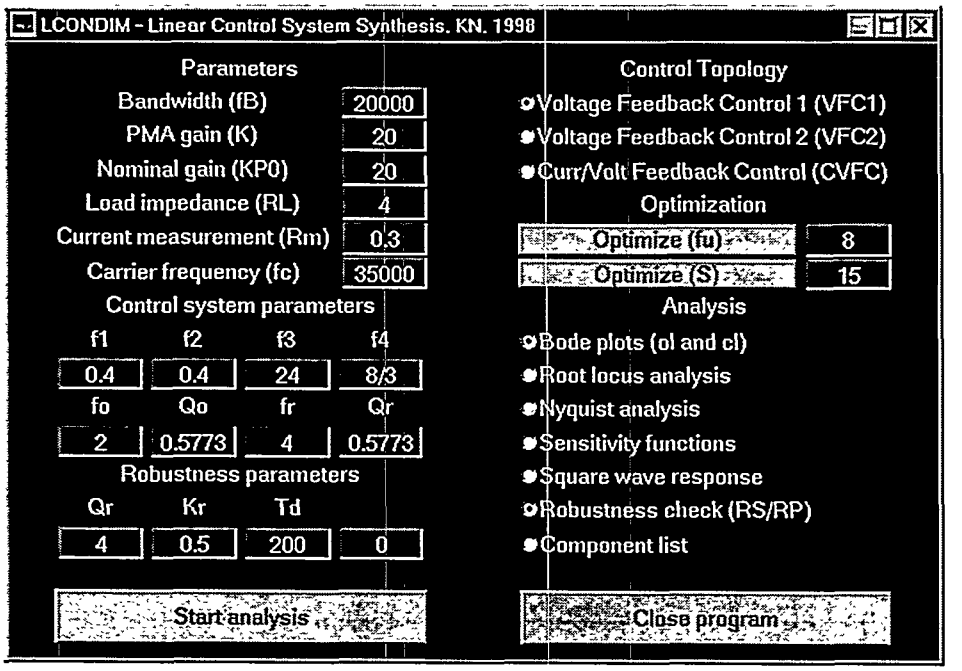
CFVC is more complex than the two topologies, especially in terms of the requirement for precision current measurement. However, there are several compensations. The current loop reduces the sensitivity to errors in the power stage considerably close to the source of the errors. The current loop furthermore provides the compensation making the global loop straightforward to apply. The voltage loop further improves the system, by reducing the

sensitivity to both power stage and filter errors. The total CVFC system proved to superior on several aspects, especially in terms of performance within a given bandwith and stability to load perturbations.

To conclude, the investigated control methods offer a remarkable value compared with the hardware needed for implementation. Generally, the control system will only marginally increase system complexity and cost since the system complexity in PMAs is dominated by the power stage and filter exclusively. From this point of view, it is paradoxical that control systems have received so little attention in previous work.

6.7.1 LCONDIM design toolbox for MATLAB

A toolbox for control system design and verification has been developed for MATLAB. A GUI controlled MATLAB program simplifies the systematic and automated design of the VFC1, VFC2 and CVFC control structures. The graphical user interface is shown below.



Based on the primary PMA input and performance specifications the toolbox provides push button access to:

- Control system synthesis and verification using standard analysis methods.
- Application of Uncertainty to the plant for robustness investigations.
- Controller component synthesis for non-linear simulation and practical evaluation.
- Manual tuning of individual parameters for specific applications.

The software tool has been used extensively throughout the present chapter for the analysis and verification of the VFC1, VFC2 and CVFC topologies.

Part III

Chapter 7

Optimized Linear Control

The paper proposes a novel control method for analog PMAs – *Multivariable Enhanced Cascade Control (MECC)*[1]. The topology has been devised to match the specific problems in general PMA systems. The primary motivation has been to meet any performance requirements even with very nonlinear and noisy plants. Recall that the fundamental control topologies analyzed in Chapter 6 were all bonded by inherent limitations, especially when attempting to realize high performance PMA systems. The proposed multiple-loop MECC topology overcomes several of these constraints, and enables flexible control of all essential system parameters by relatively simple means. MECC(N) and MECC(N,M) will be introduced as two general multiple-loop control methods. A general analysis of the properties will be presented. Following, the issue of robust MECC based PMA design is addressed by presenting optimized loop shaping methods. Case examples studies are investigated using the step-wise methodology for design and verification that was developed in Chapter 6.

7.1 Multivariable Enhanced Cascade Control (MECC)

MECC has two fundamental variants henceforth referred to as MECC(N) and MECC(M,N). A general block diagram for the N-loop MECC(N) topology is shown in Fig. 7.1, and Fig. 7.2 shows the extended general (N+M)-loop MECC(N,M) topology. Fundamentally, MECC is based on a recursive structure of N loops formed as an *enhanced*

[1] The MECC topologies and design methods are protected by a pending patent under the PCT arrangement (PCT/DK97/00497). The rights of the author and co-applicant (Bang & Olufsen A/S) shall be respected.

cascade from a single feedback source. MECC(N) is founded on feedback of v_p to one or several loops feeding into one or several pre-amplifier stages preceding the modulator and power switch. It may not seem obvious at first that MECC(N) should add any obvious advantages over VFC2. However, it will become apparent that this simple "extension" offer significant advantages with optimized compensator realization. MECC(N) is characterized by the following distinct points:

- A *single* feedback source.
- A *single* feedback path $A(s)$ independent upon the number of loops N, providing a minimal system complexity.
- The feedback path has a *low-pass* characteristic, to filter the noise from v_p *and* compensate the demodulation filter.
- An initializing $B_1(s)$ compensator block with special characteristics.
- A *recursive* structure with a set of preferably *identical* forward path compensator blocks $B_i(s)$.

Thus, the *Enhanced Cascade* refers to these special cascade control characteristics or this dedication of the cascade to the PMA control problem. Cascade control methods have previously been applied to linear power amplifier systems, in terms of e.g. the well known Nested Differential Feedback Loop method (NDFL's) [Ch82]. This cascade structure has some resemblance with MECC(N) in that it uses only one feedback element with a differentiating characteristic. However, differentiating the HF- feedback source v_p in this case is clearly impossible, since it would cause the feedback compensator output to produce a severe amount of HF-output with amplitudes approaching infinity (!). Cherry's motivation for developing the NDFL control method was to realize improved control of the linear power amplification stage. The motivation for developing MECC for PMA system has been similar.

The MECC(N,M) topology shown in Fig. 7.2 is an extension in that an additional enhanced cascade is established from v_o to one or several chained pre-amplifier stages. MECC(N,M) encloses the PMA by two *connected* enhanced cascades, providing optimized control of all system parameters as distortion, noise, output impedance, PSRR etc. The connection between the enhanced cascades is established by the inherent compensation that is provided by unique A-block in the local enhance cascade. A fundamental constraint within MECC(N,M) system design is thus:

$$M \geq 1 \Rightarrow N \geq 1 \tag{7.1}$$

MECC(N) provides optimized control in dedicated applications where filter linearity is unproblematic and the load is known. The MECC(N,M) provides optimized control in all general applications. Both topologies have their place.

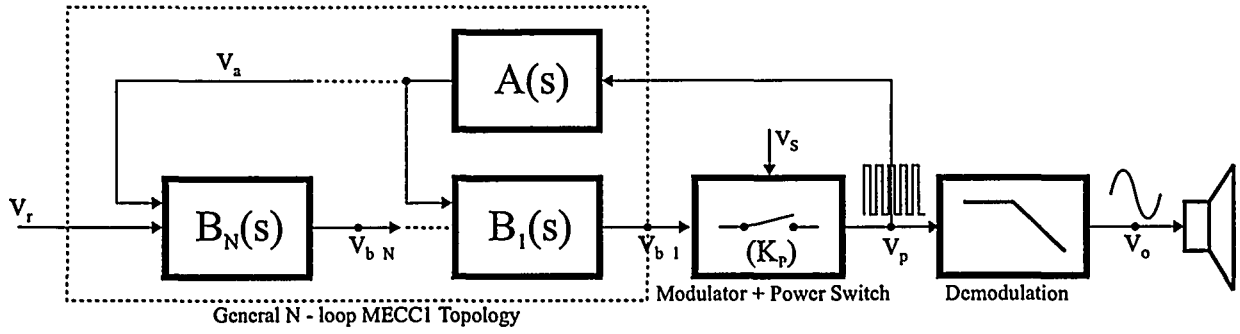


Fig. 7.1 General N-loop MECC(N) topology

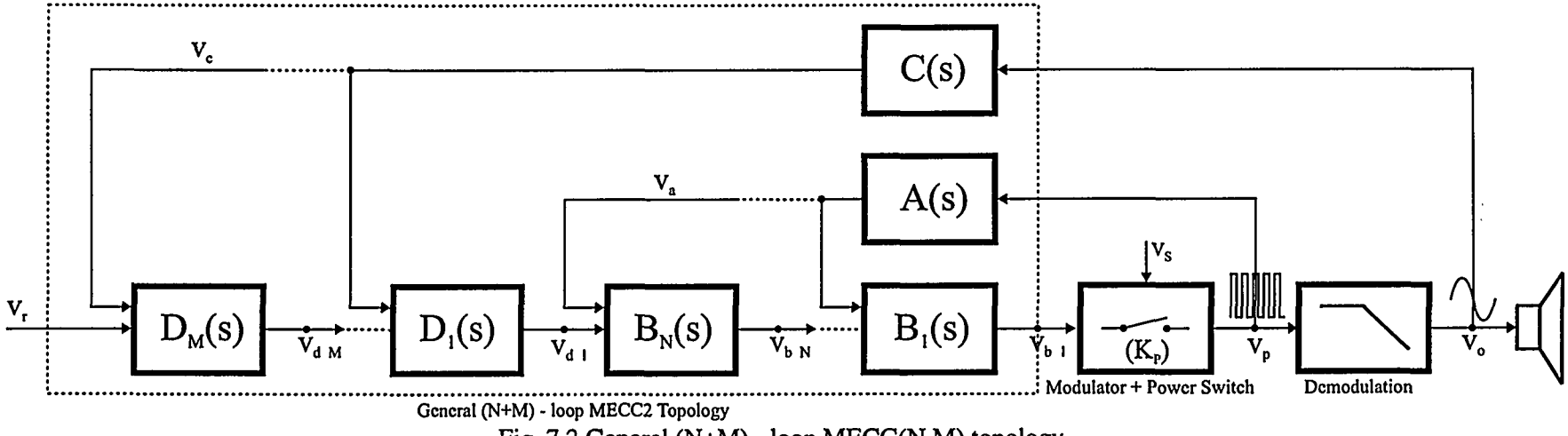


Fig. 7.2 General (N+M) - loop MECC(N,M) topology

7.1.1 Loop prototype based MECC(N) synthesis

In the following general N-loop MECC(N) controller synthesis is addressed, with the proposal of a general recursive design procedure. The foundation is a *loop prototype* based design approach that simplifies the synthesis, verification and implementation of the controller compared to individual parameter optimization of each loop in the multi-loop system. More important, prototype based design leads to a highly regular and flexible structure where the resulting performance is easily evaluated independent of the number of loops in the system. The flexibility arises from the loop number N that adds new flexibility to the loop shaping process in combination with the loop prototype specification. There are some fundamental prototypes with appealing characteristics. These prototypes and the prototype realization within the MECC(N) structure will be discussed in the following.

Leaky integrator Prototype

Consider the simple MECC(N) loop prototype specified:

$$L(s) = \frac{\tau_{il}}{\tau_{uN}} \frac{1}{\tau_{il} s + 1} \tag{7.2}$$

The "leaky integrator" characteristic of the loop prototype has the advantage of a constant gain within the frequency range determined by integrator time constant τ_{il}. This can be used to implement a constant gain characteristic of the resulting sensitivity function within the target bandwidth, with a magnitude now determined exclusively by the loop number N. The bandwidth of the loop prototype is determined by τ_{uN}. The MECC(N) topology itself does not inherently provide an improved control of the PMA system, as the comparison with the topologically similar NDFL method clearly illustrated. A crucial aspect is the implementation of the loop prototype is the forward and feedback path compensators. The prototype is realized with the following A-compensator block characteristic:

$$A(s) = \frac{1}{K} \frac{1}{\tau_1 s + 1} \tag{7.3}$$

Where K determines the resulting closed loop gain within the target bandwidth of the system. The advantages of this A-block characteristic is the filtering of HF-noise from the v_p-generator in the case that carrier based modulation is used. Furthermore, the characteristic effectively prepares the local enhanced cascade for the application of a further global enhanced cascade by implementing a closed loop compensation effect. With $A(s)$ determined the following initial compensator B_1 will realize the desired loop prototype:

$$B_1(s) = \frac{K}{K_{PN}} \frac{\tau_{il}}{\tau_1} \frac{\tau_1 s + 1}{\tau_{il} s + 1} \tag{7.4}$$

K_{PN} is the nominal gain of the plant as defined in Chapter 6. Its axiomatic that the realization of $L(s)$ in each loop, combined with the unique feedback path compensator $A(s)$ results in a system transfer function that is independent of N, i.e. a closed loop prototype for the local enhanced cascade:

$$\begin{aligned} H_N(s) &= K\frac{L(s)}{1+L(s)} \\ &\approx K\frac{\tau_1 s+1}{\tau_{uN}s+1} \end{aligned} \tag{7.5}$$

The approximation will in general be very good with a reasonable selection of parameters. This will be described at a later point. The realization of $L(s)$ in all succeeding loops requires the following compensator characteristic:

$$B_i(s) = \frac{\tau_{i1}}{\tau_{uN}}\frac{\tau_{uN}s+1}{\tau_{i1}s+1} \tag{7.6}$$

With the loop prototype based approach, MECC(N) optimization only requires optimization of a few fundamental parameters, independent upon the number of loops N. Furthermore, each compensator is simple and straightforward to implement. Both issues are pleasant features.

Modified Leaky Integrator prototype
An obvious extension is to modify the leaky integrator characteristic to a second order characteristic:

$$L(s) = \frac{\tau_{i1}}{\tau_{uN}}\frac{1}{\tau_{i1}s+1}\frac{1}{\tau_2 s+1} \tag{7.7}$$

Realized by modifying the A-compensator to:

$$A(s) = \frac{1}{K}\frac{1}{\tau_1 s+1}\frac{1}{\tau_2 s+1} \tag{7.8}$$

The additional pole improves the demodulation in the local feedback path and lowers the bandwidth to carrier frequency ratio.

7.1.2 MECC(N) properties

The analysis of MECC(N) now proceeds with a more fundamental investigation of the system properties, based on the loop prototype and compensator characteristics. General expressions are derived for the effective sensitivity function and the resulting closed loop transfer function. First the simplified case where $N=2$ is considered. From Fig. 7.1 we get by simple algebraic manipulations:

$$v_o = K_{PN}B_1(B_2(v_r - Av_p) - Av_p) = K_{PN}B_1B_2\, v_r - K_{PN}(B_1B_2 + B_1)Av_p \tag{7.9}$$

Hence:

$$H_N = \frac{K_{PN} B_1 B_2}{1 + K_{PN} A (B_1 B_2 + B_1)} \qquad (N = 2) \tag{7.10}$$

Generalized to the general N-loop case we have from Fig. 7.1:

$$v_p = K_{PN} B_1 (B_2 (B_3 (\cdots B_N (v_r - A v_p) \cdots - A v_p) - A v_p) - A v_p) \tag{7.11}$$

This leads to the closed loop expression:

$$H_N = \frac{K_{PN} \prod_{i=1}^{N} B_i}{1 + K_{PN} A \left[\prod_{i=1}^{N} B_i + \prod_{i=1}^{N-1} B_i + \prod_{i=1}^{N-2} B_i + \cdots + B_2 B_1 + B_1 \right]} \tag{7.12}$$

Which reduces to the following compact expression:

$$H_N = \frac{K_{PN} \prod_{i=1}^{N} B_i}{1 + K_{PN} A \sum_{j=0}^{N-1} \left[\prod_{i=1}^{N-j} B_i \right]} \tag{7.13}$$

With the proposed leaky integrator prototype realized in each loop, it can be shown that H_N realizes the approximate expression as defined in (7.5). The significant importance of (7.13) becomes evident when investigating the effective system that is implemented by the MECC(N) topology. The *effective loop transfer function* L_N and – equivalently – the *effective sensitivity function* S_N are defined as:

$$L_N = K_{PN} A \sum_{j=0}^{N-1} \left[\prod_{i=1}^{N-j} B_i \right] \tag{7.14}$$

$$S_N = \frac{1}{1 + K_{PN} A \sum_{j=0}^{N-1} \left[\prod_{i=1}^{N-j} B_i \right]} \tag{7.15}$$

These parameters will be used to gain insight in the performance and robustness of the effective system that is realized by the MECC(N) topology. Consider a typical case where $|B_i| >> 1$ within the target frequency band. S_N is simplified to:

$$S_N \approx \frac{1}{K_{PN} A \prod_{i=1}^{N} B_i} \quad \forall \omega \quad \textit{within target frequency band} \tag{7.16}$$

This approximate relation shows that the effective sensitivity within the target frequency band is the product of the contributions of each individual loop. Subsequently, the performance can be controlled simply by the number of loops N. Every loop individually exhibits excellent stability, so adding or removing (identical) compensator blocks does not influence stability. Another important aspect is the *successive* improvement afforded by the enhanced cascade configuration as opposed to a single high bandwidth, high gain approach. The successive approach proves more efficient than a one-loop realization.

Control signal characteristics

Another important aspect is the control signal level throughout the system, in terms of the response of the individual compensator blocks to the reference input. The control signal transfer functions are easily derived:

$$H_{Bi,N} = \frac{v_{bi}}{v_r} = \frac{v_p}{v_r}\left(\frac{v_p}{v_{bi}}\right)^{-1} = \frac{H_N}{H_i} \approx 1 \tag{7.17}$$

$$H_{A,N} = \frac{v_a}{v_r} \approx 1 \tag{7.18}$$

The balanced control signals are another advantage gained by the loop prototype based design. The unity gain control signal transfer functions minimizes the requirements for e.g. dynamic range and linearity of the compensator components. Systems with non-balanced control signal may be limited by the compensator performance. A typical example of a system with non-balanced control signals is a single loop higher order control system with multiple series connected compensators.

7.1.3 MECC(N) loop shaping

In general, the process of MECC system design covers the same fundamental steps as for other linear control systems. The actual parameter optimization involving the specification of loop prototype and selection of the fundamental parameters is addressed in the

Parameter	Value	Comment
$f_1 = \frac{1}{2\pi\tau_{p1}}$	f_o	A-block parameter
$f_{i1} = \frac{1}{2\pi\tau_{i1}}$	$\frac{1}{10} f_{uN}$	Pole frequency for loop prototype $L(s)$
N	$N \leq 4$	Limit on necessary (and practical) number of loops in the MECC(N) structure
$f_2 = \frac{1}{2\pi\tau_2}$	20	Parameter for modified leaky integrator prototype
f_o	2	Demodulation filter natural frequency
Q_{oN}	$\frac{1}{\sqrt{3}}$	Demodulation filter Q (Bessel)
f_r	4	Reference filter natural frequency
Q_r	$\frac{1}{\sqrt{3}}$	Reference filter Q (Bessel).

Table 7.1 Proposed general MECC(N) parameter values.

following. Table 7.1 proposes a general set of parameters that serve as guideline to optimized MECC(N) design. The free parameters are the number of loops N and the loop prototype bandwidth f_{uN}. It should be emphasized that the parameters are optimized for the MECC(N) topology specifically, i.e. the parameters change if the system is extended to MECC(N,M). The fundamental parameter τ_{i1} is chosen to realize the desired characteristic of the loop prototype. The A-block parameter τ_1 is optimized to compensate the demodulation filter best possible and to demodulate the power stage output.

The tradeoffs between bandwidth, number of loops and loop prototype will be become clearer throughout the more detailed investigations of an illustrative case example.

7.1.4 MECC(N) case example

MECC(N) system synthesis is illustrated by a case example, using the general controller synthesis and verification steps in coherence with the methodology that was used throughout Chapter 6. A parametric analysis is performed where N is a variable parameter.

STEP 1: Specification

A case example system is considered for the full audio bandwidth with a desired system gain of $K = 26dB$. The equivalent power stage gain is assumed $K_{PN} = 26dB$. No specific performance criteria for the target frequency band are specified. Instead, a parametric analysis of the achievable performance vs. N is carried out.

STEP 2: Synthesis

The simple leaky integrator has been chosen as loop prototype. The prototype bandwidth is selected to $f_{uN} = 5$. The proposed parameters in Table 7.1 are used, and all sub-controllers in the MECC(N) structure are now defined.

STEP 3: Verification

Fig. 7.3 shows the components of first loop and the realization of the loop prototype $L(s)$. Following loops in the enhanced cascade are realized by the addition of further B_i blocks is shown in Fig. 7.4. Fig. 7.5 and Fig. 7.6 illustrate the effective loop transfer function L_N and sensitivity function S_N with the specified parameters. The Nth order transition caused by N poles and N-1 zeros in effective loop transfer is very pronounced from the parametric analysis in Fig. 7.5. The parametric investigation of the effective sensitivity function S_N verifies the excellent stability characteristics for the MECC(N) topology:

$$\|S_N\|_\infty < 1 \quad \forall \omega, N \tag{7.19}$$

This is a general property of MECC(N) with the proposed parameter values in Table 7.1. With the given loop prototype bandwidth we have:

$$S_M = -13 \cdot N \ (dB) \tag{7.20}$$

The system response is shown in Fig. 7.7. The response is dominated by the post filter. With the specified parameters, the resulting system frequency response is acceptable in the nominal load. Clearly, an improved frequency response and reduced sensitivity to load perturbations can be realized by increasing f_0. All essential specifications for the synthesized MECC(N) system are summarized in Table 7.2.

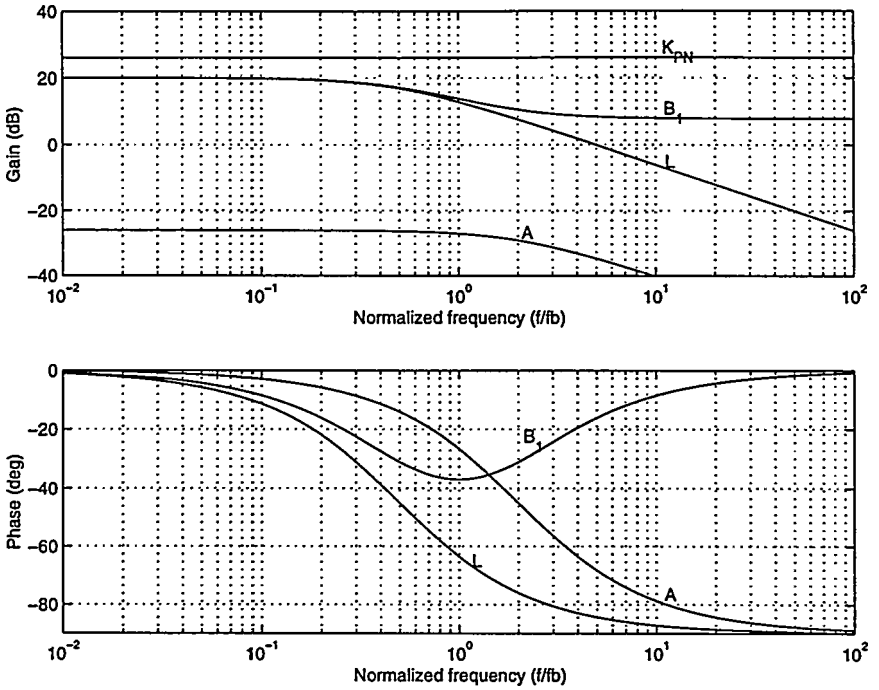


Fig. 7.3 MECC(N) Case example. Components of the first loop and resulting loop prototype $L(s)$.

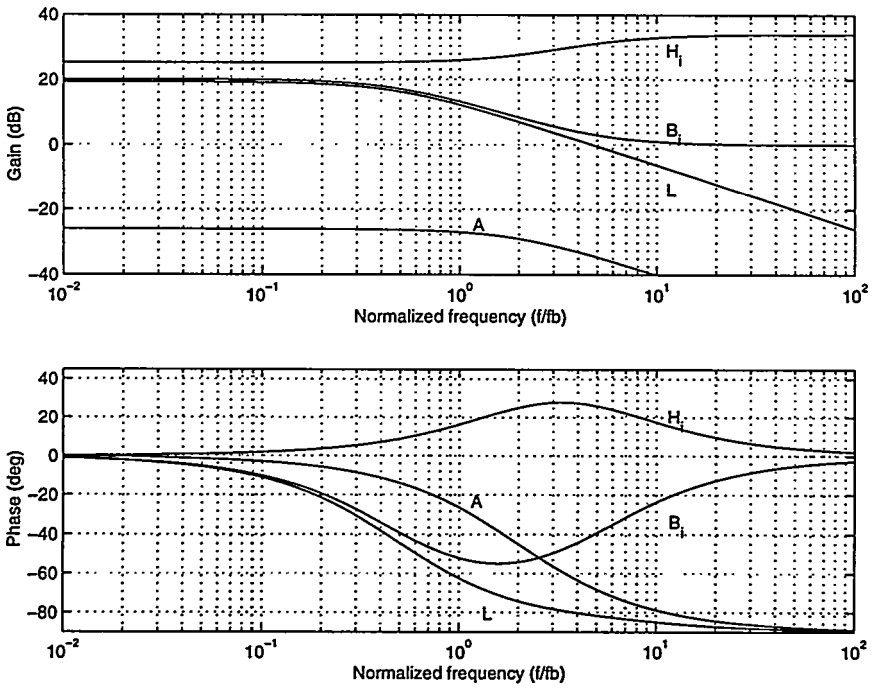


Fig. 7.4 MECC(N) case example. Components of any successive loop.

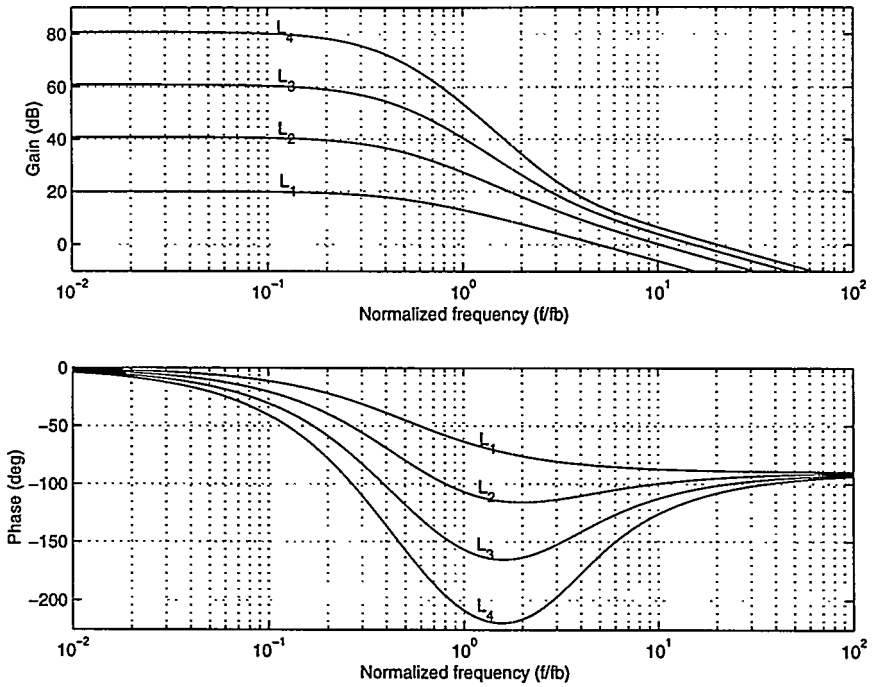


Fig. 7.5 MECC(N) parametric analysis of effective loop transfer function L_N . (N = *1,2,3,4*).

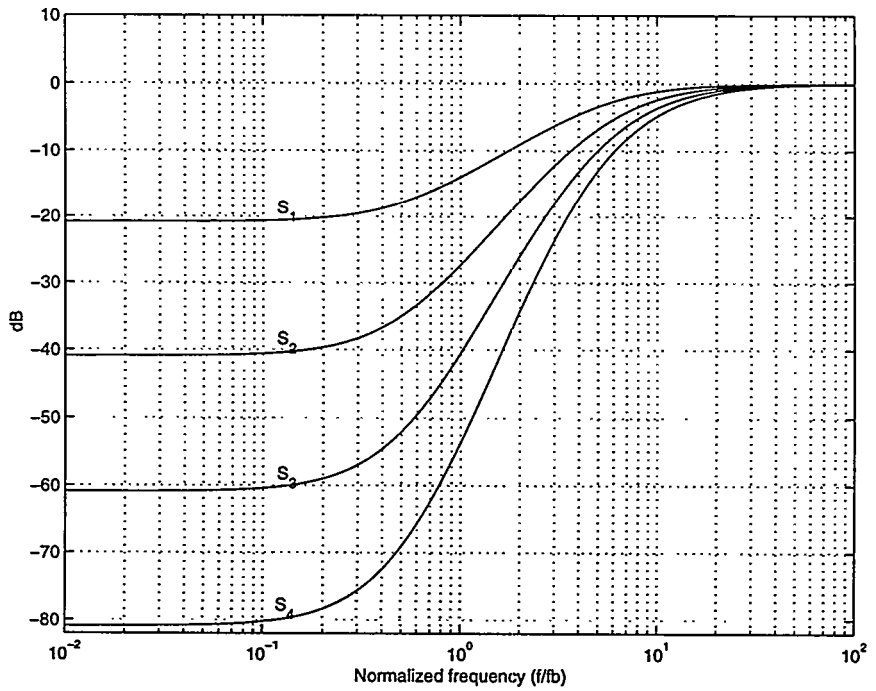


Fig. 7.6 MECC(N) parametric analysis of effective sensitivity function S_N . (N = *1,2,3,4*).

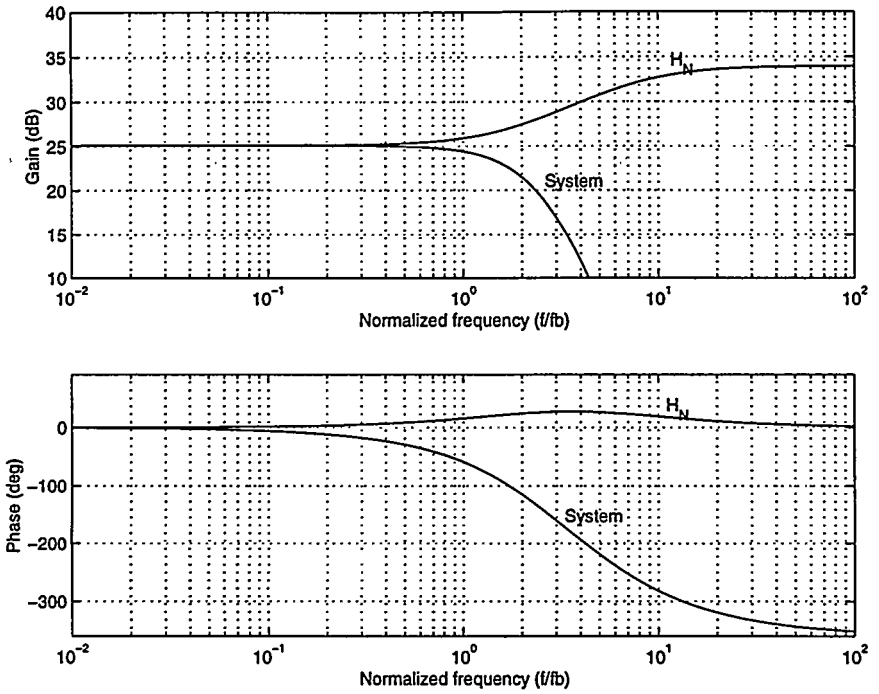


Fig. 7.7 MECC(N) case example system transfer function (independent of N).

Specification	Value	Comments
System gain	*25.1 dB*	20dB feedback.
Bandwidth	2	-3dB normalized system bandwidth.
Frequency response	$\pm 0.5dB$	Nominal system.
Phase response	$\pm 60^0$	Nominal system.
S_M	$-13 \cdot N\ dB$	Nominal system
$\|S_N\|_\infty$	$<1 \quad \forall \omega, N$	Peak of effective sensitivity function.

Table 7.2 Essential stability and performance of the synthesized general MECC(N) system

Modified Leaky Integrator Prototype

The realization of the proposed second order loop prototype is considered:

$$L_N(s) = \frac{\tau_{i1}}{\tau_{uN}} \frac{1}{\tau_{i1}s+1} \frac{1}{\tau_2 s+1} \tag{7.21}$$

The additional pole has the positive effect of improving the demodulation within the feedback path for all carrier based modulation methods and furthermore minimizes the effects of any non-modeled dynamics at higher frequencies. The bonding of the new parameter τ_2 to τ_{uN} (see Table 7.1) prevents any new degrees of freedom that would complicate the otherwise simple controller synthesis. Fig. 7.8 shows a parametric analysis of S_N for (N = *1,2,3,4*). In terms of performance characteristics within the target frequency band, the differences are insignificant. The significant differences lies in the stability characteristics, i.e. $\|S_N\|_\infty$. Recall that $\|S_N\|_\infty < 1 \quad \forall \omega, N$ with the first order prototype whereas the following is realized with the second order loop prototype:

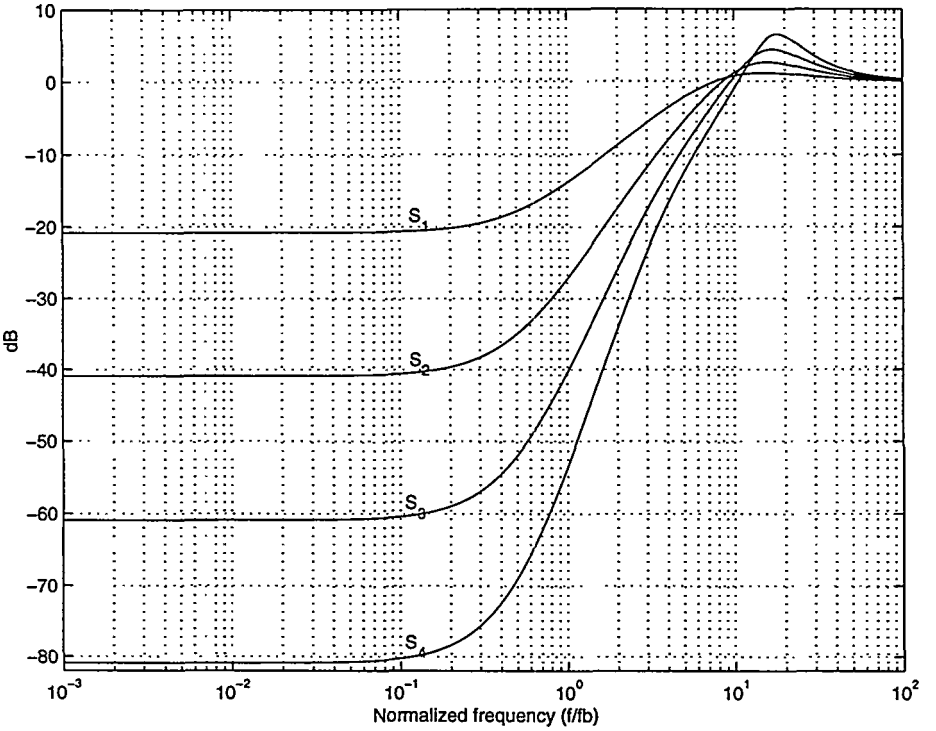


Fig. 7.8 S_N with the modified second order loop prototype. (N = *1,2,3,4*)

N	1	2	3	4
$\|S_N\|_\infty$	1.13	1.35	1.65	2.11

Correspondingly, the second order prototype based design is accompanied by compromises on performance, i.e. *NP* requires $N<3$. Clearly, the second order prototype based system converges towards instability with N. It is possible to optimize each individual compensator in the MECC(N) structure to minimize this effect but the result is hardly as elegant and general as the simple recursive design. Instead, τ_2 should be modified if a higher order system is desired with the second order loop prototype.

STEP4: Robustness properties

With the given first order prototype based design there is no theoretical limit to the number of loops that can be implemented in the MECC(N) structure. In practice however, there will be restrictions on the number of loops in the local enhanced cascade arising from uncertainty on K_P and t_p. Due to the local feedback source, only perturbations on these parameters within the fundamental PMA are of concern. The important effects of K_P and t_p uncertainty are investigated by considering the following set of perturbed loop transfer functions:

$$L_{N,p}(r_K,t_p) = r_K K_{PN} A \sum_{j=0}^{N-1}\left[\prod_{i=1}^{N-j} B_{i,p}\right] e^{-t_p s} \qquad (7.22)$$

$$= r_K e^{-t_p s} L_N$$

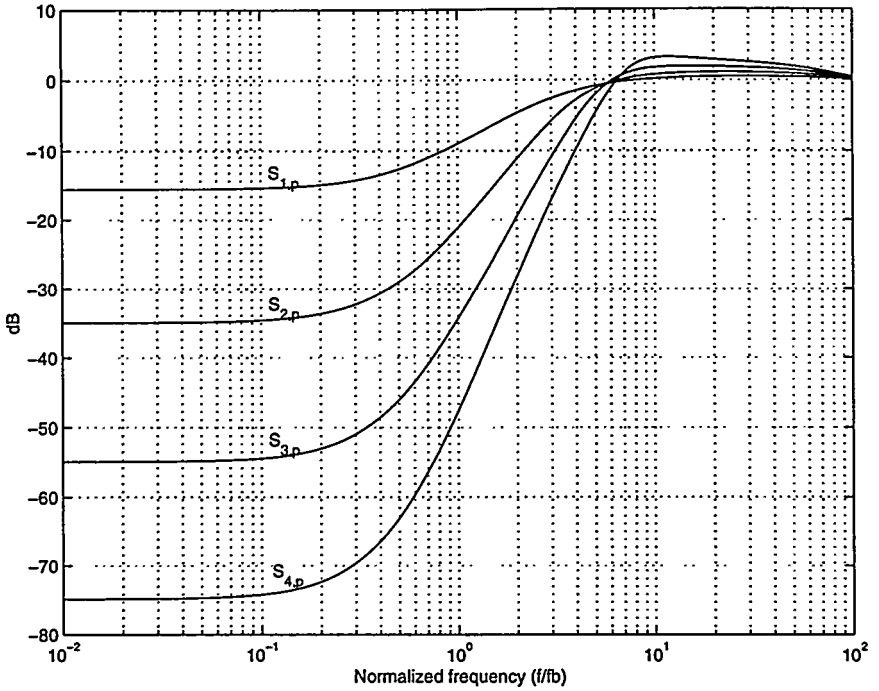


Fig. 7.9 Perturbed sensitivity functions $S_{N,p}(0.5,200ns)$ for the MECC(N) case example.

The isolation of the uncertain parameters from the sum in (7.22) makes the effects of perturbations easy to predict. This *visibility* of both types of perturbations should be credited to the regular expandable MECC(N) structure. Generally, it is difficult to directly predict the effects of perturbations in multi-loop systems. A parametric investigation of the robustness of the specific case is shown by the effective sensitivity is shown in Fig. 7.9. Only the worst-case plant is considered where $r_K = 0.5$ and $t_p = 200ns$. $\|S_{N,p}\|_\infty$ is determined in the four cases from Fig. 7.9:

N	1	2	3	4
$\|S_{N,p}\|_\infty$	1.05	1.13	1.24	1.44

Clearly, the topology is remarkable stable toward any perturbation within the *US*. *RS* and *RP* are satisfied. Specifically, it is worth noticing that the stability properties are nearly insensitive towards perturbations on K_P. Only performance is compromised in the *first* loop as shown in Fig. 7.9. This is a very pleasant characteristic of a higher order control system as MECC(N). Uncertainty on any parameter within the filter (e.g. on Q_o) will have the same influence on system performance as for the VFC2 system. Stability and robustness are not affected, but the frequency response of the total system is compromised since the filter is not controlled.

The parametric uncertainty within the compensator blocks is a concern in higher order control systems. The most important type is uncertainty on the compensator zeros which can be expressed as:

$$B_{i,p}(s) = \frac{\tau_{i1}}{\tau_{uN}} \frac{\alpha\tau_{uN}s+1}{\tau_{i1}s+1} \qquad \alpha_{\min} \le \alpha \le \alpha_{\min} \tag{7.23}$$

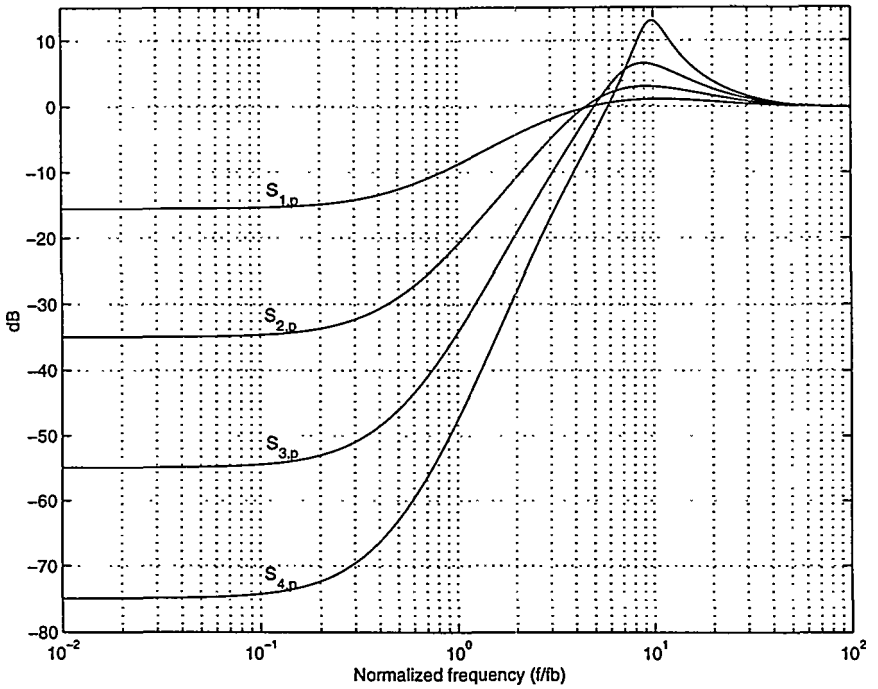


Fig. 7.10 Robustness investigations of MECC(N) with the proposed second order loop prototype.

The compensator poles will affect the target band performance but only marginally influence the stability characteristics that are determined by the characteristics well beyond the target frequency band. Investigations have shown that even 10% tolerance on the compensator zeros will only marginally influence stability and performance. To conclude, the MECC(N) system is a very robust higher order control system.

The robustness of MECC(N) based on the second order loop prototype is investigated in Fig. 7.10 by the perturbed sensitivity functions corresponding to the worst case parameter set within the Uncertainty Set. The following maximal peaks are determined:

N	1	2	3	4
$\|S_{N,p}\|_\infty$	1.13	1.42	2.12	4.47

Robust performance requires $N < 4$ in this worst case situation. The second order design approach is as such a viable alternative to the first order loop prototype.

STEP5: Non-linear simulation

The case example is simulated with the non-linear 200W power stage, that has been used throughout the investigations in Chapter 6. The investigations will focus on a illustrative triple loop case example, with sufficient compensation effect to honor even the most demanding investigations with a $S_M \approx -40$dB. The noisy NADD modulation method is chosen to illustrate the influence of carrier components on the controller signals. The carrier frequency selection is again based on SRI considerations. With $f_c = 500KHz$, the first order prototype design will potentially unstable due to SRI since $|L_3(j\omega_c)| \approx -6dB$ (see Fig. 7.5), whereas the second order loop prototype will have a sufficient margin to SRI since $|L_3(j\omega_c)| \approx -9dB$. The parameters for the non-linear investigation of MECC(3) are summarized below:

Parameter	Value
V_S	50V
V_T	2.5V
f_b	20KHz
f_c	500KHz
N	3
S_M	-40dB
$\|S_{N,p}\|_\infty$	2.12

Fig. 7.11 and Fig. 7.12 shows a functional simulation of the MECC(3) based PMAs with both first and second order loop prototypes. The system operates as desired with the specified gain with both prototypes. The compensator signals v_{b1}, v_{b2} and v_{b3} are *balanced* as determined in (7.17) and (7.18), and the simulation thus verifies this pleasant characteristic of MECC(N). The significant residual from the power stage superposed on v_{b1} is as predicted. The system is clearly on the edge of Slew Rate Instability, and the system is potentially unreliable since e.g. gain perturbation will lead to SRI. With the second order loop prototype, the HF content on all controller signals are reduced significantly as shown in the simulation in Fig. 7.12. The simulation documents the general advantages of the second order loop prototype.

Correction of General Non-linearity

The general correction effect offered by the MECC(N) system is investigated with non-linear model of the power stage in the form:

$$v_P(M) = K_{PN}(1 + c_1 M + c_2 M^2 + c_3 M^3) v_{b1} \tag{7.24}$$

This model has no direct relation with the actual non-linear PMA power stage, but exclusively serves to provide simple means form a *parametric* investigation of the error correction performed by the MECC(N) systems. Fig. 7.13 clearly verifies the successive improvement in performance with *N*. With quadruple loop control system applied to the non-linear model the improvement is 57dB or a reduction from 3.3% open loop THD to only 0.0044% THD with MECC(4). This verifies the successive correction effect of the multiple-loop system. Fig. 7.14 shows the compensator signals at M=0.9 for MECC(4). All controller outputs have the same magnitude as expected from (7.17) and (7.18).

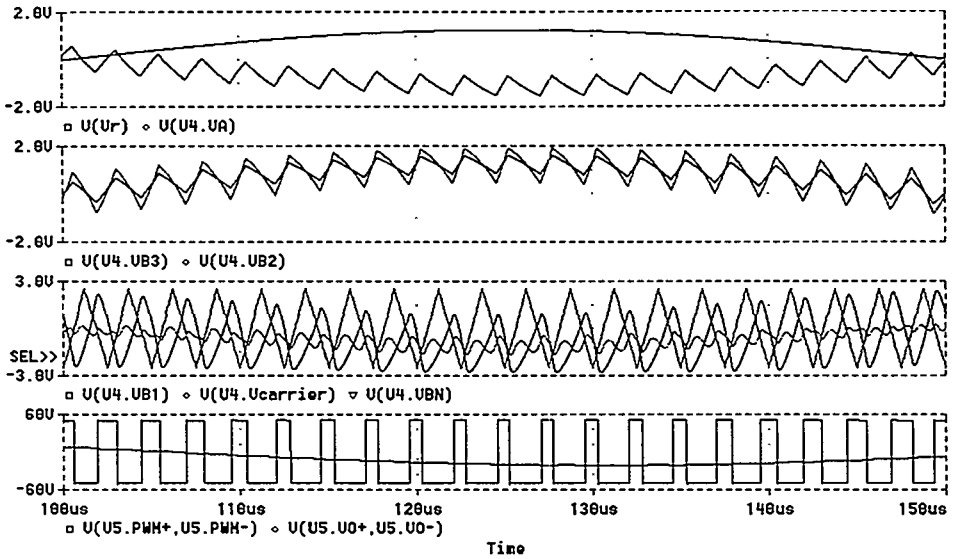


Fig. 7.11 Functional simulation of MECC(3) based on *first order loop prototype*. With $f_c = 500KHz$ the system operates on the edge of SRI. Top - Reference v_r and feedback v_a, Upper Mid - Forward compensator signals v_{b3} and v_{b2}, Lower mid – carrier and compensated output v_{b1} that is input to the modulator. The modulator input is also shown with the fundamental carrier removed by a tuned circuit. Bottom - power outputs v_p and v_o.

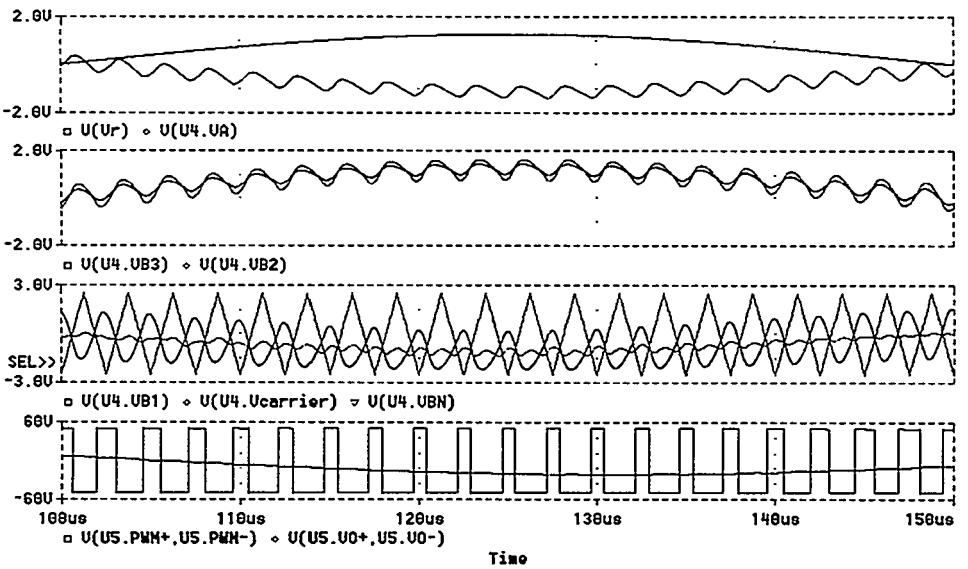


Fig. 7.12 Functional simulation of MECC(3) PMA system based on *2nd order loop prototype*. Top - Reference v_r and feedback v_a, Upper Mid - Forward compensator signals v_{b3} and v_{b2}, Lower mid – carrier and compensated output v_{b1} driving the modulator. Bottom - power outputs v_p and v_o.

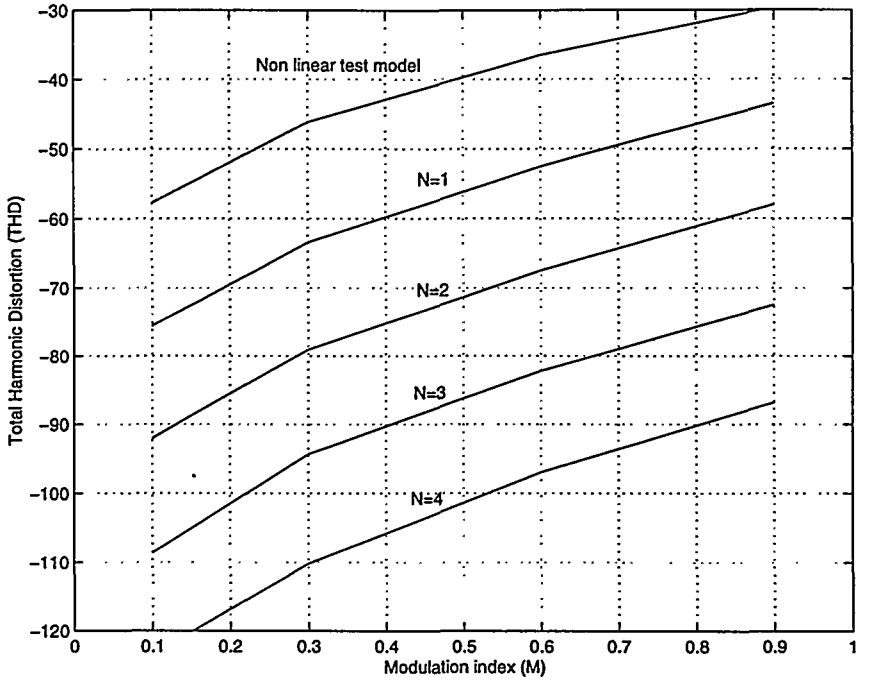


Fig. 7.13 THD vs. M with MECC(N) applied the non-linear plant. The signal frequency is 5KHz.

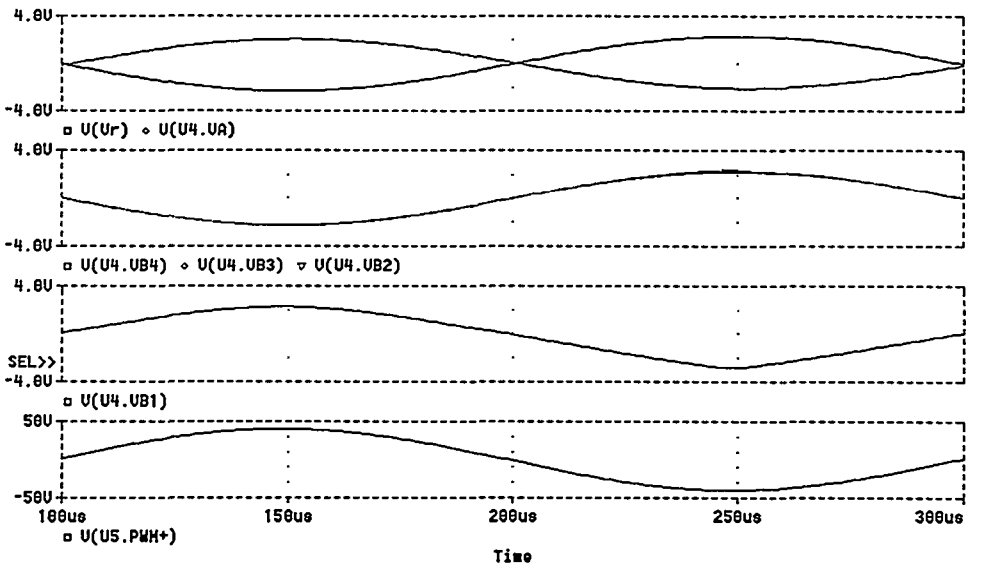


Fig. 7.14 THD vs. M with MECC(N) applied the non-linear plant. The signal frequency is 5KHz and M=0.9. Top - Reference v_r and feedback v_a, Upper Mid - Forward compensator signals v_{b4}, v_{b3} and v_{b2} (nearly identical), Lower mid – carrier and compensated output v_{b1} driving the modulator, Bottom - power outputs v_p and v_o. Note, that all control signals have equal magnitudes.

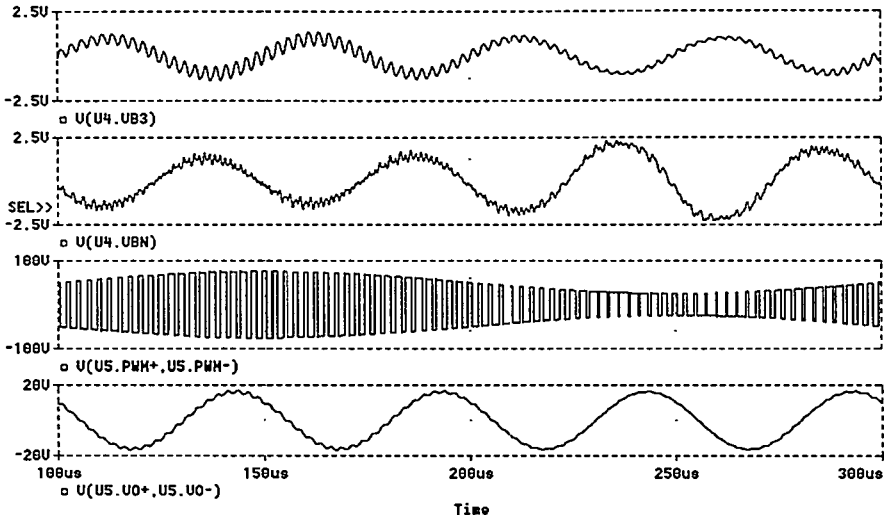


Fig. 7.15 Simulation of PAE error correction with MECC(3) system. Top – B_3 compensator output v_{b3}, Upper mid – B_1 compensator output v_{b1} with the carrier fundamental notched out. Lower mid and bottom shows the power stage outputs. The IM-distortion is effectively eliminated by a PSRR of 40dB at 20KHz.

PTE and PAE Correction

A simulation of PTE effects with a 5KHz signal frequency will verify a reduction in THD of about 40dB with the triple loop MECC(N) based controller, as theory would predict ($S_M \approx -40dB$). In terms of PAE error correction, the triple system has been simulated with a significant 50Vpp/5KHz perturbation superposed on V_S as show in Fig. 7.15. The intermodulation distortion is essentially eliminated by a PSRR of 40dB at 20KHz.

7.2 MECC(N,M)

The focus now turns to the extended topology with N local and M global loop formed in two linked enhanced cascades. The topology is founded on a MECC(N) design and should be seen as a direct extension of this topology. The MECC(N,M) topology is characterized by:

- A MECC(N) system, that is optimized specifically for the global enhanced cascade.
- A *single* feedback source v_o.
- A *single* feedback path compensator C.
- An D_1 compensator to initialize the cascade.
- A *recursive* structure with a set of preferably *identical* compensator blocks D_i.

The topological resemblance between MECC(N) and MECC(N,M) also leads to similarities in the synthesis of the to cascade structures. However, MECC(N,M) is constituted of two closely connected enhanced cascades, where the global enhanced cascade relies on the compensation from the local cascade. The following section will address all aspects MECC(N,M) design.

7.2.1 Loop prototype based MECC(N,M) synthesis

The control plant for the global enhance cascade is the MECC(N) controlled system $H_N(s)$ in series with the demodulation filter $F(s)$, which is assumed to be a standard second order characteristic:

$$H_N(s) \cong K\frac{\tau_1 s+1}{\tau_{uN} s+1} \tag{7.25}$$

$$F(s)=\frac{\omega_o^2}{s^2+\frac{\omega_o}{Q_{oN}}s+\omega_o^2} \tag{7.26}$$

MECC(N,M) synthesis will be based on the specification of a unique loop prototype consistent with the approach for MECC(N) synthesis. A desirable loop prototype is again a leaky integrator characteristic:

$$L(s)=\frac{\tau_{i2}}{\tau_{uM}}\frac{1}{\tau_{i2}s+1} \tag{7.27}$$

Clearly, the unity gain frequency (bandwidth) of the loop prototype is determined by τ_{uM}. The requirement for a system gain K locks the compensator characteristic of the feedback path:

$$C(s)=\frac{1}{K} \tag{7.28}$$

No specific filtering is needed in C since the feedback source is demodulated. A connection between the local system and the global system is established by the following parameter assignments:

$$\tau_1 = \frac{1}{\omega_0} \quad \text{and} \quad f_{uN} > f_{uM} \tag{7.29}$$

This specific parameter assignment causes $H_N(s)F(s)$ to have a first order characteristic within the bandwidth of the of the local loop prototype for MECC(N). The initial compensator D_1 that will realize the global loop prototype can now be specified:

$$D_1(s) = \frac{\tau_{i2}}{\tau_{uM}} \frac{\tau_1 s + 1}{\tau_{i2} s + 1} \tag{7.30}$$

Assuming that $f_{uN} >> f_{uM}$, the general MECC(N,M) system response will be:

$$H_{N,M}(s) \approx K \frac{1}{\tau_{uM} s + 1} \tag{7.31}$$

$H_{N,M}$ should be considered as a closed loop prototype that is synthesized independent of M. This is axiomatic with a unique loop prototype and a unique feedback path. The general D_i - compensator that will realize the loop prototype in any succeeding loops is:

$$D_i(s) = \frac{\tau_{i2}}{\tau_{uM}} \frac{\tau_{uM} s + 1}{\tau_{i2} s + 1} \tag{7.32}$$

7.2.2 MECC(N,M) properties

Since the structure of both the local and global enhanced cascade is the same, many of the pleasant properties for MECC(N) can be generalized to MECC(N,M) directly. Fig. 7.2 yields the following relation:

$$v_o = H_N F D_1 (D_2 (D_3 (\cdots D_M (v_r - C v_o) \cdots - C v_o) - C v_o) - C v_o) \tag{7.33}$$

Or equivalently:

$$H_{N,M} = \frac{H_N F \prod_{i=1}^{M} D_i}{1 + H_N C F \sum_{j=0}^{M-1} \left[\prod_{i=1}^{M-j} D_i \right]} \tag{7.34}$$

The (N,M)-subscript in $H_{N,M}$ refers to that the M-loop MECC(N,M) design is based on the general N-loop MECC(N) system. The effective loop transfer function $L_{N,M}$ for the MECC(N,M) system is defined as:

$$L_{N,M} = H_N C F \sum_{j=0}^{M-1} \left[\prod_{i=1}^{M-j} D_i \right] \tag{7.35}$$

And the effective sensitivity function $S_{N,M}$ for MECC(N,M) equivalently:

$$S_{N,M} = \frac{1}{1 + H_N C \sum_{j=0}^{M-1} \left[\prod_{i=1}^{M-j} D_i \right]} \tag{7.36}$$

Within the target frequency band $S_{N,M}$ can be approximated by:

$$S_{N,M} \approx \frac{1}{1 + H_N C \prod_{i=1}^{M} D_i} \quad \forall \omega \text{ within target frequency band} \tag{7.37}$$

Looking at the resulting sensitivity function that specifies the reduced sensitivity to any errors within the fundamental elements of the PMA it is straightforward to show that the resulting sensitivity function is simply $S = S_N \cdot S_{N,M}$.

7.2.3 MECC(N,M) loop shaping

Table 7.3 proposes a set of parameters for generalized MECC(N,M) loop shaping. Again, is has been attempted to minimize the degrees of freedom without compromising performance. The free parameters with the general parameter assignment in Table 7.3 are N, M and the bandwidths of the local global prototypes f_{uN} and f_{uM}. It should be emphasized that the MECC(N) should be optimized specifically towards the application of the global enhanced cascade. The local system should be optimized to provide best possible compensation, i.e. the bandwidth of the local system should be as high as possible. Reaching desired performance goals can carried by adjusting N and M. Only one local loop is necessary to provide the compensation. A feasible approach is to implement a MECC(1) system with sufficient compensation effect, and following adjust M to the

Parameter	Value	Comment
f_{uN}	≥ 8	MECC(N) parameter
$f_{i1} = \frac{1}{2\pi\tau_{i1}}$	f_o	MECC(N) parameter
f_{uM}	$\leq \frac{f_{uN}}{2}$	MECC(M,N) bandwidth defined
$f_1 = \frac{1}{2\pi\tau_1}$	f_o	Connection between local and global enhanced cascade.
$f_{i2} = \frac{1}{2\pi\tau_{i2}}$	$\frac{f_{uM}}{10}$	MECC(N,M) loop prototype parameter.
f_o	1	Demodulation filter natural frequency
Q_o	$\frac{1}{\sqrt{3}}$	Demodulation filter Q (Bessel)
f_r	3	Reference filter natural frequency
Q_r	$\frac{1}{\sqrt{3}}$	Reference filter Q (Bessel).

Table 7.3 Proposed MECC(N,M) parameter assignments.

desired performance. It should be emphasized, that the global enhanced cascade is independent upon N, since MECC(N) synthesizes a unique closed loop prototype as shown previously. The tradeoffs in MECC(N,M) design will become clearer throughout the more detailed investigation an illustrative case example.

7.2.4 MECC(N,M) case example

In the following, the characteristic of MECC(N,M) will be illustrated in detail with a case example.

STEP 1: Specification

The basic parameters are as for the MECC(N) case example. Performance requirements are only set for $\|S_{N,M}\|_\infty$, which should obey the general specifications in the nominal and perturbed case, as they were defined in Chapter 6. In terms of performance within the target band, a parametric analysis is carried out instead of designing towards a specific S_M specification. The prototype bandwidths of the specific case are set to:

$$f_{uN} = 10 \text{ and } f_{uM} = 4$$

These specifications obey the specified relationship in Table 7.3. M will be considered a variable parameter. N does not influence the global enhanced cascade and is set arbitrarily to 1.

STEP 2: Synthesis

With all fundamental parameters now determined, the MECC(N,M) controller synthesis is straightforward from the general parameter assignments in Table 7.3.

STEP 3: Verification

First consider the limiting case $f_{uN} \to \infty$. In this limiting case the global enhanced cascade realizes a higher order system with excellent stability, i.e.

$$\|S_{N,M}\|_\infty < 1 \quad \forall \omega, M \tag{7.38}$$

However, the bandwidth of the local MECC(N) system is inherently limited at $f_{uN} = 10$, and $S_{N,M}$ for the synthesized MECC(N,M) controller is shown in Fig. 7.16. The following is found by investigating $\|S_{N,M}\|_\infty$:

M	1	2	3	4
$\|S_{N,M}\|_\infty$	1.20	1.5	2.21	3.57

The system converges towards instability as the number of loops increase. *NS* is always guaranteed, however *NP* requires that $M \leq 2$.

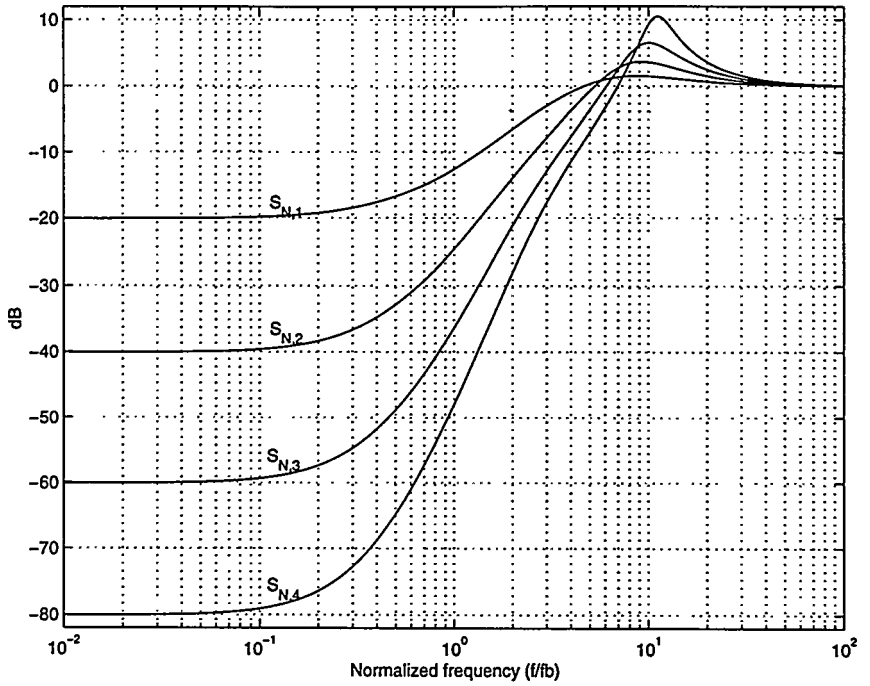


Fig. 7.16 $S_{N,M}$ for synthesized MECC(N,M) system $M = 1,2,3,4$.

Fig. 7.17 shows Bode-plots of all components of the MECC(N,M) system and Fig. 7.18 shows the system transfer function $H_{N,M}$ for $M = (1,2,3,4)$. Clearly, MECC(N,M) provides a much improved frequency response with the given parameters. Especially, the resulting response is excellent with both $M = 1$ and $M = 2$. The demodulation filter natural frequency is unity ($f_o = 1$), so the excellent frequency response characteristics do not compromise demodulation. The performance problems with $M \geq 2$ are also pronounced on the closed loop frequency response. Table 7.4 summarizes the essential results for the parametric results of the synthesized MECC(N,M) case example.

Specification	Value	Comments
System gain	*25.1 dB*	20dB feedback.
Bandwidth	2.5	Determined by R(s).
Frequency response	$\pm 0.01dB$	Nominal load. $M = 1$.
Frequency response	$\pm 0.3dB$	Nominal load. $M \leq 4$.
Phase response	$\pm 15^0$	Nominal load. $M \leq 4$
S_M	$-12 \cdot M$ *dB*	Maximal effective sensitivity within bandwidth of interest

Table 7.4 Stability and performance specifications for the synthesized MECC (N,M) system.

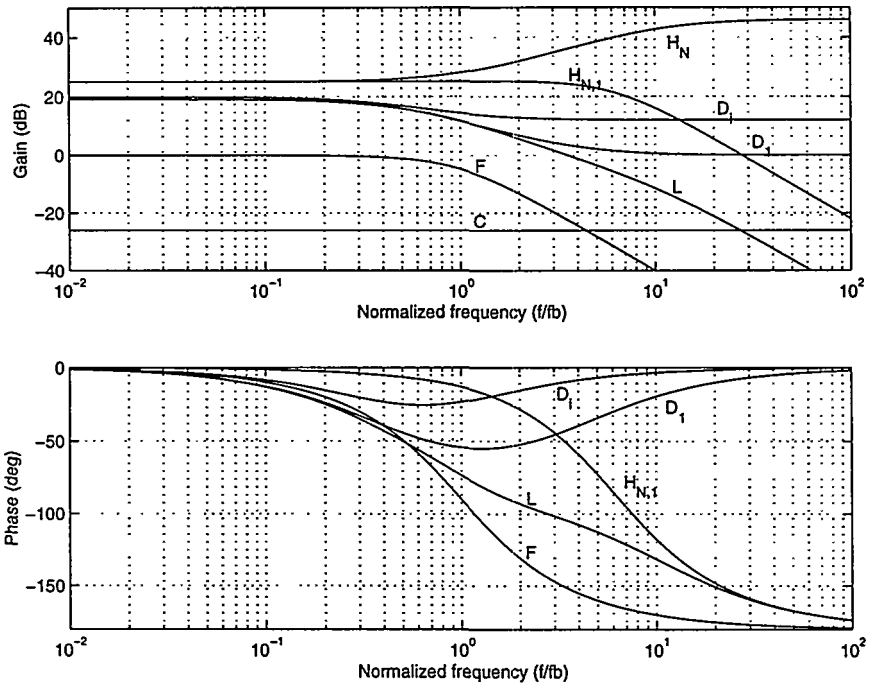


Fig. 7.17 Components of the MECC(N,M) system.

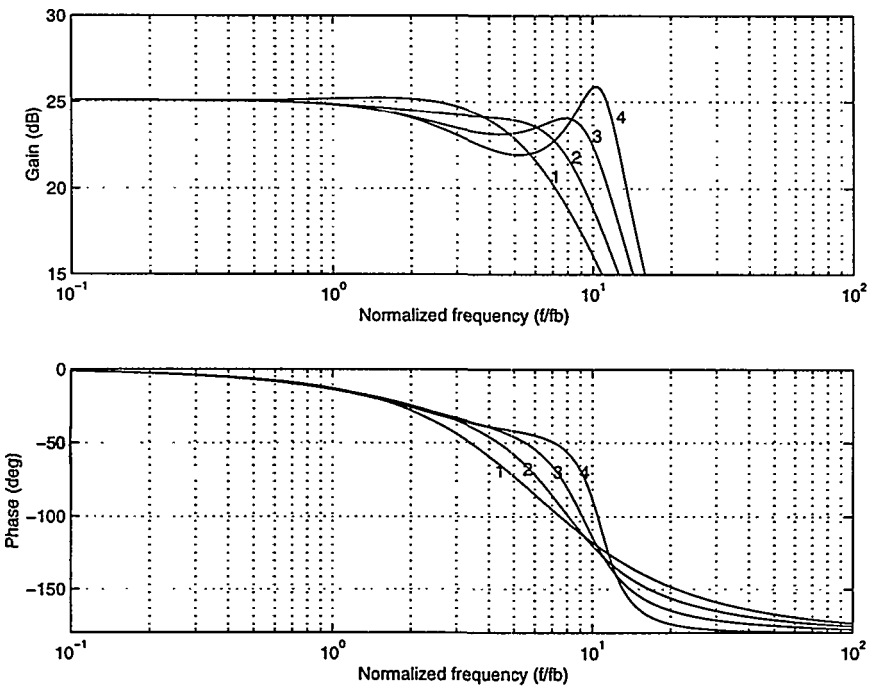


Fig. 7.18 Resulting system transfer function $H_{N,M}$, $M = 1,2,3,4$.

STEP4: MECC(N,M) Robustness properties

Recall from above, that MECC(N) proved very robust towards uncertainty on K_P and t_p. However, uncertainty on Q_0 will influence the MECC(N) frequency response notably, since the filter is not controlled. It is a more involved process to analyze the robustness properties for the general (N+M) loop MECC(N,M) topology. The perturbed loop transfer functions for the MECC(N,M) system can be written as:

$$L_{N,M,p}(r_K,r_Q,t_p) = H_{N,p}(r_K,r_Q,t_p)\cdot C\cdot F_p \sum_{j=0}^{M-1}\left[\prod_{i=1}^{M-j} D_i\right] \tag{7.39}$$

Where $H_{N,p}$ and F_p represents the perturbed version of the system response for MECC(N) and the demodulation filter, respectively. MECC(N,M) requires $f_{uM} << f_{uN}$ to implement the loop prototype in each loop. If this is not obeyed the stability and performance characteristics will be compromised, since the compensation provided by MECC(N) is only partial. Hence, it follows directly that MECC(N,M) is sensitive to uncertainty on K_P, since a reduced gain directly influences the *bandwidth* of the MECC(N) system. Fig. 7.19 shows a parametric investigation of the worst case perturbation within the Uncertainty Set, i.e. $S_{N,M,p}(0.5,4,200ns)$. The following peaks are found:

M	1	2	3	4
$\|S_{N,M,p}\|_\infty$	1.66	4.5	12.2	(unstab.)

Consequently, RS requires $M<4$ and RP requires $M=1$.

The effects of Q_o uncertainty are significantly different from MECC(N) since the filter is enclosed by the global enhanced cascade, with all the positive effects that follows. Fig. 7.20 shows the perturbed closed loop transfer function $H_{N,M,p}(1,4,0)$. Clearly, MECC(N,M) provides a much improved insensitivity to load variations. It can be concluded, that the system effectively suppresses the effects of filter uncertainty within the PMA bandwidth. The perturbed sensitivity function $S_{N,M,p}(1,4,0)$ corresponding to a worst-case perturbation on Q_o has the following maximal peaks:

M	1	2	3	4
$\|S_{N,M,p}\|_\infty$	1.29	1.81	2.83	5.40

RS always hold whereas RP requires $M<4$.

To conclude on the robustness investigations for MECC(N,M), the topology is specifically sensitive to large scale uncertainty on K_P due to the proportional relationship between the power stage gain and MECC(N) bandwidth. In the worst case-situation, only M=1 will satisfy both *RS* and *RP*. The robustness can be improved by a higher local bandwidth (f_{uN}) or alternatively a lower global bandwidth (f_{uM}). Perturbations on Q_o seen isolated are effective suppressed.

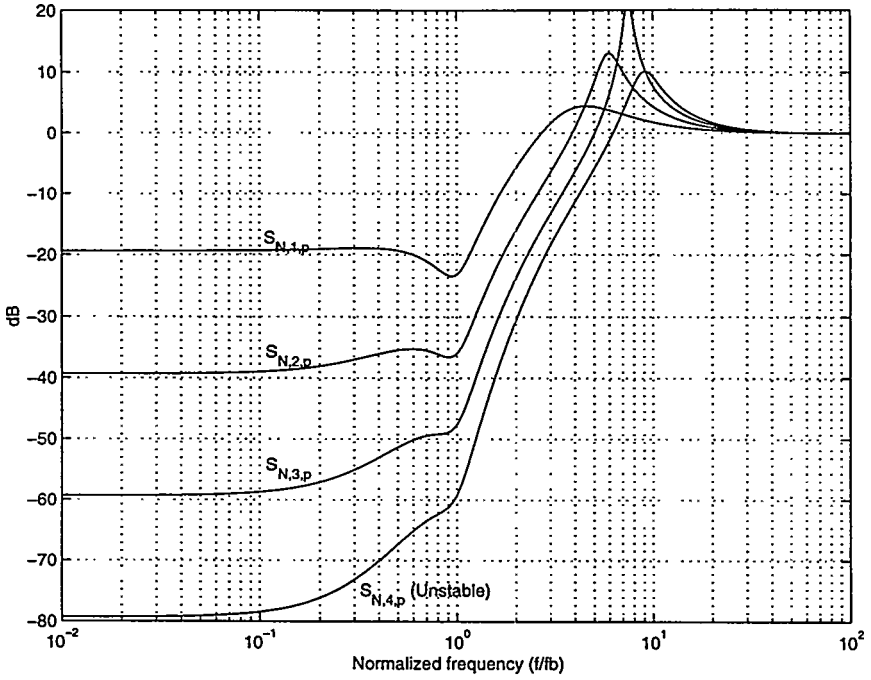


Fig. 7.19 Effective sensitivity function $S_{N,M,p}$ with $(M = 1,2,3,4)$.

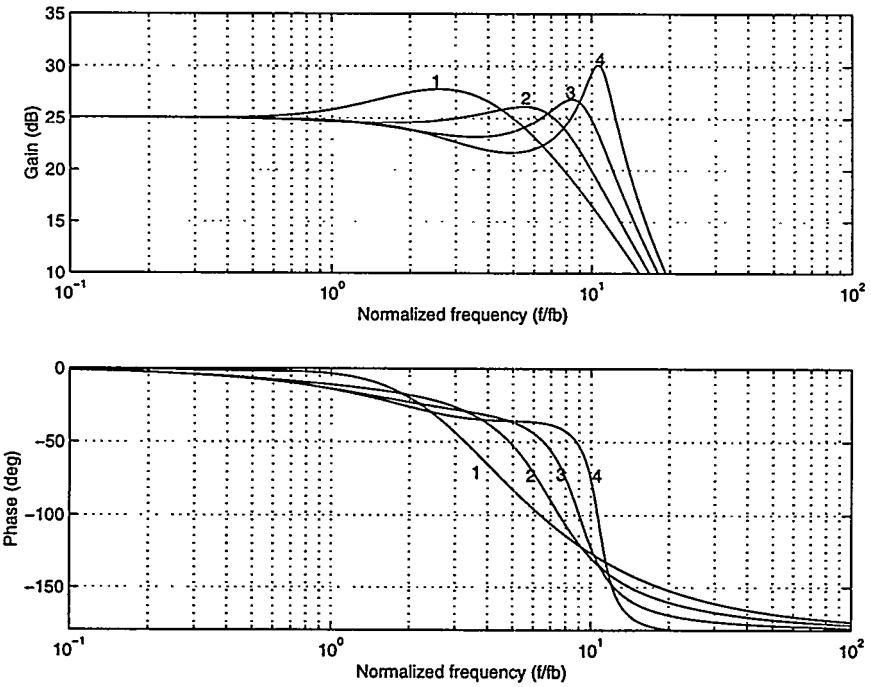


Fig. 7.20 System response $H_{N,M,p}$ with $r_Q = 4$ (worst-case). $(M = 1,2,3,4)$.

STEP 5: MECC(N,M) - Nonlinear simulation

A triple loop case example (N,M)=(1,2) has been investigated on the non-linear PMA system, to investigate the properties for MECC(N,M) at low level. We derive for S_M :

$$S_M = S_1 \cdot S_{1,2} \approx -44dB$$

The parameters are as for the MECC(N) non-linear simulation and the local system has been implemented using the second order loop prototype to prevent Slew Rate Instability in the local feedback system. Fig. 7.21 shows a functional verification of the triple loop MECC(1,2) system. Note the pleasant signal levels on all compensator outputs (similar magnitude) – this is a general characteristic of both MECC(N) and MECC(N,M). It is also noted that the D_i compensator outputs are effective demodulated with a minimal amount of switching noise superposing the variables.

The MECC(1,2) topology has been subjected to the same tests in terms of correction effect towards different types of error sources, and the topology shows a correction capability that is comparable to the MECC(3) topology with the given parameters. This was to expect since the two systems have similar S_M, a since the fundamental concept of successive correction by the enhanced cascade has already been verified in the MECC(3) non-linear simulation.

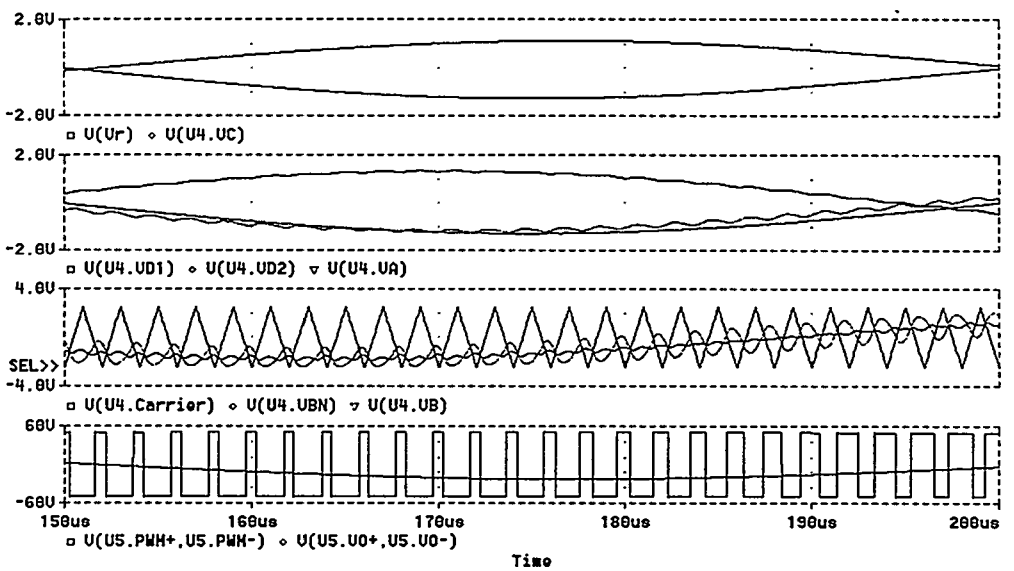


Fig. 7.21 Functional simulation of triple loop MECC(1,2) system. Top - Reference v_r and global feedback compensator (C) output v_c. Upper mid - Forward compensator (D_1, D_2) signals v_{d1}, v_{d2} and the local feedback compensator (A) output v_a. Lower mid – carrier and B_1 compensator output v_{b1}. Bottom – power stage output signals v_p and v_o.

7.3 Summary

The chapter has introduced an optimized control method – Multivariable Enhanced Cascade Control - that is dedicated to solve the problems within analog PMA systems. Two variants were introduced MECC(N) and MECC(N,M). Generally, MECC realizes a practical higher order system by an enhanced cascade structure, comprising a unique feedback path and a recursive structure of preferably identical forward paths compensators.

The concept of loop prototype based design was introduced to minimize the degrees of freedom within the higher order control structure. Loop prototypes were presented, and the general properties of MECC was investigated. General loop prototype based loop shaping was following addressed. The functionality of both MECC(N) and MECC(N,M) approaches has been verified by synthesizing and evaluating illustrative case examples.

Fundamentally, MECC offers a practical and robust method for higher order control system implementation with MECC(N) for dedicated applications and MECC(N,M) for general applications. MECC(N) has shown to provide several pleasant properties:

- Powerful and flexible control of the power stage is realized, with successive improvements for every loop added.
- Pleasing signal levels throughout the control structure. This provides immunity to e.g. switching noise from the power stage and other noise sources.
- Simplicity. The single feedback path minimizes complexity. Furthermore, the performance requirements of the individual compensator blocks are low.
- Excellent robustness to any perturbation within the *US*.
- Effective compensation of the demodulation filter, thus preparing the system for a global enhanced cascade.

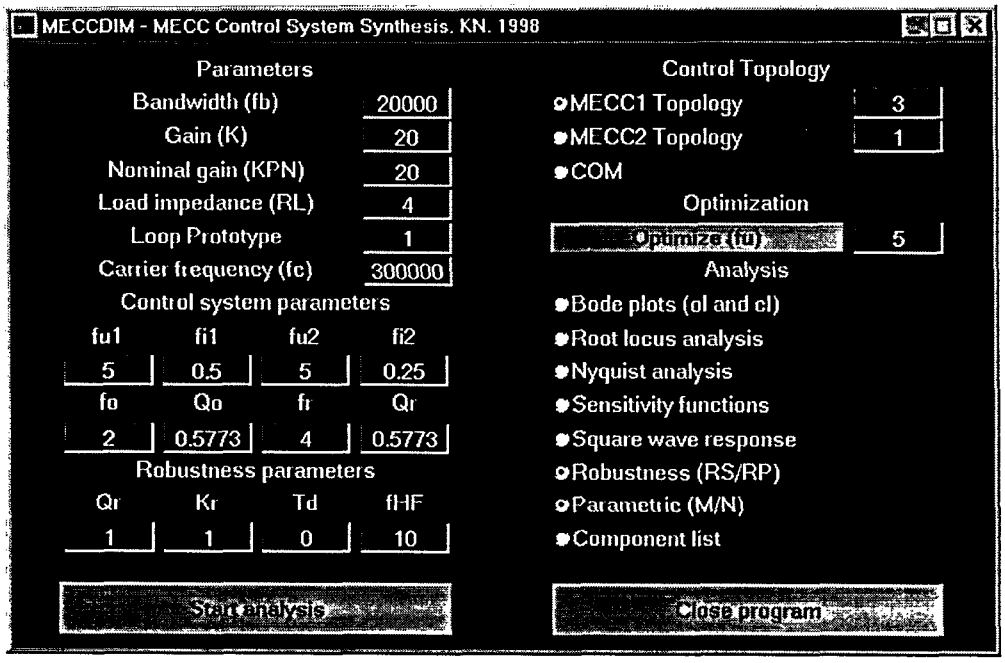
MECC(N,M) encloses the PMA by two closely connected enhanced cascades. The additional properties of the MECC(N,M) are:

- Improved frequency response, insensitive to variable loading etc. Phase and amplitude response of the amplifier is much less dependent on the output filter.
- Error correction of filter errors, lowering the requirements for filter inductor linearity etc.

Although the chapter has been devoted to a generalized analysis, it should be emphasized that simple configurations as MECC(1,1), MECC(1,2) or MECC(1,2) can provide sufficient performance for even very non-linear and noisy plants. The pleasant combination of features combined with the simple realization, makes MECC the most powerful and flexible control method existing for general analog PMA systems.

7.3.1 MECCDIM – A GUI controlled toolbox for MATLAB

A GUI controlled MATLAB toolbox for systematic and automated design of MECC based PMAs has been developed. The graphical user interface is shown below.



The toolbox provides automated design by simple push button access. Based on the primary amplifier input parameter specifications the interface gives access to:

- Optimal control system synthesis and verifications
- Parametric analysis (vs. M and N).
- Robustness investigations.
- Controller component synthesis for low-level non-linear simulation.
- Manual access to individual parameters for fine-tuning of performance to e.g. a specific applications.

The program has been used extensively throughout the present chapter.

Part III

Chapter 8

Non-linear Control

The control methods investigated so far have all been based on linear feedback control. Recently, non-linear control techniques related to One Cycle Control [Sm95] have been investigated for PMAs in several publications [La96b], [Sm97], [Ta97], [Ni98a]. The results indicate that there are some complications in making non-linear control realize the desired control objectives. However, the basic principles have an indisputable appeal from a theoretic point of view. Subsequently, the topic for the following will be an analysis of non-linear control techniques, and it will be investigated if various improvements could make non-linear control a viable alternative to the linear control methods. After a short introduction to the principles of One Cycle Control and the perspectives and motivating factors for the application of non-linear control to PMAs, the investigations will focus on an extended non-linear control configuration - Three-level One Cycle Control (TOCC). The method [Ta97], [Ni98a] has certain advantages over previously proposed nonlinear methods in PMA applications.

There are many non-linear elements within the PMA as shown in Chapters 3 and 4. PWM is inherently a non-linear process, power supply perturbation multiply with the modulating signal, there are several non-linear saturation/limitation characteristics etc. Subsequently, all control systems for PMAs may all be considered as non-linear control systems, i.e. control systems that operate on a non-linear plant. The distinction between the previously investigated systems and true non-linear controlled system lies in the characteristics of controller itself. Non-linear control systems are characterized by non-linear elements within the actual controller. Non-linear control excels by several potential advantages over

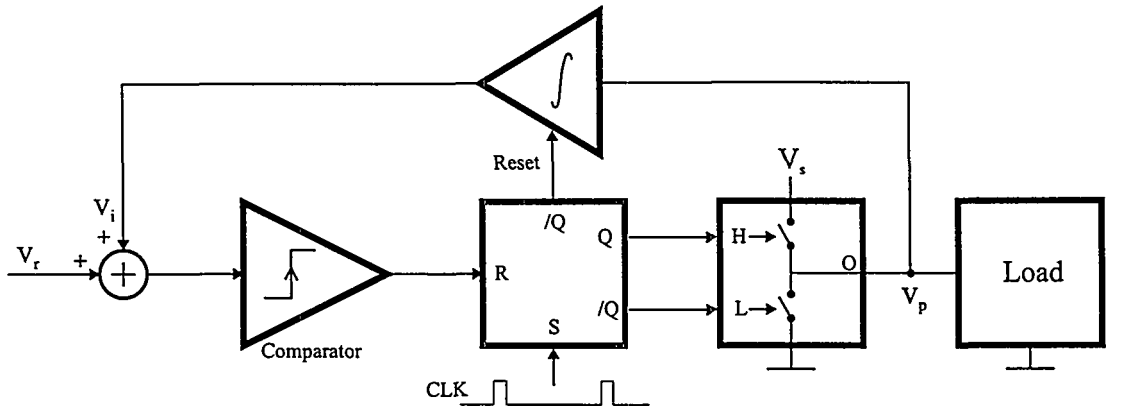


Fig. 8.1 Switching OCC power amplifier topology using single switching leg.

linear control, as unlimited correction corresponding to a sensitivity function of zero. Furthermore, the bandwidth constraints of linear control systems are not necessarily present with non-linear control. Clearly, non-linear control methods are only a viable alternative provided that there are practical implementation strategies. It will become apparent, that non-linear controller synthesis, analysis and verification are significantly different from the analysis methodology used for linear control systems.

8.1 Non-linear One Cycle Control

Fig. 8.1 shows a simple implementation of OCC in a fundamental DC-DC converter application. The controller is simple, consisting of an integrator with reset, a comparator, a flip-flop element and an oscillating clock that determines the carrier frequency. The control scheme involves four fundamental actions that are repeated in every cycle is illustrated in Fig. 8.2:

1. The switching power stage is turned ON by a constant frequency clock with period t_c. This forms the beginning of a switching period.
2. The switched variable v_p is integrated and compared with a reference voltage.
3. When the integrated output v_i reaches the reference voltage v_r at time t_{on}, the comparator output changes state.
4. The comparator state change resets the flip-flop which following turns the switch OFF.

This sequence of actions causes the average value of the switched variable v_p within each switching interval to be proportional to the reference input v_r. If the clock frequency (the carrier frequency) is considerably higher than the bandwidth of the reference v_r, the average of the switched variable, $\tilde{v}_p$, will be determined by the duty cycle $d = t_{on}/t_c$ as:

$$\tilde{v}_p = v_s d \tag{8.1}$$

The integrator output where $v_i = v_r$ is found by simple integration:

$$v_i = v_r = \int_o^{d \cdot t_c} \frac{1}{RC} v_s dt = \frac{t_c v_s d}{RC} = \tilde{v}_p \frac{t_c}{RC} \tag{8.2}$$

Consequently, the relation between the reference input v_r and the average of the switched output $\tilde{v}_p$ is a constant gain:

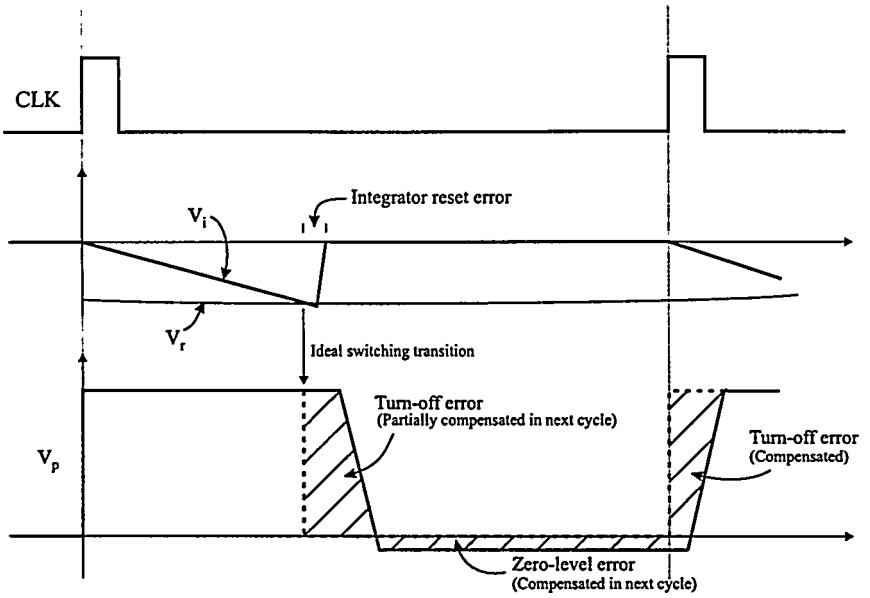


Fig. 8.2 OCC Non-linear control technique

$$K_{OCC} = \frac{\tilde{v}_p}{v_r} = \frac{RC}{t_c} \tag{8.3}$$

The closed loop gain is therefore determined alone by the switching frequency and the integrator time constant. In theory, this control method yields an infinitely fast transient response to steps on e.g. the power rail v_s or the reference input v_r. The equivalent bandwidth of the OCC based system may consequently be considered infinite. Furthermore, the integration does not stop until the output is a constant times the input, i.e. one should intuitively expect a complete elimination of all power stage error sources. This is in perfect harmony with the fundamental control objective, as specified in Chapter 6.

For PMAs (or DC-AC conversion) specifically, another interesting property is that the controller and modulator are in effect combined. The basic system does not involve a discrete modulator, although a clock signal is still required. The troubles of making a carrier generator (or multiples in the case of MICPWM) are saved. The basic topology synthesizes single sided PWM (LADS) in DC-AC applications. The system may as such be considered a modulator that is very robust towards errors, or a modulator with inherent control.

8.1.1 Fundamental limitations

Notwithstanding the appealing characteristics of OCC, there are a range of problems and inherent limitations connected with it practical realization the results presented in PMA applications have been of modest quality. The sources of these problems are discussed in the following, based on the simple two transistor converter in Fig. 8.1.

Propagation delays and finite switching times

An inaccuracy occurs as a consequence of the turn-off characteristic of the power switch, which is delayed and does not happen infinitely fast (see Chapter 4). The turn-off is constituted of the comparator propagation delay, flip-flop propagation delay and the delay from turn-off to the power switch turn-off transition actually happens. These inherent propagation delays combined with finite turn-off time of the switch causes suboptimal

modulator/controller operation as indicated in Fig. 8.2. Fortunately, most of the turn-off "area" and zero-level "area" are compensated in the next cycle and OCC is in reality *two-cycle* control.

Reset complications
The implementation of a reset switch is impossible without a reset delay. The switch that performs the reset has to be implemented as a difficult trade-off between speed and switch impedance. A low reset switch impedance is required for a fast integrator reset. On the other hand, a high integrator switch speed is desirable. The finite reset-time leads to a small interval with no feedback in every cycle.

Limited PSRR
It can be shown that perturbations on v_s are only partially compensated by One Cycle Control [Ta97]. The general effects of a perturbation on the power rail are very difficult to analyze, as it is the case with many aspects of non-linear control. It has been shown that the power supply rejection ratio is both dependent on modulation method, frequency ratio and modulation depth. In general, the rejection is below what can be achieved by linear controllers, where the power supply rejection ratio is determined by the sensitivity function exclusively. But then again, OCC is in effect a combined modulator/control system, so a comparison with a linear feedback controlled system is not directly possible.

Stability problems
The extension of the topology in Fig. 8.1 to a PMA application requires a dual supply system for operation in all quadrants. Unfortunately, this extension is not trivial and leads to potential stability problems [La96b]. The only presented solution is a feed-forward of the power rail leading to an increase in controller complexity.

8.2 Enhanced non-linear control

An improved OCC topology is investigated in the following. The non-linear control topology, henceforth reference to as Three-level One Cycle Control (TOCC), is shown in Fig. 8.3. The method solves some of the above outlined problems and errors and furthermore has other pleasant characteristics. The apparent advantages are:

- The controller in effect synthesizes NBDS PWM (see Chapter 3 for NBDS characteristics). NBDS has superior spectral characteristics to two-level PWM waveform as NADS and NADD.
- An improved Power Supply Rejection Ratio.
- Improved stability. There is no need to feed-forward the supply voltage to stabilize the topology. The inherent stabilization reduces the complexity compared to a dual supply system.
- Relatively simple hardware implementation.

As seen on Fig. 8.3 the full bridge TOCC based PMA consists of to independent parallel sections that are synchronized by the same clock. Each of the controller legs needs an offset v_f added to the input in order to allow the output swing to have symmetric limitations. Perturbations on the power rail result in similar errors at the two outputs now only generating a common mode error. Consequently, the TOCC topology improves PSRR compared to normal OCC. Still, it is not possible to eliminate the dependency of power supply perturbations.

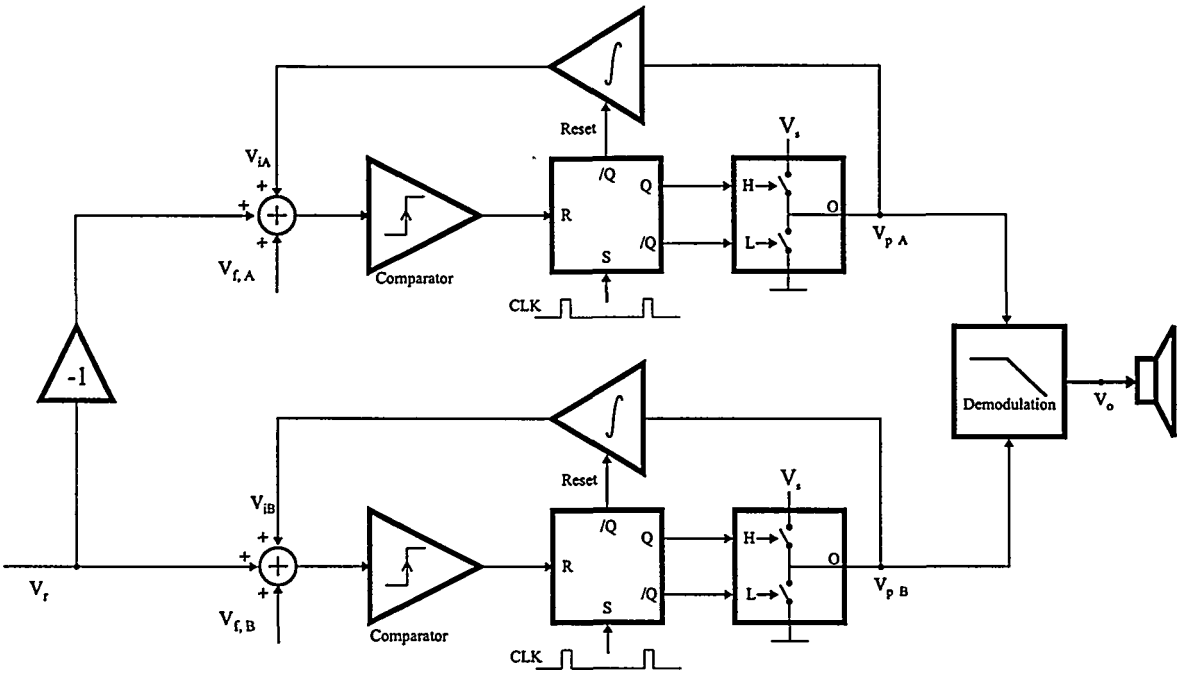


Fig. 8.3 Three-Level One Cycle Control (TOCC) effectively synthesizing NBDS PWM.

8.2.1 TOCC synthesis

The synthesis and optimization of a TOCC based PMAs requires the following fundamental steps:

- Design of power stage to meet power and bandwidth specifications.
- Design of the integrator w. reset to meet the gain specification.
- Verification of the system through non-linear simulation
- Implementation and verification in hardware.

Due to the nonlinear nature it is not possible to base the controller synthesis and optimization on a linear model of the system. The design has to be carried out a low circuit level.

8.2.2 TOCC non-linear modeling and simulation

A non-linear simulation model, shown in Fig. 8.4, has been developed using PSPICE to provide means for a detailed investigation of the behavior of the modulator/control system. The model is used throughout the following for both functional simulations with an ideal power stage and for parametric investigations where the correction effect towards non-linear behavior is investigated. The model is as ideal as possible with controllable perturbing parameters and allows analysis of one problem/effect at a time, without losing the connection between cause and result.

The integrator w. reset is modeled as shown in Fig. 8.5. It is impossible to implement the integrator fast enough using just one switch connected across the integrating capacitor. One way of achieving near instantaneous reset is by using two integrator capacitors and a more complex switch network. Only one of the two capacitors is active at a time and the other shorted, when a fast reset is needed the shorted capacitor is made active and the other is shorted. This configuration leaves one switch period to discharge a capacitor, and the swiftness of the reset is now determined only by the speed of the switches interchanging and discharging the capacitors. There are two serious drawbacks of this integrator

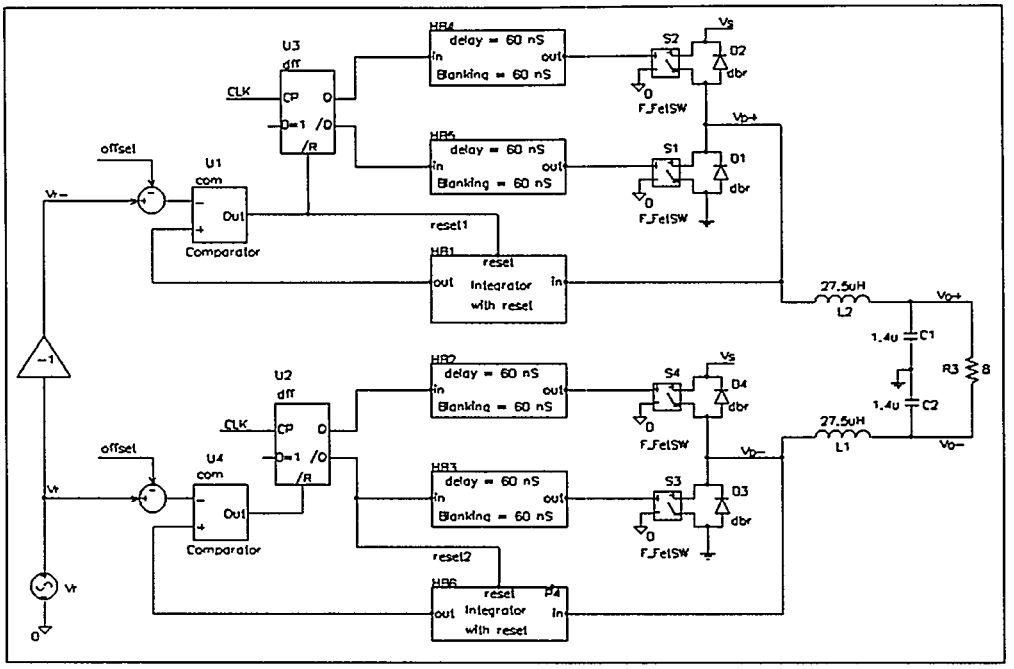


Fig. 8.4 PSPICE Model of TOCC system.

topology: The capacitors have to be matched to keep K_{OCC} constant, and the multi-switch topology is certainly not simple. The total reset capacitance is constituted of the parasitic capacitance of the switch and the integrator capacitance.

8.2.3 TOCC case example

A case example is subjected to a more detailed investigation in the following:

- The amplifier is designed for the full audio bandwidth, with a maximal power output of 350W in 8Ω. The desired power range requires a bus voltage V_S for the bridge of 80V.
- The carrier frequency is selected to be 300KHz.
- The maximal signal level at the integrator output is specified to 2.5V.

With these fundamental components now determined, the resulting system gain for each individual system on each side of the load is:

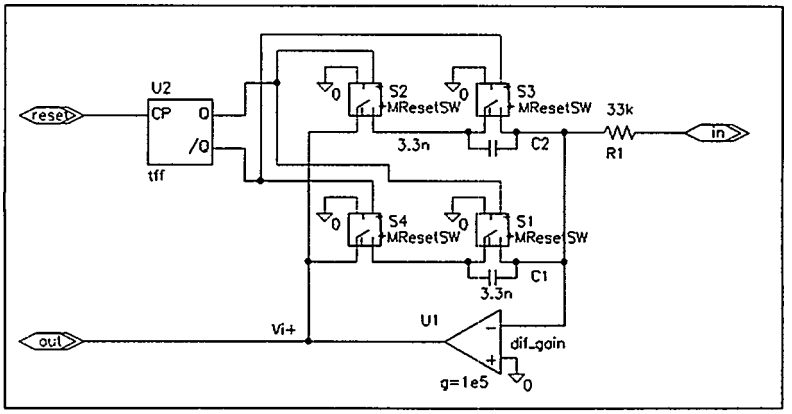


Fig. 8.5 Integrator w. reset (PSPICE model).

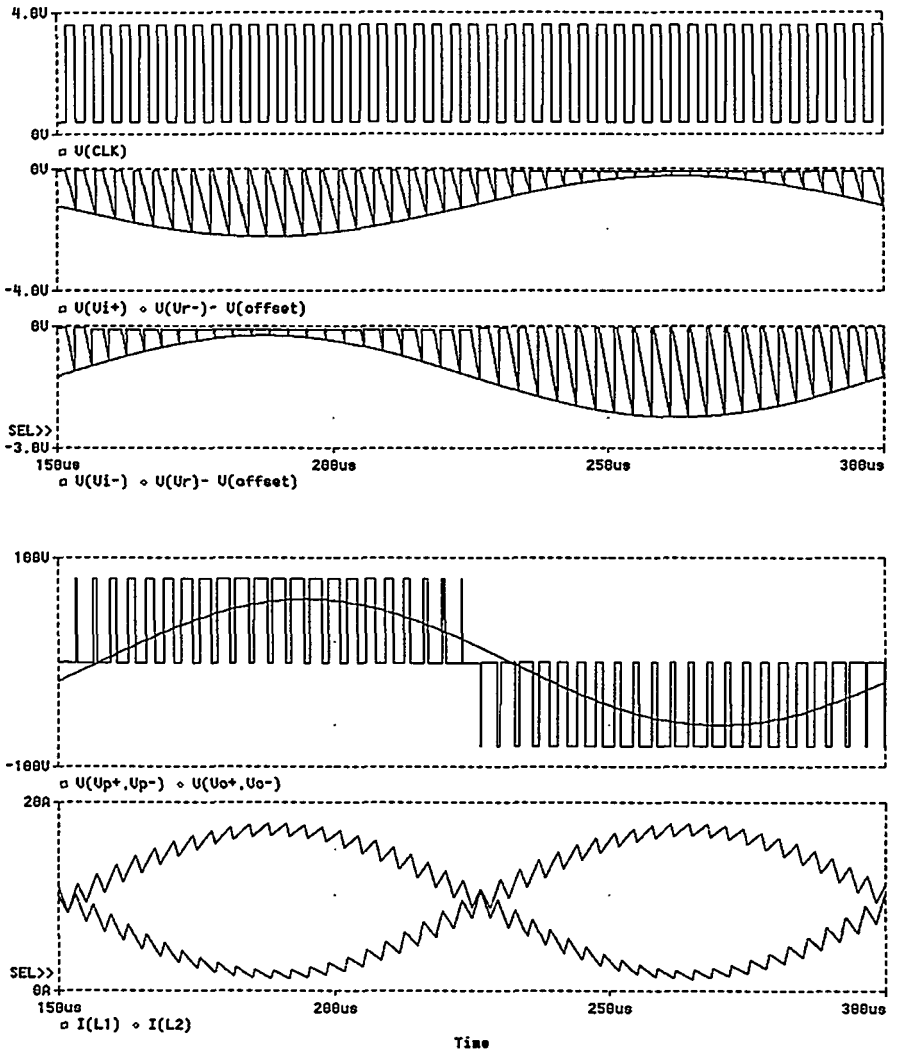


Fig. 8. 6 Functional simulation of case example with TOCC. From top to bottom: (1) Common clock, (2)-(3) control signals on both sides in terms of integrator output v_i and reference v_r-v_f, (4) Differential power stage output and demodulated output. (5) Inductor currents in the output stage illustrating the balanced drive of the load.

$$K_{OCC} = \frac{V_S}{\hat{v}_i} = 32 \tag{8.4}$$

The resulting system gain is doubled to 64 since the amplifier output is the difference between right and left side OCC systems. From (8.3) the time constant is determined:

$$RC = t_c K_{OCC} \tag{8.5}$$

With the specific integrator model the specification of R and C are not crucial, and R=33K and C=3.3nF are chosen arbitrarily to realize the time constant. Nevertheless, there are several factors to consider regarding the practical implementation. These implementation issues are addressed in Chapter 10.

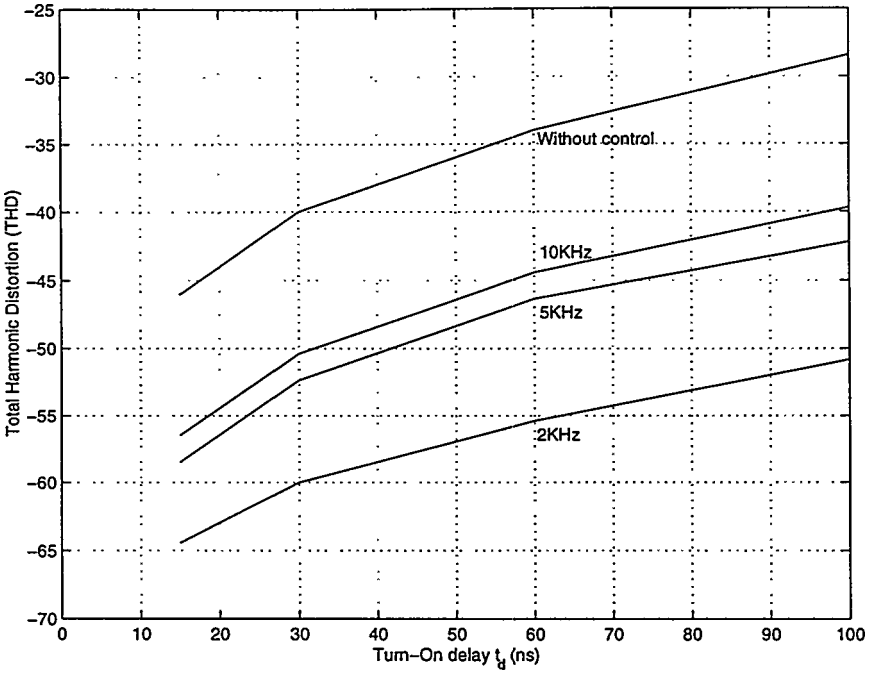


Fig. 8.7 Simulation of correction of PTE. THD vs. blanking delay t_d is investigated without control and with the TOCC controller.

Functional simulation

The functional verification of the TOCC based PMA is shown in Fig. 8. 6. The simulated system gain is 64 as expected. Observe the clear three-level nature of the differential output corresponding to NBDS modulation.

Correction of PTE

It is very interesting to investigate the correction of any kind of non-linearity that is introduced with the switching power stage, since this is very difficult to predict by theoretical investigations. Despite the non-linear nature of the controller, it is reasonable to expect a similar correction of all types of errors. However, it is difficult to predict the parametric dependency of the correction, i.e. the dependency on frequency and modulation depth. A complete investigation of various error sources within the complete frequency and power range would lead to an exhaustive set of simulations. Hence, a limited but accurately selected set of points within the parameter space has been selected for simulation. This comprises the following limited set of parameters:

- Frequencies 2KHz, 5KHz and 10KHz.
- Modulation index = 0.9.
- Blanking delays 0ns - 100ns.

Fig. 8.7 shows the simulated results. It is concluded that the controller does provide correction of errors from the PTE category, but the correction is strongly dependent of frequency. The suppression resembles what can be achieved by the linear VFC2 topology, both in terms of magnitude and frequency dependency. This is certainly somewhat disappointing, given that TOCC in theory should cancel PTE completely.

Correction of PAE

The effects of pulse amplitude errors is investigated by a simulation a perturbed system where a large 5KHz error signal of 40Vpp is superposed on the supply voltage. The signal

frequency is 20KHz and the modulation index 0.75. Fig. 8.8 illustrates the control signals and resulting demodulated output. Clearly, the intermodulation is not visible in the time domain output. A frequency domain analysis reveals intermodulation components of 300mV at 15KHz and 25KHz corresponding to a power supply rejection ratio of about 30dB. Simulations at lower frequencies and lower modulation indices show improved power supply rejection than in this worst-case situation. This is to expect from previous investigations of OCC [Ta97].

Stability and Overload

One cycle control methods (TOCC included) have very distinctive characteristics regarding stability, robustness and overload. These are investigated in the following on the basis of the TOCC-model. One cycle control differs from linear control methods by exhibiting excellent stability characteristics. Fig. 8.9 shows the ideal response to a 20KHz square wave input with modulation index 0.5. The major benefit is that the control loop / modulator bandwidth can be considered infinite. The frequency response is exclusively determined by the demodulation filter. Furthermore, the controller is inherently stable and independent on any perturbation within the power stage. In terms of stability and robustness, the non-linear controller has indisputable advantages over the linear control methods that have been investigated throughout section III of this thesis.

It terms of overload, the TOCC based PMA also differs considerably from general linear control. The simulation model is used to investigate the effects of overload. Fig. 8.10 shows the essential control variables and output signals in with 5% over modulation. Clearly, even minor over modulation has dramatic effects on the output, since this immediately introduces completely *missing pulses* as opposed to the expected *full pulse* corresponding to a 100% duty cycle. The output distortion in this particular case is more that 10% or about an order of magnitude higher that would normally be expected at this level of overload. Needless to say, control circuitry is needed to limit both minimum and maximum duty-cycle. Such limiting circuitry adds complexity to the resulting system.

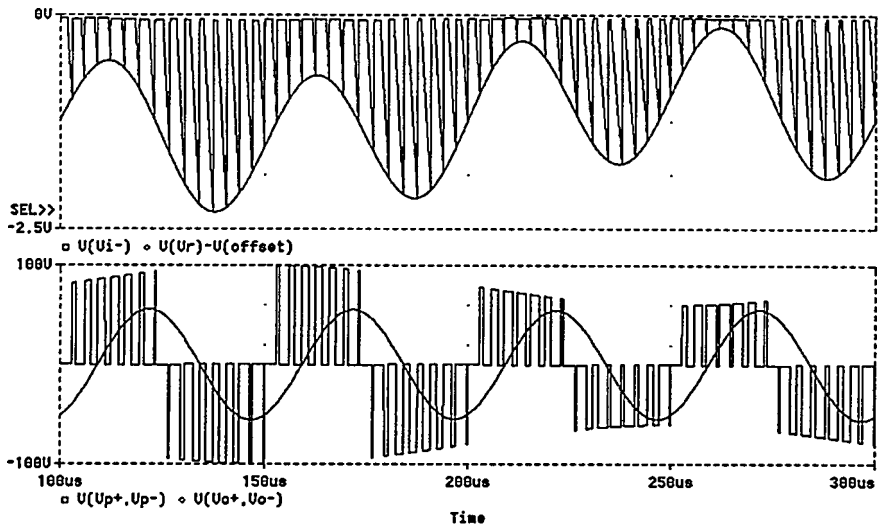


Fig. 8.8 Investigation of the effects of large 5KHz, 40Vpp perturbation on the power supply. Signal frequency and modulation index are 20KHz and 0.75, respectively. No intermodulation is visible from the time domain output. The non-linear controller provides a PSRR of 30dB in this worst-case situation.

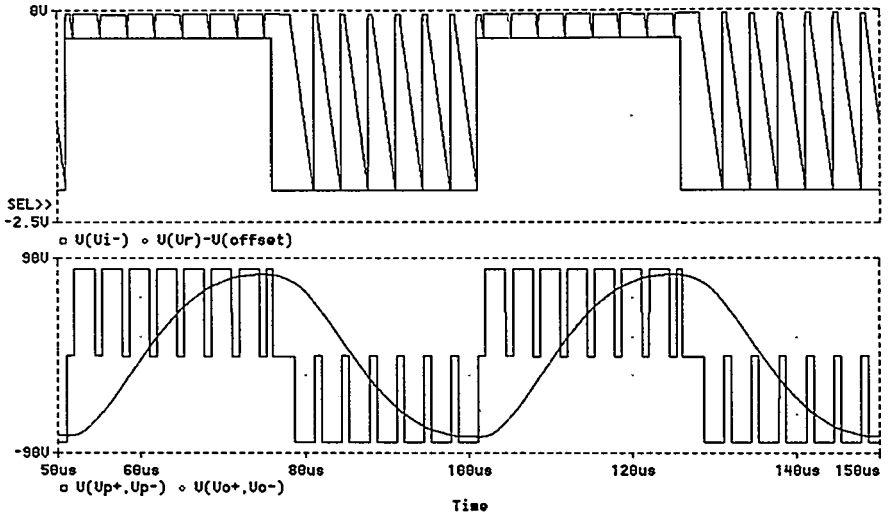


Fig. 8.9 Simulation of response to a 20KHz squarewave input. TOCC realizes ideal stability and transient response since the controller is inherently stable an the equivalent bandwidth is infinity.

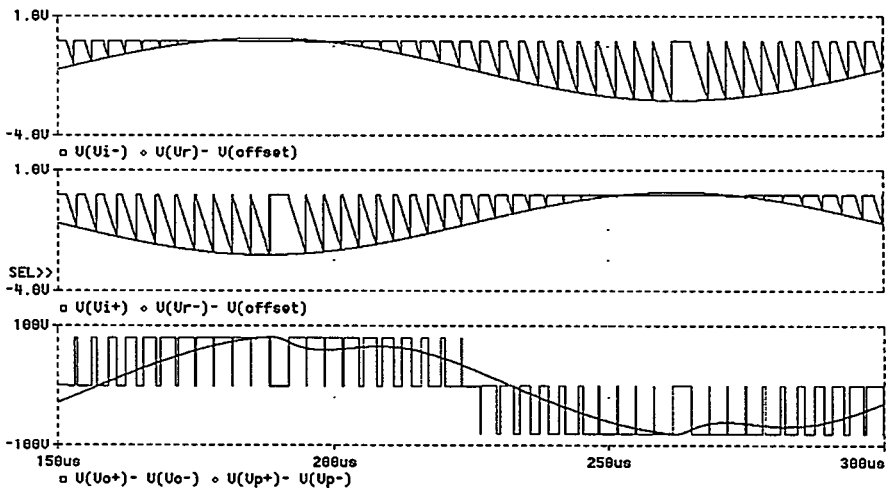


Fig. 8.10 Simulation of TOCC based system with 5% over modulation. The consequences of over-modulation are dramatic due to completely *missing* pulses as opposed to normal clipping with full (100% duty cycle) pulses.

8.2.4 TOCC extensions

An obvious extension includes the application of double sided modulation to synthesize NBDD which has further improved spectral characteristics compared to NBDS, as it was found in Chapter 3. However, implementation of double sided modulation significantly complicates the implementation [Ta97]. In addition, all error sources present within the single sided controller will also be present when using double sided modulation. The improved characteristics come at a high cost, and will do nothing with the fundamental problems within the controller.

The application of a global feedback (VFC1) is possible to improve performance. For global feedback to be applied it is vital to limit the modulation index at the modulator section. However, a linear feedback loop is considered an irrational extension, since this leaves the system with all the design constraints of linear control systems, whereby the

advantages of non-linear control vanish. The system might as well be realized by VFC1 or any of the more powerful linear control schemes as MECC in combination with conventional PWM.

8.3 Summary on non-linear control

The application of non-linear control methods for analog PMAs has been investigated in with focus on One Cycle Control. Non-linear control excels by potentially unlimited correction corresponding to a sensitivity function of zero. Furthermore, the bandwidth constraints of linear control systems are not necessarily present with non-linear control.

The basic OCC properties and failings were reviewed, and an enhanced three level non-linear controller (TOCC) that effectively synthesizes NBDS PWM has been devised. The topology offers improved modulation, robust realization without stability problems and relatively simple implementation. A PSPICE model was developed to evaluate the general correction capabilities of OCC and to enable a more detailed investigation of the TOCC circuit specifically. The non-linear controller proved indisputable advantages over any linear control method in terms of transient response, stability and robustness to uncertainties.

Unfortunately, the performance in terms of the correction towards PTE and PAE was limited. More fundamental and general constraints of OCC and similar non-linear control methods in general are concluded to be:

- Modeling and optimization is difficult. This complicates the formalization of general design methods.
- Performance improvements cannot be estimated and are difficult to control.
- Lack of flexibility. The system does operate on other feedback sources (as the global demodulated output). The are considerably difficulties in realizing double-sided modulation and other extension, etc.

The general conclusion is therefore that OCC and similar non-linear control schemes are inferior compared to the simple yet powerful control schemes that has been investigated throughout part III of this thesis. Even with significant technological advances, the considered non-linear topologies are not considered competitive with pure linear control.

Part III

Chapter 9

Pulse Referenced Control

Recall from Chapter 3, that naturally sampled PWM provides optimal modulator performance from a theoretical perspective. It was furthermore shown that there are significant complications in the implementation of digital PCM-PWM conversion. Nevertheless, the digital PMA topology is appealing from a theoretical point of view, in applications where the source material is digital. No analog modulator or carrier generator is needed and the digital modulator can provide a very consistent good performance. As clarified in chapter 4, the non-linearity of the switching power stage presents a significant impediment to maintain the modulator performance throughout the subsequent power conversion by a switching power stage. Unfortunately, no methods have been presented for power amplification of an already pulse-modulated signal, which incorporates effective means to compensate or eliminate these error sources. The extensive research activity within digital PMA systems has almost exclusively focused on the digital signal processing aspects.

This chapter investigates solutions to this fundamental problem that has persisted in digital PMA systems. A novel pulse referenced control method is proposed – henceforth referenced to as *Pulse Edge Delay Error Correction (PEDEC)*[1]. The PEDEC concept is introduced as a general method for enhanced power amplification of a pulse modulated

[1] PEDEC topologies and design methods are protected by a pending patent under the PCT agreement (PCT/DK98/00133). The rights of the author and co-applicant (Bang&Olufsen A/S) shall be respected.

signal. Following, the method is applied to digital PMA systems, and three general digital PMA topologies are proposed.

9.1 Fundamental considerations

Undoubtedly, a switching power amplification stage can be tuned to high linearity, much better performance than that of linear output stages. However, this is a complex task that requires e.g. (see Chapter 4):

- Perfect control over the switching transitions.
- Power supply stabilization., i.e. a low noise switch mode supply is needed.
- A linear filter. The filter design gets more complicated, and requires much attention. Linear core-materials are necessary.

Obviously, direct digital PCM-PWM based power conversion will never be very *elegant* or *practical.* A control system is desirable to eliminate this dependency of the many uncontrollable parameters relating to semiconductor physics, magnetics etc, such that the performance is controlled by a few e.g. passive components. The control system should be able to correct *effectively* for power stage errors by *simple* means. This will lead to improved and much more consistent performance than can be achieved with any power output stage operating open-loop.

Digital PMAs do not have an analog reference to enable linear control systems as e.g. MECC to be applied. Digital feedback control referenced to the digital source, as shown in Fig. 9.1, requires an A/D converter (or more in case of a multiple sourced control system as MECC), which renders this straightforward approach both impractical and non-elegant. The inevitable errors and failings of the A/D converter are not compensated for due the placement of the converter in the feedback path. Nothing would be gained if the saving the demodulation filter from the D/A converter [Ni96] requires the introduction of a complex, precision A/D converter. Digital feedback control for digital PMAs has been investigated [Sm94] in terms of a ripple shaping algorithm to compensate power supply perturbations. Unfortunately, besides requiring A/D conversion this leaves all other error sources in the switching power amplification stage unchanged. An interesting alternative approach to power stage error correction was presented in [Lo94], using a quantized pulse edge correction based on an analog delay line. Unfortunately, the correction effect was shown to be difficult to predict, and the correction system has its own error sources, e.g. noise generated from the quantized pulse length correction. For practical digital PMA realization, a method for improved power amplification of an already pulse modulated signal is required, where all error sources related to the power stage and demodulation filter are effectively suppressed. A novel pulse referenced control method is presented in the following, in an attempt to realize this primary objective.

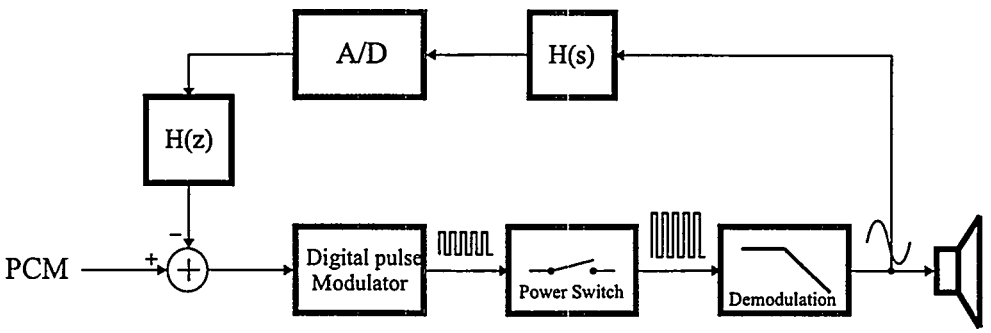


Fig. 9.1 Digital PMA based on digital feedback.

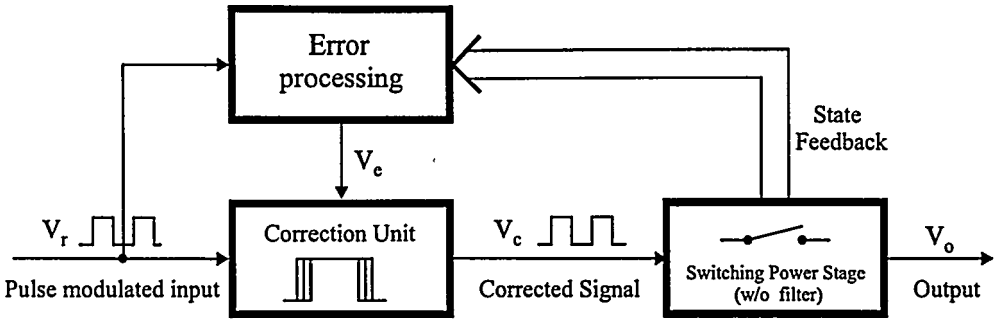


Fig. 9.2 Basic principle of Pulse Edge Delay Error Correction (PEDEC).

9.2 Pulse Edge Delay Error Correction (PEDEC)

Pulse Edge Delay Error Correction (PEDEC) [Ni97c], [Ni98b] is a novel general pulse referenced control method for enhanced power amplification of a pulse modulated signal. Applications are digital PMAs and general DC-DC and DC-AC power amplification where accurate and distortion free power amplification of a pulse modulated signal is required. The basic idea is to introduce a correction unit in-between the (ideal) pulse modulator and the switching power amplification stage. The general block diagram for a PEDEC controller is shown in Fig. 9.2. The modulator output is feed to a correction unit that provides compensation by intelligently delaying the individual pulse edges, controlled by an input control signal. The re-timing is controlled to have a "pre-distorting" effect, such that the resulting switching power stage output is free from distortion, noise or any other undesired contribution. The validity of this approach are two fundamental facts:

- Digital modulators will generate a high quality output. The pulse-modulated signal may as such be used as reference for error correction.
- *All* power stage error sources can be corrected by intelligent pulse re-timing, *and* all error sources only need minor pulse edge re-timing for perfect elimination.

A perfect reproduction of the modulated signal requires that the pulse to pulse integrated average within each cycle (or within a few cycles) is maintained. A drop in power supply level can easily be compensated for by a widening of the pulse within the cycle interval, since the output is obtained by averaging (i.e. low-pass filtering) of the pulse modulated signal. The general structure of a PEDEC controller is shown in Fig. 9.3. The general controller can be viewed as a dual reference input pulse reference feedback control system comprising:

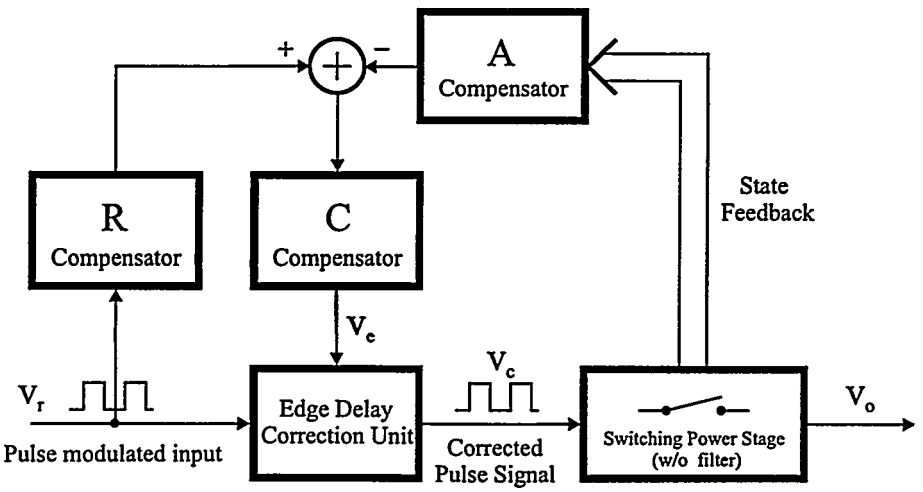


Fig. 9.3 The general elements of a PEDEC controller.

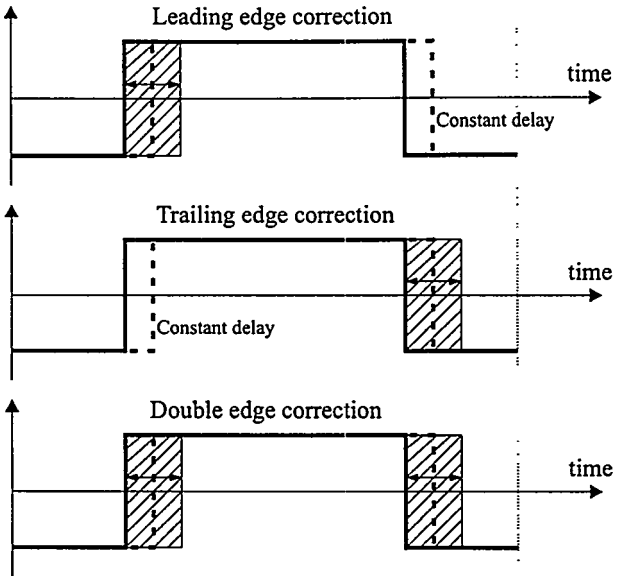


Fig. 9.4 Basic approaches to PEDEC implementation.

- The PEDEC unit with means to control the delays of the individual edges on the reference input v_r, based on a control input v_e. The PEDEC unit output is the corrected or "pre-distorted" signal.
- A state feedback block A that includes compensation from the power stage block.
- An optional reference shaping block R that serves to optimize the error estimation.
- A subtraction unit to generate error information.
- A compensator C to shape the error that feeds the PEDEC unit (v_e).

Several approaches to pulse edge correction are illustrated conceptually in Fig. 9.4. Both leading edge, trailing edge or double edge delay error correction are feasible solutions. The following sections will introduce a range of new parameters, defined in Table 9.1, in order to provide a coherent analysis.

9.2.1 Control function specification

A central aspect is the specification of the PEDEC unit control function. For simple analysis and implementation, it is of course desirable with the simplest possible control function. Let the control error signal to the PEDEC unit realize a controlled function on the pulse edges, such that the effective change in pulse width Δt_w at the end of the switching cycle is proportional to the control signal v_e:

$$\Delta t_w = k_w \cdot v_e \tag{9.1}$$

I.e:

$$\frac{dt_w}{dv_e} = k_w \tag{9.2}$$

Parameter	Description
v_e	Control error signal to PEDEC unit
v_r ($\tilde{v}_r$)	Reference signal (pulse modulator output). (~) indicates the average or low frequency part of the signal.
v_c ($\tilde{v}_c$)	Pulse edge delayed PEDEC unit output voltage. (~) indicates the average or low-frequency component of the modulated signal.
t_s	Switching period.
t_0	Central PEDEC unit parameter, corresponding to the maximal effective pulse width change.
$t_l, \hat{t}_l$	Leading edge transition time before and after (^) correction
$t_t, \hat{t}_t$	Leading edge transition time before and after (^) correction
$t_w, \hat{t}_w$	Pulse width before and after (^) correction: $t_w = t_t - t_l$
V_R	Pulse modulator output voltage level.
V_I	Limited integrator output pulse voltage level.
V_C	PEDEC unit output pulse level.
V_{CC}	Power rail voltage level.

Table 9.1 Definition of fundamental PEDEC parameters.

By averaging within a single switching cycle, the relationship between an increment in pulse width Δt_w and the corresponding change in the average of the PEDEC output $\Delta\tilde{v}_c$ can be established. Assuming for simplicity here, that the PEDEC output pulse amplitude is unity:

$$\Delta\tilde{v}_c = \frac{1}{t_s}\left(\int_0^{d\cdot t_s+\Delta t_w} 1\cdot dt + \int_{d\cdot t_s+\Delta t_w}^{t_s}(-1)\cdot dt\right) = \frac{2}{t_s}\Delta t_w \tag{9.3}$$

Where d is the duty-cycle within the present switching cycle. Hence:

$$\frac{d\tilde{v}_c}{dt_w} = \frac{2}{t_s} \tag{9.4}$$

Combining (9.2) and (9.4), the fundamental linear PEDEC control function arrives:

$$\boxed{k_{PEDEC} = \frac{d\tilde{v}_c}{dv_e} = \frac{2k_w}{t_s}} \tag{9.5}$$

Such a simple linear control function dramatically simplifies PEDEC controller design, since the whole machinery of linear control system design and verification can be fully utilized. Obviously, other control functions (e.g. non-linear functions) could be interesting alternatives for PEDEC. This could be a subject for future research.

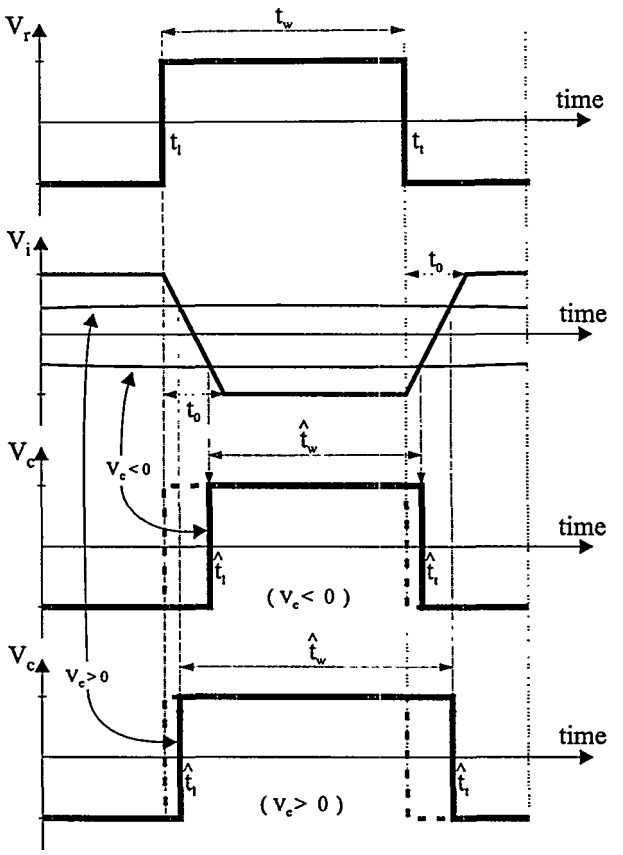


Fig. 9.5 Proposed realization of a linear double edge PEDEC control function.

9.2.2 Realizing the control function

This section proposes a simple approach to implement the double sided PEDEC unit, which implements the above specified control function. The method is shown in Fig. 9.5. The pulse delay correction is realized by a limited integration of the incoming (ideal) pulse waveform generating the signal v_i, and comparing this modified reference with the control signal v_e. The effective pulse width change, Δt_w, will be the difference between the leading edge delay and the trailing edge delay. From Fig. 9.5 it is obvious that $v_e > 0$ will increase the pulse width, whereas $v_e < 0$ will lead to a negative Δt_w. The following relations are obtained from the proposed double edge correction scheme in Fig. 9.5:

$$\hat{t}_l = t_l + \frac{t_0}{2} + t_0 \frac{v_e}{2V_I}, \quad \hat{t}_t = t_t + \frac{t_0}{2} - t_0 \frac{v_e}{2V_I} \tag{9.6}$$

Δt_w is derived:

$$\hat{t}_w = \hat{t}_t - \hat{t}_l = t_w - t_0 \frac{v_e}{V_I} \quad \Rightarrow$$

$$\Delta t_w = \hat{t}_t - \hat{t}_l = \begin{cases} t_0 & (v_e > V_I) \\ t_0 \dfrac{v_e}{V_I} & (-V_I \le v_e \le V_I) \\ -t_0 & (v_e < V_I) \end{cases} \tag{9.7}$$

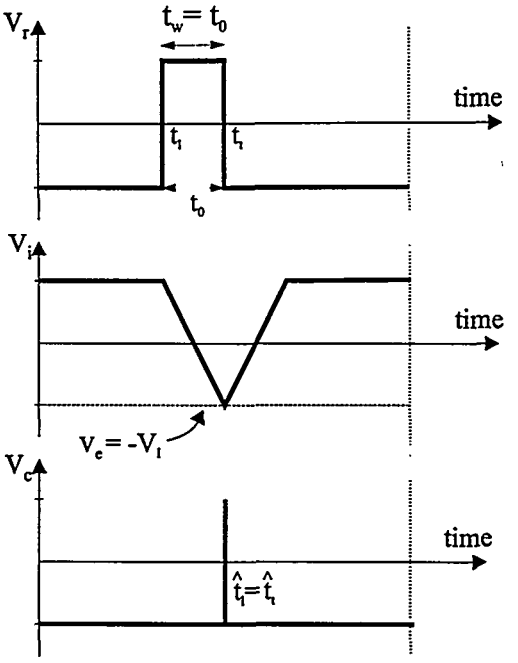


Fig. 9.6 PEDEC constraints on minimal pulse width.

In other words k_w as defined in (9.1) is:

$$k_w = \frac{dt_w}{dv_e} = \frac{t_0}{V_I} \tag{9.8}$$

From Fig. 9.5, the following relationship between and increment in pulse width dt_w and $\tilde{v}_c$ is established:

$$\frac{d\tilde{v}_c}{dt_w} = \frac{2V_C}{t_s} \tag{9.9}$$

Combining (9.8) and (9.9):

$$k_{PEDEC} = \frac{d\tilde{v}_c}{dv_e} = \frac{2V_C}{V_I}\frac{t_0}{t_s} \tag{9.10}$$

Assuming without loss of generality that the pulse amplitudes are adjusted to $V_C = V_I$, the following expression of the equivalent PEDEC unit control gain emerge:

$$\boxed{k_{PEDEC} = \frac{2t_0}{t_s}} \tag{9.11}$$

The validity of this simple linear model will be investigated throughout the simulation and verification of various topologies later in this chapter.

For optimal control with the proposed PEDEC block realization, the pulses need to have a certain minimal width. This limits the available modulation index range with digital PWM. The *minimum* pulse width is related to the modulation index M and switching period t_s as:

$$t_{w,\min} = (1-M)\frac{t_s}{2} \tag{9.12}$$

Since the minimal pulse width for correct PEDEC operation is indeed t_0 as illustrated in Fig. 9.6 the maximum modulation index is:

$$t_{w,\min} \geq t_0 \Rightarrow M_{\max} = 1 - \frac{2t_0}{t_s} \tag{9.13}$$

This constraint on pulse width and modulation index does not present a fundamental limitation, since the correction will still work partially beyond this limit. The situation in Fig. 9.6 is the absolute worst case, where the control voltage takes its *maximal* negative value. The digital input signal to the PMA could be limited at $M_{\max}$ for optimal control performance within the complete operating range for the PMA. Such a limitation is straightforward to implement in the digital domain.

9.3 Applying PEDEC to Digital PMA systems

PEDEC can be considered as a general control method for improved power amplification of a pulse-modulated signal. The generality of the principle means that it can be used advantageously in combination with a range of different control structures. With the linear control function within the PEDEC unit, a linear model for PEDEC based digital PMA can be derived. Following, the controller design may follow the general 6 step methodology for controller design and verification. However, there are some significant differences between linear controller design for analog PMAs, and linear controller design using PEDEC. First of all, the loop in the PEDEC based system does not enclose a modulator. The equivalent linear gain of the power is the pulse amplification factor:

$$K_P = \frac{V_{CC}}{V_R} \tag{9.14}$$

Another significant difference is the effects of v_p, i.e. the tradeoffs between bandwidth and carrier frequency is different. An interesting property of PEDEC control is that the noise from v_p may be nearly eliminated by proper reference shaping (R), such that the noise on the control signal v_e is also minimized. PEDEC also differs from conventional control systems by the limited correction range of the PEDEC unit. This has significant importance in terms of gain control in that the range of system gain adjustment will be limited. Furthermore, the switching frequency has determining influence on the control system. This has to be taken into account during controller design.

9.3.1 Defining control structures

Three basic topologies based on single loop control are defined and investigated in more detail in the following. The topologies differ mainly in terms of feedback source and error estimation. The double edge PEDEC unit will be used throughout the investigations.

Without loss of generality, it is assumed throughout the investigations, that the pulse levels in the controller are identical, i.e. $V_R = V_C = V_I$. The three topologies are introduced below.

PEDEC Voltage Feedback Control – Type 1 (VFC1)
PEDEC VFC1 is characterized by a voltage feedback from the switching power stage output v_p. The feedback path compensator is a simple attenuation, and the compensator block C is a linear filter. The topology is furthermore characterized by a *zero order reference shaping*, i.e. the reference shaping block R is completely omitted such that the error estimation is based on a direct comparison of input and output pulses. Despite the simple controller structure of PEDEC VFC1, the system introduces a powerful and flexible control of system performance.

PEDEC Voltage Feedback Control – type 2 (VFC2)
PEDEC VFC2 resembles PEDEC VFC1 in terms of feedback source. However, the topology differs by *first order reference shaping* in combination with a *matched first order output feedback shaping* in the A block. This also lead to different compensator characteristics (C).

PEDEC Voltage Feedback Control – type 2 (VFC3)
PEDEC VFC3 differs significantly from the other two topologies by utilizing *global* feedback from v_o, in combination with *second order reference shaping* for optimal error estimation. Including the filter in the loop significantly changes the compensator characteristics.

The three topologies will be subjected to a detailed investigation in the following. Loop shaping methods will be addressed by presenting a general frequency normalized loop synthesis methods. Following, illustrative case example will be synthesized and evaluated for each topology.

9.4 PEDEC VFC1

The control structure is shown in Fig. 9.7. Despite the simplicity of the controller, the system enables powerful control of the performance of the switching power amplification stage. Note how the audio signal remains digital or pulse modulated throughout the main audio chain. No analog modulator or carrier generator is needed in the digital PMA system. The system is essentially controlled by the digital modulator.

9.4.1 Analysis

Given the linear control function in (9.11), it is straightforward to derive the equivalent linear model of the system as shown in
Fig. 9.8. The individual elements of the controller are also defined in the figure. The loop components are:

$$\begin{cases} C(s) = K_C \dfrac{(\tau_{z1}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)} \\ B(s) = K_P k_{PEDEC} \\ A(s) = \dfrac{1}{K} \\ R(s) = 1 \end{cases} \tag{9.15}$$

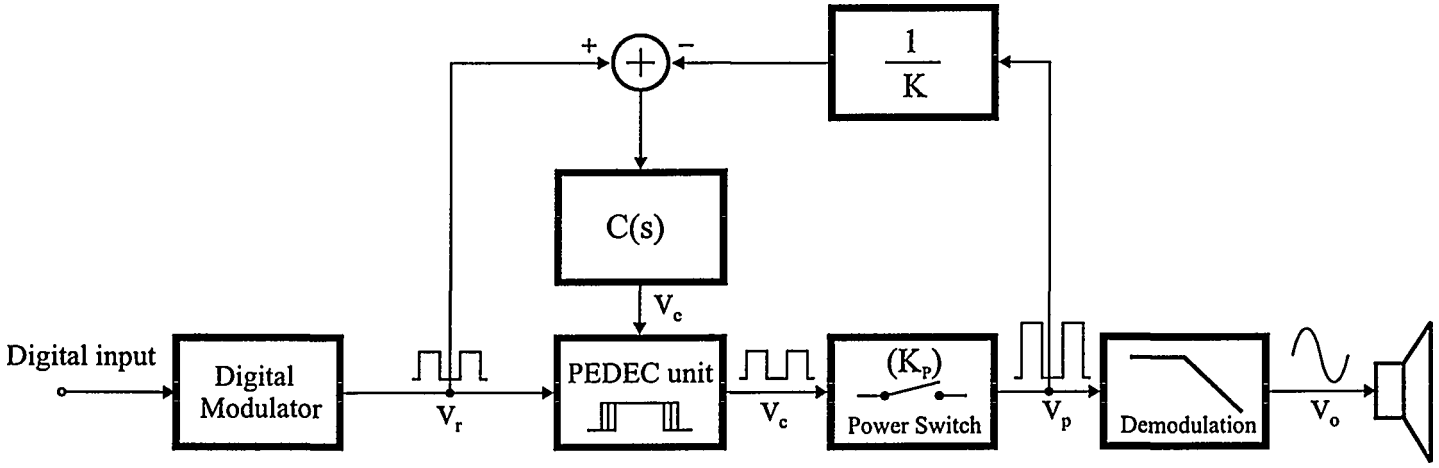


Fig. 9.7 PEDEC VFC1 Topology.

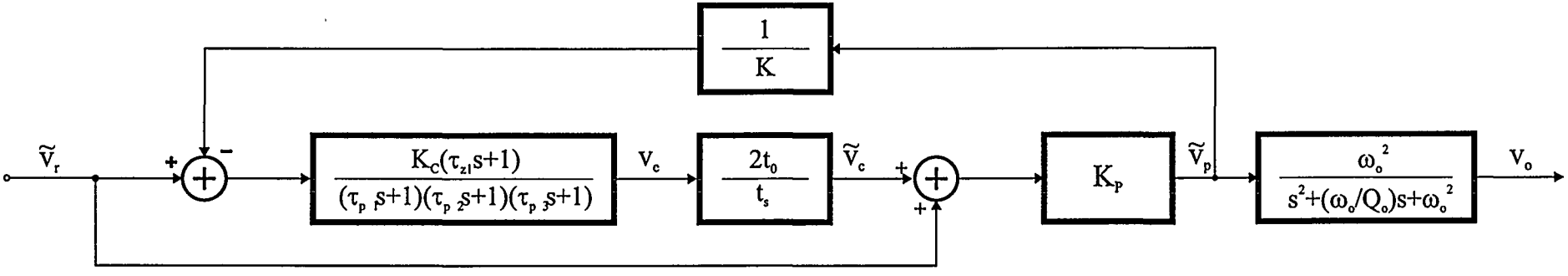


Fig. 9.8 Dual input linear model of PEDEC VFC1 Topology with all compensator elements defined.

The C compensator provides sufficient flexibility for loop optimization. The loop transfer function is:

$$L_1(s) = \frac{K_P k_{PEDEC} K_C}{K} \frac{(\tau_{z1}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)} \tag{9.16}$$

The compensator gain K_C has to be tuned to realize the desired loop bandwidth. The linear model in Fig. 9.7 illustrates the *dual* input configuration, i.e. the system transfer function from v_r to v_p has two contributions:

$$\begin{aligned} H(s) &= \underbrace{\frac{C(s)B(s)}{1+A(s)C(s)B(s)}}_{H_{1A}} + \underbrace{\frac{K_P}{1+A(s)B(s)C(s)}}_{H_{1B}} \\ &= \frac{K_P[C(s)k_{PEDEC}+1]}{1+A(s)C(s)B(s)} \end{aligned} \tag{9.17}$$

In the special but not unusual case where $K = K_P$, the transfer function is *constant*:

$$H(s) = \frac{K[C(s)k_{PEDEC}+1]}{1+C(s)k_{PEDEC}} = K \tag{9.18}$$

This characteristics is significantly different from the previously analyzed control methods. The explanation is that PEDEC VFC1 is *only contributing to system performance as all as long as there are errors present.* In the general case, corresponding to $K \neq K_P$:

$$H(s) \approx \begin{cases} K & (f < f_u) \\ K_P & (f >> f_u) \end{cases} \tag{9.19}$$

$K \neq K_P$ can be viewed as a linear error that the PEDEC controller will attempt to correct for. Obviously, this correction is only possible within the bandwidth of the system. With a standard second order filter for demodulation:

$$F(s) = \frac{\omega_o^2}{s^2 + \frac{\omega_o}{Q_o}s + \omega_o^2} \tag{9.20}$$

The system transfer function will essentially be determined by the demodulation filter.

9.4.2 PEDEC VFC1 loop shaping

Table 9.2 proposed a set of general system parameters. The specification of the PEDEC unit gain is based on an estimation of the necessary correction range, and the specified gain of 0.2 represents a good compromise. A higher k_{PEDEC} compromises the modulation index range with optimal control and the lower gain on the other hand compromises the range of error size. This will especially be a problem in terms of the correction of large magnitude linear errors.

Parameter	Value	Comment
$k_{PEDEC} = \frac{2t_o}{t_s}$	$\frac{1}{5}$	Equivalent PEDEC unit gain.
$f_{p1} = \frac{1}{\tau_{p1}}$	$\frac{1}{20} f_u$	Loop parameter
$f_{p2} = \frac{1}{\tau_{p2}}$	f_{p1}	Loop parameter
$f_{p3} = \frac{1}{\tau_{p3}}$	$2f_u$	Loop parameter
$f_{z1} = \frac{1}{\tau_{z1}}$	$\frac{1}{2} f_u$	Loop parameter
f_o	2	Filter natural frequency
Q_o	$\frac{1}{\sqrt{3}}$	Filter Q

Table 9.2 Proposed general parameters for PEDEC VFC1 loop shaping.

9.4.3 Case example

Specification

A case example is considered for the full audio bandwidth with a system gain of $K = 20dB$ and an equivalent power stage gain of $K_P = 20dB$.

Synthesis

The synthesis is trivial with the defined general loop shaping procedure. The bandwidth of the considered case example is $f_u = 5$.

Verification

Fig. 9.9 shows Bode plots for each component in the loop and the resulting loop transfer function. The characteristics are much alike the VFC2 topology that was investigated in Chapter 6. The main difference is that the $C(s)$ compensator has to have a higher gain. Fig. 9.10 shows Bode plots for the individual components that contribute the closed loop system response. The following is verified:

- Within the bandwidth of the control system, the "feedthrough path" is suppressed, i.e. the system is controlled exclusively by the loop.
- Around the frequency of unity gain, both paths contribute to the system response such that the system gain remains constant.
- Beyond the bandwidth of the loop, the "feedthrough" path exclusively determines the system response.
- With a constant gain characteristic of PEDEC VFC1, the demodulation filter determines the system respnose.

Robustness properties

PEDEC VFC1 is influenced by uncertainty on the same parameters as VFC2 in chapter 6. Since the loop transfer function characteristics are similar, the same conclusions can be drawn, i.e. PEDEC VFC1 will obey *RS* and *RP* within the *US*. However, it should be emphasized that the correction range of PEDEC is physically limited such that the control system will not operate correctly over the complete range of gain perturbations. The correction range is related to t_0, i.e. k_{PEDEC}.

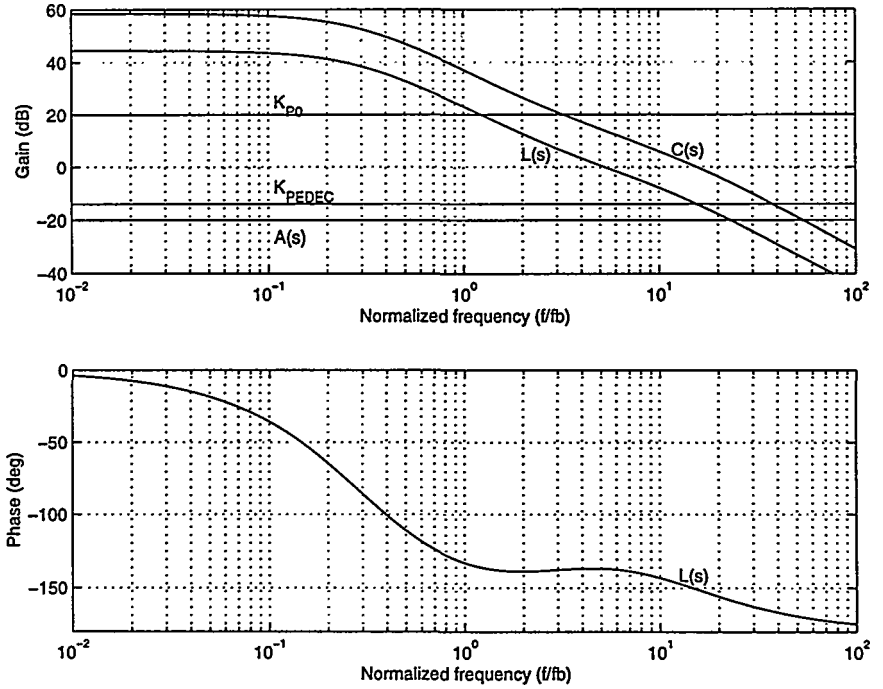


Fig. 9.9 Lop components and the resulting loop transfer function for PEDEC VFC1.

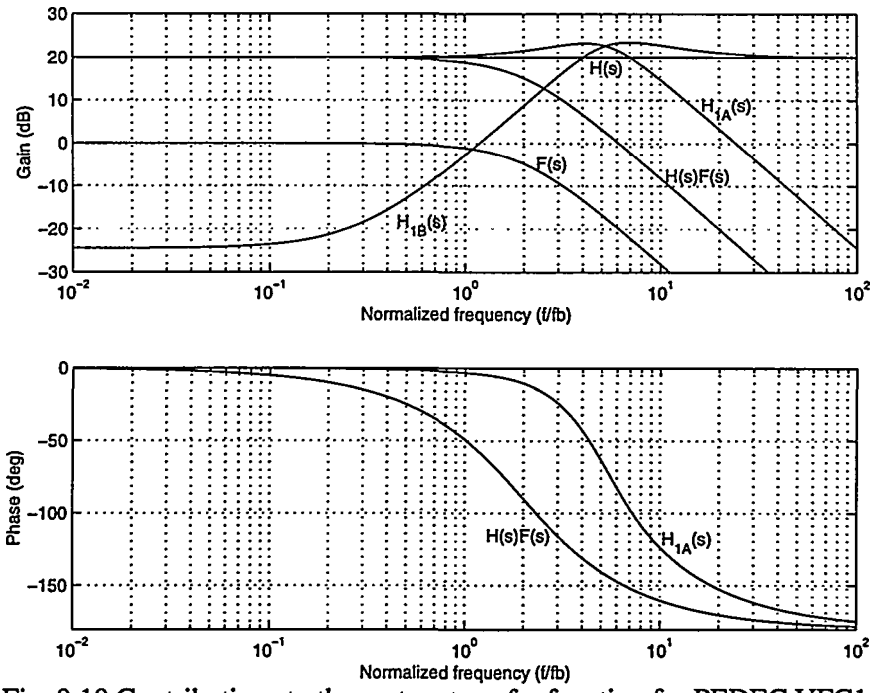


Fig. 9.10 Contributions to the system transfer function for PEDEC VFC1.

Non-linear simulation

The system considered is again a 200W power stage, operating on a V_S power supply level. The parameters are summarized below:

Parameter	Value	Comment
f_B	20KHz	Bandwidth frequency
K	20dB	Amplifier gain
V_S	50V	Power supply rail
f_s	350KHz	$t_s = 2.86\mu s$
t_0	286ns	Realizes desired PEDEC unit gain
V_C, V_I, V_R	5V	Pulse amplitude levels.

There are quite a few differences between the linear feedback topologies presented in the previous chapter and a PEDEC controlled digital PMA. Some of the important differences are:

- The limited correction range.
- The dual input topology.
- The carrier frequency influences on e.g. stability.

PEDEC VFC1 has been subjected to a thorough low level simulation. The essential results will be presented in the following.

Fig. 9.11 shows a simulation of the complete PEDEC VFC1 system at idle operation. The feedback compensator output has the opposite phase of the PWM reference, such that most of the carrier related signals are eliminated at the difference point. This initial functional simulation of the system verifies that the correction system is stable and operating exactly as specified. As specified in (9.19), the system gain can be adjusted by the A-compensator in the feedback path. This is verified by the functional simulation in Fig. 9.12. The A-compensator gain is adjusted to 1/8, 1/10 and 1/12 to realized various closed loop system gains. Note the significant fundamental component in v_e where $K \neq K_P$. It is concluded, that the gain can be adjusted over a small range while maintaining system performance.

Correction of PTE

The capability to suppress PTE errors has been investigated by a parametric investigation of the near worst-case situation $M = 0.5$, $f = 5KHz$. Fig. 9.13 shows the PEDEC unit control signal and the resulting output in the two cases $t_d = 10ns$ and $t_d = 100ns$, respectively. There is no visible distortion i.e. the outputs are identical. The improvement in distortion is about 25dB, corresponding to theory. It is very interesting to observe, how the controller applies anti-distortion with by widening the pulse when the error signal with a positive error signal during the positive going cycle and vice versa. The square wave error is recognized from the distortion analysis in Chapter 4, i.e. the control signal to the PEDEC unit *directly envisions the distortion type.* A parametric analysis of THD vs. t_d is shown in Fig. 9.14. The improvement is constant and independent of t_d. Furthermore, the reduction in distortion depends on the loop gain linearly as seen from the three simulations. The frequency dependency of the correction has been verified in [Ni97c]. In general, PEDEC VFC1 provides effective control over PTE errors and the performance improvements are easily controlled.

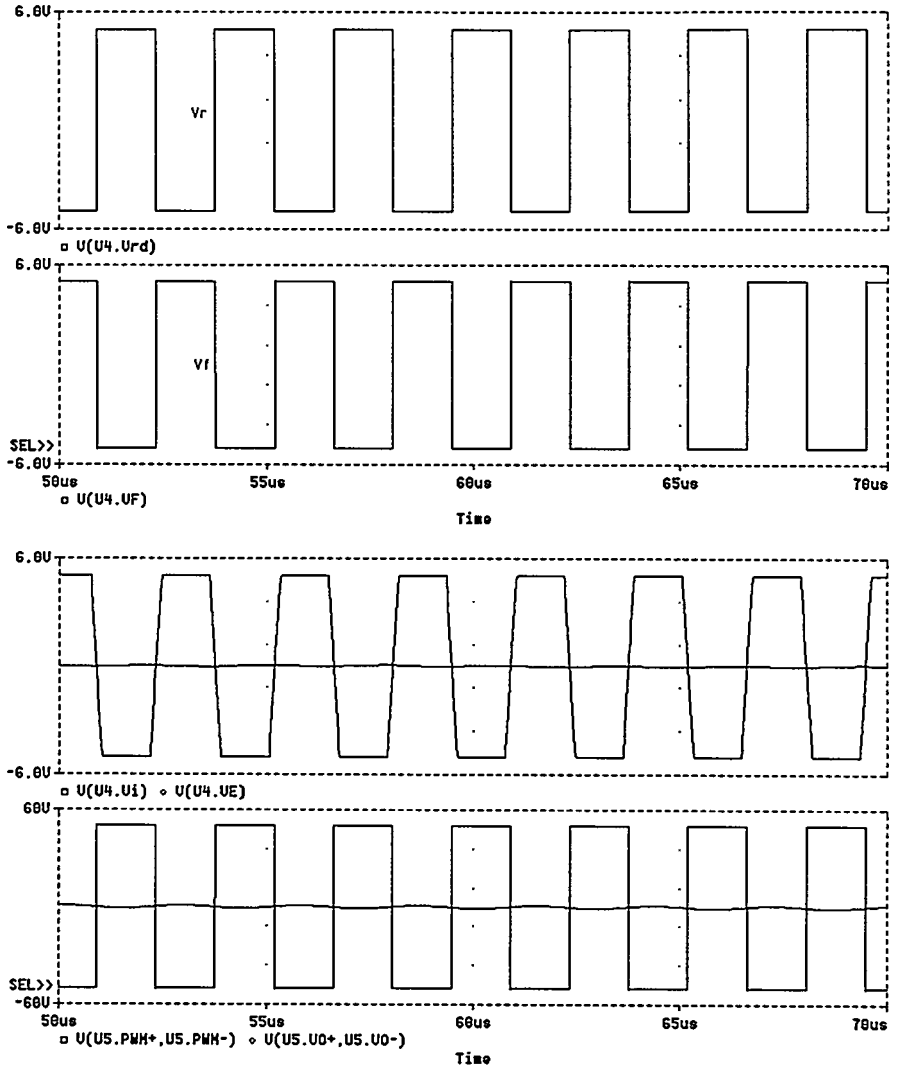


Fig. 9.11 Functional simulation of PEDEC VFC1 system. Reference input v_r and feedback v_f, PEDEC unit signals v_e, v_i and finally the resulting corrected power stage output.

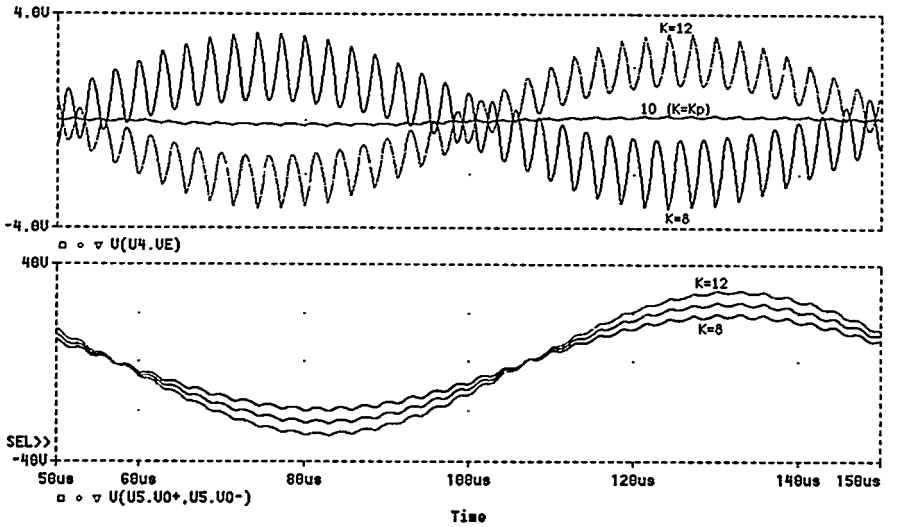


Fig. 9.12 Functional simulation of gain control with the PEDEC VFC1 Controller. A-block compensator gain is adjusted to 1/8, 1/10 and 1/12, corresponding to gains of 8, 10 and 12 respectively. Top - PEDEC unit control signal v_e. Bottom – PMA output.

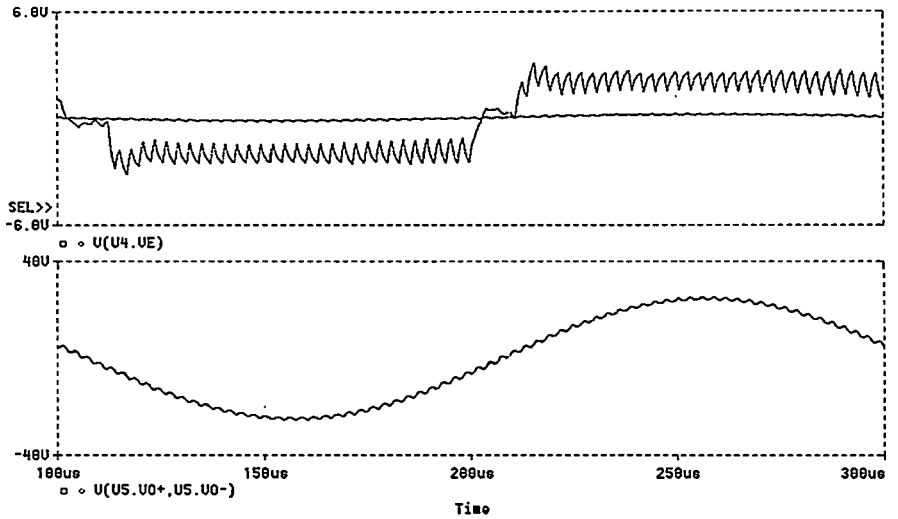


Fig. 9.13 PTE correction for PEDEC VFC1. *M=0.5. f=5KHz.* Top – v_e with t_D=*10ns* and t_D=*100ns.* v_e clearly envisions the distortion type. Bottom – Resulting output. Even large linear and non-linear errors are corrected effectively by the PEDEC controller.

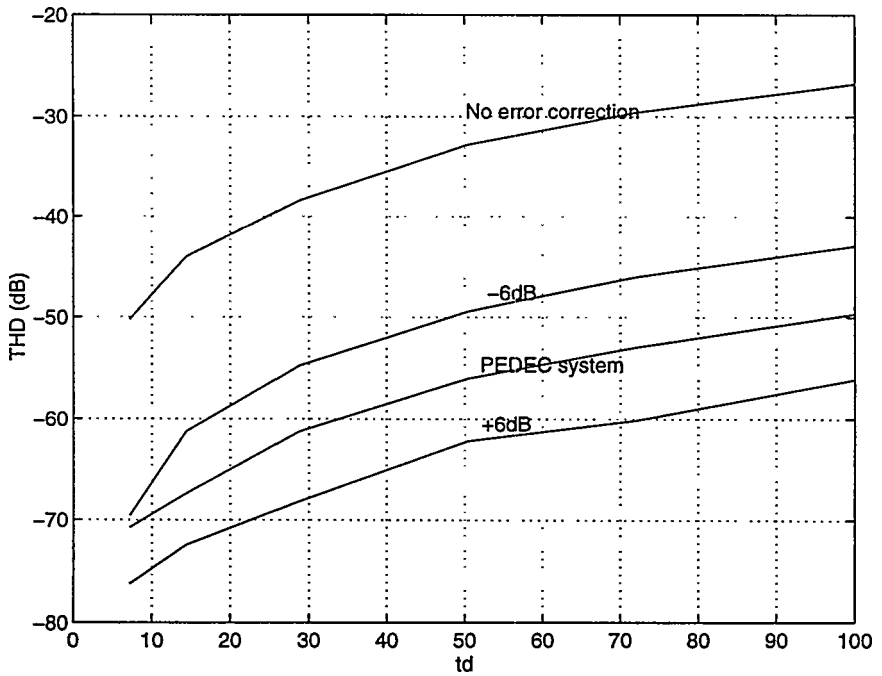


Fig. 9.14 Parametric investigation of THD vs. t_d for PEDEC VFC1. The controller improves THD 20dB - 30dB, corresponding to theory. Equally important - the performance improvements are controllable by the compensator.

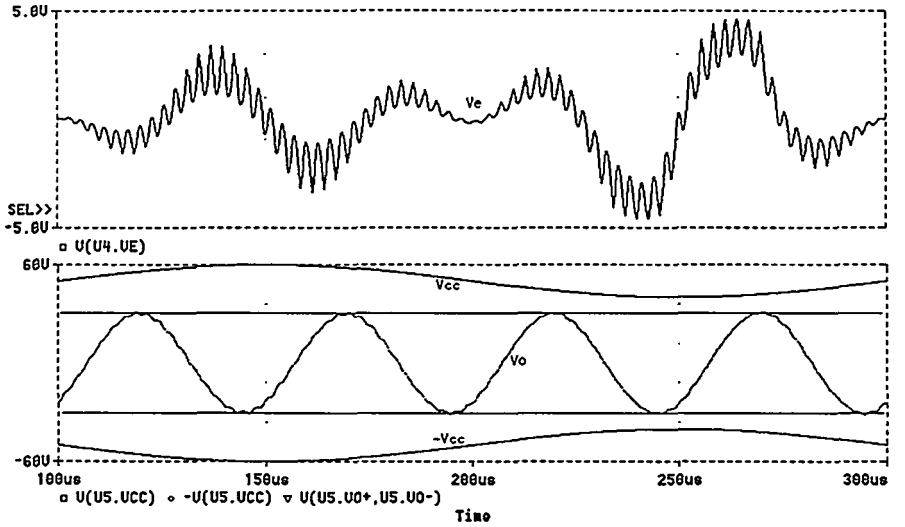


Fig. 9.15 Simulation of the correction of PAE for PEDEC VFC1. Power supply is perturbed with a 5KHZ, 10Vpp error signal. *M=0.5. f = 20KHz* (worst-case). The PEDEC controller effectively reduces the intermodulation and improves PSRR by about 25dB corresponding to theory.

Correction of Pulse Amplitude Errors (PAE)

Pulse amplitude errors can have significant magnitude, especially if a simple non-stabilized power supply is used. The rejection of power supply perturbations is investigated by superposing the power rail with a 5KHz, 10Vpp harmonic perturbations. This causes an IM-distortion in the order of 5%-10% as shown in Chapter 4. Fig. 9.15 shows a simulation of the perturbed system with the PEDEC controller. The intermodulation is reduced by approximately 25dB in this worst case situation as expected from theory, and no intermodulation is visible in the time domain. The PEDEC controller compensates for the effect by widening the pulses (positive control signal v_e) where the PWM signal is compressed and vice versa. This is observed by looking at the control signal v_e in Fig. 9.15.

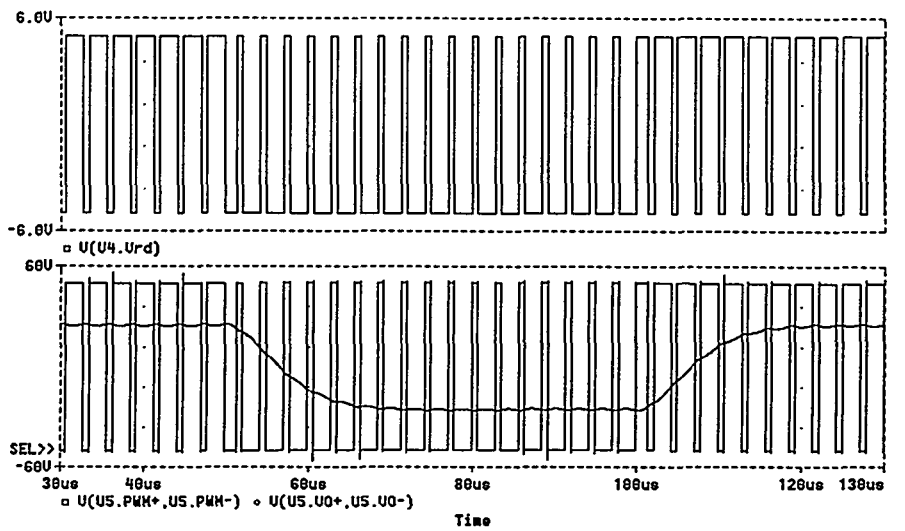


Fig. 9.16 A simulation of the excellent transient response characteristics of PEDEC VFC1. Close investigation of the pulse output v_p shows exact and *instant* amplification of the reference. The explanation is that PEDEC VFC1 only "works" when errors are generated, and does not affect the amplification otherwise.

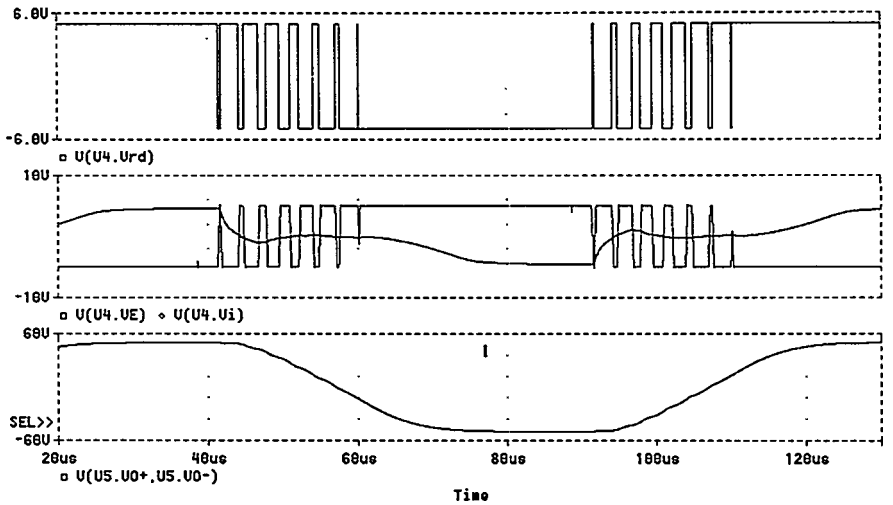


Fig. 9.17 A simulation of a severe 50% overload situation for PEDEC VFC1. Top – Clipping reference. Mid – Control signal to the PEDEC unit and integrated reference. Bottom- The resulting output with 50% overload. The recovery from overload is instant, and the clipping characteristics are as acceptable.

Stability and overload

An interesting characteristic of PEDEC control is that PEDEC will not oscillate in the traditional way at some unity gain frequency above the audio band, since the correction range is limited. Accordingly, the stability is limited and the effects thereof are equally limited (no tweeter burn out etc.). Another interesting aspect is the excellent transient response of the control system. This instant transient response is illustrated in Fig. 9.16.

The special characteristics in overload situations are simulated in Fig. 9.17. The clipping characteristics and recovery from overload very satisfying. Correspondingly, the minimum pulse width constraint merely indicates the range where the correction afforded by PEDEC VFC will correspond to theory.

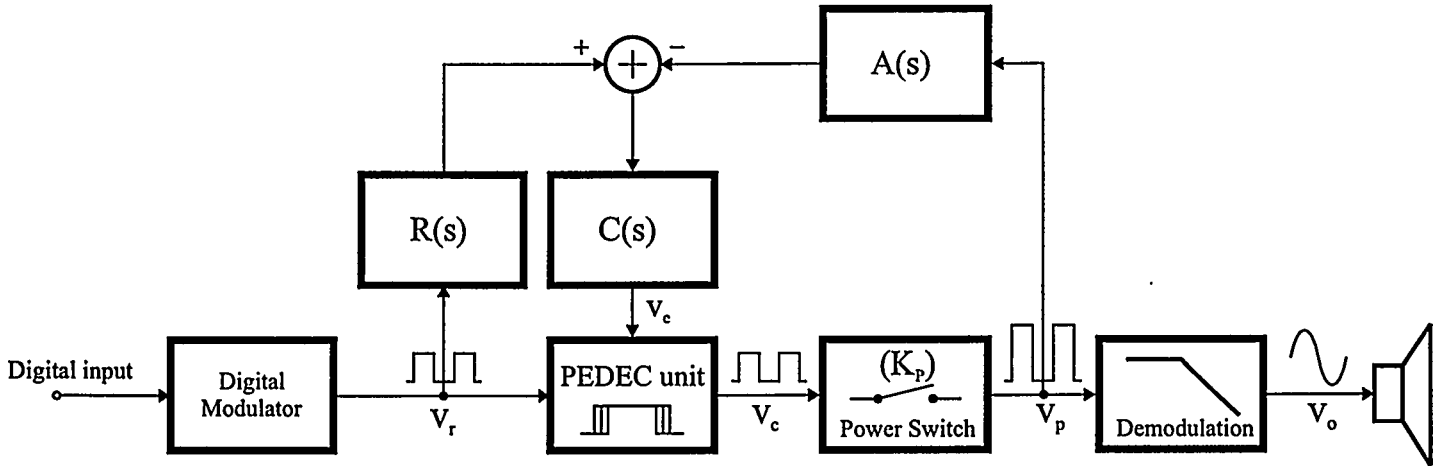


Fig. 9.18 PEDEC VFC2 Topology.

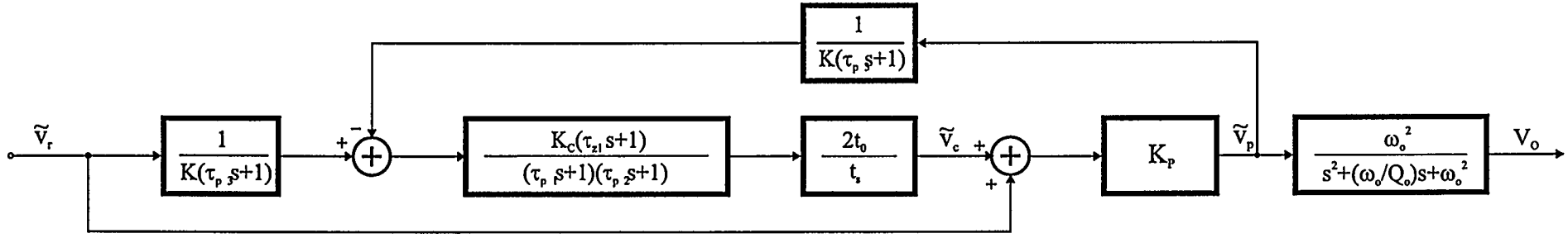


Fig. 9.19 Linear model of PEDEC VFC2 topology with all compensator elements defined. PEDEC VFC2 is characterized by first order error estimation.

9.5 PEDEC VFC2

Fig. 9.18 shows the general block diagram for PEDEC VFC2. The topology is closely related to VFC1, in that the feedback source is the switching power stage output. The significant difference lies in the error estimation, which is based on first order reference shaping in that the reference shaping block and feedback path compensator now have first order characteristics. The motivation of this modified error estimation is a simplification of the feedback block (in terms of bandwidth requirement). Recall that pulse modulated signals are inherently *analog*, so there are no essential advantages in maintaining the signals "digital" or pulse modulated at the difference point where reference and attenuated output are compared. On the contrary, it is of primary importance to optimize the estimation of *relevant* errors, i.e. the errors that are introduced in terms of distortion and noise within the audio band. Appropriate first order filtering on the pulse-modulated signal does not change this error estimation within the target frequency band.

9.5.1 Analysis

Fig. 9.19 shows the complete linear system model for the proposed PEDEC VFC2 controller. The individual components that constitute the topology are:

$$\begin{cases} C(s) = K_C \dfrac{(\tau_{z1}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)} \\ A(s) = K_P k_{PEDEC} \\ B(s) = \dfrac{1}{K}\dfrac{1}{\tau_{p3}s+1} \\ R(s) = \dfrac{1}{\tau_{p3}s+1} \end{cases} \tag{9.21}$$

Again, the proposed compensator $C(s)$ is a tradeoff compromise between loop shaping freedom and complexity. The reference shaper and feedback path compensator poles are matched for optimal error estimation. From Fig. 9.19, the resulting loop transfer is derived:

$$L(s) = \frac{K_C K_P k_{PEDEC}}{K} \frac{(\tau_{z1}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)} \tag{9.22}$$

The resulting loop transfer function is identical to VFC1. The resulting transfer function of the system is equally devised from the linear model in Fig. 9.19:

$$\begin{aligned} H(s) &= \underbrace{R(s)\frac{C(s)A(s)}{1+A(s)B(s)C(s)}}_{H_A} + \underbrace{\frac{K_P}{1+A(s)B(s)C(s)}}_{H_B} \\ &= \frac{K_P[R(s)C(s)A(s)+1]}{1+A(s)B(s)C(s)} \end{aligned} \tag{9.23}$$

The expression differs mainly from (9.17) in that the reference shaper influences $H_A(s)$.

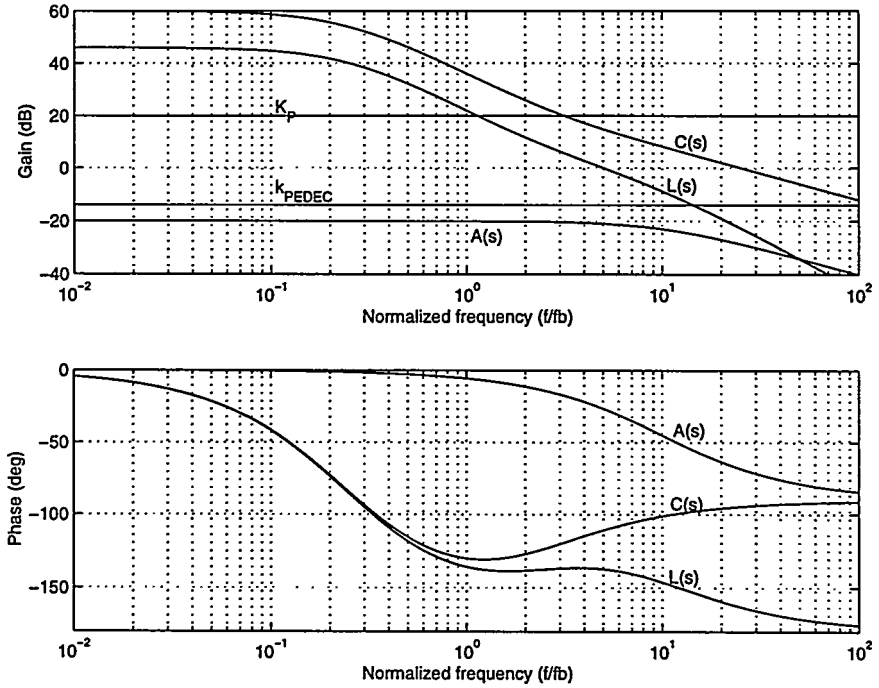


Fig. 9.20 Loop components and resulting loop transfer function of PEDEC VFC2 case example.

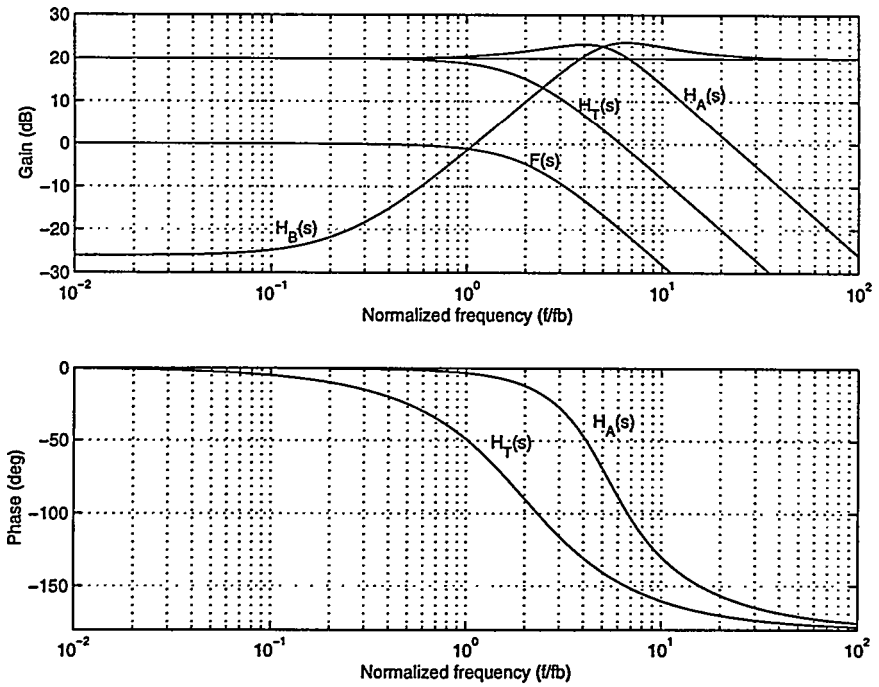


Fig. 9.21 Contributions to total system response for PEDEC VFC2

Assuming, that the pole $s=\tau_{p3}{}^{-1}$ is placed at a frequency well beyond the unity gain frequency of the control loop, the closed loop approximation will be as for VFC1:

$$H(s)\approx\begin{cases}K & (f<f_u)\\ K_P & (f>>f_u)\end{cases} \tag{9.24}$$

And $H_T(s)=H(s)F(s)$.

9.5.2 PEDEC VFC2 loop shaping

Despite the topological differences, the PEDEC VFC1 parameters also provide pleasant characteristics for PEDEC VFC2 topology. Since the loop transfer functions are identical, PEDEC VFC1 will be identical to PEDEC VFC2 in terms of performance and robustness.

9.5.3 Case example

A case example is considered with the same fundamental parameters as PEDEC VFC1. The results will only be discussed briefly, with focus on the differences to PEDEC VFC1.

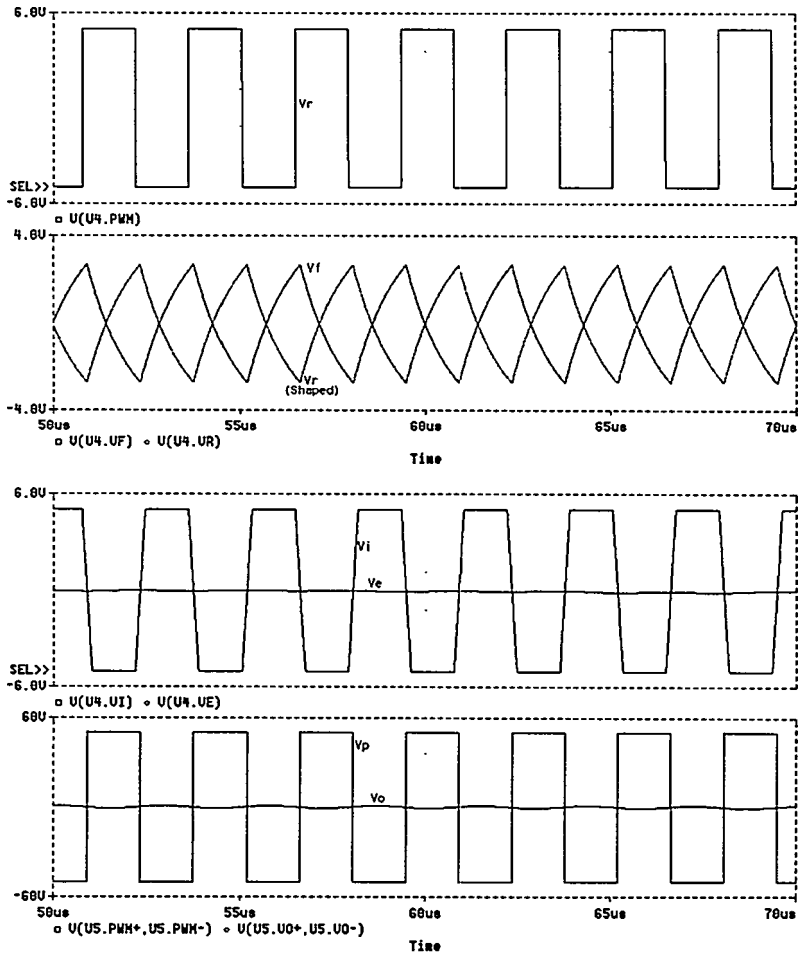


Fig. 9.22 Essential signals in the PEDEC VFC2 controlled system. From top to button - Pulse modulated reference, shaped reference and feedback v_f, PEDEC unit signals v_e, v_i and finally the resulting corrected power stage output.

Fig. 9.20 shows the resulting characteristics of the loop. Fig. 9.21 shows the resulting closed loop transfer functions. The reference shaping does not influence the transfer characteristics notably, since the pole is placed considerably above the loop bandwidth where the direct feedthrough path $H_{B,CL}(s)$ dominates the system characteristics.

The results of functional simulation of the system are shown in Fig. 9.22. Observe, how the reference and feedback path compensator are significantly different from PEDEC VFC1, as a consequence of the first order filtered error estimation. Note, how the error signal to the PEDEC unit is nearly free from HF components. VFC2 has been investigated on the same points as PEDEC VFC1 in terms of error correction, robustness and stability. The results are exactly as for VFC1, and the first order filtered error estimation does as such not compromise performance. As shown with the practical evaluation in Chapter 10, performance can be gained due to simpler controller implementation. To conclude, the investigations of the modified PEDEC VFC2 topology has shown that the error estimation may well be based on modified reference. In terms of compensator implementation, PEDEC VFC2 is clearly preferable compared to PEDEC VFC1.

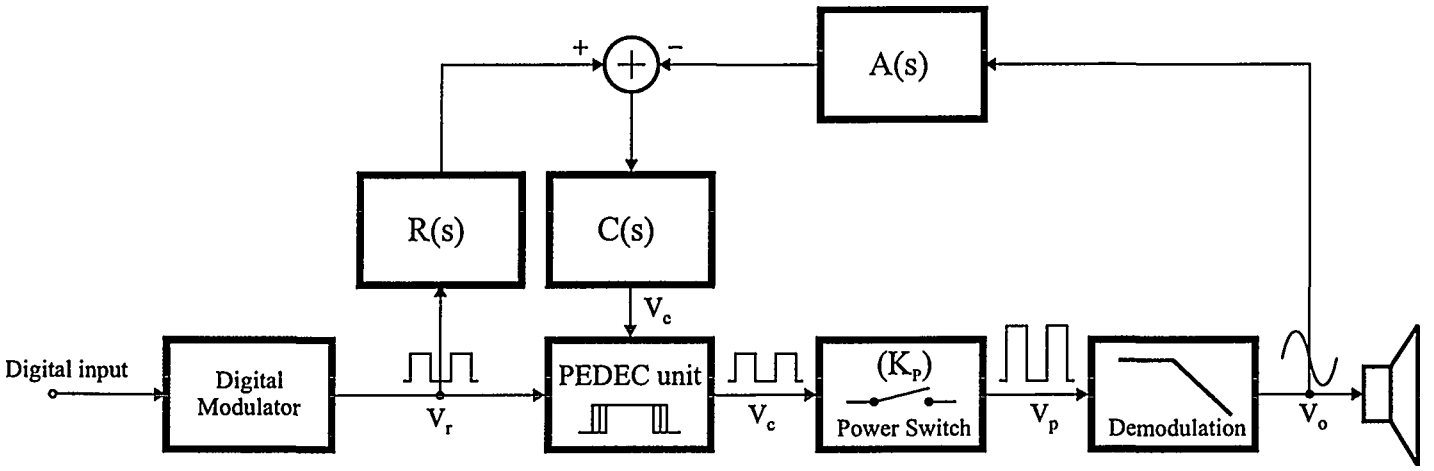


Fig. 9.23 PEDEC VFC3 Topology.

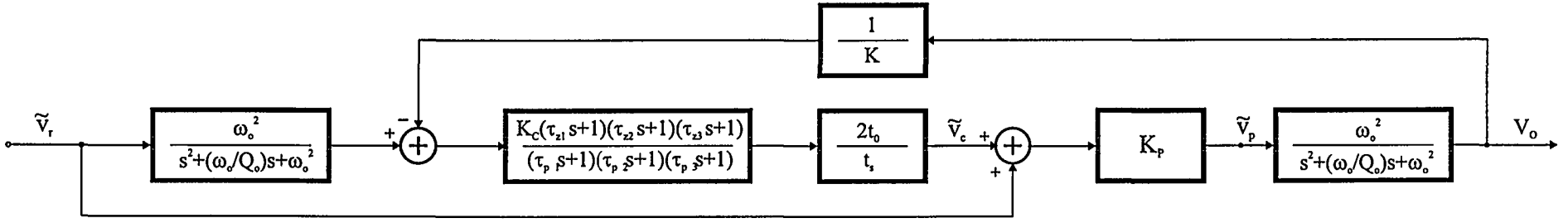


Fig. 9.24 Linear model of PEDEC VFC3 Topology with all compensator elements defined. The topology is characterized by global feedback and error estimation based on second order reference shaping.

9.6 PEDEC VFC3

Recall that PEDEC can be considered as a general control method for improved power amplification of a pulse-modulated signal. The generality of the principle means that it can be used advantageously in combination with a range of different control structures. To illustrate this generality, a global feedback topology, defined as PEDEC VFC3, will be investigated. A block diagram for the topology is shown in Fig. 9.23. For optimal error estimation, the reference should resemble the A-block best possible i.e. the R-compensator should match the second order demodulation filter, leading to second order reference shaping.

9.6.1 Analysis

The linear model for PEDEC VFC3 is shown in Fig. 9.24. The components of the controller are:

$$\begin{cases} C(s) = K_C \dfrac{(\tau_{z1}s+1)(\tau_{z2}s+1)(\tau_{z3}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)} \\ A(s) = K_P k_{PEDEC} \\ B(s) = \dfrac{1}{K} \\ R(s) = \dfrac{\omega_o^2}{s^2 + \frac{\omega_o}{Q_o}s + \omega_o^2} \end{cases} \tag{9.25}$$

This leads to the following loop transfer function $L(s)$:

$$L(s) = \frac{k_{PEDEC}K_C}{K_P} \frac{(\tau_{z1}s+1)(\tau_{z1}s+1)(\tau_{z1}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)} \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q_0}s + \omega_0^2} \tag{9.26}$$

The system transfer function is equally found from the linear model:

$$\begin{aligned} H(s) &= \underbrace{R(s)\frac{C(s)A(s)F(s)}{1+A(s)B(s)C(s)F(s)}}_{H_A} + \underbrace{\frac{K_P F(s)}{1+A(s)B(s)C(s)F(s)}}_{H_B} \\ &= \frac{F(s)K_P[R(s)C(s)A(s)+1]}{1+A(s)B(s)C(s)} \end{aligned} \tag{9.27}$$

9.6.2 PEDEC VFC3 Loop shaping

Except for the PEDEC unit, the loop is equivalent to the proposed linear VFC1 in Chapter 6. Subsequently, the loop shaping approach can be transformed directly to PECEC VFC3. The parameters are given in Table 9.3. The stability and robustness will be as the VFC1 in Chapter 6, under the assumption that PEDEC operates within the correction range.

Parameter	Value	Comment
$k_{PEDEC} = \frac{2t_o}{t_s}$	$\frac{1}{5}$	Equivalent PEDEC unit gain.
$f_{p1} = \frac{1}{\tau_{p1}}$	$\frac{1}{20} f_u$	Loop parameter
$f_{p2} = \frac{1}{\tau_{p2}}$	$\frac{1}{20} f_u$	Loop parameter
$f_{p3} = \frac{1}{\tau_{p3}}$	$3 f_u$	Loop parameter
$f_{z3} = \frac{1}{\tau_{z3}}$	$\frac{1}{3} f_u$	Loop parameter
$f_{z1} = f_{z2}$	f_o	Compensation of output filter
f_o	2	Demodulation filter / reference shaping filter
Q_0	$\frac{1}{\sqrt{3}}$	Q of reference and demodulation filter

Table 9.3 Proposed parameters for PEDEC VFC3.

9.6.3 Case example

The case example considered has $f_u = 5$. Fig. 9.25 shows the system the loop components and the resulting loop transfer function and Fig. 9.26 shows the response of the closed system. PEDEC VFC3 suffers from the requirement for a high compensator gain at high frequencies, which requires a wide-band controller.

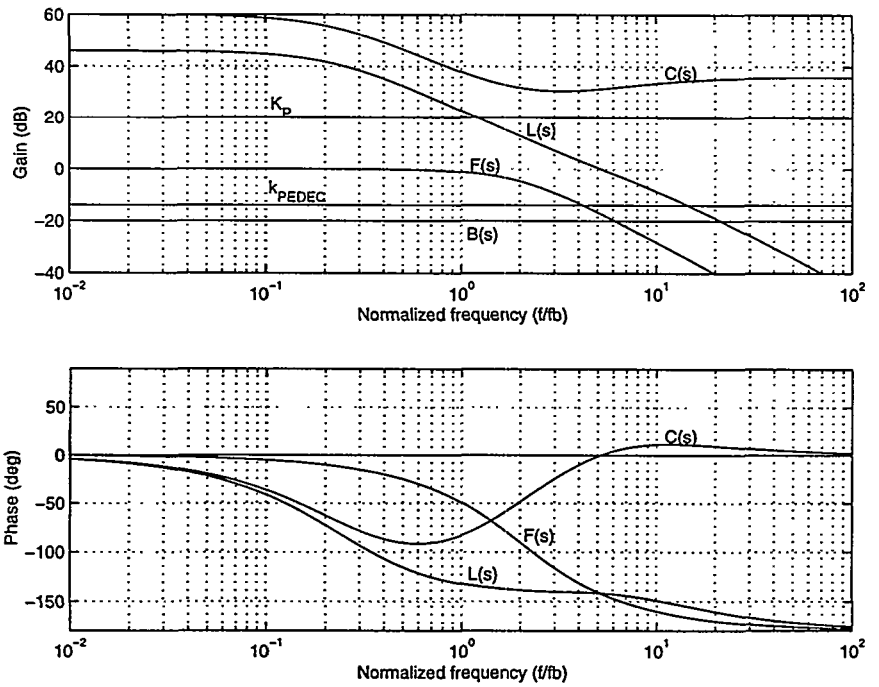


Fig. 9.25 Components for PEDEC VFC3 case example and loop transfer function $L(s)$.

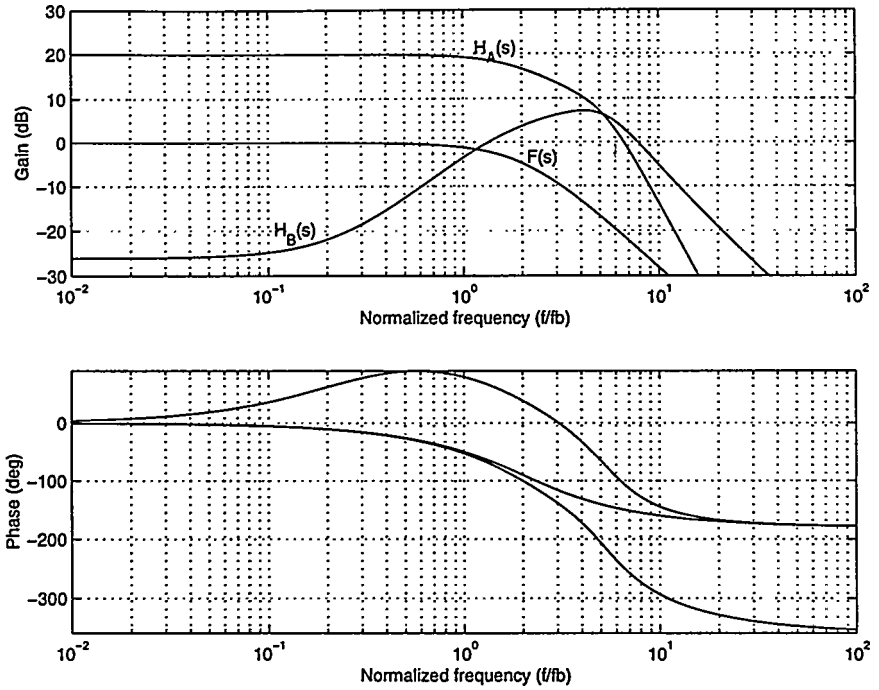


Fig. 9.26 Components of the system and the resulting system transfer function.

Non-linear simulation

Fig. 9.27 shows a simulation of the essential signals in the PEDEC controller in the idle situation. The simulation shows that the controller is stable and works as desired. Note, how the feedback signal v_f and the reference at the summation point has the opposite phase of the reference signal v_r at the summation point. A benefit of the second order reference shaping is, that the error control signal to the PEDEC unit has minimal HF-content. PEDEC VFC3 has been simulated using the same simulation sessions as for the other topologies. The controller works exactly as desired but there are special considerations and pitfalls when using this topology. A special consideration is, that the reference shaper should match the demodulation filter reasonably, in order to minimize the correction space needed to compensate for such a mismatch. The general error correction capability corresponds has been found to correspond with theory. Fig. 9.28 shows the simulation of PTE error correction.

9.7 Extensions

Due to the minimal pulse width constraint, three-level (BD) PWM schemes are not directly applicable in combination with PEDEC. Some changes in the basic system topology is needed, i.e. a PEDEC controller is needed for each of the modulators driving the two half-bridges. An area of future research is to develop PEDEC controllers for alternative modulation methods as three level systems. Furthermore, only three simple control methods have been presented in this chapter to illustrate the general characteristics of PEDEC. Other control systems may be investigated if the correction offered by the three proposed topologies is not sufficient. Finally, the issue of PEDEC unit realization is a field of its own. Other control functions may be investigated, e.g. non-linear control functions. Furthermore, alternative realizations of the linear control function are an area of future research, although the non-linear simulations suggest that the approach is very feasible.

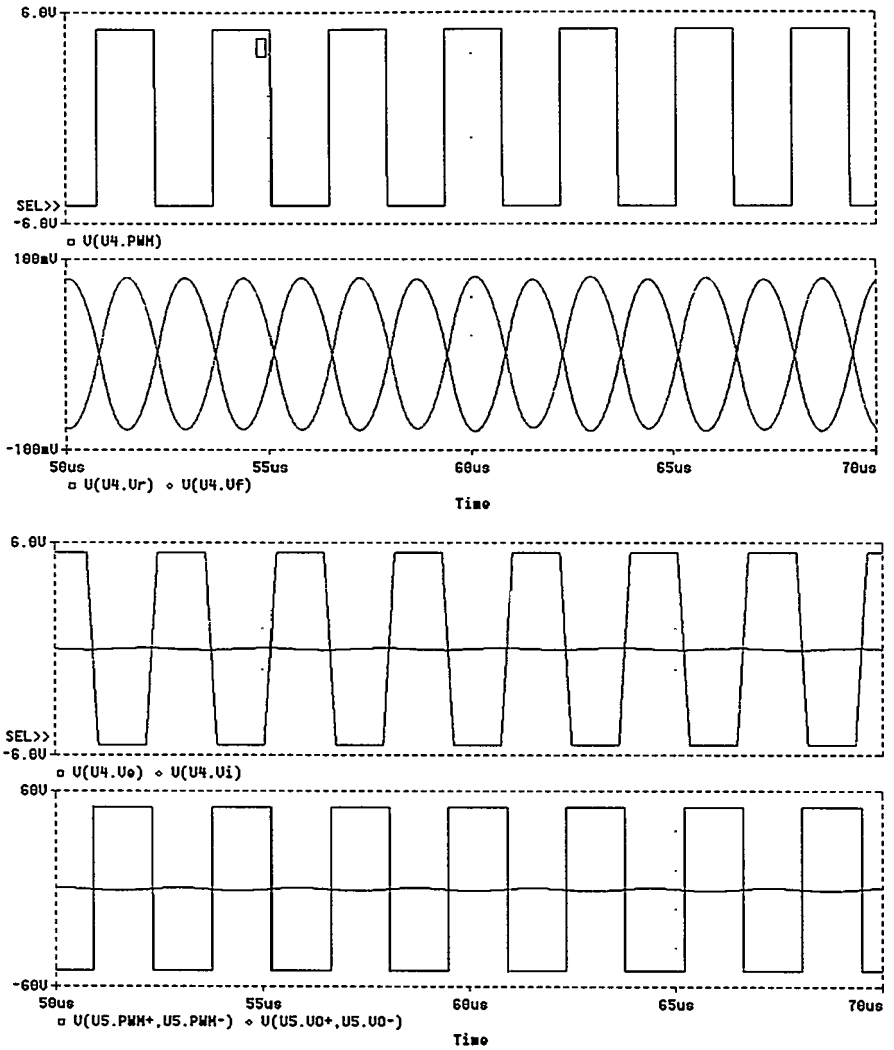


Fig. 9.27 Functional simulation of PEDEC VFC3. From top to button – Pulse modulated input, feedback v_f and shaped reference v_r, then v_i and the error signal v_e and finally the compensated power stage output signals.

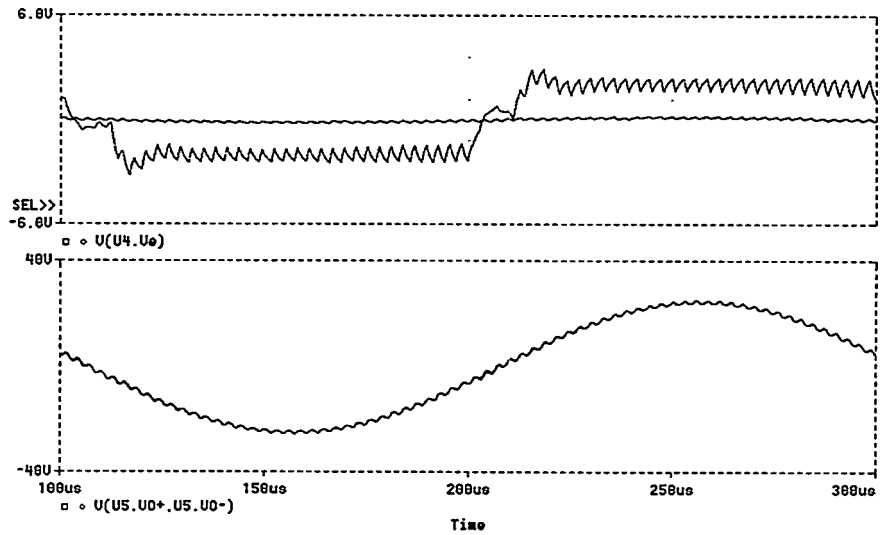


Fig. 9.28 Simulation of PEDEC VFC3 system with t_D=*0ns* and t_D=*100ns*. f=5KHz. M=0.5. Both the linear gain error and distortion are reduced (bottom= v_o). The controller reduces THD by 25dB. The anti-distorting PEDEC unit input v_e (top) clearly shows the nature of the distortion.

9.8 Summary

This chapter has been devoted to the complicated issue of error correction in systems without an analog LF reference. A novel pulse referenced error correction principle – Pulse Edge Delay Error Correction (PEDEC) – has been proposed. The method uses a pulse modulated signal as reference for error correction, and performs a re-timing of the pulses edges to compensate for power stage and filter errors. PEDEC was first introduced as a general method for enhanced power amplification of a pulse modulated signal. The desired linear control function was defined and a method of realizing this control function by a PEDEC unit was presented.

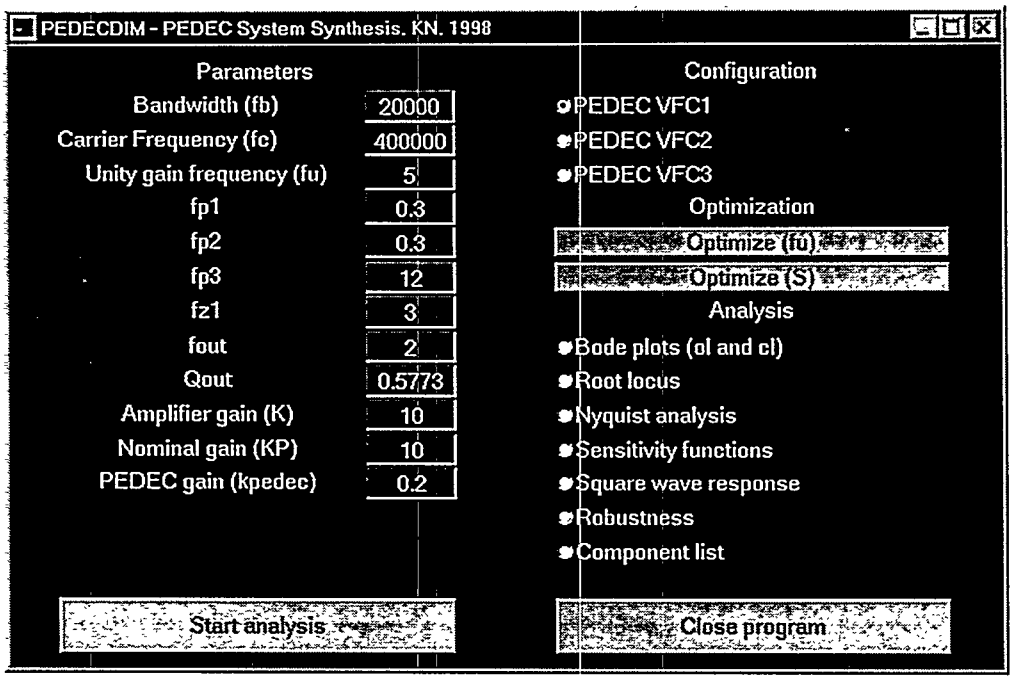
Three simple PEDEC based PMA topologies were proposed with different characteristics in terms of error estimation and feedback source. Loop shaping was addressed, and illustrated by example for the three digital PMA topologies. All topologies proved to realize a significantly reduced sensitivity to any error source existing in a switching power amplification stage. It is concluded, that PEDEC has several interesting properties, some of which are somewhat different from other error correction systems. Three important properties are outlined below:

- *Simplicity.* The proposed system is build of simple linear active components and by resistors and capacitors, causing only a marginal increase in complexity and cost compared to a non-controlled system.
- *Performance.* PEDEC controller can correct all error types and equally important - the improvements are easily *controlled* with the system model.
- *General pulse referenced control scheme.* The inherent pulse referenced nature of the control system leads to an interesting independence of modulation method.

Based on the detailed investigation in both time and frequency domain of the principle, PEDEC is concluded to be a simple and efficient approach to power stage error correction, which makes the realization of high quality digital PMA systems more practical.

9.8.1 PEDECDIM - GUI based PEDEC design toolbox for MATLAB

A GUI controlled MATLAB toolbox for systematic, automated and consistent design of PEDEC based digital PMAs has been developed. The graphical user interface is shown below:



Clearly, the interface has some similarity with LCONDIM and MECCDIM, and PEDECDIM fundamentally has the same functionality. Based on the primary amplifier input parameter specifications the interface gives access:

- PEDEC control system synthesis and verifications.
- Controller component synthesis for low-level non-linear simulation.
- Manual access to individual parameters for individual fine-tuning

Part IV

Chapter 10

Practical Evaluation

This chapter is devoted to the practical evaluation of investigated principles and topologies. All considered topologies have been implemented and optimized in hardware, generally using careful layout with SMT technology and multi-layer PCB's. The implementation phase is important, since several aspects simply cannot be investigated mathematically or by simulation. A few of important issues that can only be investigated on a physical hardware prototype are:

- Actual power stage linearity and noise characteristics.
- Efficiency measurement and optimization. As mentioned in Chapter 5, accurate modeling of power dissipation in switching power stages is impossible. Measurements are necessary for exact specifications on efficiency and energy efficiency.
- Limitations caused by controller components, e.g. noise, linearity or bandwidth.
- Limitations caused by e.g. switching noise superposing control variables.
- Undesired coupling paths e.g. between the power stage and modulator section, caused by e.g. poor PCB layout of the power conversion stage. The high *di/dt* and *dv/dt* in the power stage requires use of HF design techniques.
- EMC/EMI aspects.

Practical documentation for all the implemented systems would require a comprehensive report. The following will mainly focus on the essential results and conclusions that have been drawn on the feasibility study of the individual topologies. The observed performance of the hardware prototypes will be compared with the theoretically expected performance, and specific advantages and disadvantages will be emphasized.

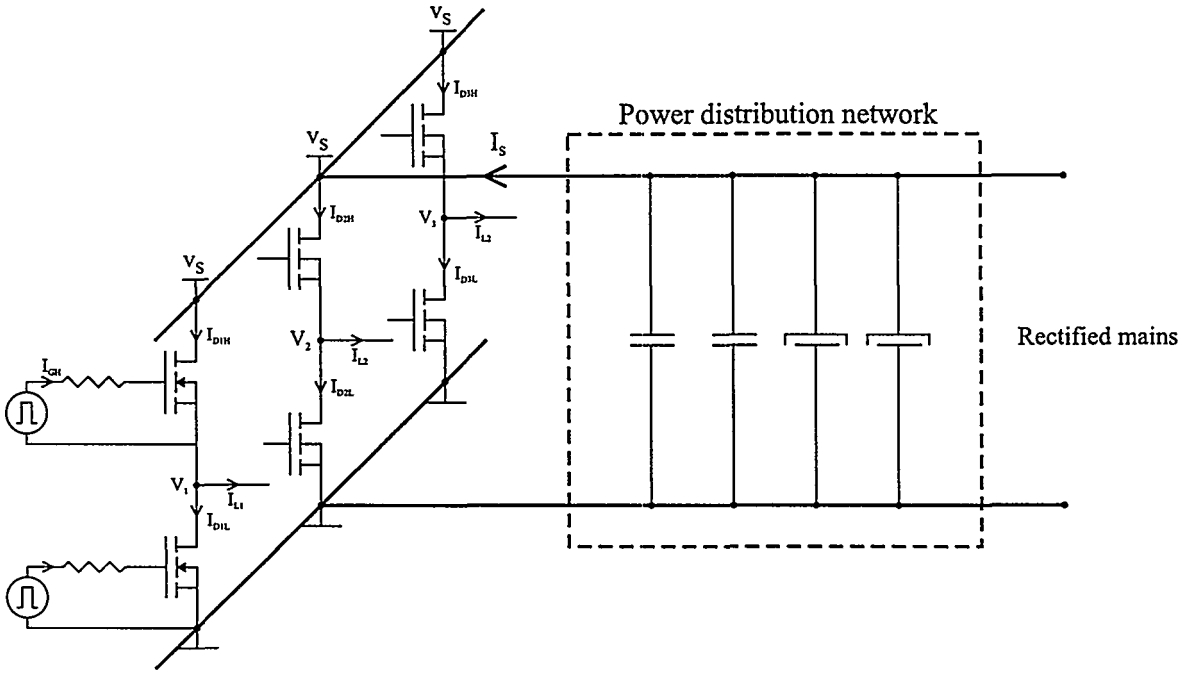


Fig. 10.1 General power stage, consisting of switching leg building blocks and a power distribution network.

10.1 Power Stage Implementation

The modulator, driver and power stage are crucial elements in the system. A carefully designed circuit and layout is essential to achieve the expected system performance and efficiency. The demands on power stage design increase with amplifier power handling capability. In recent years, the field of power switching devices and driver circuitry has seen much progress. This has made the realization of power conversion stages for PMAs practical. Some important issues and considerations regarding power stage design will be addressed in the following.

10.1.1 The switching leg building block

General PSC and BPSC power stage design can be decomposed into the optimization of each individual switching leg as shown in Fig. 10.1. Essentially, all paths in the switching output stage are critical. The switching of currents between output devices in each switching leg leads to immense di/dt in the drain and source connections of the switches. Also, the gate to source current path is a switching circuit although the currents are lower. Only the output current *di/dt* is limited, since each switching leg feeds an inductor.

To understand the design problem, it is illustrative to consider a case example where:

$$t_{lr} = t_{lf} = 10ns \tag{10.1}$$

Assume, that the maximal peak current to the load is $\hat{I}_L$=10A, corresponding to the general 200W case example that has been considered throughout the thesis. In this case the current derivative is:

$$\frac{di}{dt} = 1000A/\mu s \tag{10.2}$$

This current derivative is present in all of the above mentioned critical paths in the output stage. This immense current derivative will inevitably cause a resonant action between the parasitic inductance and the parasitic capacitance's (e.g. the output capacitance of the switches). There are more solutions to minimize this effect:

- Reduce the current in the switching leg.
- Reduce the worst-case current derivative.
- Minimize the Q of the parasitic resonant circuits.
- Minimize the parasitic capacitance and inductance.

The first and second solution will inevitable introduce additional power loss and less ideal switching, since the ideal switching transition from the perspective of minimizing both distortion and power dissipation is infinitely fast. The third remedy however, is possible by optimized circuit layout. Subsequently, the essence of PMA power stage design is:

- Minimize the parasitic inductance in each individual switching leg to a minimum.
- Design the power distribution network to cope with the current requirements in terms of both current magnitude and current bandwidth.

10.1.2 Power distribution network considerations

All switching legs "share" the power distribution network, as shown in Fig. 10.1. The output impedance of the distribution network has to be sufficiently low over the frequency range where significant current components are required. Otherwise, undesirable HF perturbations will be introduced on the power rail V_S.

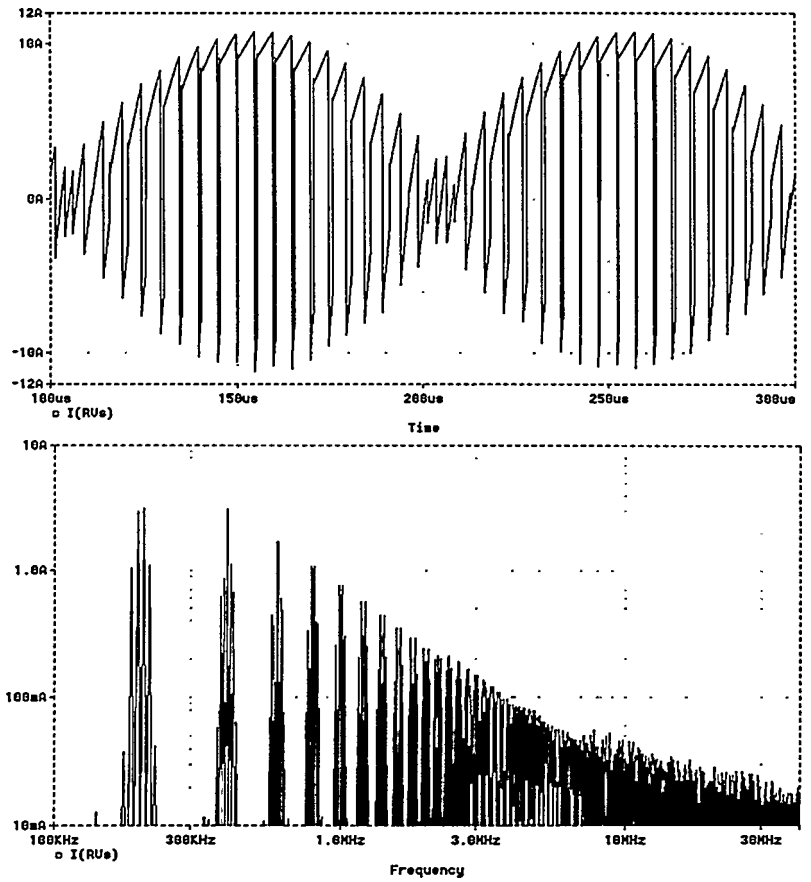


Fig. 10.2 Current requirements from the power distribution network shown in both time and frequency domain for a bridge implementation of **NADD** (N=2). Output power = 200W.

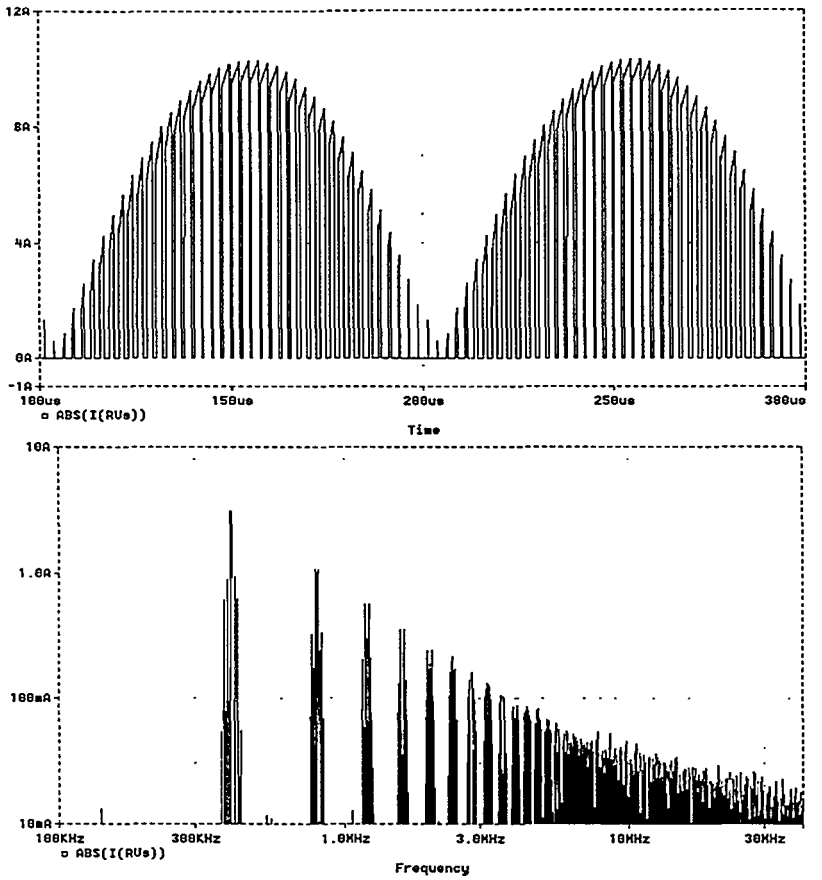


Fig. 10.3 Current requirements from the power distribution network shown in both time and frequency domain for a bridge implementation of **BND2 PSCPWM** (N=2). Output power = 200W.

The current requirements varies significantly with the number of switching legs N. Furthermore, the requirements are different for the PSC and BPSC topologies. Fig. 10.2 and Fig. 10.3 compares the supply current I_S for the fundamental NADD and BND2 (N=2) PSCPWM modulation schemes. I_S is constituted of:

- A rectified version of the signal current.
- HF current components that relates to harmonics of the carrier and intermodulation components between signal and carrier.

There are many similarities between the differential HF output of PSCPWM and the current requirements from the power distribution network, i.e. the harmonic elimination is seen also seen on I_S as N increases. This effect is seen when comparing Fig. 10.2 and Fig. 10.3. For three-level PSCPWM scheme (that corresponds to NBDD), the output current is chopped at twice the frequency. The frequency domain analysis clearly illustrates the harmonic elimination.

To prevent significant perturbations on V_S and EMC problems, it is essential that the power distribution network is able to deliver the current components required. The problem of designing a proper distribution network is a problem of network analysis. For the simple switching leg, the power supply frequency spectrum will have a first order characteristic from the fundamental switching frequency f_c up to the corner frequency [Ma96b]:

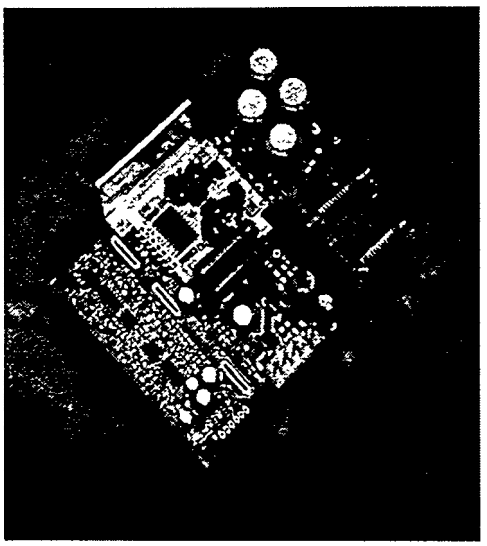


Fig. 10.4 Optimized power stage realization (N=2) on a ceramic substrate (Hybrid IC). The IC is integrated in 250W/8Ω MECC based PMA system.

$$f_{Ic} \approx \frac{0.35}{t_{Ir}} \tag{10.3}$$

The corner frequency of the supply current becomes:

$$f_{Is} \approx 35MHz \tag{10.4}$$

The current components will decrease with a second order characteristic beyond f_{Ic}. A well-designed power distribution network should represent the lowest possible (preferably lossy) impedance from DC to this frequency. This is carried out by parallel connecting de-coupling capacitance, as shown in Fig. 10.1. The capacitors should be considered as parallel coupled series resonant circuits, and the design task is to meet the impedance requirements by carefully selecting the de-coupling capacitors.

10.1.3 Hybrid IC – Optimized power stage realization

The optimal realization of high power switching power stages has been investigated, to research in the limits on achievable performance. Although much can be gained by proper layout using HF design techniques, the current paths are inevitable constrained by the inherent parasitic inductance within the connectors, bonding wires and connecting PCB tracks. Subsequently, it has been attempted to eliminate this fundamental constraint by realizing the complete power conversion stage (two switching legs in a bridge configuration) on in a hybrid IC. The result is an extremely compact power stage realization as illustrated in Fig. 10.4, where the IC is shown integrated in a complete PMA system. With a reduction in parasitic inductance to a few nH, the resulting switching waveforms are close to the ideal. The significant improvement in HF characteristic were observed in practice within thee system since coupling effects are minimized to an absolute minimum, allowing close integration of modulator, control system and power stage. Linearity, noise etc. are not inherently improved compared to a discrete system, since blanking effects and power supply perturbations, modulator noise etc. is not solved by optimal power stage realization. Most error sources are fundamental, and will exist independent upon implementation technology.

10.1.4 Power stage performance

This will be illustrated by investigation a non-controlled 300W/8Ω bridge power stage (BPSC with N=2), with the following parameters.

Parameter	Description
Modulation method	NADD
V_S	80V
f_c	350KHz

Fig. 10.5, Fig. 10.6 and Fig. 10.7 shows THD+N vs. output power, swept from 100mW - 300W for the three cases $t_d = 30ns$ (low), $t_d = 70ns$ (typical), and $t_d = 100ns$ (high). At lower levels, THD+N is exclusively dominated by the noise (RMS ≈ 1mV). The primarily noise source in the test circuit was the carrier generator which produces audio band noise that is amplified by the power stage. However, the intention here is primarily to verify the theoretically estimated relationships between blanking delay and output distortion. The investigations verifies the theoretical expected characteristics and parametric dependencies (see Chapter 4)

- The power stage distortion is relatively constant with frequency. At 10KHz however, the harmonics are attenuated by the filter yielding a lower distortion on the output.
- Blanking introduces a significant contribution to power stage distortion. This is especially observed with $t_d = 100ns$.
- The ripple current cancels the effect of blanking at lower output levels.

The following was measured on the power stage:

	THD @20W	P_Q
$t_d = 40ns$	0.1%	25W
$t_d = 70ns$	1.3%	2W
$t_d = 100ns$	4%	1.2W

At $t_d = 100ns$, both the characteristic of THD+N vs. output power and the absolute value of distortion correspond very well with theory, with a blanking delay factor of $\alpha_d = 0.035$. The distortion below the $I_L = I_T$ breakpoint is not zero due other contributions. With lower blanking delays, the distortion characteristics dramatically change to the better. Note, that THD is reduced 30dB (!) with a blanking delay factor $\alpha_d = 0.014$, much better than expected. The explanation lie in the much improved distortion characteristics that shoot-through introduces. With significant shoot-through, the switching characteristics will be nearly unaffected by the load current – correspondingly the correlation between load current and switching action is reduced and harmonic distortion reduces correspondingly (but audio band noise increases slightly). The price however is high, in terms of a clearly unacceptable 25W power dissipation at quiescence. The limit of performance with the present power stage was found to be 0.02% THD+N with a blanking delay of 30ns or $\alpha_d = 0.01$.

The practical evaluation of the bridge power stage has documented some of the theoretically expected characteristics. The compromise between power stage linearity and efficiency / energy efficiency has been illustrated.

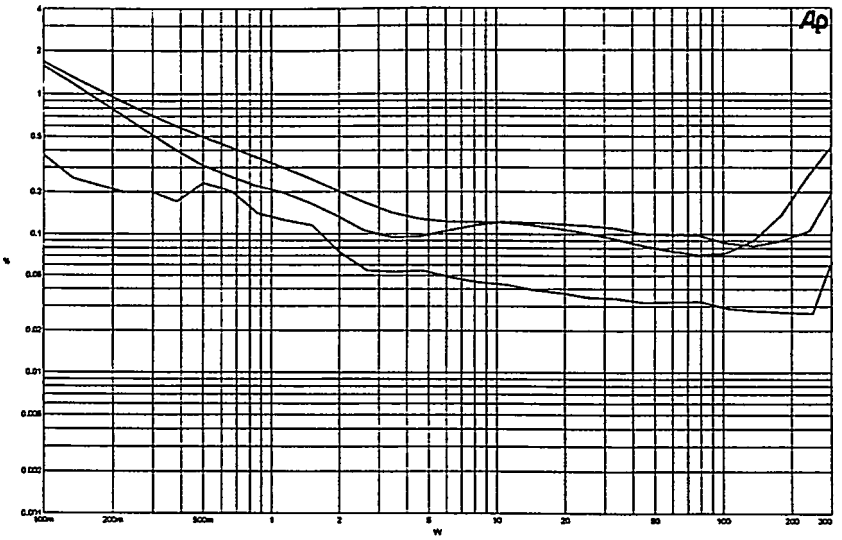


Fig. 10.5 Non-controlled PMA THD+N vs. Po (100Hz, 1KHz, 10KHz). $t_d = 40ns / \alpha_d = 0.014$.

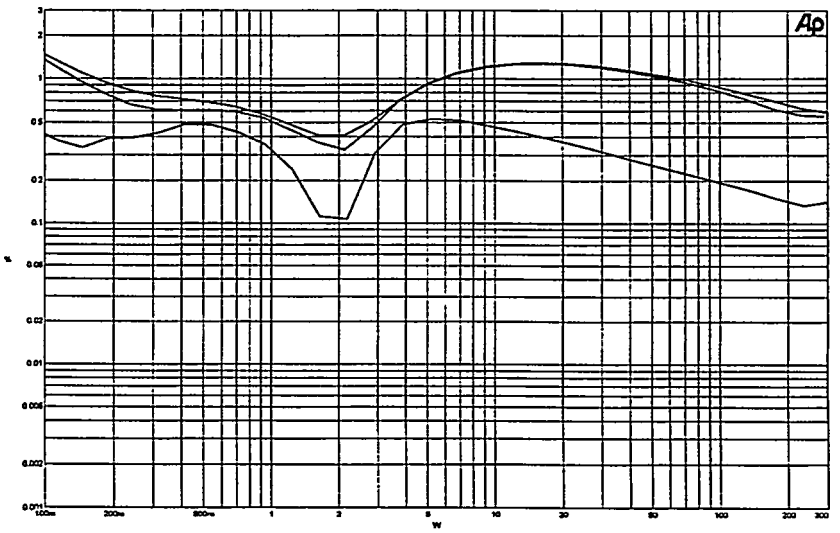


Fig. 10.6 Non-controlled PMA THD+N vs. Po. (100Hz, 1KHz, 10KHz). $t_d = 70ns / \alpha_d = 0.024$.

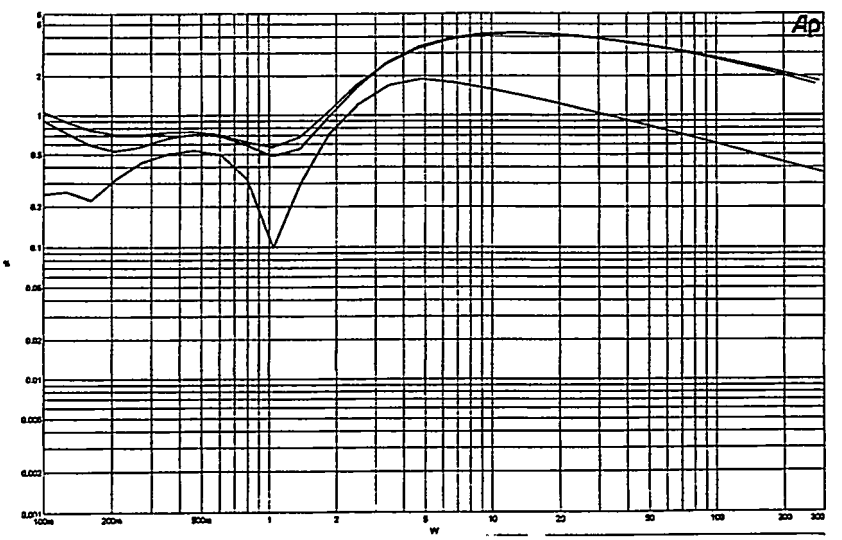


Fig. 10.7 Non-controlled PMA THD+N vs. Po. (100Hz, 1KHz, 10KHz). $t_d = 100ns / \alpha_d = 0.035$.

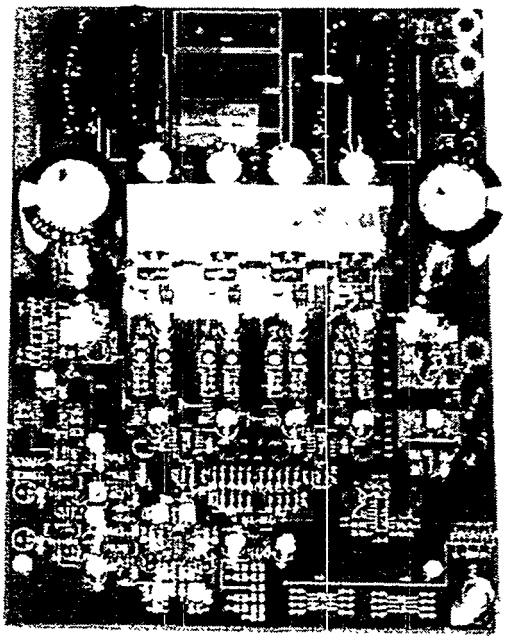


Fig. 10.8 BPSC power stage with four switching legs (N=4) and four summing inductors for open loop evaluation of 5-level Balanced PSCPWM methods (BND1, BND2 and BND3).

10.2 PSCPWM Evaluation

As illustrated in Chapters 3 and 4, PSCPWM [Ni97b] provides both improved modulation and higher efficiency. The potential of PSCPWM has been investigated in various high power systems [Ch98]. The focus has been on the BPSC topology due to the advantages in terms of single supply operation and breakdown voltage requirements. The implementation of the fundamental PSCPWM principle (BND1) will be demonstrated by considering an 500W power stage. All double-sided methods BND1, BND2 and BND3 have been successfully implemented with comparable results. As introduced above, each individual switching leg can be designed individually. PSCPWM power stage realization is as such relatively simple and straightforward and this flexibility in power stage design is a desirable feature. In this particular case, 100V switching technology has been used in the power stage. The essential parameters are outlined below.

Parameter	Description
Max. output power	500W / 4 Ω
Modulation method	BND1
N	4
V_S	70V
f_c	150KHz
L_N	27 μH
$\hat{I}_{O,\max}$	16A
$\hat{I}_{LN,\max}$	8A

It was found that the most significant noise generator resided from the carrier generators. The noise source will be reduced considerably by a control system.

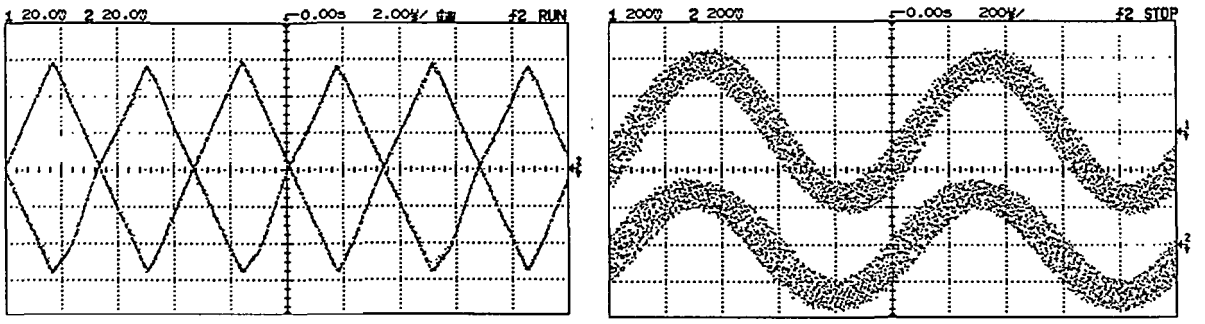


Fig. 10.9 Currents in summing inductors at quiescence (left) and at 500W (right). Scale 200mV = 8A. Offsets are forced on the currents at 500W, and there is no DC current flowing between switching legs.

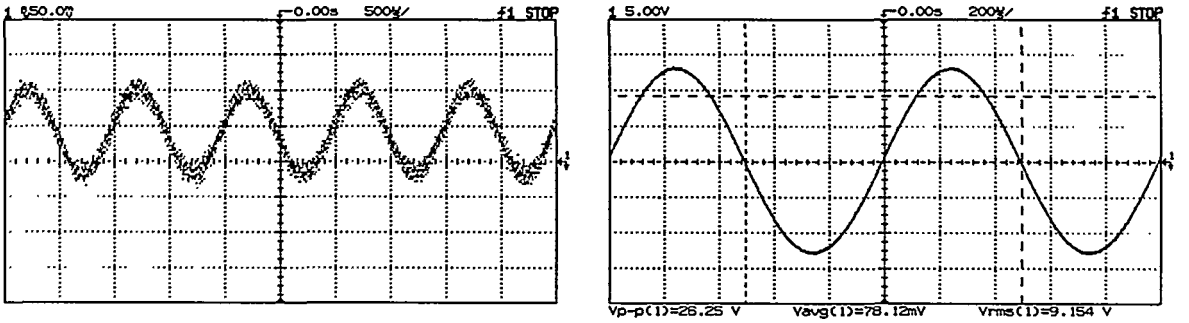


Fig. 10.10 10mW RMS output (left) and 500W RMS output (right). Scale on probe 1:5. The harmonic cancellation offered by PSCPWM is obvious, since no switching components are visible on the resulting output although the carrier frequency is as low as 150KHz.

Fig. 10.9 shows the currents in two of the summing inductors at quiescence and at 500W power output. Measurements have verified that the current characteristics in the other two summing inductors the same. Clearly, the ripple currents have the opposite phase as the BND1 control algorithm specifies. Fig. 10.10 shows PMA output near quiescense (at 10mW) and at 500W output. These fundamental investigations verifies the concept of PSCPWM:

- The currents divide as desired between summing inductors, and there is no circulating current flowing in the summing inductors.
- The output is close to perfectly demodulated although the carrier frequency is only 150KHz in each switching leg. The harmonic cancellation of PSCPWM, leading to both improved efficiency and superior modulator performance is a reality in practice!

The residual switching ripple at idle operation is about 10mV RMS. This corresponds to more than 40dB reduced switching amplitude compared to a simple switching leg implementation. Fig. 10.11 shows the distortion characteristics of the 5-level BND1 PSCPWM output stage, with blanking delays optimized to a very acceptable 4W of idle loss (no shoot-through). The residual output noise open loop is about 1.5mV, corresponding to the THD+N measured at lower output powers. The measured distortion is highly acceptable for a non-controlled output stage, and this verifies that PSCPWM does not compromise audio performance, compared to switching leg or bridge implementations of the output stage.

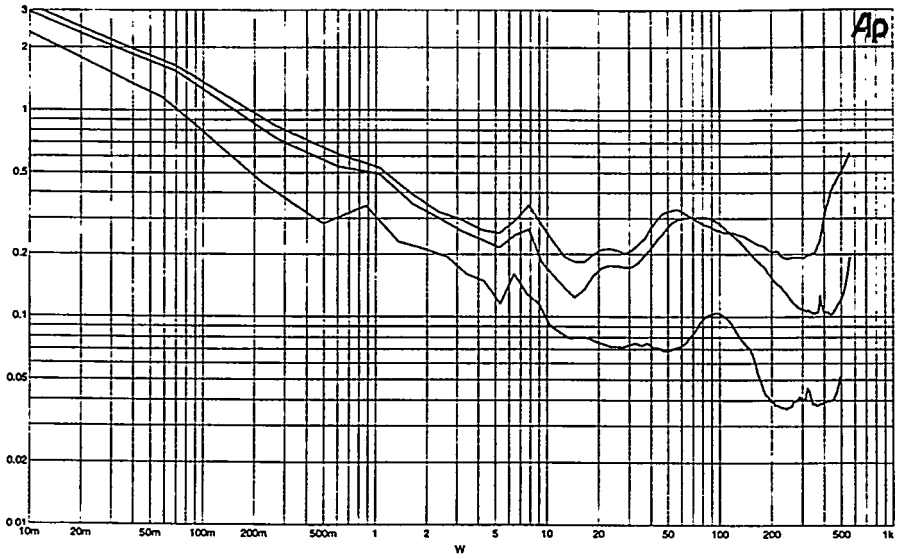


Fig. 10.11 THD+N vs. output power (100Hz, 1K, 10K) for the non-controlled 500W PSCPWM power stage synthesizing BND1.

The resulting specifications that have been measured on the non-controlled PSCPWM output stage (without error correction) are summarized below:

THD+N @ 1W/1KHz	0.3%
THD+N (1W-500W)	0.05%-0.5%
Residual noise 20Hz-20KHz (unw.)	1.5mV RMS
Efficiency	96%
Idle power dissipation	4W

The measured efficiency is in excellent correspondence with the estimation provided by theory (Chapter 5), using the Power Stage Optimization Tool. The idle power dissipation is a bit higher than expected, due to the tradeoff between audio performance and losses at quiescence.

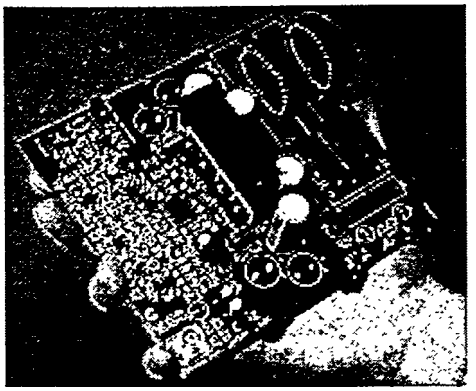


Fig. 10.12 200W VFC2 prototype (NBDD, 4KHz).

10.3 VFC1/VFC2 evaluation

VFC1 has been evaluated in [Ha97] in a dedicated 500W application. The results verify that it is difficult to achieve the desired performance specifications with VFC1. This corresponds well with the documented limitations (see Chapter 6). The main problem relates to the realization of the compensator, which requires a high bandwidth control element can realize a high gain at high frequencies. Furthermore, there is the trivial limitation of single loop compensation in terms of achievable S_M within a given bandwidth.

The VFC2 topology has been investigated in [Ni96] for dedicated applications. A dedicated VFC2 based PMA concept has been developed for active speaker systems specifically. The concept is optimized to realize the highest possible energy efficiency in active speaker systems. Fig. 10.12 shows the implemented prototype. The concept is based on a switching frequency of only 44.1KHz, independent of bandwidth. The low carrier frequency provides a high open-loop linearity, i.e. a simple control method is feasible. For further details on the selection of parameters, see [Ni96]. The essential system parameters are summarized below:

Parameter	Value
V_S	50V
f_b	< 4 KHz
f_c	44.1 KHz
f_u	10
f_o	1

Two high power examples have been developed to demonstrate the performance. The essential specifications are summarized in Table 10.1. Detailed measurements on the two implemented examples are given in [Ni96]. Fig. 10.13 shows the measured THD+N for example two at selected output levels. Example 2 shows reasonable distortion varying from very low levels up to 0.1% at maximum continuos output power. The continuous power is specified at 200W for both examples, although very good distortion figures (determined by the post filter mainly) were obtained up to the clipping level at approximately 300W where distortion rapidly rises to 1%. In general, the maximal power level can simply be changed by changing the supply level. On of the advantages of PMAs, is this tremendous flexibility to change in the output power capability without changes in the construction other the power supply level. Further specifications are given in [Ni96].

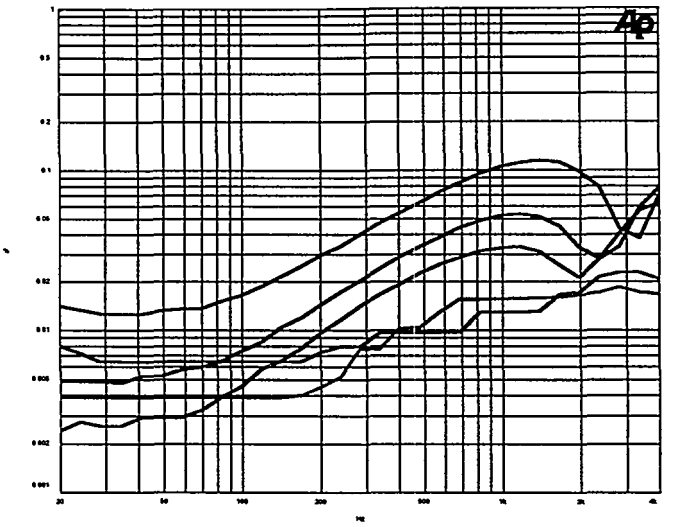


Fig. 10.13 THD+N vs. frequency for Example 2.

To conclude, VFC2 proves to provide satisfying performance in dedicated, bandwidth limited dedicated applications with defined load impedance and a minimal carrier frequency (good open loop linearity). The local feedback is very effective in linearizing the output stage, and the major concern in these applications is thus filter volume, linearity and filter efficiency.

	Example 1	Example 2
Bandwidth	700Hz	4KHz
Modulation strategy	NADD	NBDD
THD+N (complete operating range)	<0.1%	<0.15%
Residual noise (unw)	60µV RMS	120µV RMS
Dynamic range (unw)	115dB	108dB
Idle consumption – Total	1.5W	1.5W
Max. power stage efficiency	96%	96%
System efficiency	92%	94%
Energy efficiency	20%	20%
Estimated energy savings	>90%	>90%

Table 10.1 Examples of dedicated PMA concept for active speaker systems [Ni96].

10.4 CVFC Evaluation

CVFC has been investigated with the implementation of a 200W prototype for the full audio band [An96]. NBDD was chosen as modulation method for the implementation to minimize the loop bandwidth to carrier frequency ration. The table below summarizes the important parameters:

Parameter	Value
V_S	70V
f_b	20 KHz
f_c	315 KHz
f_{uc}	10
f_{uv}	5
f_o	1
M_{max}	0.85

At this point of CVFC implementation, robust design was not fully developed and the parameters in the investigated system were thus slightly different that the parameters that were proposed in Chapter 6. These small indifferences do not change on the resulting conclusions. The power supply level of 70V corresponds to a maximum modulation index of 0.85. As documented in Chapter 6 the CVFC topology excels by the stability to perturbations on the filter Q, i.e. in stability to load variations. This has been verified in practice [An96].

THD+N versus frequency is measured at four output powers levels increasing from 40mW to 200W in Fig. 10.14. The distortion and noise characteristic are concluded to be reasonable. However, the measured specifications required a low blanking delay, compromising efficiency and idle losses. Thus, the idle power loss is 12W. The table below summarizes the obtained amplifier specifications:

Max. power (continuous)	200W
THD+N (complete range)	<0.15%
Residual noise (unw)	90μV RMS
Dynamic range (unw)	113dB
Idle consumption – Total	12W
Maximal efficiency	90%

The prototype has not quite realized the theoretical performance potential of the CVFC topology. In conclusion, the CVFC has proved both advantages and disadvantages:

- Acceptable performance in terms of distortion and noise, however noiseless current measurement is problematic.
- The system has excellent stability to load variations, corresponding well with theory (see Chapter 6).
- Efficiency is compromised by e.g. current measurement and the requirement for high open linearity to reach the desired specifications.

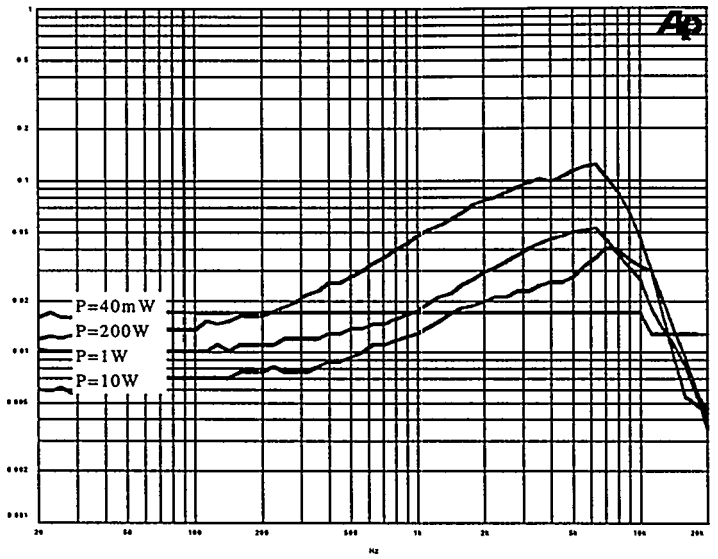


Fig. 10.14 THD+N vs. frequency and output power for the full bandwidth CVFC realization.

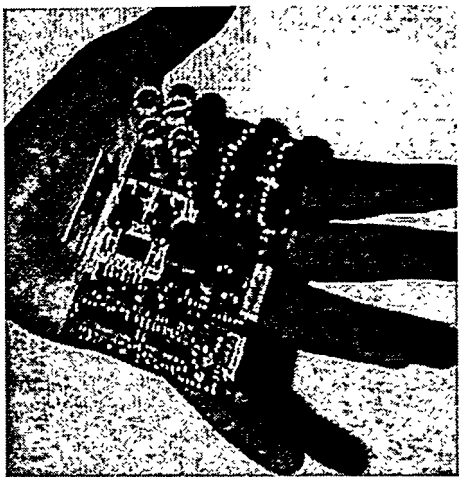


Fig. 10.15 MECC based 250W/8Ω PMA prototype for the full audio bandwidth.

10.5 MECC evaluation

Recall from chapter 7 that the MECC topology provides flexible control of the PMA system, such that the design of the complex power stage and demodulation filter blocks can be relaxed. The performance of MECC will be demonstrated by a simple MECC(1,1) realization [Ni97a] of a 250W system for the full audio band. The system is based on the hybrid IC power stage that has been tuned to maximize efficiency and energy efficiency, i.e. the open loop THD approaches 2% worst case. NBDD PWM has been chosen for implementation to maximize the control bandwidth to carrier frequency ratio, and minimize the noise on controller variables. The second order loop prototype has been chosen for the implementation (see Chapter 7). The general parameters for the case example are defined below.

Parameter	Assignment
V_S	70V
K	26dB
t_d	70ns
f_b	20KHz
f_c	300KHz
N	1
M	1
f_{uN}	10
f_{uM}	4

Fig. 10.16 illustrate THD+N vs. output power for 100Hz, 1KHz and 10KHz. Generally, the performance corresponds well with the theoretical expected performance with the given parameters. However, at higher output levels the control system gets less effective mainly due to switching components superposing all controller signals. The level of performance is superior to CVFC or any other of the investigated linear control methods, even-though MECC(1,1) is actually simpler in implementation that CVFC. Fig. 10.17 shows the harmonic residue at (1W/1KHz) where all harmonics are damped more than 95dB relative to the fundamental.

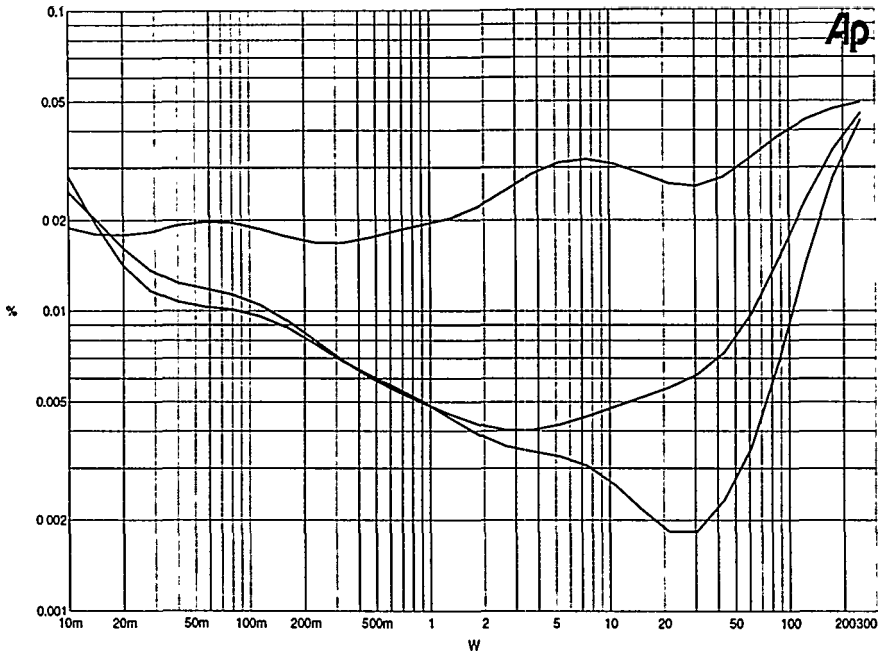


Fig. 10.16 THD+N vs. output power at 100Hz, 1KHz and 10KHz.

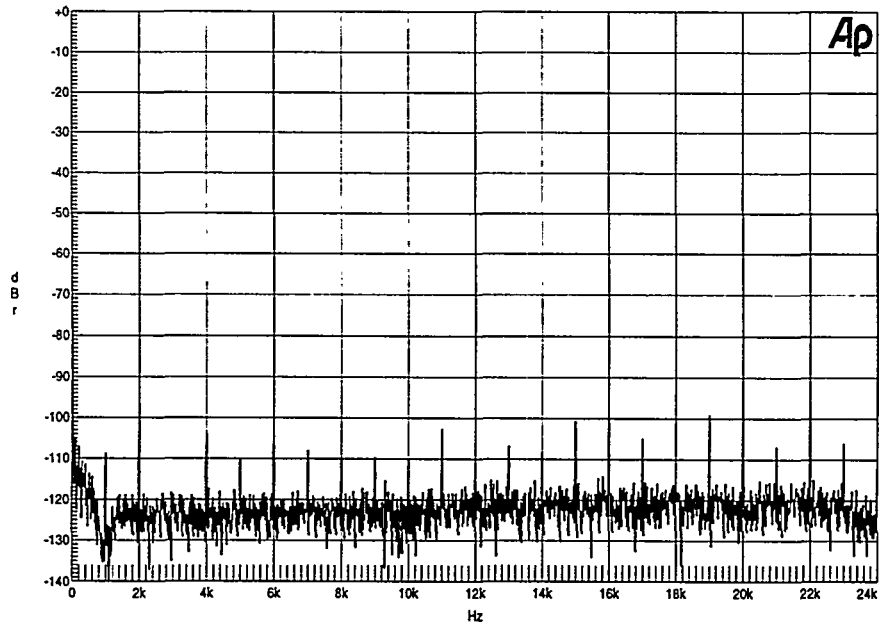


Fig. 10.17 FFT of MECC(1,1) PMA output at 1W. THD+N=0.005%.

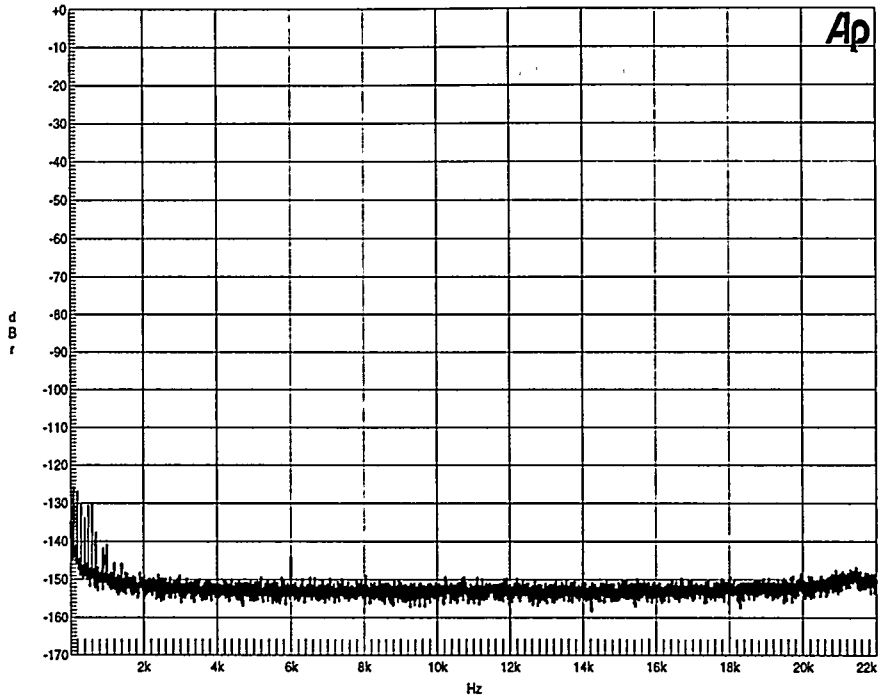


Fig. 10.18 Residual noise from MECC(1,1) PMA system.

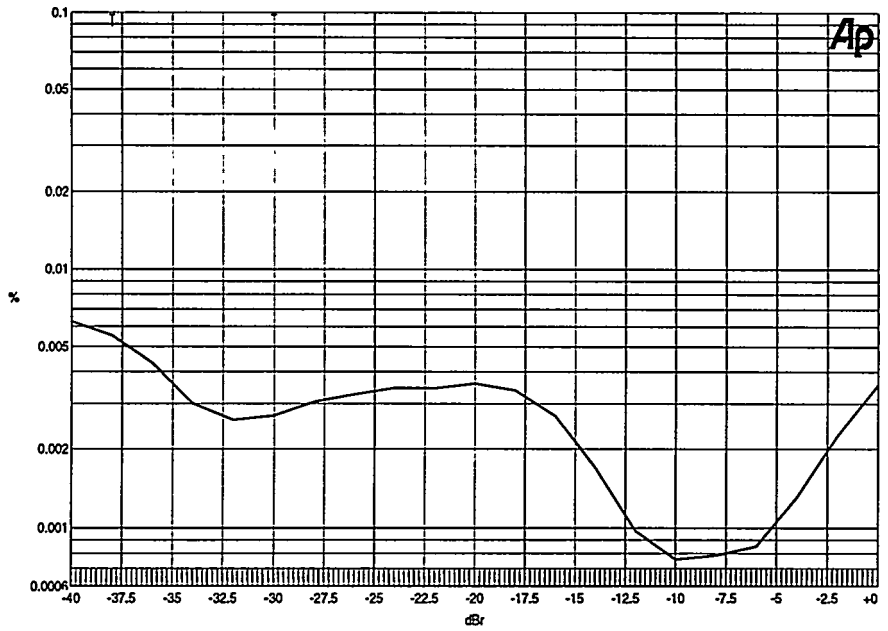


Fig. 10.19 CCIF intermodulation distortion. (19KHz, 20KHz)

This is very good for such a high power PMA system and fully comparable with what is achieved by the best linear amplifiers. Fig. 10.18 further documents the PMA output noise at idle. The small components from the mains arrive from the input and not from the amplifier itself. The unweighted noise level is 50μV RMS, which is excellent for such a high power, full bandwidth system. Fig. 10.19 shows the CCIF intermodulation distortion vs. relative output level, where two 20KHz and 19KHz are swept over a 40dB amplitude range. The intermodulation distortion characteristics are equally concluded to be excellent.

The efficiency and idle consumption for the system compare well with was is estimated by the Power Stage Optimization Toolbox. The total idle losses include all essential contributions in the system. The specifications for the MECC(1,1) based PMA system are summarized below:

Cont. output power	250W
Bandwidth (3 dB)	0Hz – 50KHz
Load impedance range	2-16Ω
Supply voltage (single)	70V
THD+N	<0.05%
CCIF IMD	<0.01%
Residual noise 20Hz-22KHz (unw)	50μV RMS
Dynamic range (unw)	118dB
Maximal efficiency	93%
Idle consumption – Total	2W

Measured specifications on a full bandwidth MECC(1,1) based PMA [Ni97b].

The practical evaluation of the MECC(1,1) controlled PMA system has verified, that the topology provides powerful control of all system parameters. With the given plant performance in terms of distortion and noise, the simple topology has proved sufficient to realize the specifications well beyond the initially specified design goals (Chapter 1). More complicated plants should be attacked by a higher order MECC structure.

Based on the practical evaluation of this specific case example, it is concluded that the theoretical benefits are well implemented in practice.

10.6 Enhanced Non-linear Control (TOCC)

The enhanced three level controller has been implemented in practice to compare the performance with linear control systems operating on a similar power stage. The investigations have been based on a 100V switching power amplification stage, with reasonable open loop performance. The general parameters were as used in the simulation model in Chapter 8:

Parameter	Assignment
K_{OCC}	32
f_o	25KHz
f_c	300KHz
V_S	80V
v_f	$\frac{V_S}{2K_{OCC}}$

The offset voltage was adjusted to the optimal value - half the supply voltage divided with the small signal gain K_{occ} of one switching leg. The complete reset circuit required quite a bit of hardware: One opamp, one TFF, two matched capacitors, one resistor and four bilateral CMOS switches. Further details on the implementation and verification are given in [Ta97], [Ni98a].

Fig. 10.20 shows the integrator output with the output phase voltage at idle for the TOCC controlled PMA, illustrating the functionality of the combined controller/modulator works. However, the practical implementation of the TOCC based PMA revealed a range of limitations. The fundamental problem was the finite reset time of the integrator. It was found that the integrator and reset topology introduces audio band noise in the feedback path. Despite a range of attempts to minimize this noise, it was not possible to reach an acceptable level of noise performance. The total audio band noise level was actually increased with the TOCC non-linear controller / modulator, compared to a normal carrier based open loop PWM system. Another observation was that the system only marginally improved distortion compared to open loop PWM. This is illustrated in Fig. 10.21 in terms of THD+N vs. output power for five different frequencies within the audio band (100Hz-10KHz). The distortion is comparable to that of open loop PWM. Thus, the only benefit of the non-linear controller was the improvement in PSRR ratio of around 45dB.

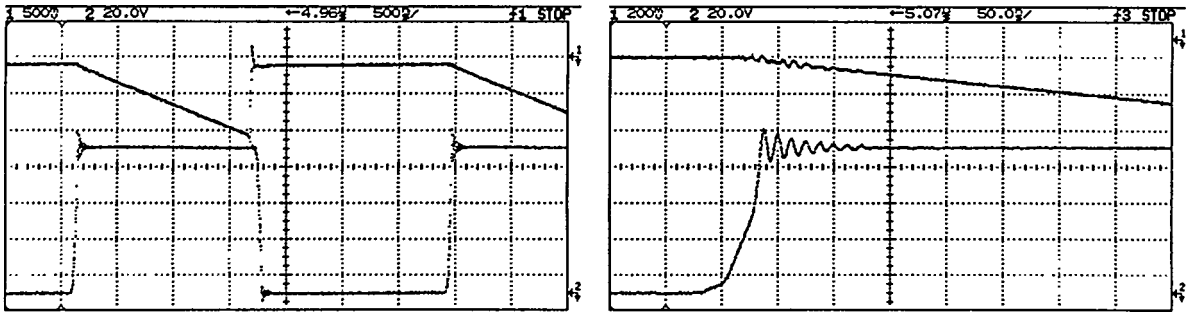


Fig. 10.20 Functional verification of the TOCC system. Integrator signal and bridge phase outputs are shown for the TOCC controlled system (right). A close-up is also shown (left). Note the inherent delays from the integrator reset to the switching action in the power stage.

The measured specifications for the TOCC based system are summarized below:

Max. continuos output power (@ 80V)	300W
Load impedance	4Ω
THD+N @ 1W/1KHz	0.6%
THD+N (Complete frequency and power range)	0.05%-2%
Residual noise 20Hz-20KHz (unw)	2mV RMS
Dynamic range	88dB
Maximal efficiency	92%
Idle power dissipation	3W

A more general observation of practical importance is the apparent complexity of non-linear controllers, compared to linear control system. Furthermore, the non-linear controller only provide improvements on some parameters, and the results are not well defined and difficult to analyze. Another constraint is the undesirable characteristics at overload, which were simulated in Chapter 8. Fig. 10.22 shows a practical investigation of this special clipping phenomenon. The TOCC based PMA produces extreme distortion at overload, where the RMS actually reduces with increasing modulation index. Subsequently, limitation of the modulation index is of paramount importance.

To conclude, the practical investigations of TOCC shows that the method is inferior compared to linear control schemes. The linear controlled systems show orders of magnitude better performance. The fundamental advantage of linear control for analog PMAs is simple modeling and optimization, low implementation complexity, controllable performance and an effective correction of all power stage generated error sources.

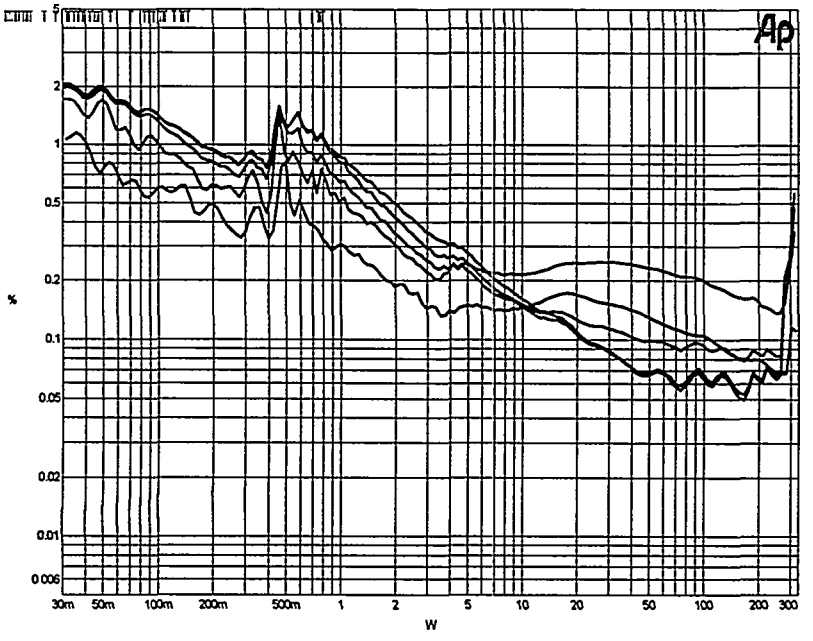


Fig. 10.21 THD+N vs. output power with TOCC controller. The results are clearly below the desired performance level. The controller only marginally improves open loop performance.

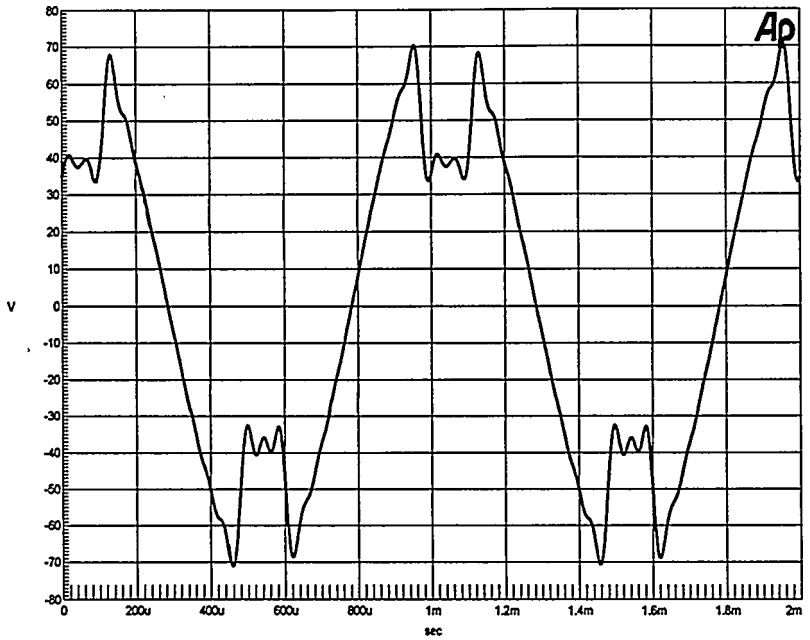


Fig. 10.22 Over-modulation with TOCC controller. As opposed to full pulses the individual switching legs will produce a missing pulses. This causes a highly unpleasant overload characteristic, where the RMS is reduced with increasing modulation index.

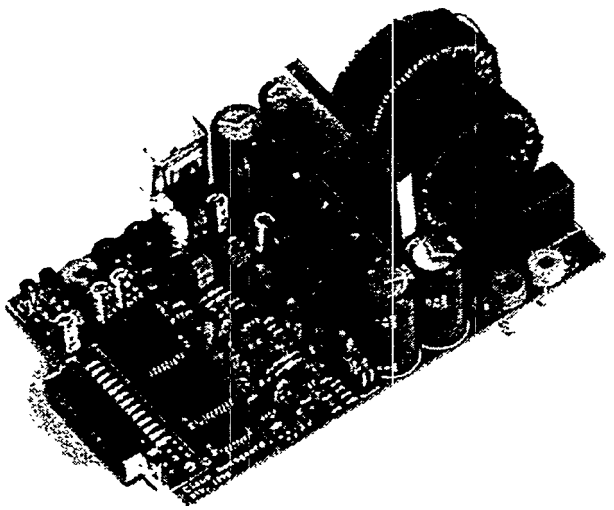


Fig. 10.23 200W PEDEC based digital PMA. The digital input (8 bit) connector is seen left.

10.7 PEDEC based Digital PMA

A prototype PCB has been developed for a detailed practical verification of the proposed PEDEC based digital PMA topologies in Chapter 9. The modulator has been implemented on a dedicated SHARC (ADSP21060) processor based PCB which outputs the 8 bits from the noise shaper to a second dedicated PCB that realizes:

- The PWM DAC, i.e. the conversion of the digital 8 bit word to a physical PWM waveform that is input to the PEDEC controlled power stage.
- Power stage and filter.
- Controller hardware for the three controller variants PEDEC VFC1, VFC2 and VFC3.

The digital PMA printed circuit board is shown in Fig. 10.23. Overall, the PEDEC controller is simple in implementation with a active and passive components. Thus, the controller only marginally influences the complexity of the system. A dedicated realization for a reduced 2KHz bandwidth is considered. The synthesized LPWM modulator case example in Chapter 3, has been implemented in practice only normalized to the specific bandwidth of 2KHz. PEDEC is investigated with a 200W power stage.

The parameters for the implemented PEDEC digital PMA system are given below:

Parameter	Assignment
S	3
b_{rq}	8 bits
f_b	2KHz
f_c	44.1KHz
f_o	2KHz
Filter order	4
V_S	50V
K	26dB
t_d	80ns

Recall from Chapter 9, that the fundamental concept of PEDEC control is to *force equivalence* between the power stage output and the digital pulse with modulated (ideal) reference in all situations. With the specified gain of 26dB, a bipolar ±2.5V reference is needed. This is realized using a simple multiplexing circuit that operates on stabilized ±2.5V power supplies. In a more detailed investigation of this reference [Ne98] it was found that the amplitude was not well defined at higher modulation depth. Correspondingly, the reference in the following is below the theoretical (digital) performance level at higher modulation indices. It is considered trivial to realize a small signal reference with well-defined amplitude, and the focus in the following investigation will thus be on the *PEDEC performance*, i.e. the resemblance between the pulse modulated reference and the output.

10.7.1 Open loop performance

The open loop digital PMA output is illustrated in Fig. 10.24 and Fig. 10.25 with two different noise shaping filters, the fifth order FIR and IIR prototypes that were devised in Chapter 3. The noise shaping characteristic is clear with the two noise shaping filters (note the 24dB/octave slope caused by the filter with the 5. order IIR NTF).

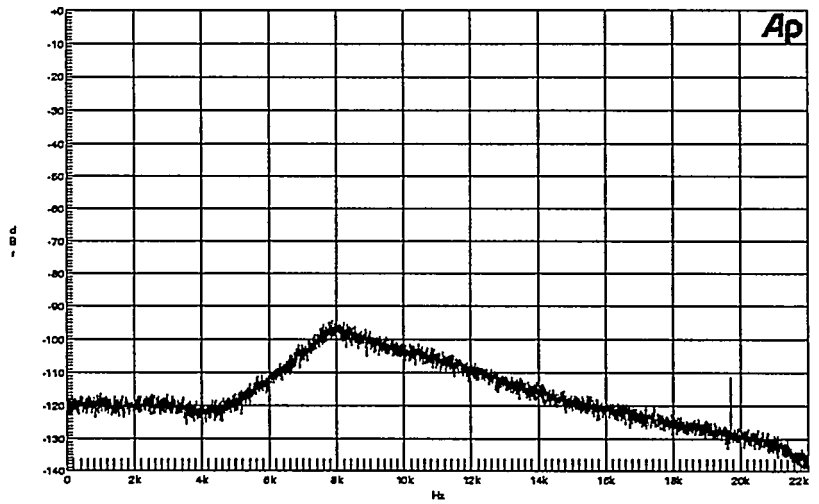


Fig. 10.24 Residual output with IIR5 noise shaping filter (defined in Chapter 3).

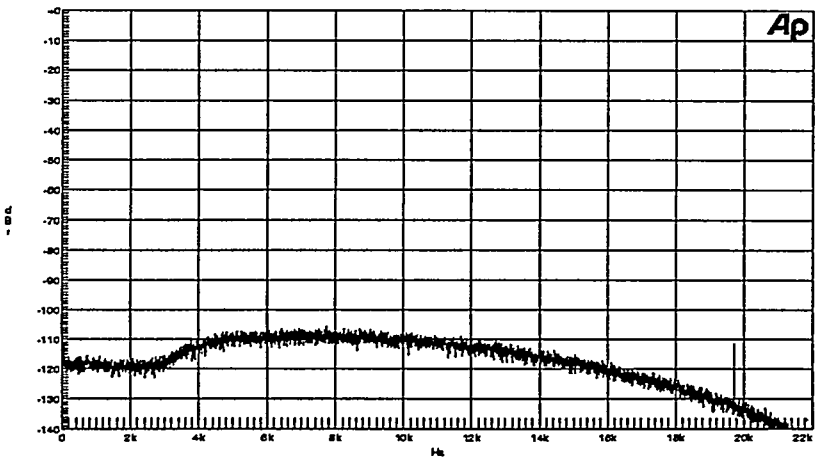


Fig. 10.25 Residual output with FIR5 noise shaping filter (defined in Chapter 3).

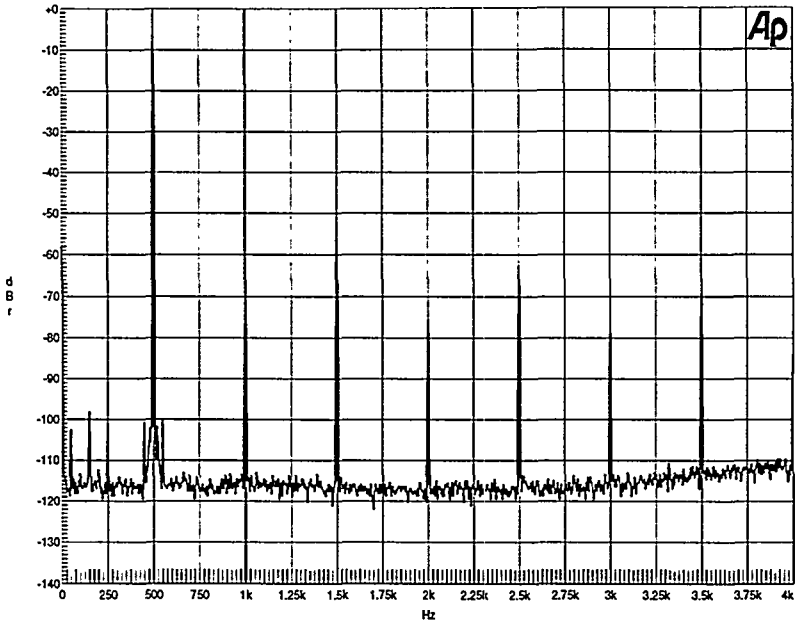


Fig. 10.26 Non-controlled output at f=500Hz, M=0.5. Stabilized power supply.

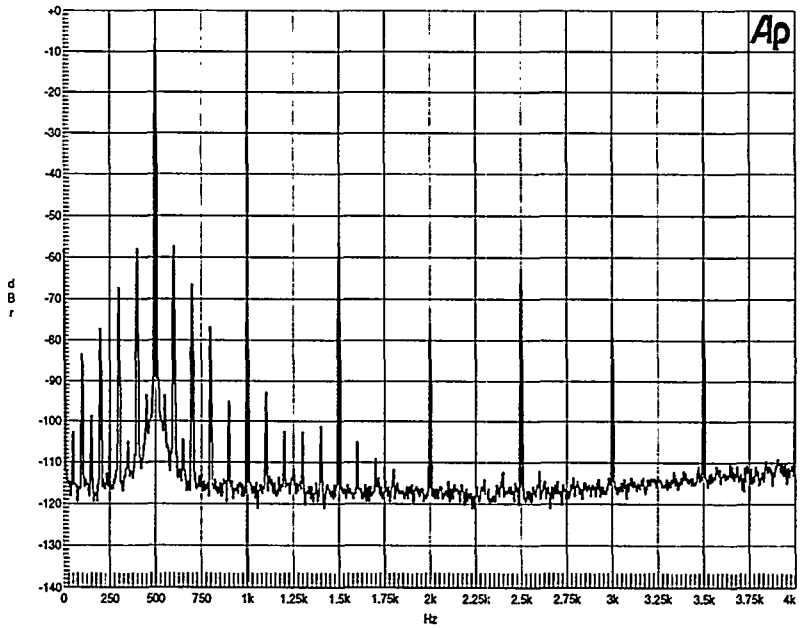


Fig. 10.27 Open loop output at f=500Hz and M=0.5. **NON**-stabilized supply (10000μF).

The dynamic range is measured to:

$$D = \frac{\sigma^2_{x,\max}}{\sigma^2_{q(2KHZ)} + \sigma^2_{nb(2KHZ)}} \approx 97dB$$

This corresponds well with theory (16 bit input with dither). Note, that the noise measured over the complete audio bandwidth yields a much lower dynamic range. However, this is not a fair approach, e.g. this would correspond to a noise bandwidth of 160KHz in full bandwidth PMAs. The out of band noise can be removed completely (in theory) by filtering without affecting the system performance.

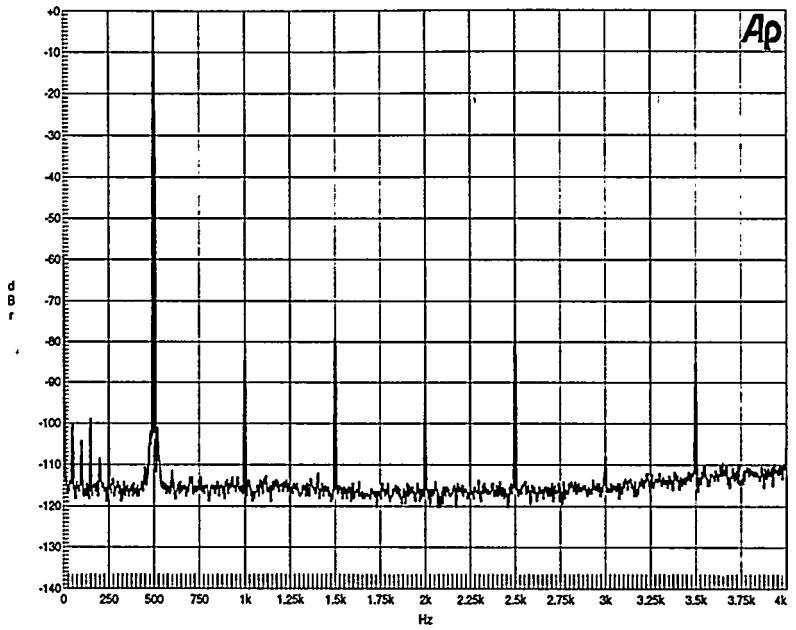


Fig. 10.28 PEDEC **VFC1**. 500Hz and M=0.5. **NON**-stabilized power supply. Comparing with the open loop system, PSRR is improved 40dB and THD 20dB with PEDEC VFC1.

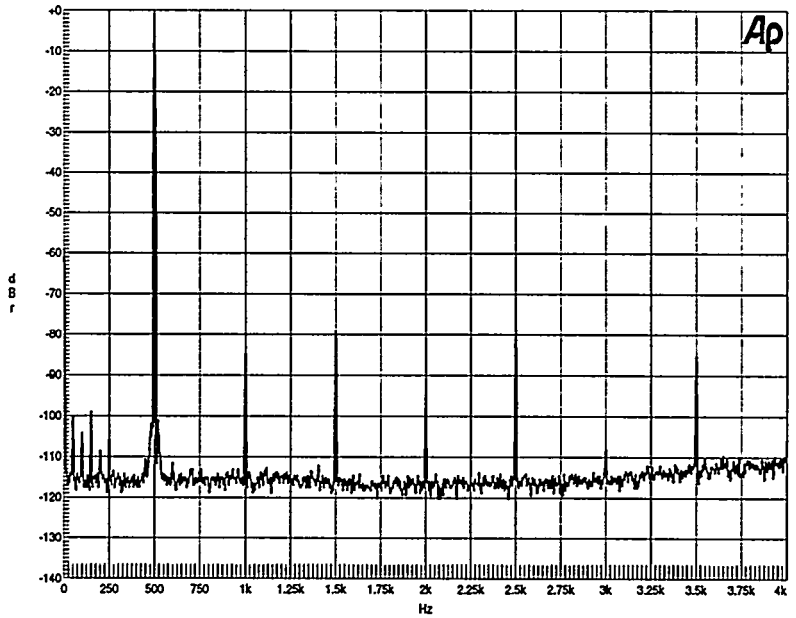


Fig. 10.29 PEDEC **VFC2**. 500Hz, M=0.5. **NON**-stabilized supply. Comparing with the non-controlled system, PSRR is improved 40dB and THD 22dB with PEDEC VFC2.

Fig. 10.26 and Fig. 10.27 shows the PMA output with f=500Kz and M=0.5 with both a stabilized and a non-stabilized power supply (10000μF). The intermodulation caused by power supply perturbations is significant (see Chapter 4). The PEDEC controller significantly reduces both THD and IM as shown in Fig. 10.28 and Fig. 10.29, where the output is investigated with the exactly same parameters set, only with PEDEC VFC1 and PEDEC VFC2 respectively.

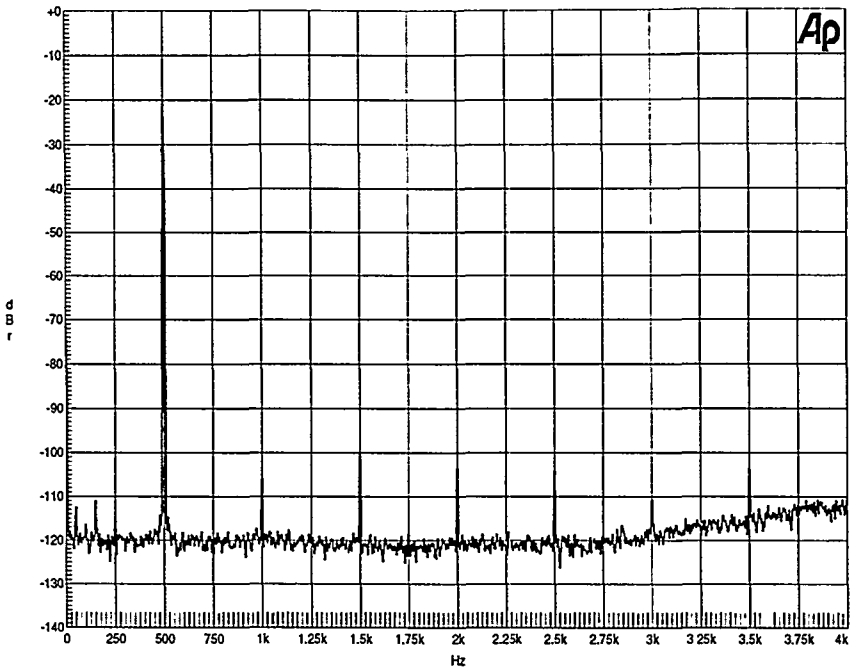


Fig. 10.30 PEDEC VFC2. 500Hz, M=0.1 (**NON**-stabilized supply). The improvement in THD is 26dB leading to THD=0.018%.

Comparing the PEDEC controlled systems with the open loop system, the improvements are significant, about 20dB in distortion and 40dB in intermodulation (PSRR). Note that the VFC2 topology performs somewhat better than VFC1, and is furthermore simpler in implementation. Thus, the digital PMA output with PEDEC VFC2 is very close to the reference performance. Fig. 10.30 shows the output at M=0.1. The distortion improvement is 26dB resulting in 0.018% THD, verifying that the improvement in independent of output level.

Fig. 10.31 shows the residual output with the proposed PEDEC VFC3 controller. The noise characteristics differ significantly from the residual output with PEDEC VFC1 and VFC2. This is caused by the second order reference shaping, i.e. the PEDEC controller *forces the output to resemble the shaped reference best possible*. VFC3 offers superior noise performance compared with VFC1 and VFC2 with a 10dB lower noise floor in the frequency range 1KHz-8KHz. The may be interpreted as *noise reshaping*. Fig. 10.32 shows the output at 1KHz, M=-20dB. The improvement in distortion is about 20dB as with the other topologies.

Although further investigations on PEDEC control are needed to reveal the limits of performance, the simple prototype has verified the principle works in all three configurations. One order of magnitude improvement in distortion and two orders of magnitude improvement in IMD (PSRR) is exactly what is needed to make digital PMAs practical and much less dependent upon the performance of the power conversion stage. Future research will reveal the levels of performance that can be reached by PEDEC based digital PMA systems.

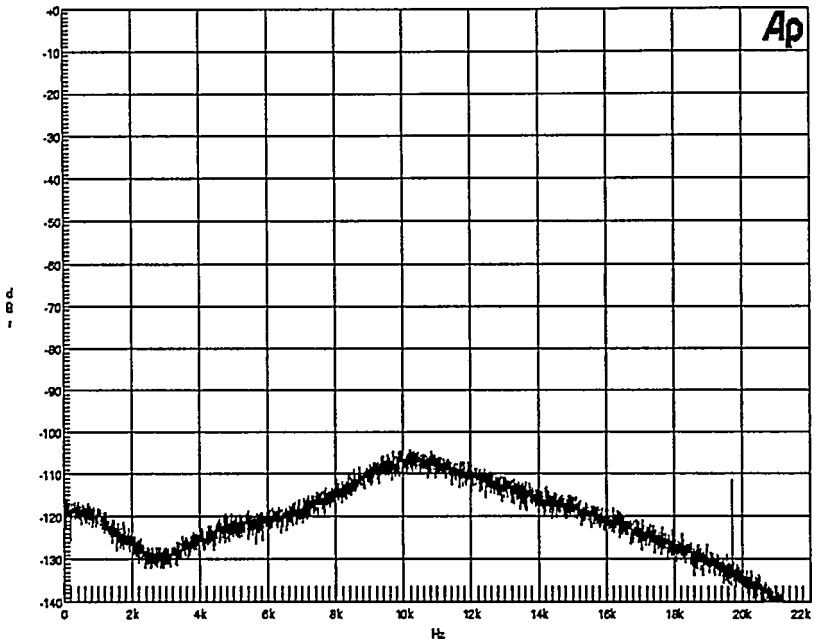


Fig. 10.31 PEDEC VFC3 output at idle. Note the significantly changed characteristic. The loop modifies the output to resemble the second order shaped reference best possible. This leads to noise "reshaping" by the PEDEC VFC3 system.

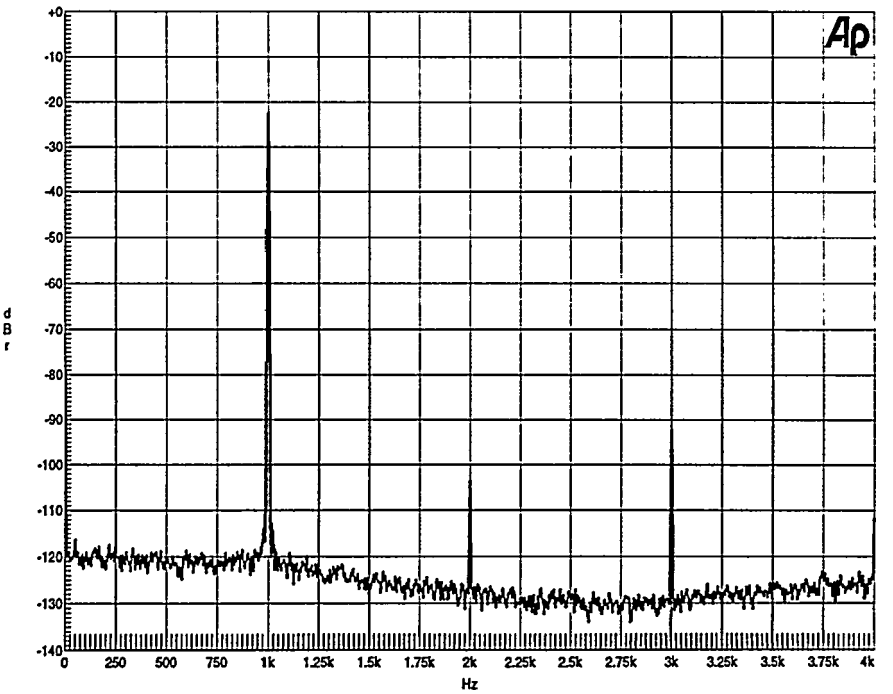


Fig. 10.32 PEDEC VFC3. 1KHz and M=0.1. (200W NON-stabilized supply). THD is reduced 20dB and PSRR is reduced approximately 40dB.

10.8 Summary

This chapter was devoted to implementation and practical evaluation of the principles and topologies that have been investigated theoretically throughout the thesis. The general problems of power stage implementation were discussed and illustrated, and the fundamental error sources were documented.

The functional verification of PSCPWM was addressed, by an eight transistor, 500W, 5-level PSCPWM realization (BND1). It has been verified, that the BPSC switching power stage topology offers a linearity that is comparable to that of the simple switching leg, i.e. there are no linearity or noise compromises in PSCPWM. The theoretical efficiency advantage of PSCPWM was also verified in practice.

Following, all control methods were documented by presenting the essential results that have been achieved in various configurations. MECC proved to realize state-of-the art power amplifier performance on all parameters, by achieving specifications well beyond the desired objectives in a simple MECC(1,1) configuration. It was shown that the simple VFC2 topology may suffice in e.g. dedicated applications with reduced bandwith, although it has proven difficult to reach all the desired control objectives. CVFC was shown to offer reasonable performance, but is compromised by the requirement for precision current measurement.

The theoretically interesting non-linear TOCC controller showed very disappointing performance, inferior to open-loop PWM. Most of the problems relate to the noisy (and complex) integrator with reset.

Ultimately, PEDEC has been evaluated in practice in a dedicated bandwidth limited application. Although the hardware prototype had sub-optimal performance on the pulse modulated reference, PEDEC was shown to provide a much improved power amplification of the pulse modulated signal, forcing equivalence between the digital modulator output and the digital PMA output.

Chapter 11

Summary and Conclusions

Various methods for energy efficient audio power amplification using pulse modulation techniques have been investigated in the present work. The power amplifier is generally the most energy consuming element in the audio chain with a typical the energy efficiency of only 1%, so there is much room for improvement. Furthermore, audio power amplifiers get voluminous, heavy and costly as a direct consequence of low efficiency so there are several motivating factors to research in new improved solutions. Previous research has shown that pulse modulation based amplifier systems are connected with several problems and it has been difficult to realize a sufficient level of performance. The fundamental problems have been addressed with a great deal of fundamentalism, leading to multi-disciplinary research is various scientific fields as analog and digital modulation theory, various fields of power electronics, signal processing and control system design. This ultimate chapter will summarize the essence of the work performed and emphasize the essential conclusions.

A detailed study analog pulse modulation method was carried out, founded on the Harmonic Envelope Surface (HES) as an effective tool for analysis and consistent comparison of methods. NPWM methods were concluded to be very well suited for PMA applications to the excellent linearity and simple realization, combined with simple implementation of the power conversion stage. However, the significant HF output of the fundamental schemes presents a significant problem in PMA systems. A novel class of modulation methods – Phase Shifted Carrier Pulse Width Modulation (PSCPWM) was introduced as a contribution to the field of modulation theory for PMA systems. The analysis concluded on the advantages of the double-sided balanced PSCPWM methods, BND1, BND2 and BND3, implemented in the BPSC power stage topology. Some of the proven advantages of these modulation methods include:

- An improved multi-level synthesis of the modulating signal, where the HF content of the pulse modulated output is minimized.
- A controllable increase in effective sampling frequency.
- Minimal power supply complexity (single supply).
- Reduced switching frequency in each switching leg reducing the effects of error sources.
- Improved total efficiency by a combination of reduced conduction and switching losses.

The focus turned towards digital pulse modulation methods in Chapter 3. Various enhanced digital PWM methods were reviewed and LPWM was selected on a performance / complexity scale. Previous research on LPWM was extended by a detailed investigation of both linearity and HF performance. A simple LPWM modulator design methodology was devised based on a separation of linearity and dynamic range demands. An important conclusion is, that optimized digital modulators for digital PMA systems provide excellent performance, well beyond what can be reproduced by the subsequent power conversion stages. Consequently, the digital modulator is not a limiting factor on digital PMA system performance.

The inherent error sources within the power conversion stage was addressed in Chapter 4, by studying the physical limitations within the switching devices and following investigate the effects of these limitations on PMA system performance. The error sources were separated in Pulse Amplitude Errors (PAE) and Pulse Timing Errors (PTE) and following subjected to a qualitative analysis. In was concluded that the power stage, independent on modulation method and power stage topology, is the fundamental limitation in all PMA systems. Chapter 5 extended the investigations of power conversion, by addressing efficiency optimization for the general PSC and BPSC switching power stage topologies. Case example power stage designs were presented, illustrating the excellent efficiency approaching 95% and energy efficiency in the area of 30% that can be achieved with the present stage of technology. Future development in switching power devices and magnetics will only improve these figures. The PSC and BPSC power stages proved advantageous in terms of system efficiency due to reduced total conduction and switching losses. In general, optimized PMA systems completely redefine the level of energy efficiency in power amplification. The practical evaluation of various power stage topologies verified the theoretically expected levels of power and energy efficiency.

The application of robust linear feedback control methods to analog PMA systems was the subject of Chapter 6. A design methodology for robust control system design was introduced, based on an initial study of the plant to be controlled and the uncertainty within the plant. Three fundamental linear control methods were investigated, VFC1, VFC2 and CVFC, and robust case example designs were synthesized and evaluated. The practical verification of the methods revealed that even simple linear control methods offer a remarkable value, by reducing the sensitivity to any kind of disturbance significantly. The three topologies proved to have their own advantages and disadvantages.

Chapter 7 introduced an enhanced linear control topology dedicated to PMA systems – Multivariable Enhanced Cascade Control (MECC). The topology is based on a recursive structure of loops formed as an enhanced cascade from a single or alternatively two feedback source in the MECC(N) and MECC(N,M) versions, respectively. Fundamentally, MECC offers a practical and robust method for higher order control system

implementation with MECC(N) for dedicated applications and MECC(N,M) for general applications. The advantages covers e.g. flexibility in loop shaping, balanced signal levels throughout the control structure and simplicity in implementation with low requirements for the compensator blocks. This combination of features makes MECC the most powerful and flexible control method existing for general analog PMA systems. The theoretical advantages were also demonstrated in practice, by the implementation of a high power, full bandwidth analog PMA with state-of-the-art performance.

A radically different approach, in terms of a combined modulator/controller method realizing non-linear control of the PMA, was investigated in Chapter 8. The non-linear controller proved indisputable advantages over any linear control method in terms of transient response, stability and robustness to uncertainties. Unfortunately, the topology proved to have limited corrected effect and the implementation of the system illustrated further problems that are difficult to compensate for. A more fundamental and general constraint was concluded to be the difficulty in modeling and optimization of the system.

A contribution to the field of digital PMA systems was presented in Chapter 9, in terms of a new pulse reference control method for improved power amplification of the digital pulse modulated signal. The principle - Pulse Edge Delay Error Correction (PEDEC) – is proposed as a general method for enhanced power amplification of a pulse modulated signal. The introduction of a simple linear PEDEC unit control function simplifies both modeling of the principle and the practical implementation. The method was applied to digital PMAs by defining three topologies with different characteristics in terms of error estimation and feedback source. The evaluation of the topologies by simulation and practical implementation verified the functionality of the principle, i.e. PEDEC provides a significantly reduced sensitivity to towards any error within the power conversion stage. PEDEC is concluded to be a feasible method for practical, high performance digital PMA realization without a need for stabilized power supplies, tuned power stages etc.

To conclude on the present research, various methods for high efficiency power amplification has been presented to cover a broad range of applications. It has been shown that the energy efficiency can be improved by about an order of magnitude using optimized output stages. Whether to use the analog or digital PMA approach is a rather academic issue, with the solutions that have been presented for both approaches. The essence of PMA systems clearly is the revolutionary potential that lies in the unique combination of high efficiency, extreme compactness, low cost and audio specifications approaching state-of the art for power amplification – generally speaking. The present work has indicated that this delicate combination is realizable in both analog and digital PMA systems, using e.g. MECC and PEDEC, respectively. As the digital expansion continues with time, the digital PMA approach may conquer the majority of applications. In any case, with the newfound possibilities analog power amplification seems irrational from any point of view. Thus, it is to expect that high efficiency PMA systems will invade the complete application range of audio power amplification within a foreseeable time. It is hoped that the contributions to the field within this work will help to catalyze this development.

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