Process Scale Up for Thermoelectric Superlattices

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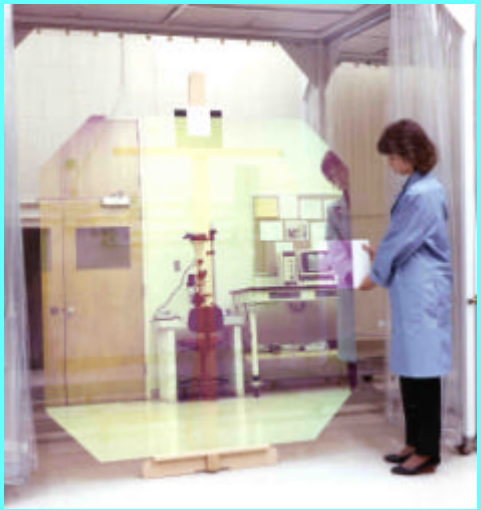
Objectives

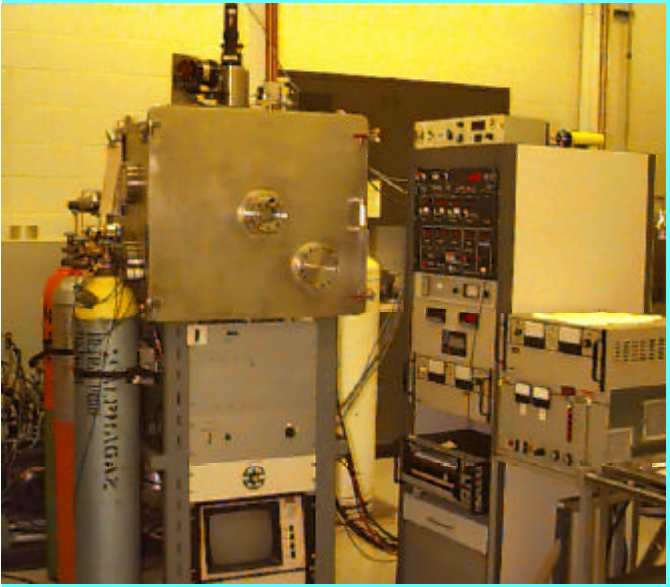
- Develop methods to scale up deposition of quantum well thermoelectric devices
  - Scale up $Si/Si_{0.2}Ge_{0.8}$ structures
  - Scale up B_4C/B_9C structures
  - High volume
  - Low cost
  - Heavy truck applications
- Transfer deposition technology to High-Z

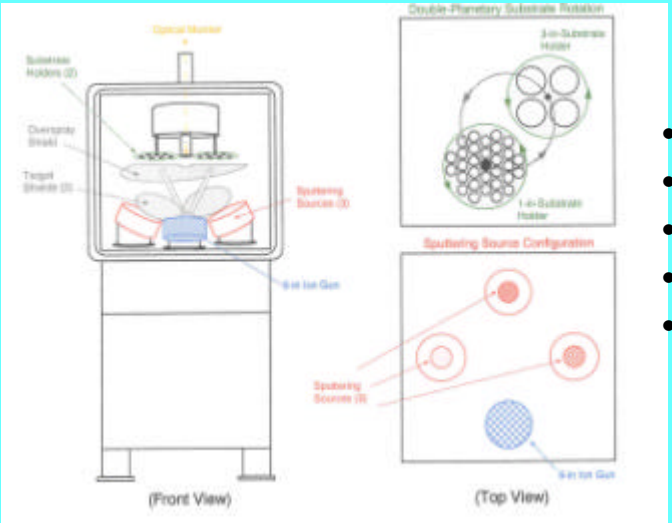
LARGE AREA COATINGS

- SPACE OPTICS
- AIRCRAFT OPTICS
- WINDOWS
- PLASTICS
- LASER OPTICS
- TCO's



Midsize Coating Chambers





Small Box Chamber

- Coatings and ion milling
- 28” Box chamber
- 2 available
- RF diode and DC magnetron
- Max 14”-diameter substrate

DOE TE Program

- Project initiated April 2002
- Replicate High-Z quantum well structures in mid-size chambers
  - $Si/Si_{0.8}Ge_{0.2}$ quantum well
  - B_4C/B_9C quantum well
- Scale up process to
  - Multiple 15 cm (or larger) substrates
  - Web substrates, plastics (roll coater)
  - Magnetron sputtering

Scale Up Issues

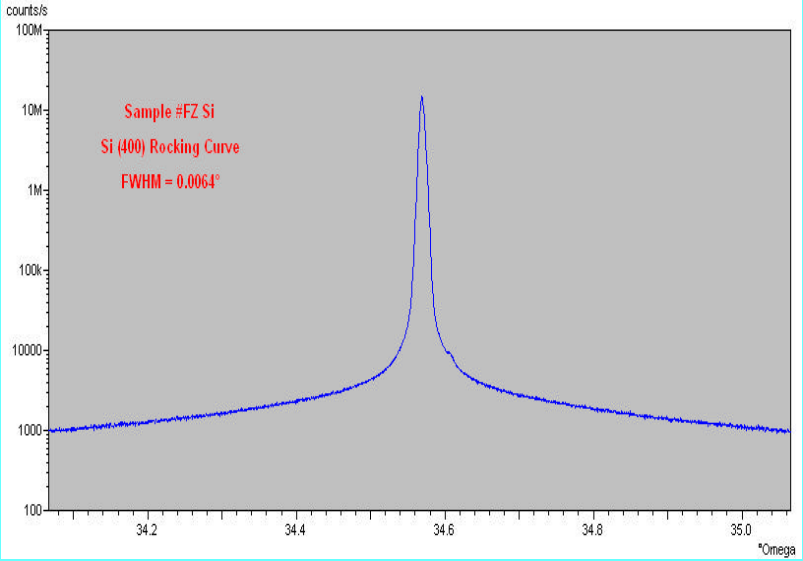
- ZT increase looks promising for small scale TE devices
- Scale up for TE power generation for heavy duty trucks is challenging
  - Substrate size/surface
  - Low cost substrates/process
  - Coating thickness uniformity
  - Crystallinity
  - Same properties as small scale devices
  - Substrate heating
  - Measure ZT

Progress to Date

- Deposition evaluated and defined
  - 400 ºC substrate temperature appears optimum
- Seebeck coefficient depends on deposition rate
- Eight 101-layer $Si/Si_{0.8}Ge_{0.2}$ superlattices deposited
  - N-type
  - P-type
- Release/buffer layer investigated
- Apparatus for automated deposition of superlattices being tested
- Harmon method to measure ZT in progress

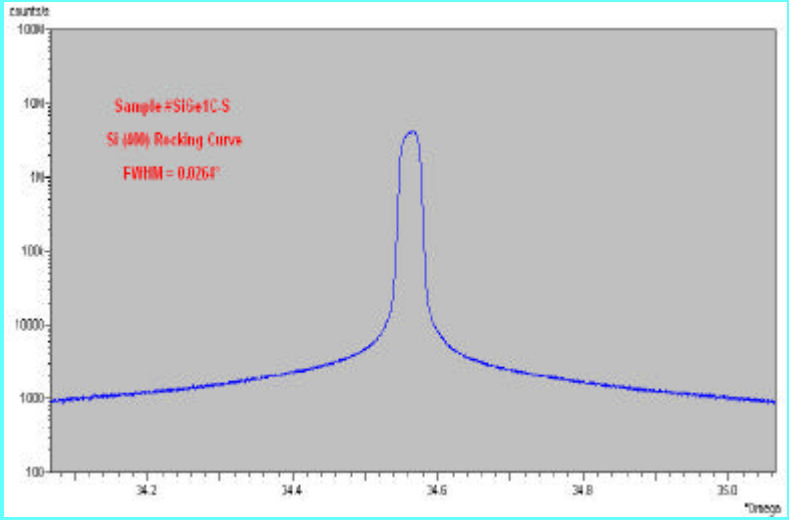
XRD Results For Sputtered Si On Si

Si (400) Rocking Curve
FWHM = 0.0064°
For Bare Si Wafer

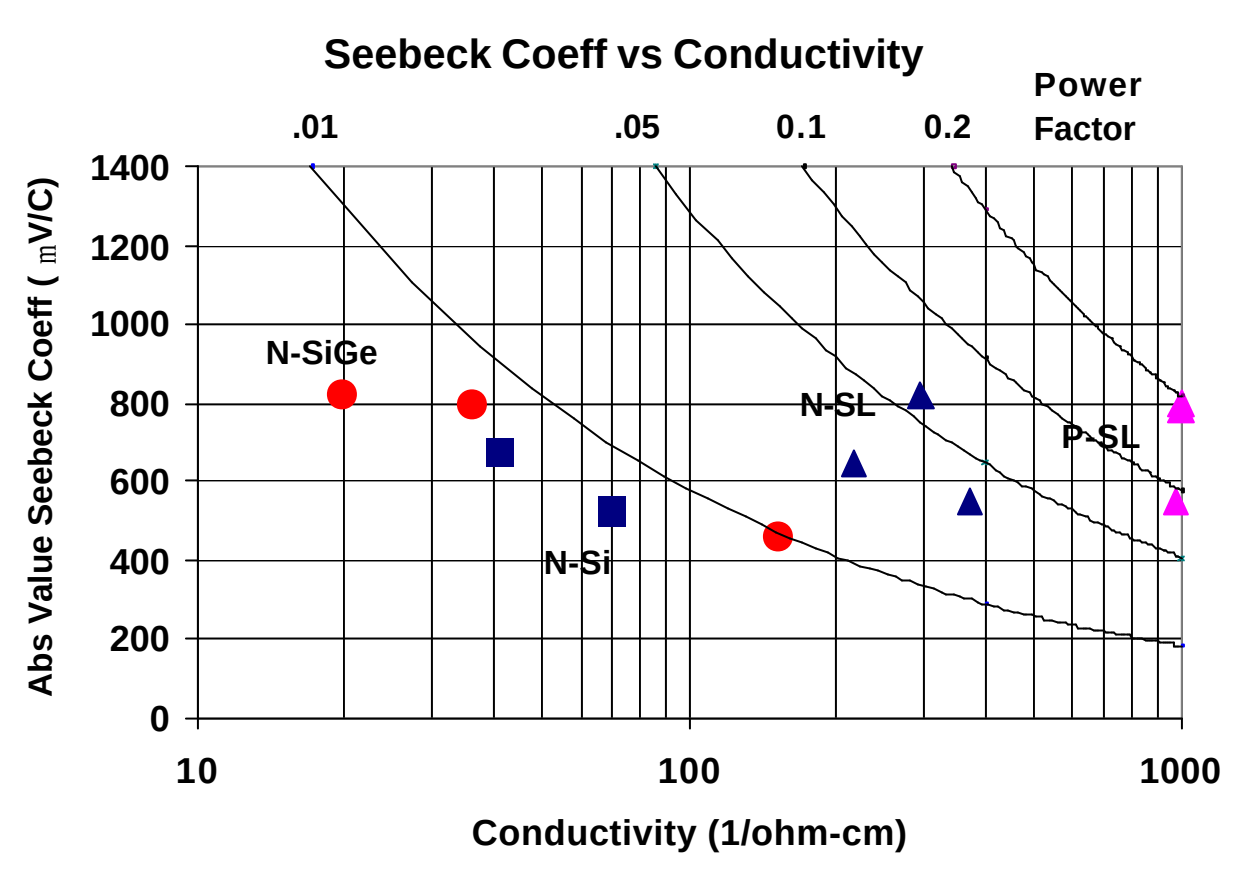


Si (400) Rocking Curve
FWHM = 0.0264°

- **For Sputtered Si Film On Single Crystal Si**
- **Results For Si Film Sputtered At Ambient Temperature Had FWHM = 0.0231°**



$Si/Si_{0.8}Ge_{0.2}$ Superlattice



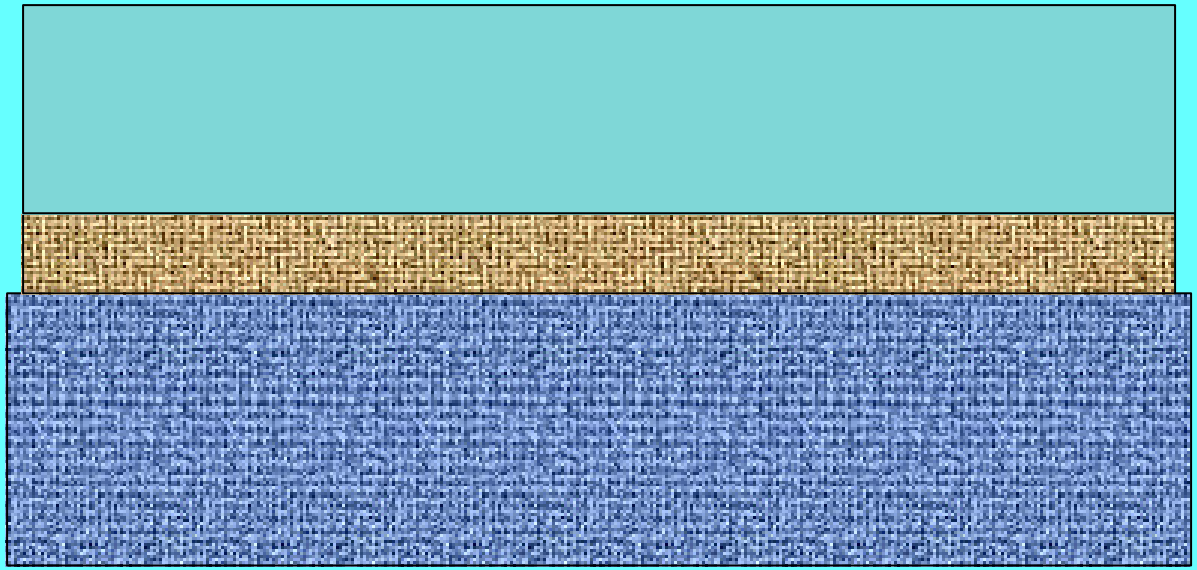
TE and Electrical Properties

Material	Seebeck (μV/K)	S(mho)	Power Factor
Si	-770	69	0.053
$Si_{0.8}Ge_{0.2}$	-1300	152	0.20
$Si/Si_{0.8}Ge_{0.2}$ SL(n-type)	-700	300	0.21
$Si/Si_{0.8}Ge_{0.2}$ SL(p-type)	480 - 800	1000	0.48 – 0.8
$Si/Si_{0.8}Ge_{0.2}$ SL/buffer	±750	1000	0.75

Buffer/release layer

Superlattice

Buffer layer

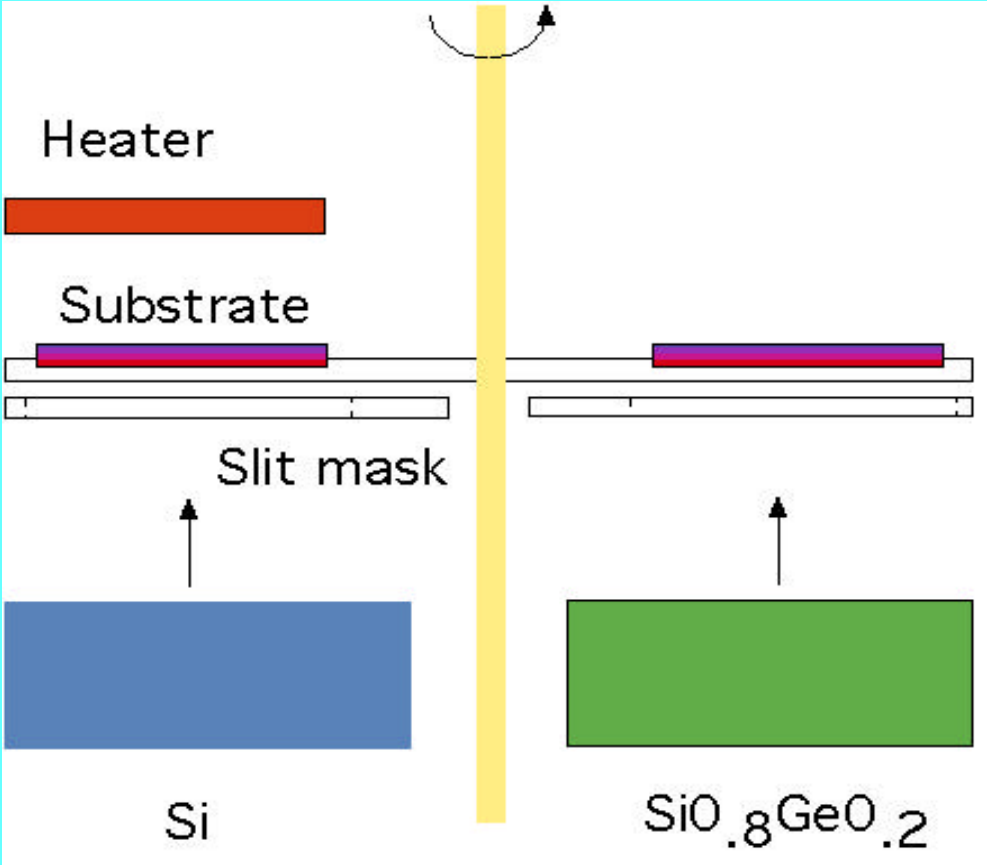


Substrate

Process Scale up

- Magnetron sputtering
- Deposit superlattice on twelve 4” wafers or 12” square substrate per run
- Stepper motor to rotate substrate holder at precise rate
- Quartz and resistive heaters to achieve substrate temperature of 400 ºC
- Deposition controlled by slits above cathode
- Harmon method to measure ZT will soon be on line

Scale Up Geometry



Summary

- Process for scale up of superlattices on track
- Initial performance results look promising
  - Results are *preliminary*, but consistent
  - Both n-type and p-type superlattices
  - TE and electrical properties look good
  - Conductivity of SL about 10 times that of single layer
  - Carrier concentration measurements needed
- Buffer/release layer under development
  - Replicates crystallinity of substrate
  - Allows measurement of ZT by Harmon method