Recent Progress in Scale Up of Multilayer Thermoelectric Films

P. M. Martin and L. C. Olsen
Pacific Northwest National Laboratory*
Richland, WA

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Thermoelectrics development needs

- **Measurement standardization**
- **Performance validation**
- Tailored nanoscale materials
- Materials design for ZT enhancement
- Low resistance contacts and interconnects
- **Process scale-up**
- Prototype device design and engineering
- Thermal management and packaging
- Device and system modeling
- **Manufacturing process optimization**

Scale up Issues

- Process modifications
- Multilayer deposition
- Substrate materials
- Substrate size/surface area
- Economics
- Coating thickness uniformity
- Stress/mechanical property management
- Materials
- Thermoelectric properties

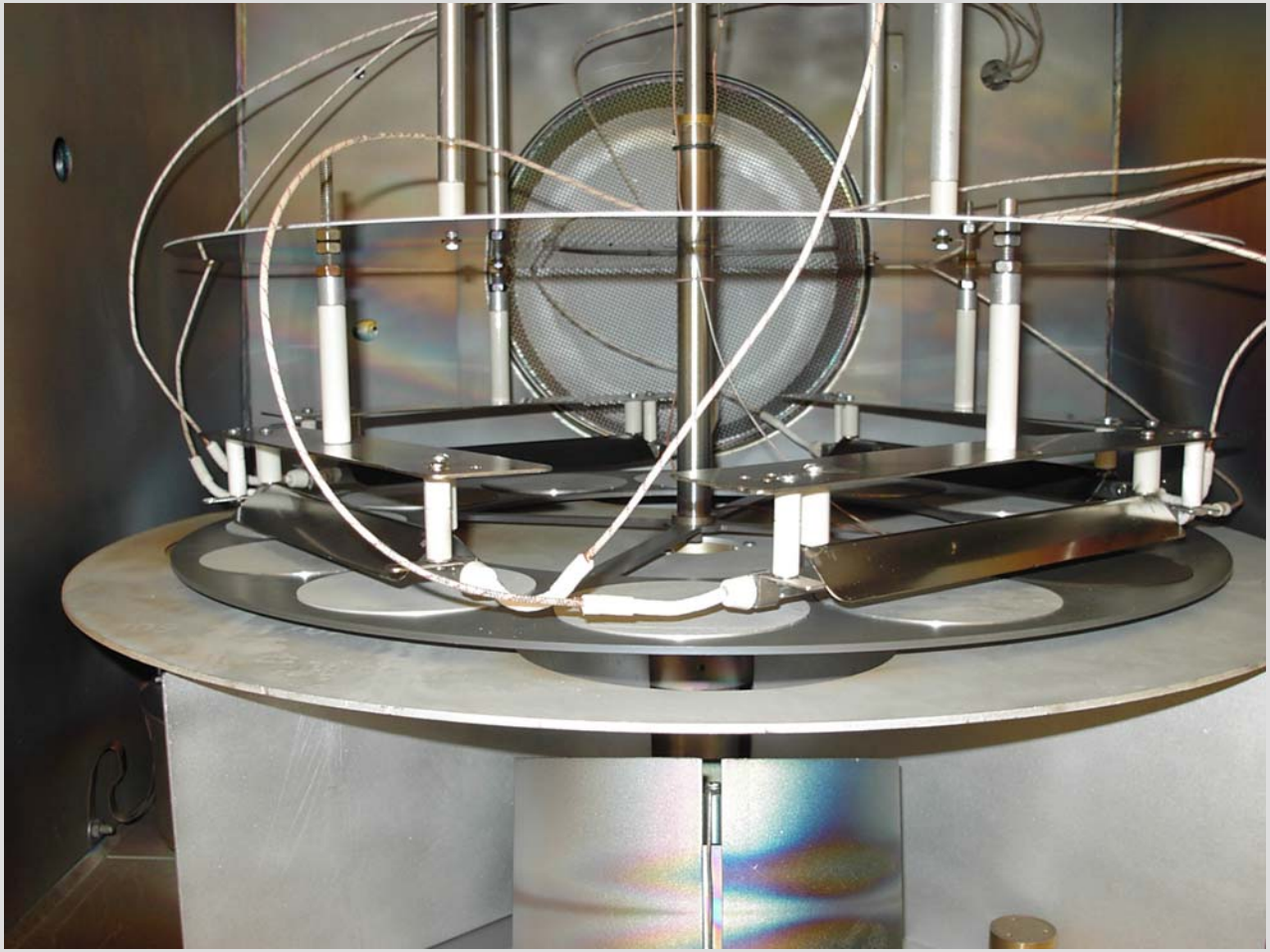
Scale up Approach

- Magnetron sputtering
- Substrate heating
- Optimize deposition parameters
- Post deposition heat treat
- Cosputtering/doping when necessary
- Alloy targets

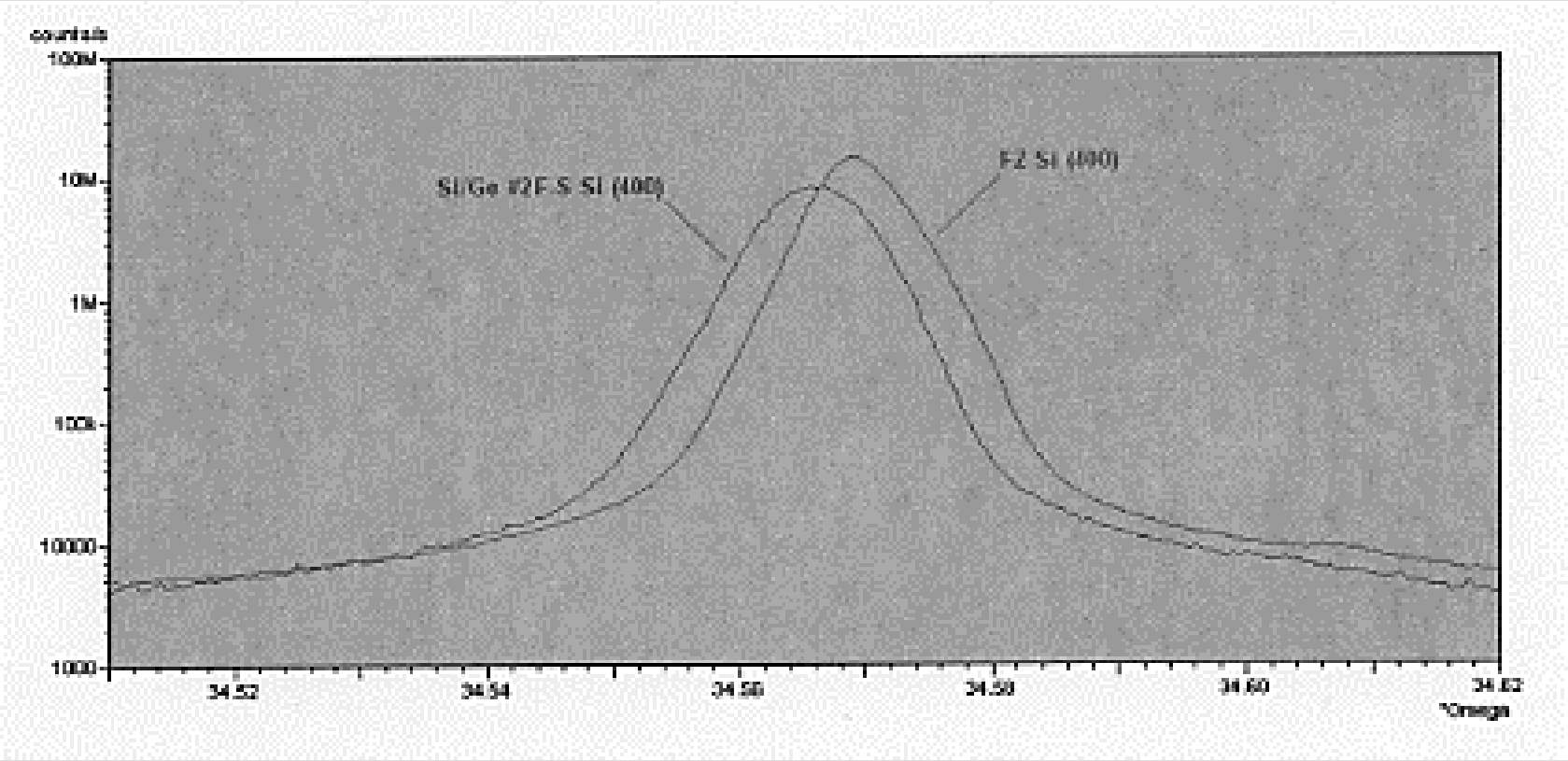
Sputtered n-type TE Multilayers

- $Si/Si_{0.8}Ge_{0.2}$
  - 50 - 100 Å layers
  - N-type layer
  - Up to 3,000 layers needed for power generation
  - Si substrate for epitaxy, insulators

Scale up to 0.5 m^2 Substrate

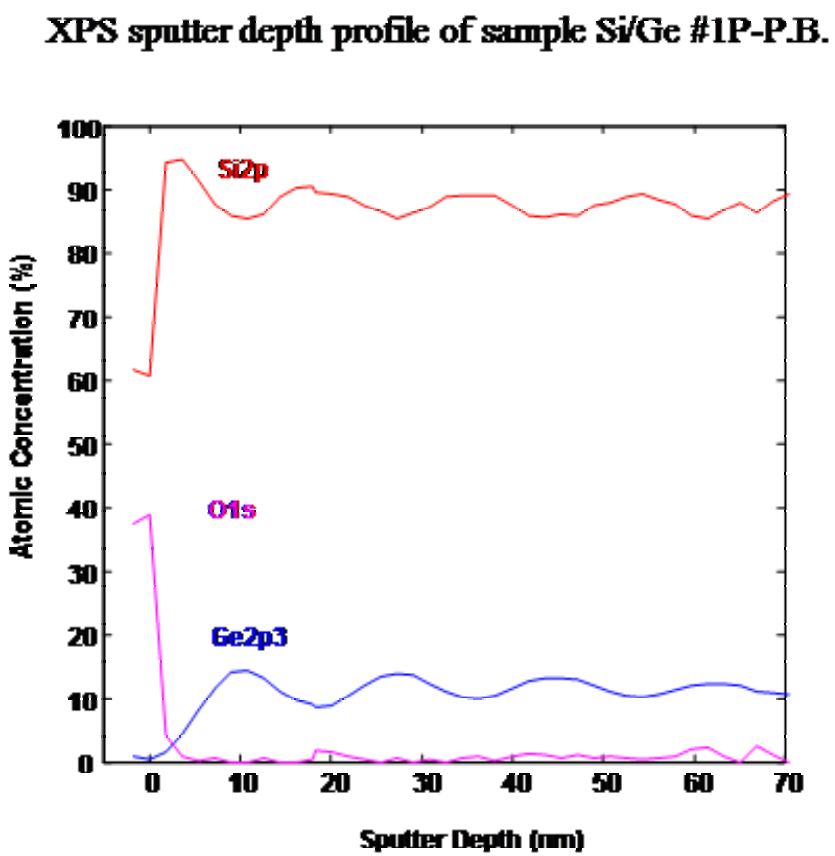


Rocking XRD Spectra of Sputtered Si



150 Å Grain size

$Si/Si_{0.8}Ge_{0.2}$ Multilayer



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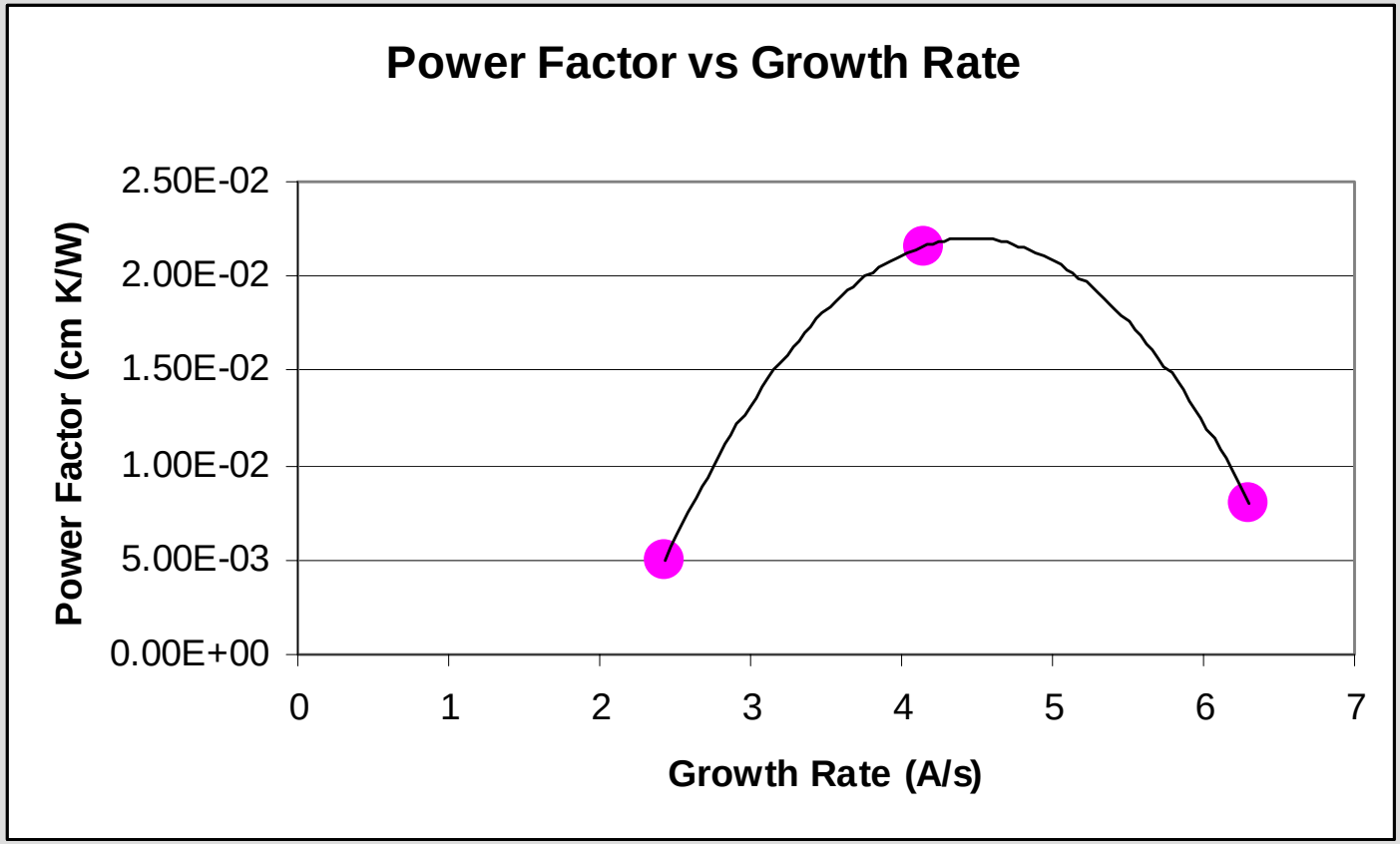
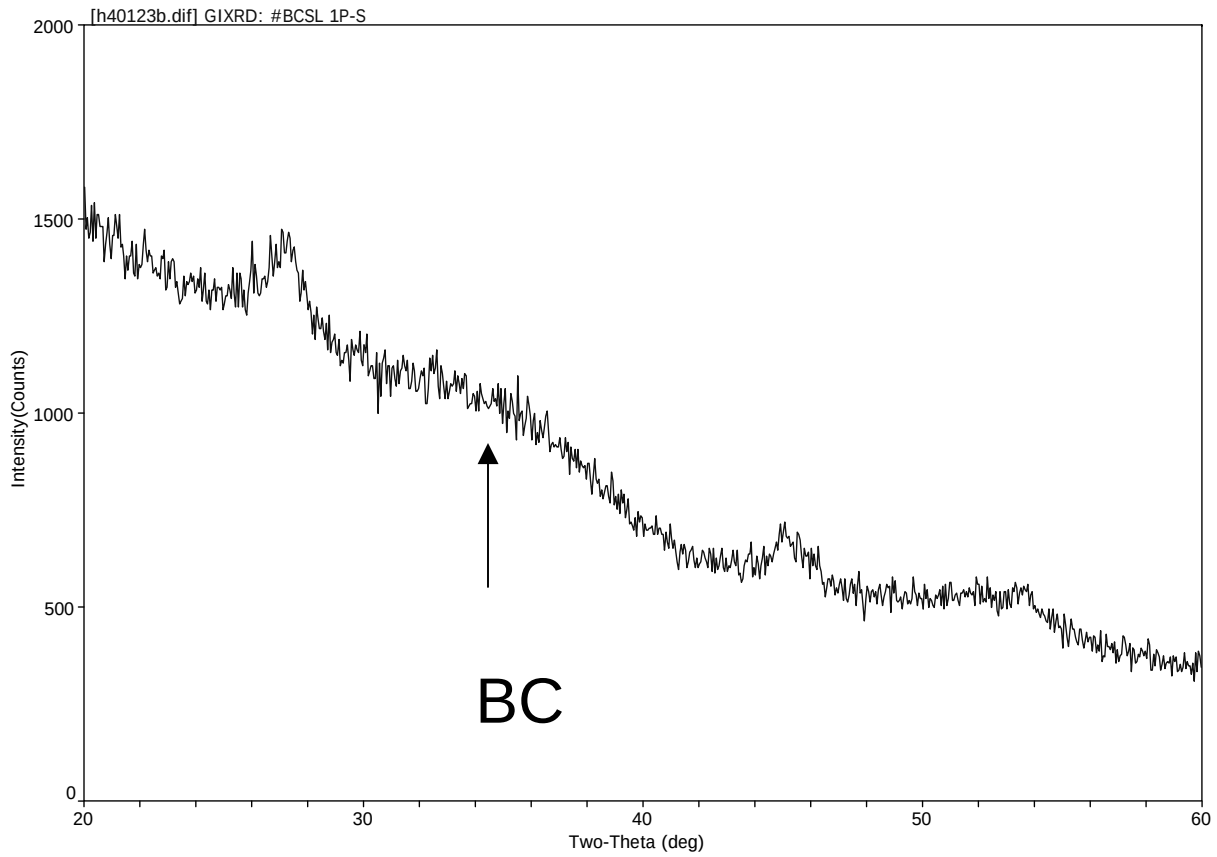
Effect of Deposition Parameters



Sputtered B_4C and B_9C layers

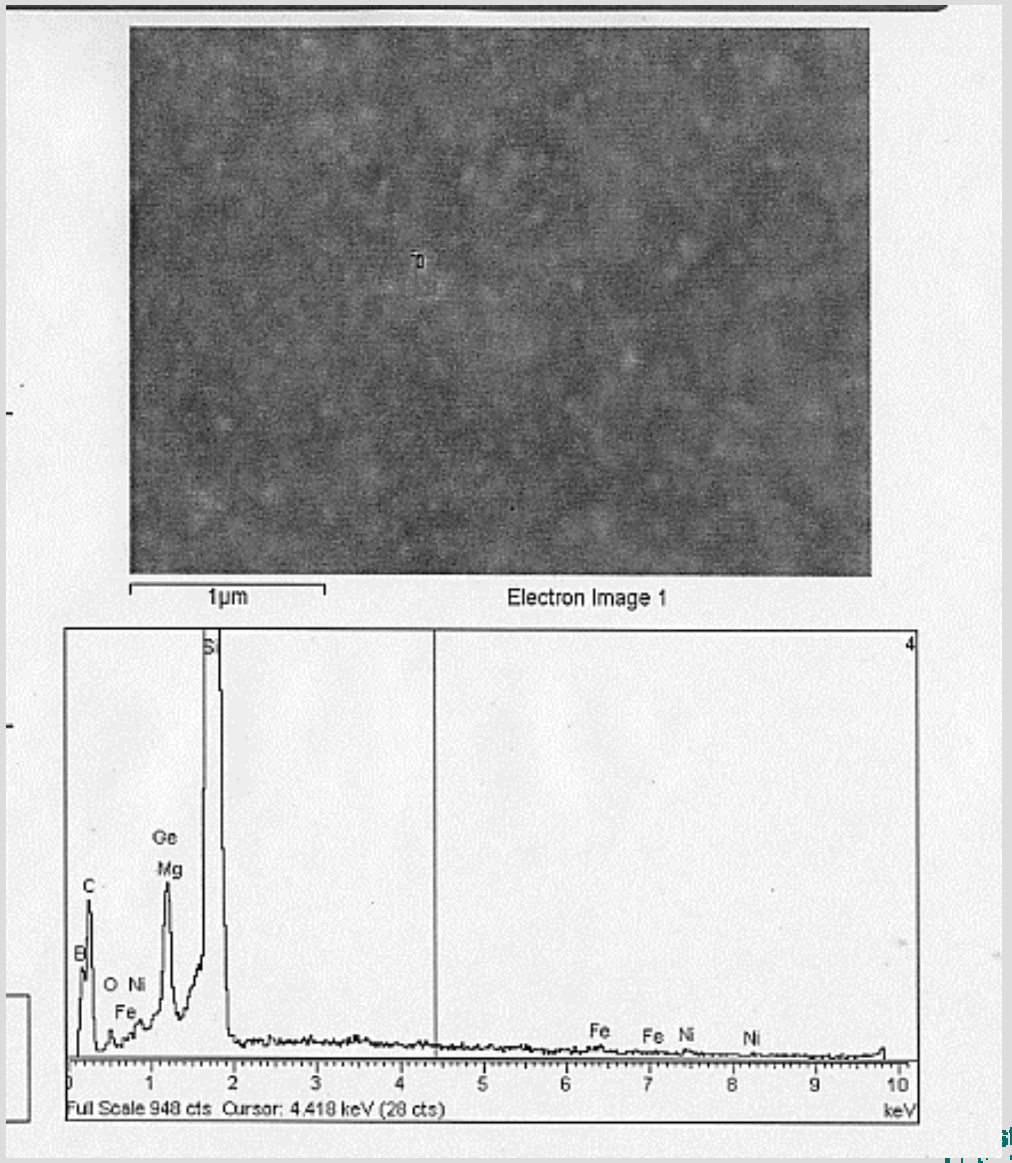
- B_4C and B targets
- Multilayers with 50 – 100 Å thick layers
- Deposit at 400 ºC – 700 ºC
- Heat treat in vacuum at 1000 ºC
- Cosputter with Ge, Si, Fe
- SiC buffer layer
- Insulating substrates (sapphire, fused silica)

Glancing Angle XRD of $(B_4C/B_9C)^{20}$

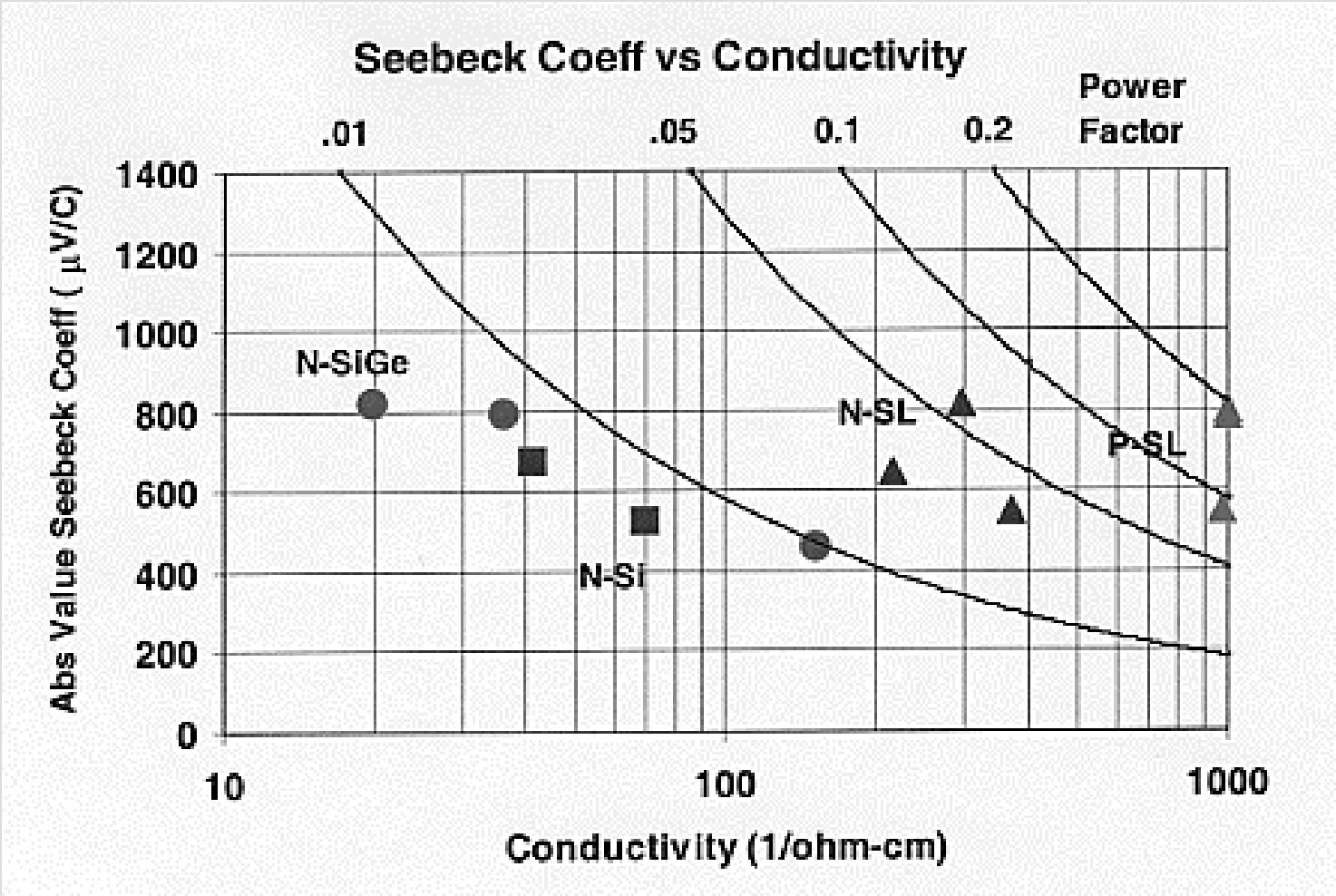


BC-Ge EDX

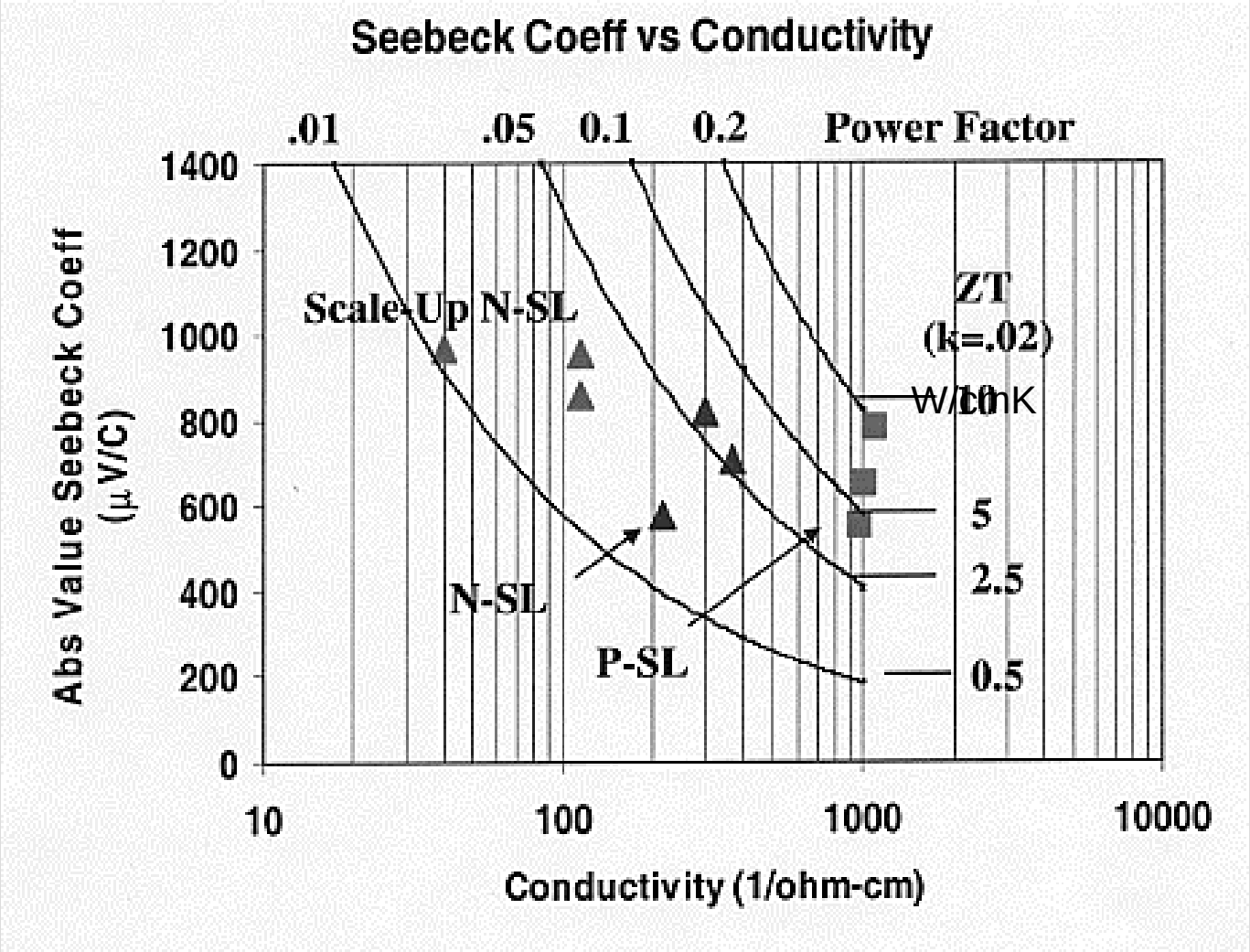
BC Phase



Results for n-type films



$Si/Si_{0.8}Ge_{0.2}$ Multilayers



Si-SiGe Results

Material	Electrical Conductivity ($ohm^{-1}cm^{-1}$)	Seebeck Coefficient (μV/ºC)	Power Factor
N-Silicon	60	600	0.0065
N-SiGe	35	800	0 .0067
N-Si/SiGe ML	300	750	0.051

Results for B-C Films

Sample	Process	σ $(\Omega\text{–cm})^{-1}$	S (μV/ºC)	PF
B_9C-Ge	600 ºC	35	340	0.0012
B_9C-Ge	HT @ 1000ºC	1660	223	0.025
$(B_4C/B_9C\text{-}Ge)^{20}$	600 ºC HT@1000 ºC	2560	201	0.031
$(B_4C/B_9C\text{-}Ge)^{10}$	600 ºC	4160	233	0.068*
B_9C/ sapphire	600ºC HT @ 1000 ºC	118	170	0.001

* Increased Ge doping

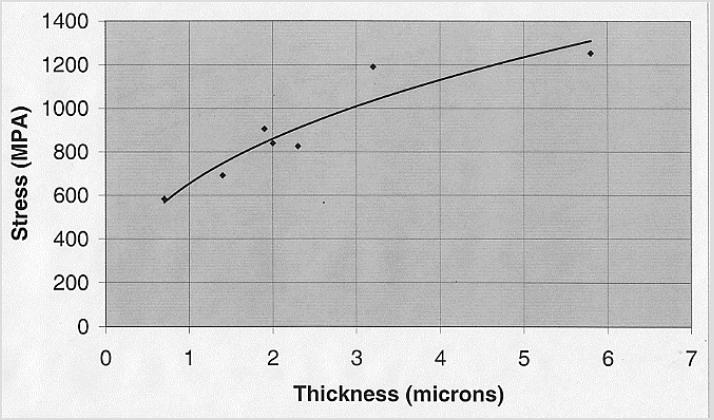
What Works Best

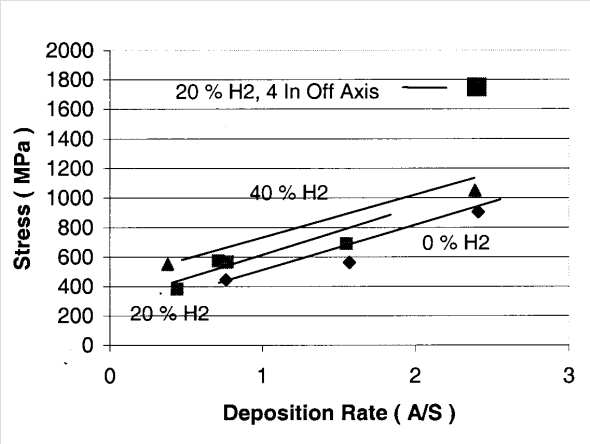
- $(Si/SiGe)^n$ deposited at 400 ºC on Si
  - Undoped
  - B-doped
- $(B_4C/B_9C)^n$ doped with Ge on p and n-type Si
  - Deposited at 500 – 700 ºC
  - Post deposition heat treat at 1000 ºC
  - Sapphire, fused silica show promise
- $(B_4C/B_9C)^n$ on p and n-type Si
  - Deposited at 500 – 700 ºC
  - Post deposition heat treat at 1000 ºC

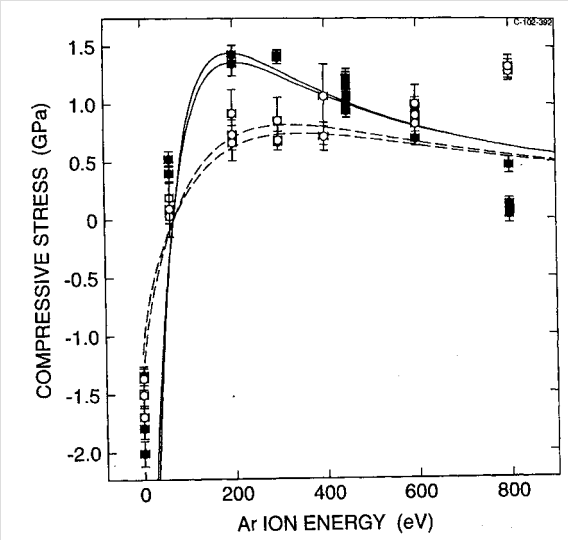
Mechanical Properties are Important!

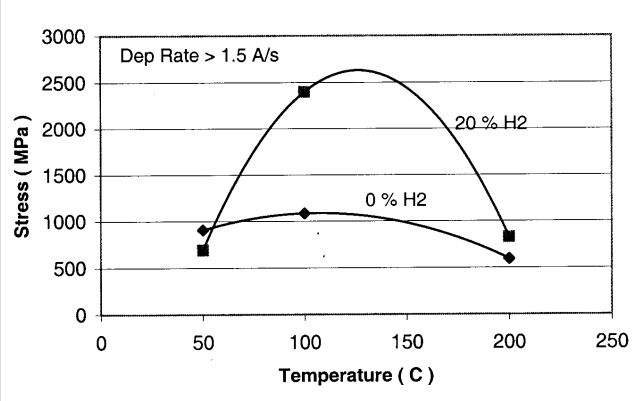
- Stress cracking and deformation must be controlled over large areas
  - Thin substrates
  - Deposition conditions
  - Post deposition annealing
  - Microstructure
- Adhesion
  - Substrate cleaning
  - Ion etch
  - Buffer layer
- Elastic properties
  - Ductility
  - Microstructure
- Hardness

Mechanical stress issues

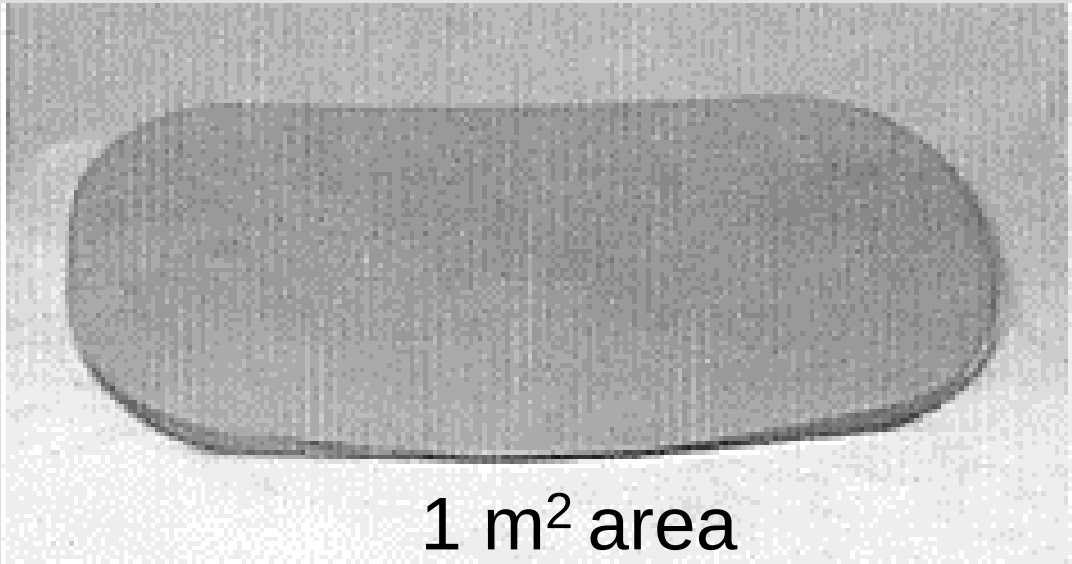






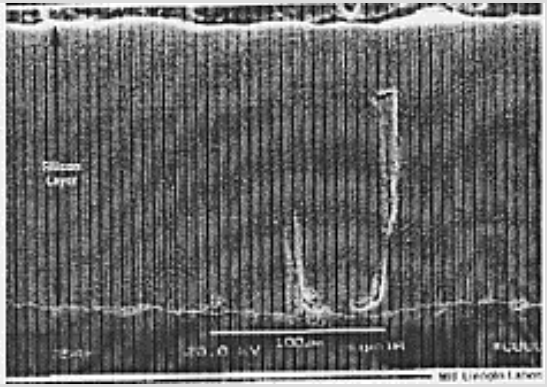


Ultrathick Si Films:
Large Area Film with Stress Control



1 m^2 area

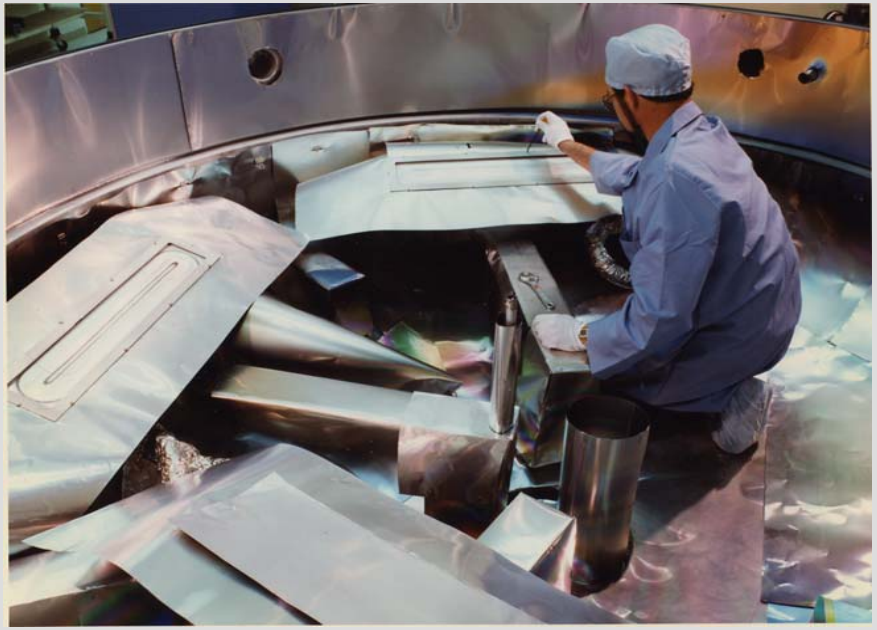
Diamond Turned SiC Telescope Mirror

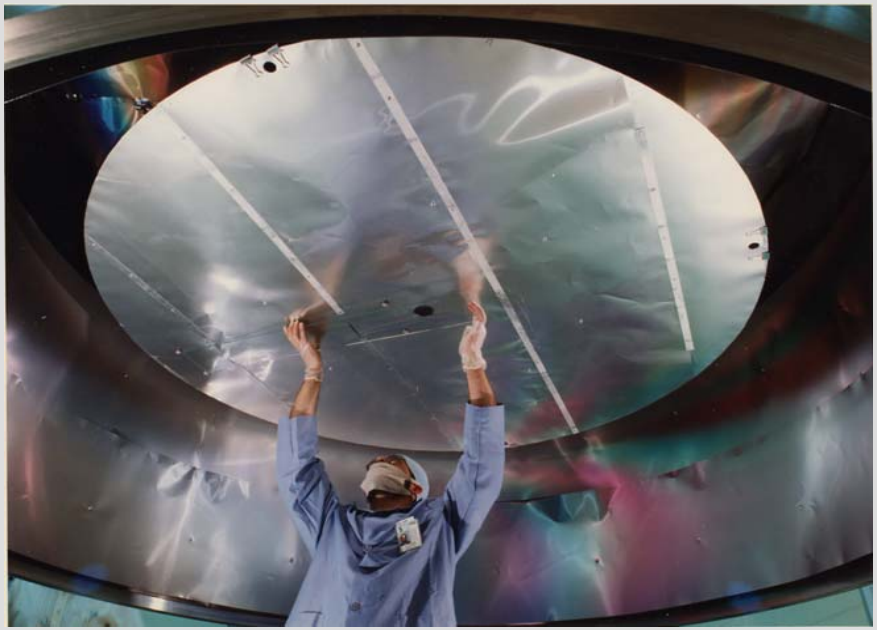


170 μm thick

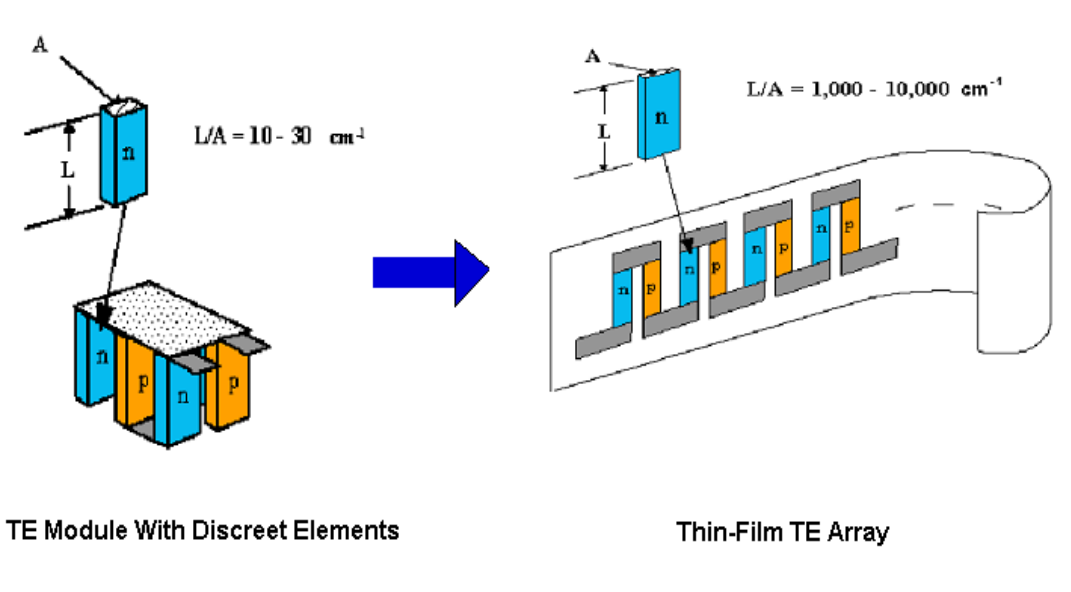
Future Scale up

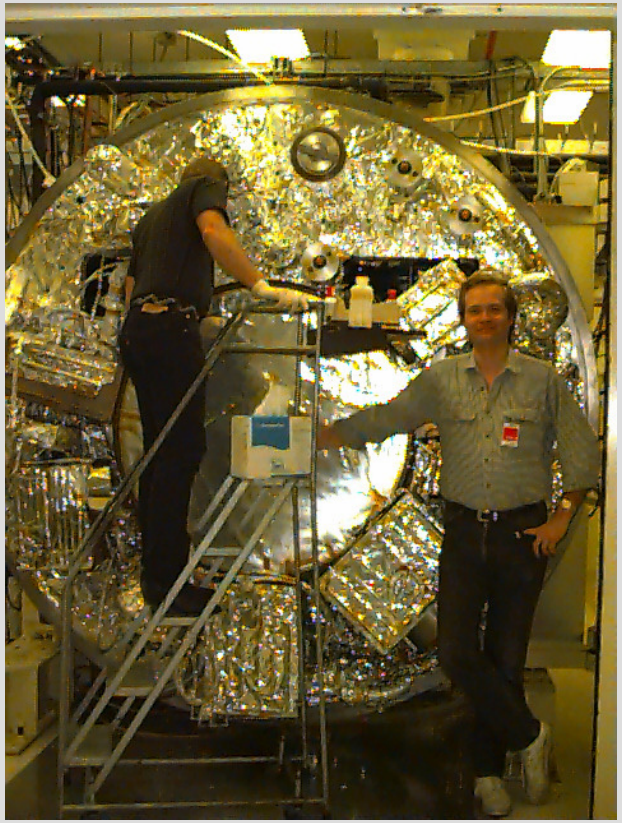
Low cost production





TE Films on Flexible Plastic Substrates





Summary

- The process for depositing multilayer TE films has been scaled up to 0.5 m^2 substrate size
- Multilayers have improved TE properties
- Best results to date for:
  - $(Si/SiGe)^n/Si$ deposited at 400 ºC
  - $(B_4C/B_9C)^n/Si$ deposited at 500 – 700 ºC
    - Ge doping
    - Post deposition heat treat at 1000 ºC
- Several issues must still be addressed for large area deposition
  - Stress control
  - Substrates (insulator, polymer)
  - Producibility for implementation into a power generating device