Cool Chips™
Power Chips™

High Efficiency Cooling and Power Generation Using Electron Tunneling

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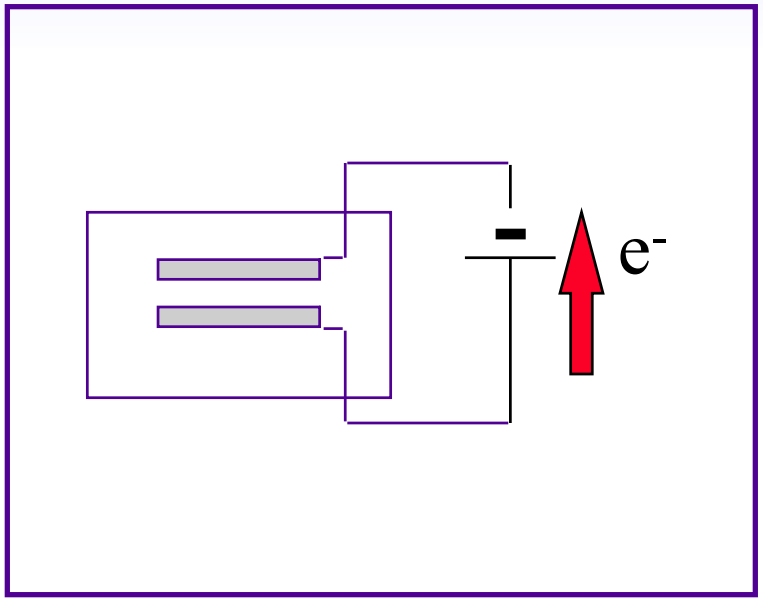
Technology Introduction



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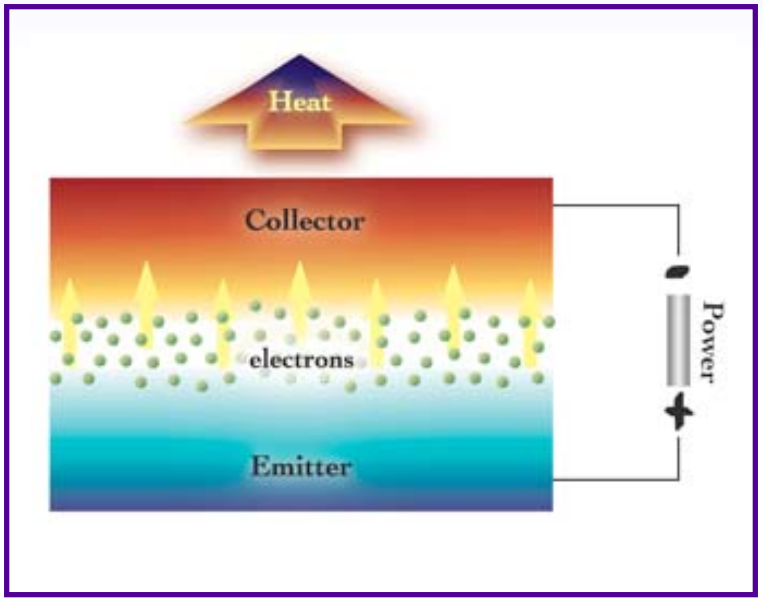

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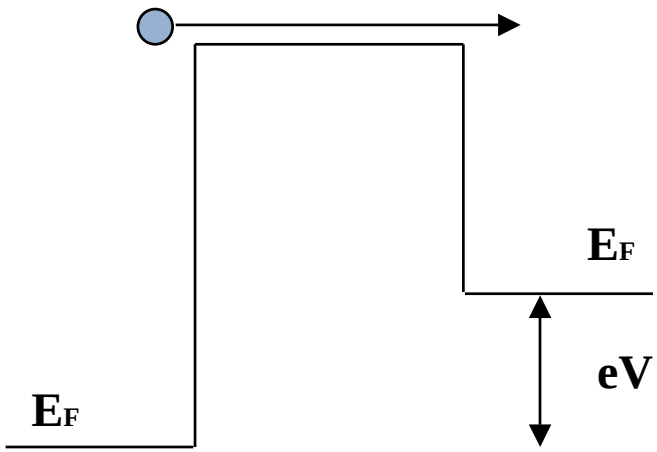
Physics Overview

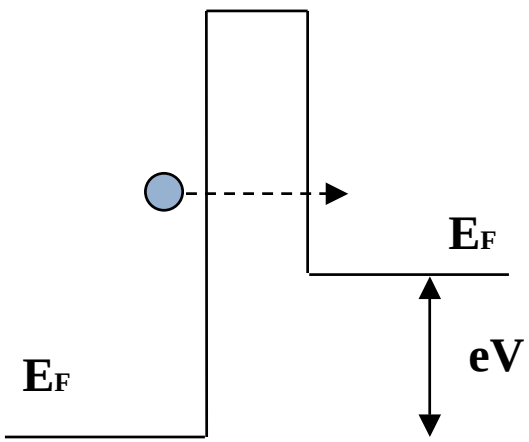
Thermionic Converter
>1700K

d=0.1-0.5 mm



Thermotunnel Converter
1K-2000K

d=1-10 nm



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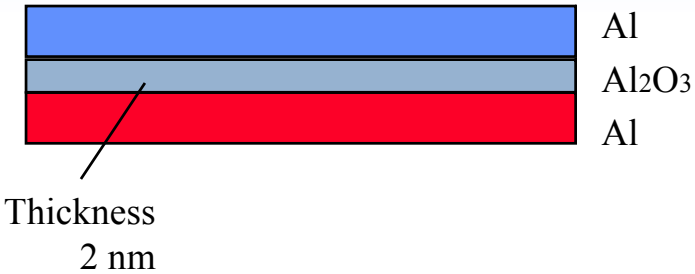
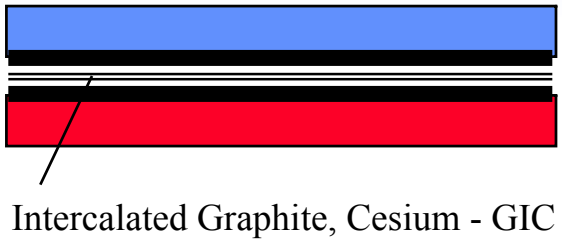
Prior Devices - Ambient

F.N. Huffman, 1965[+]



F.N. Huffman, 1985[≠]



[+] F.N.Huffman et. al.. "Thermotunnel Converter" patent 3,169,200 (1965)

[≠] F.N.Huffman (1985)

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Prior Devices - Cryogenic

A. Luukanen et. al. 2002
260mK - 80mK

A. Luukanen et. al. "Integrated SINIS Refrigerators for Efficient Cooling of Cryogenic Detectors" published in C.P.605 *Low Temperature Detectors* pps. 375-378. 2002.

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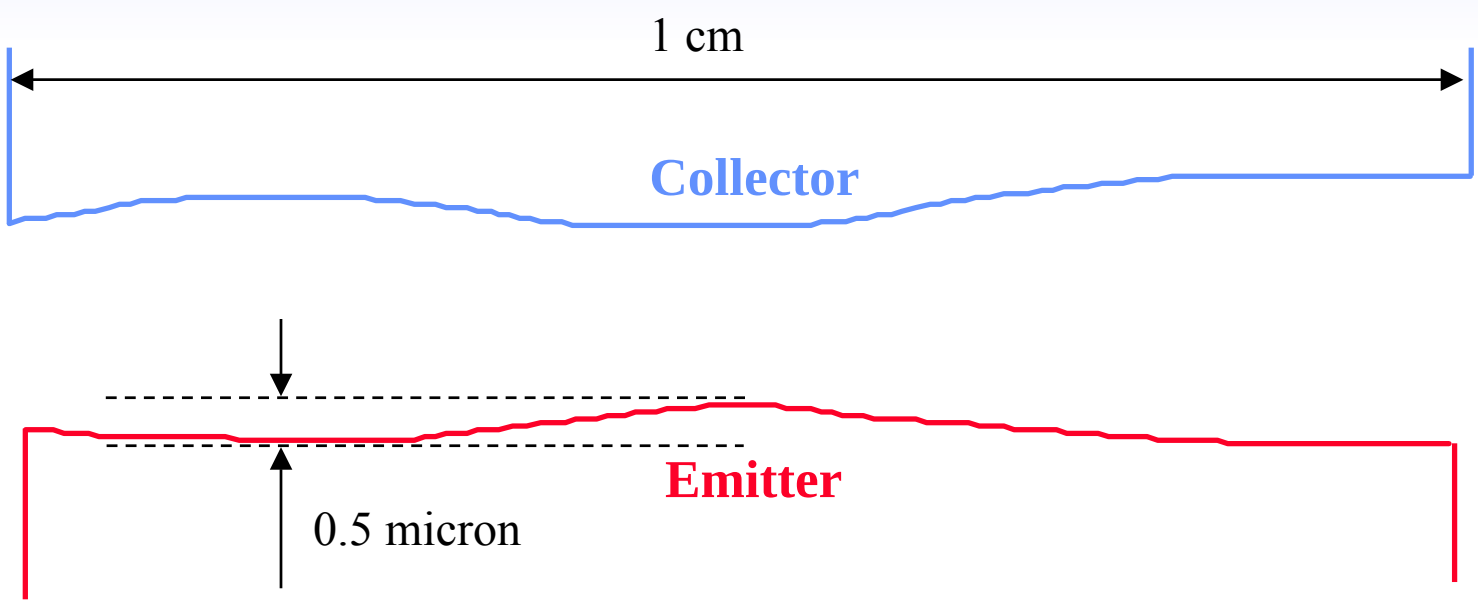
"Sandwich" Development

Limits of Electrode Polishing Technology



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“Sandwich” Development

Matching Collector and Emitter Surfaces

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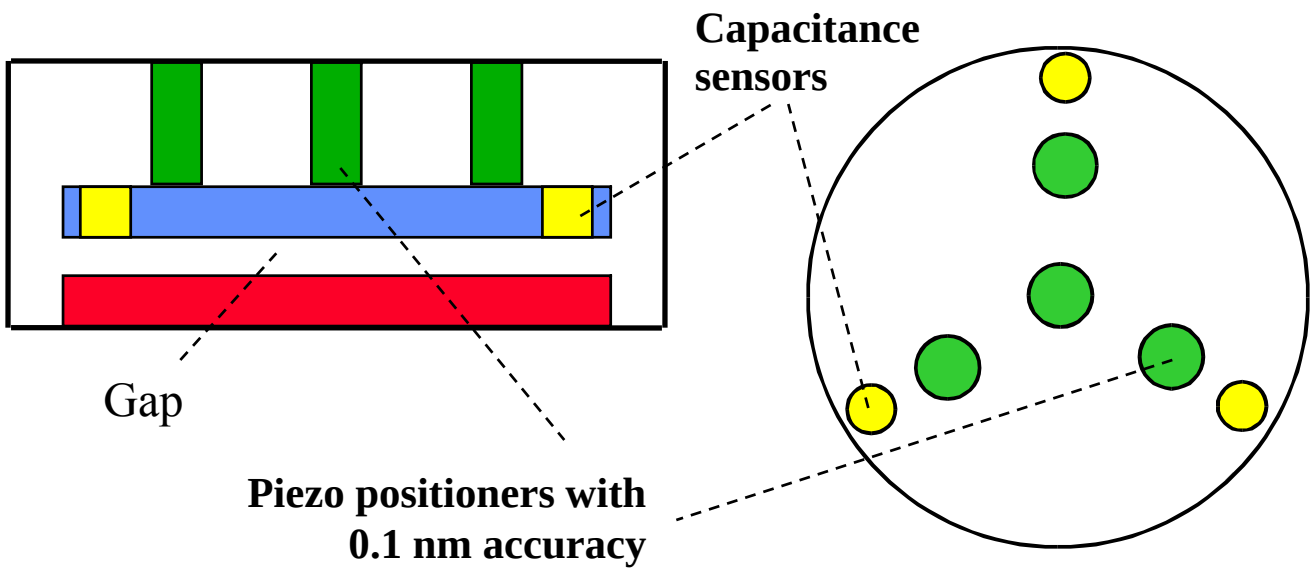
Test Machine

Interelectrode Gap Regulation using Piezo Positioners

Side View

Top-down View



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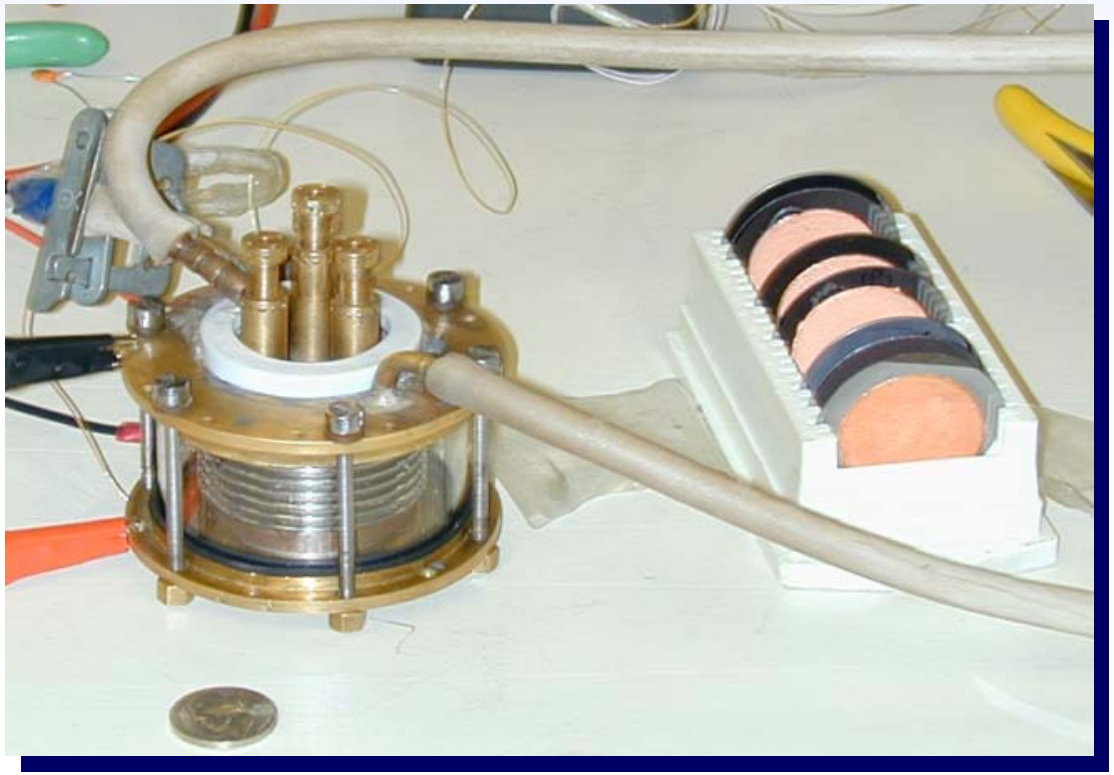
“Sandwich” and Test Machine

Photographs of Sandwich Mounting Inside Test Machine



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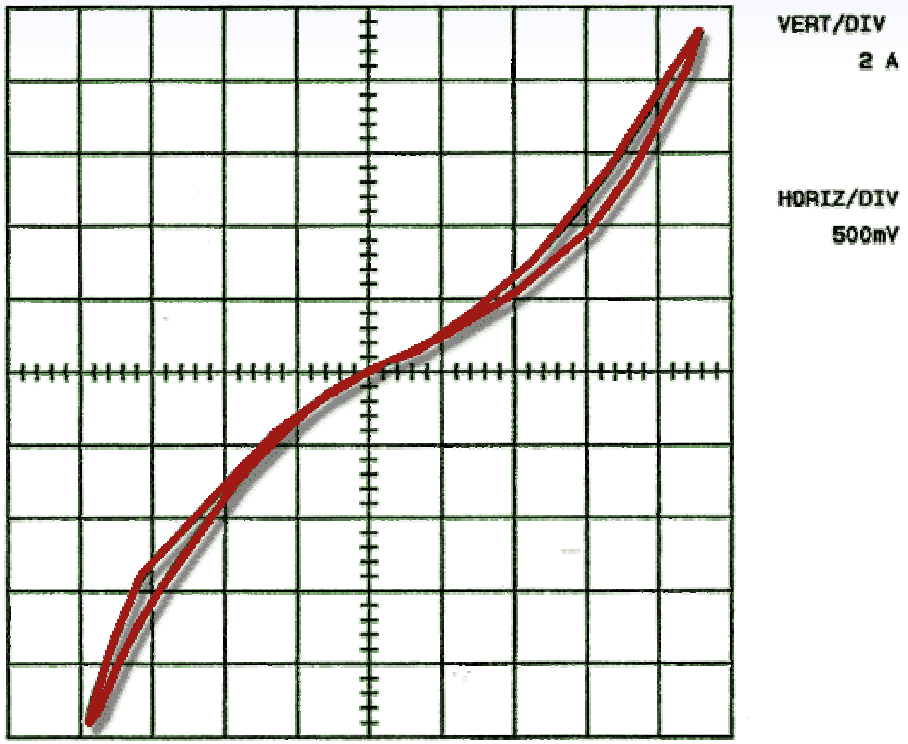
Proof of Concept

IV CURVE



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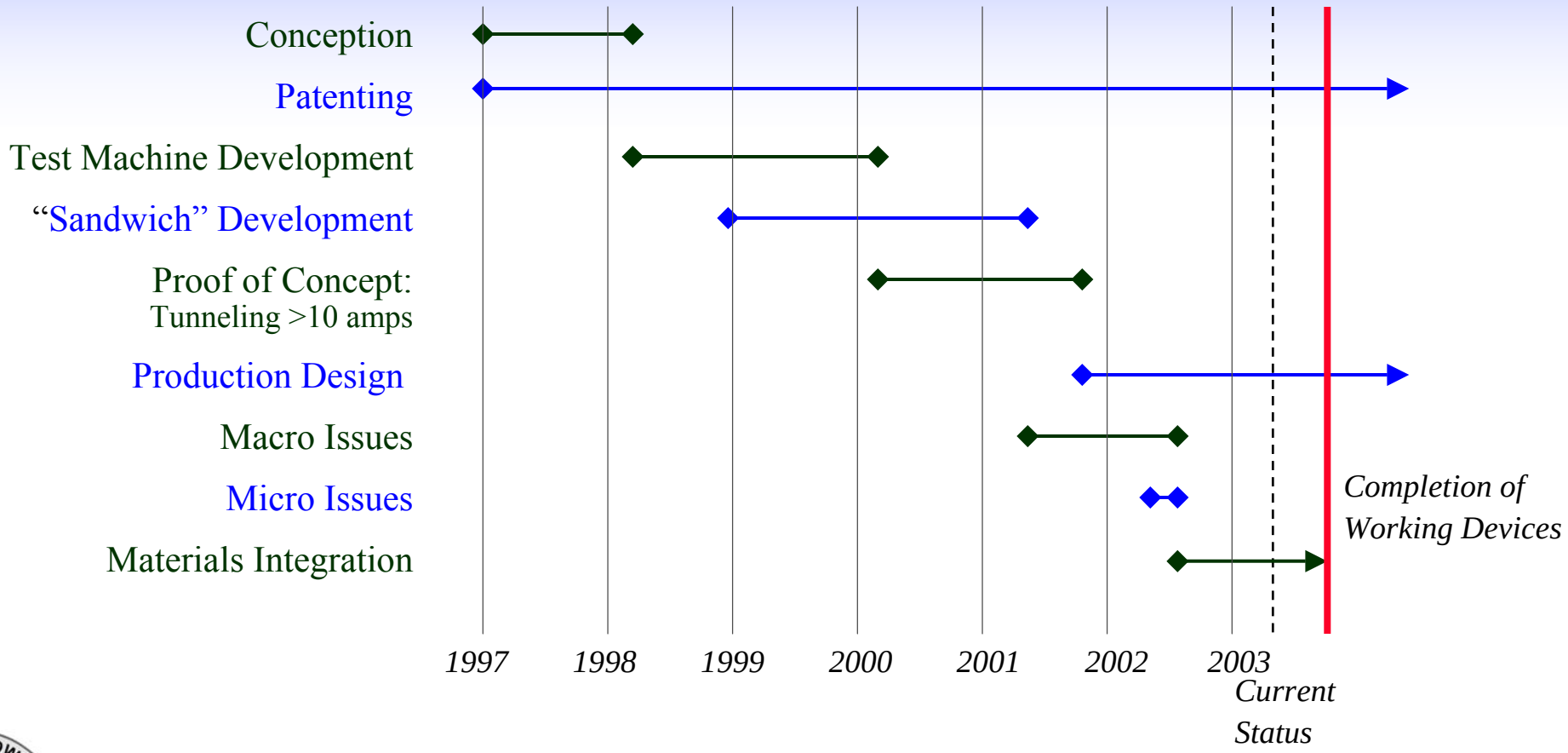
Development Roadmap



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Macro Issues

Tasks

- Development of smaller sandwich (done)
  Reduction of electrode surface area can increase percentage of active area
- Electrochemical growth temperature stabilization (done)
- Better control of production steps (done)
  Increased control and understanding of these steps will increase yields

Dozens of stress free, conformal wafers have been completed.

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Micro Issues

SEM and Profilometer testing revealed that there are no local roughness issues precluding the fabrication of high output devices, once the necessary electrode material has been integrated.

The smoothness of the wafers are as shown in the following slides.

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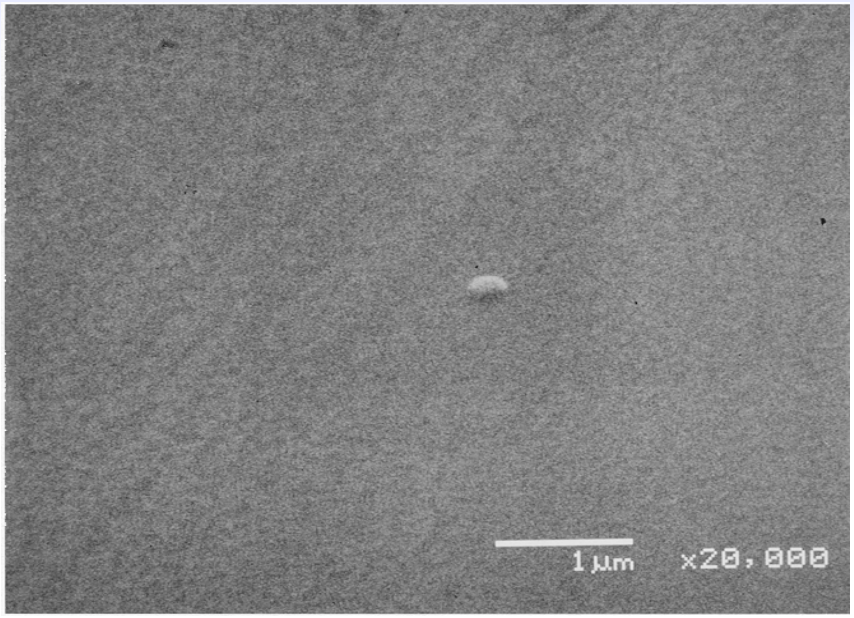
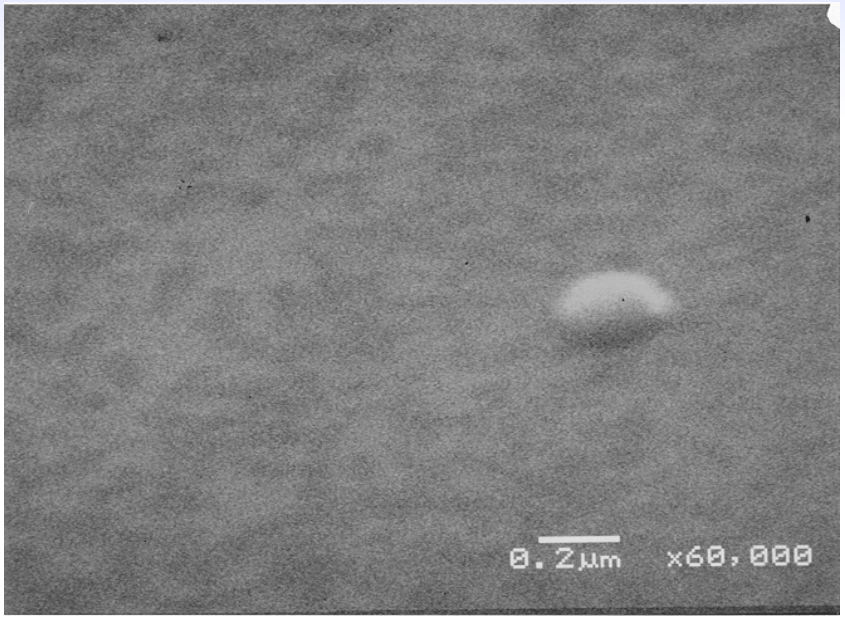
Micro Issues - SEM Imaging



Titanium Surface at 20000X



Titanium Surface at 60000X

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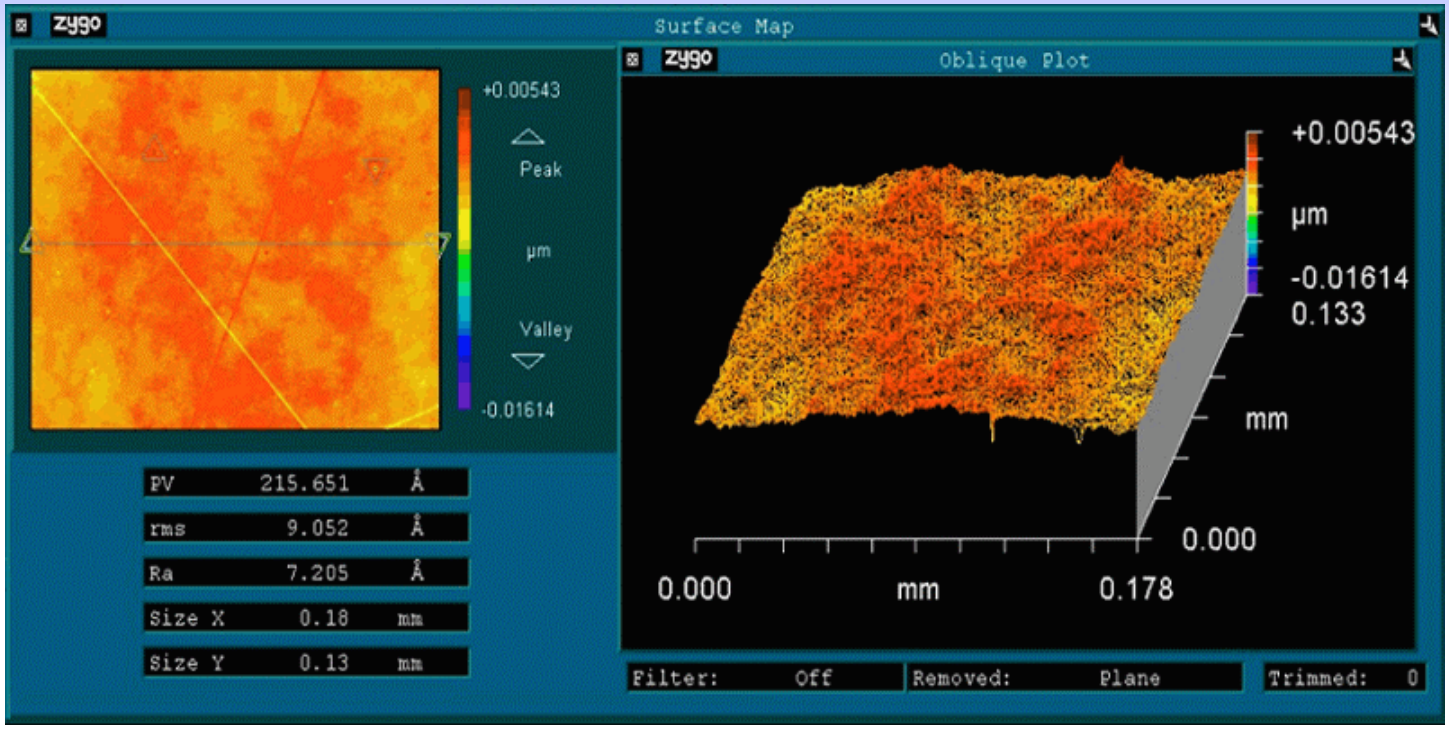
Micro Issues - Profilometry



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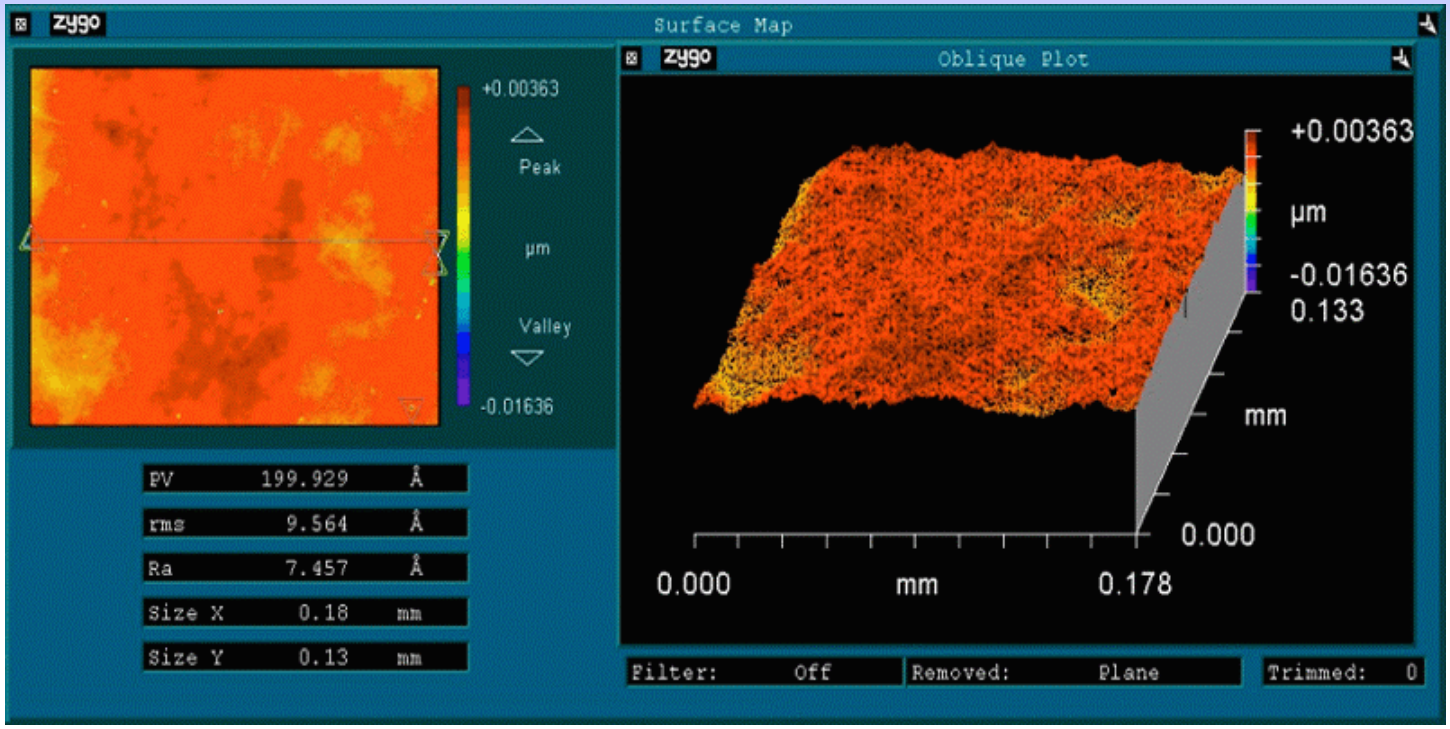
Micro Issues - Profilometry



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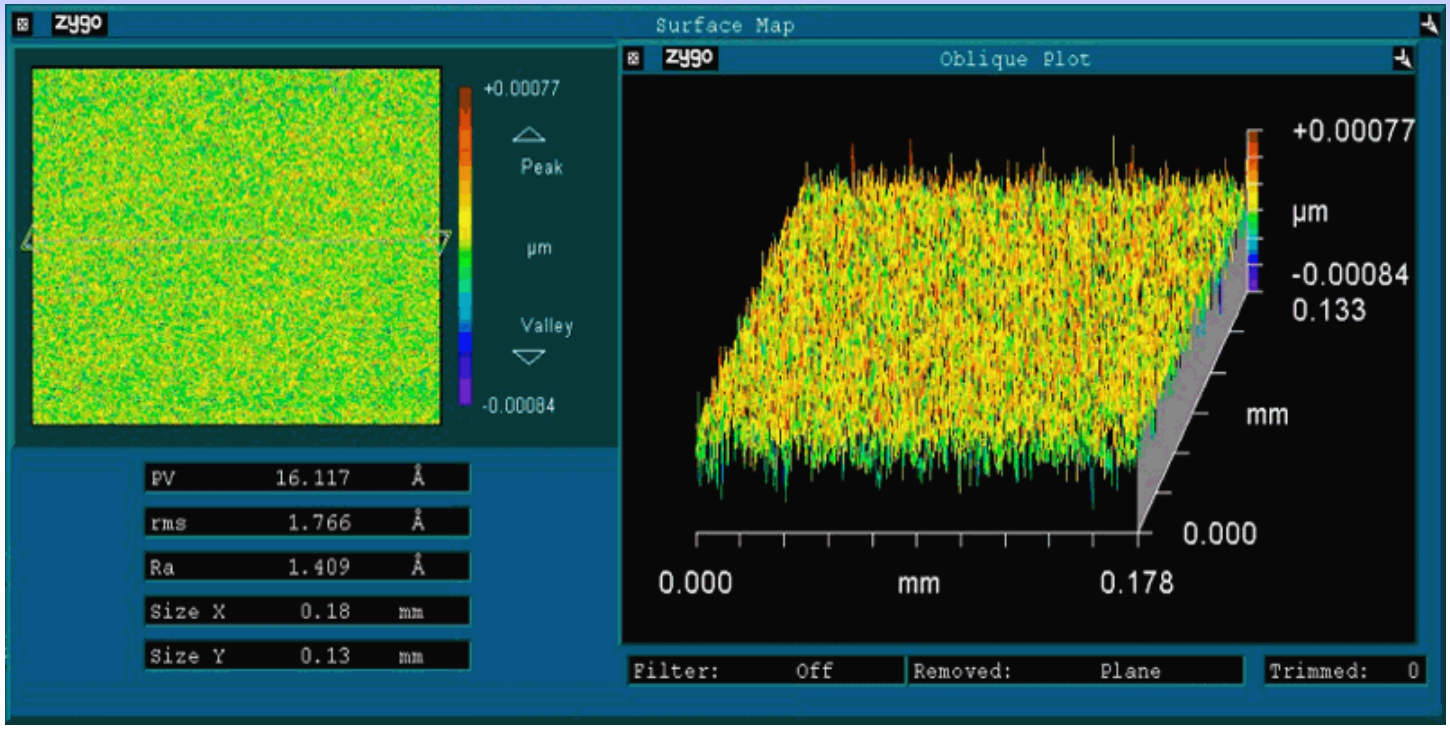
Micro Issues - Profilometry



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Materials Integration

Tasks

- Select thin films (cesiated materials) for a given thermal regime
- Integration of films

Work has commenced, and is expected to take some months to complete

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Conclusion of Development

Once prior steps are complete, high output, high efficiency Chips will be ready for:

- Application in low-volume applications
- Transition to mass production in dedicated fab

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Efficiency Calculation

Types of Calculations

- Intrinsic Efficiency
- Practical Efficiency

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Efficiency Calculation

Intrinsic Output Calculation

- Intrinsic output calculations were developed at Stanford[+]
  - Output up to 5000 watts/cm^2 is projected for room temperature cooling.

- Projected intrinsic efficiency for Cool Chips is on the order of 65% of Carnot at outputs of 3-5 watts/cm^2.

[+] (Hishinuma Y, Geballe TH, Moyzhes BY, Kenny TW (2001) Refrigeration by combined tunneling and thermionic emission in vacuum: use of nanometer scale design. *Applied Physics Letters* **78**(17):2572-2574)

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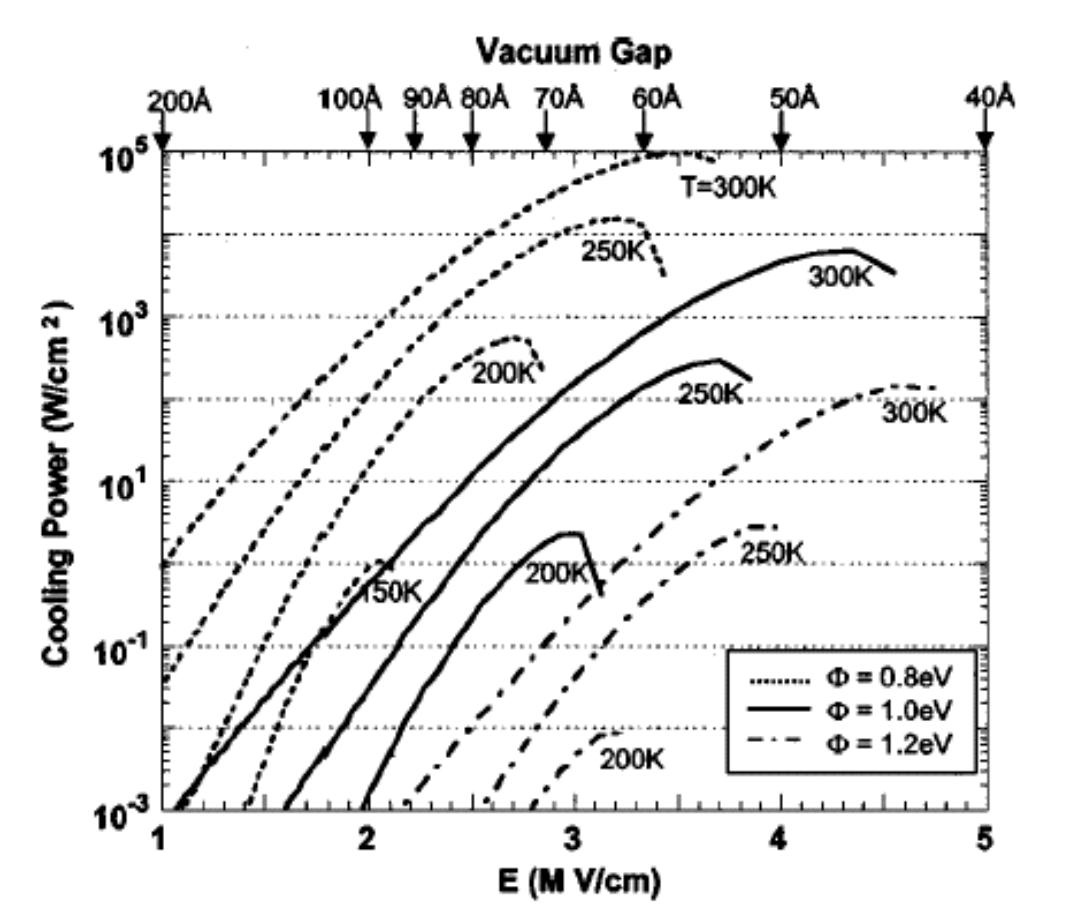
Theoretical Output



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Efficiency Calculation

Practical Losses

Loss terms for Cool/Power Chips™ include:

- Resistive heating
  - *Proportional to output*
- Radiation
- Residual gas
- Thermal backflow
  - *Higher output, higher efficiency*

As losses are temperature dependent, they are all calculated as a percentage of Carnot efficiency

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Efficiency Calculation

Radiative Losses

Radiation losses are proportional to $T_{hot\ side}^4 - T_{cold\ side}^4$.
Dropping the temperature by a factor of 5 reduces radiation losses by factor of 625.

The Stanford paper predicts <0.1 W/cm^2 at room temperature for black box radiation. Real losses are lower.

Effect on Carnot Efficiency
Radiation losses are negligible (<1%)

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Efficiency Calculation

Residual Gas Losses

Residual gases, a product of all imperfect vacuums, will be an additional efficiency loss term.

Effect on Carnot Efficiency

<1% due to the small distance between the emitter and collector, which is less than the mean free path of the gas electrons:

http://www.electronics-cooling.com/html/2002_november_techdata.html

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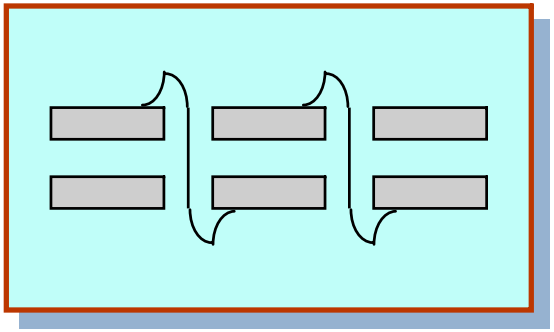
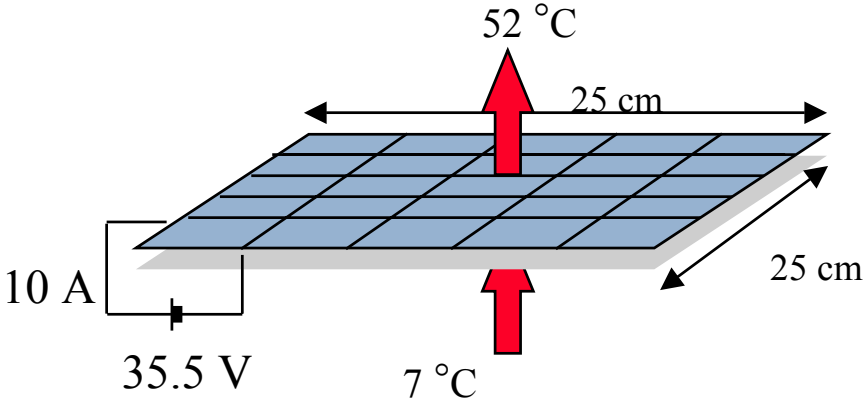
Efficiency Calculation

Resistive Losses and Heat Conduction Losses via
Electrical Connections in an Array





Effect on Carnot Efficiency

Using copper, the losses are ~12%, depending on assumptions.
If additional losses acceptable elsewhere,this is halved.

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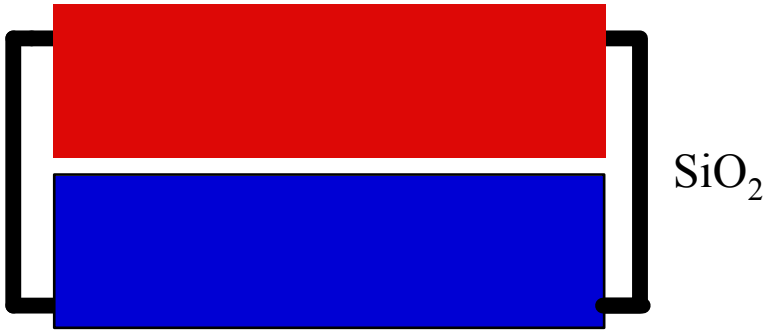
Efficiency Calculation

Thermal Backflow Losses from Separation

- These losses are geometry dependent
- To minimize separation losses, edge supports will be used, with no internal spacers. Thermal back-path is thereby minimized



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Efficiency Calculation

Thermal Backflow Losses from Separation

$$= (\Delta T)\lambda\left(\frac{A}{l}\right)$$

A=cross-sectional area
l = length

Geometry and materials will determine the precise separation loss. These will be selected based on device temperature range, efficiency, cost, and other requirements.

Effect on Carnot Efficiency

Production devices will vary

Prototype has a separation loss of <1.2 x 10^{-3} watts per degree Kelvin ΔT, or <1%

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Efficiency Calculation

Total Practical Losses

Given the assumptions used in these calculations, total practical losses are on the order of 15%

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Efficiency Calculation

Overall Efficiency

Combining Intrinsic and Practical loss terms, approximate efficiencies are:

50-55% of Carnot

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Fabrication

Cool Chips share many design elements with semiconductors, and have precise, but simple construction requirements.

- Non-exotic materials with moderate contamination tolerance
- No costly materials involved in processes
- Very small devices require small amounts of material
- Designed for rugged environment

Cool Chips should be affordable in Mass Production

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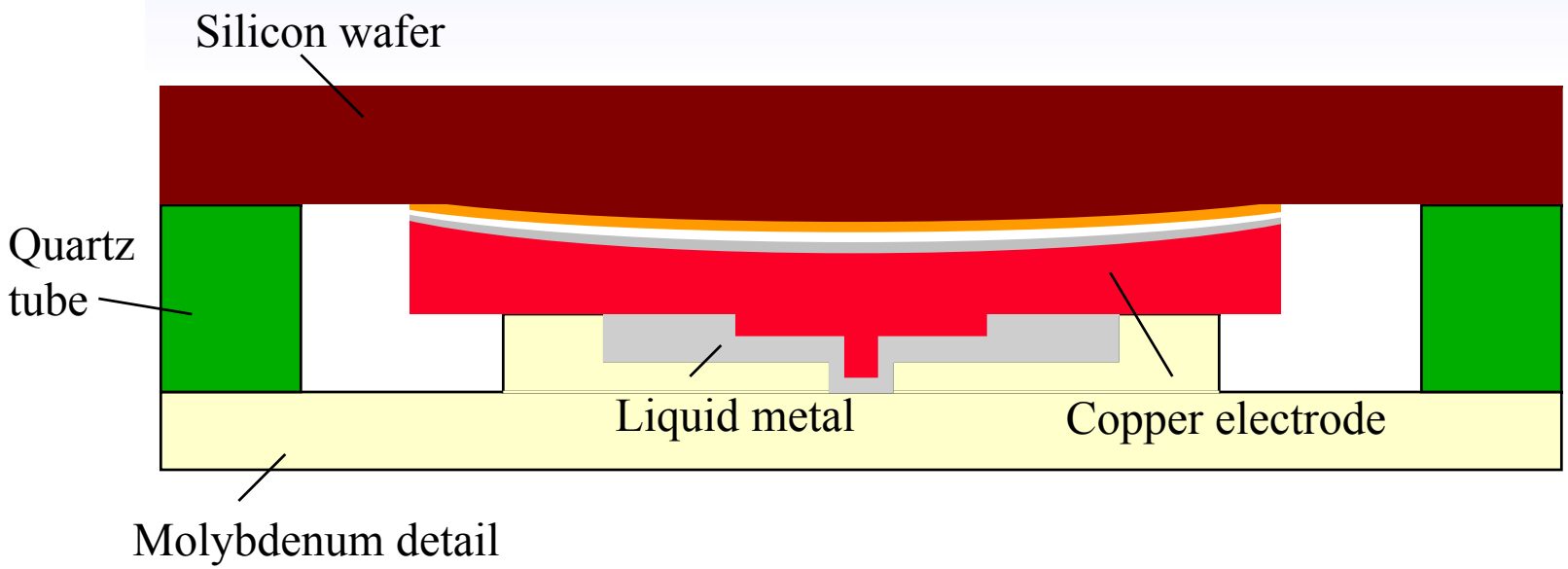
Production Design

Quartz/Piezo Chip



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The Big Picture

Cool Chips are projected to be a superb way to actively cool.

… Inexpensive to manufacture, and maintenance-free in operation
… Small and Lightweight
… Highly Efficient
… Robust, for use in hostile environments

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Critical Patent Claims

>17 issued patents to date cover the following core concepts:

- Cooling using a gap-diode
- Low temperature thermionic thermal conversion
- Thermotunneling across at least a partial gap for Sandwich replication technique
- Methods of assembly, manufacture, packaging, and applications

More than 20 additional patents are pending

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Corporate Overview

Cool Chips plc

- Founded in 1996, as a subsidiary of Borealis Technical Limited.
- Formally incorporated in Gibraltar on April 23, 1996.
- Publicly traded (Pinksheets: COLCF) since April 24, 2002
- Capital Authorized: 10 million shares.
- Capital Outstanding: approximately 7,840,000 shares.
- Over 500 shareholders.
- Holds exclusive worldwide license to all Cool Chip™-related Intellectual Property, past, present, and future. Seeks to license the technology to world class companies.

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