A [illegible] KA PULSED DC POWER SYSTEM WITH COMPUTERIZED THYRISTOR TRIGGERING *

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Summary

A pulsed dc power system provides 120 kA excitation current for the ORMAK toroidal field coils. A drive potential of 1000 volts brings the coils up to full current in about 0.5 seconds. Constant current is maintained for 0.25 seconds, then approximately 20×10^6 joules of stored energy is dumped in a free-wheeling diode and resistance network. The power system contains 8 each, 30 kA, 500 V thyristor controlled dc power modules in a series/parallel combination. A control computer generates thyristor trigger pulses in a programmed sequence as required for the desired duty cycle. A feedback network including current sensing and computer software permits trigger timing adjustments as necessary for constant current operation.

Introduction

ORMAK in its present configuration[1] is capable of operating with toroidal field, TF, intensities of up to about 18 kG. Using a set of four interleaved toroidal windings, the nitrogen-cooled windings are excited by motor-generator sets which supply up to 8570 amperes per winding at 350 volts. A rise time of about 0.30 sec and a flat-top duration of about 0.25 sec are achievable with the present TF power system.

ORMAK upgrading plans require toroidal field intensities of up to about 50 kG. The increased intensity is to be obtained via increasing the TF winding conductor cross section, improving the cooling system, and providing a larger power supply system for winding excitation. This report is restricted to the power supply aspects of the ORMAK improvement program.

Choice of Power System

The power system requirements evolved from constraints dictated by optimum TF winding parameters. Optimum supply voltage could change through sectoring of the TF winding. Basic parameters for the TF winding are listed in Table 1.

Table 1. Proposed ORMAK TF Coil Parameters

Winding configuration	4 interleaved conductors
Inductance (4 conductors in parallel)	2.8 mH
Resistance/conductor at 68°K	1.38 mΩ
Current for 50 kG field	120,000 A
Pulse flat-top duration	0.25 sec
Pulse repetition rate	1 per 3 min.
Approx. mass of Cu conductor	1700 kg
Max. allowable conductor temp.	116°K

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Permissible energy dissipation per duty cycle of the TF winding (about 20 x 10^6 joules) is that which raises the conductor temperature from the base value of 68°K to the upper limit of 110°K.

Options for the type of power system were restricted to those utilizing existing technology; for example, rotating machines (M-G sets), capacitor storage banks, storage batteries, and static converters. Cost and delivery schedule considerations, noted in Table 2, favor static converters. Consequently, a thyristor dc power supply system, henceforth referred to as the OSSPS (ORMAK Solid State Power System) was chosen.

Table 2. Cost and Delivery Comparison for Various Power System Options

Type System	Cost/joule	Delivery Time
Motor-Generator Sets	$ 0.16	2-3 years
Capacitor Storage Banks	0.10	1-2 years
Static Converter	0.05	1 year

The data shown in Table 2 are based strictly on circumstances at ORMAK and should not be taken as empirical cost and delivery information. If any system other than static converters (thyristor power supplies) is considered, equipment resembling the static converter is still required to perform high current switching operations.

Power Supply Configuration

The selection of a power supply configuration was influenced by the availability of a 40 MVA (161 kV to 13.8 kV) substation transformer, and the power supply size limitations of typical manufacturers. Following the recommendations of our consultants[2] on primary power substations, the maximum allowable pulse load on the substation was set at about 90 MVA. By using four power supplies to drive the four respective TF winding sectors, the duty cycle illustrated in Fig. 1 is possible. Direct current rise time is limited by the maximum dc voltage which in turn is limited by the substation peak load rating as well as the converter impedance.

For maximum flexibility and operating parameters common to industrial equipment, each of the four power supplies was split into a series pair of modules rated at 500 volts each. This also provides a convenient means to obtain 12-phase rectification. A simplified schematic of the power supply is shown in Fig. 2, and its specifications are listed in Table 3.

Table 3. Ratings for each of Four Series Pairs of Power Supply Modules

Open circuit voltage	1000 v dc
Maximum current	30,000 A dc
Voltage at I_{max}	600 v
Flat-Top current regulation	± 0.1% of I_{max}

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Maximum pulse duration at 30,000 A	0.6 sec
Pulse repetition rate	1 pp 180 sec
Primary 3-phase ac voltage	13,800 V
Substation impedance on 40 MVA base	j 15%

Each power supply module contains an extended delta primary and a wye secondary winding. The extended delta provides a ±15° phase shift so that a series combination of modules with leading and lagging connections respectively results in a 12-phase rectification system. Each secondary winding has an 8 equal step, manually connected tap configuration for output voltage variation. Each transformer, Fig. 3, has a full winding leakage reactance rating of j 2% on a 900 kVA base. An aircooled design was chosen so that frequent inspection of the windings is possible.

Some other transformer features include electrostatic shielding between primary and secondary. Balanced winding distribution in the primary and full width sheet conductor in the secondary are used to minimize axial strain. A cylindrical slotted steel coil form is used to minimize radial strain.

The full wave bridge rectifier in each module, Fig. 4, includes free wheeling diodes with series load dumping resistors. Each module actually contains five bridges in parallel, and ten diode-resistor networks in parallel. The thyristors are Westinghouse T920 series devices with continuous dc current and voltage ratings of 1000 A and 1200 V, respectively. During the pulse duty cycle, each device operates with up to 6000 A of dc current for a 120° conduction cycle. The load dump resistors are designed to limit reverse voltage in the TF winding to 1000 volts at 30,000 A.

The rectifiers are capable of operating in a regenerative (dc to ac conversion) load dumping mode. However, rapid external dumping of energy stored in the TF winding is the primary objective, and resistive dumping is more effective. At peak current, the stored energy is 20 megajoules and approximately 16 megajoules can be dumped in the resistive lead. The remainder is lost in the TF winding.

The short duty cycle-low repetition rate operation characteristics of the power system permits the use of relatively small components to handle enormous quantities of power. Under steady state conditions the maximum power rating of the entire system is approximately 8 to 10 MVA vs the 90 MVA pulse rating. Since a duty cycle overrun could be extremely destructive, the control system requirements are rather stringent.

Auxiliary circuits in the power supplies include optical coupling in the thyristor gate drivers and in the dc voltage and current measurement instrumentation. The gate drivers are triggered by TTL logic levels from a control computer. Fiber optic coupling between input and output stages provides isolation suitable for about 5 kV. The output stage of each driver is transformer coupled to its 5 respective thyristors. The voltage and current measurement circuits include fiber optic coupling and signal conditioning so that floating 0 to 10 volt analog signals are available from each for computerized monitoring.

Conduction monitoring of each individual thyristor is necessary, since a misfire in some units may cause unreasonable overloads in others. A Reed switch on axial strain. A cylindrical slotted steel coil form is used to minimize radial strain.

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Conduction monitoring of each individual thyristor is necessary, since a misfire in some units may cause unreasonable overloads in others. A Reed switch on each thyristor lead actuated by conduction of the respective device triggers a bistable flip-flop to the "on" state. When all flip-flops are "on", a reset signal is generated and the cycle repeats. If one or more thyristors are not conducting, the respective flip-flops remain "off" and the reset cycle is interrupted. A monostable flip-flop with a 30 msec delay is normally continually retriggered by the reset cycle. Failure to retrigger produces an interrupt logic level for the control system. When trouble shooting, one can check the annunciator circuit boards for unlighted LED's associated with respective flip-flops to

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determine which thyristors, if any, have misfired.

Control System

The OSSPS duty cycle is typically less than 1 sec and the total number of thyristor gate pulses required by the 12-phase rectifier is in the range of 500 to 1000 or less. Digital data describing the pulse sequence is easily within the storage capability of a small computer. If one also considers the complexities of an analog control system which is otherwise required for tracking the duty cycle curves in Fig. 1, the preference for a digital control system is especially clear.

OSSPS is controlled by a PDP 11/10 computer with a 16 bit, 16k core; a 1.2 meg.disk; and two 100 kHz clocks. A typical data format for a shot (a complete duty cycle as illustrated in Fig. 1) is simulated in Fig. 5. These data will cause the power system to reach peak current in 0.1 sec (6 cycles) and to maintain a flat-top for 0.1 second. Then the thyristors commutate off and the TF winding or other inductive load current decays in the dumping network. The first data column (A0) in the format represents the time delay from ac zero crossing reference to the firing of the first of 12 gates. The data is loaded into the #1 clock register at t_0 and the first gate pulse (A0) is fired when the register completes its count down (to zero). The remaining data columns represent the time delay from A0 firing to (A1) firing, (A1) to (A2), etc., respectively. A second clock is required for pulses A1 through A11, since clock #1 begins the next row of data before the previous sequence is completed. A data value of 1.39 msec or 139 clock #2 pulses indicates a constant gate phase angle. Data values in the (A0) column are related to the actual phase angle. A data value of 2.00 msec in (A0) corresponds to full forward conduction or maximum voltage, Fig. 6. A value of 6.00 in the (A0) column corresponds to zero forward conduction. A data value of 0.0 at any.point causes the computer to terminate the shot, i.e., discontinue generating gate pulses.

Gate data tables as shown in Fig. 5 are required for each desired level of duty cycle. These tables are stored in the disc memory until needed. A complete table is required in the core memory for running a shot. The data are normally hand calculated and then fine-tuned by trial and error on a sequence of shots. A closed loop mode of operation is available where the computer compares the TF winding current to a reference level and then generates an appropriate gate timing correction to maintain constant current.

The computer collects an assortment of operating data including dc voltage and current in each power supply, and primary line currents at 16.7 msec intervals during each shot. The dc current data is read into the regulator loop and also stored on the disc with the other performance data. At the end of each shot, the performance data can be printed out or permanently stored if desired. Otherwise, it is scratched during the next shot.

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The computer serves many housekeeping functions in the power system. All safety related controls are both computer monitored and hard wired to the primary ac power feeder contactor, but the computer handles most of these functions more expeditiously via its ability to instantly discontinue transmission of gate pulses. Due to the potential hazards associated with shot termination, the systems interrupts are divided into two levels of priority. The first level includes conditions immediately detrimental to equipment, such as vacuum system failure in ORMAK, faults in the power system, thyristor misfire, and loss of primary power. First level interrupts will cause shot termination. The second level includes conditions which may be permitted to continue for the duration of a shot, but require corrective action prior to another shot. Examples are loss of water coolant, overtemperature indications in the transformers or rectifiers, and loss of continuity in door interlock circuits. Second level interrupts will prevent program cycling, but they will not interrupt a shot which is already under way. Generally, the feeder breaker will not trip during a shot except in cases of overcurrent, program overrun, or computer actuated trip.

Ground fault detection is an important consideration with floating power supplies such as in the OSSPS. Due to the short duty cycle nature of the system, on-line ground fault detection does not appear to be practicable. As an alternative, the dc system is automatically hi-potted just before each shot is fired. The computer program calls for the relaying of a high voltage test power supply between each dc bus and ground with accompanying ground leakage measurement. The computer cannot begin a shot until the hi-pot measurement is satisfactorily completed.

Equipment Installation

The TF power supplies are located in a separate shelter outside the building containing ORMAK and its peripheral equipment. Approximately 300 ft of dc bus is required for connecting the TF windings to the power supplies. The control computer is located in a separate room near ORMAK. Operation is accomplished via communication with another computer in the ORMAK control system. The power supply shelter also contains 13.8 kV switchgear and most hardwired control circuitry associated with operation of the feeder breaker. Fig. 7 shows a view of the shelter frame, under construction next to the "ORMAK" building. Fig. 8 shows a view of the 40 MVA substation transformer beneath the 161 kV feeder lines approximately 500 ft away from the power supply shelter.

Preliminary Operation

During the past few months, the power supplies underwent a series of acceptance tests preceding their final installation in the power system. Testing at full power was accomplished by using the dumping network of one series pair of power supplies as the dummy load for another series pair. Some important considerations in these tests included the ability of the transformers to withstand the stresses imposed at full load, and the impact of the TF power supplies upon the primary power system. Thus far, the major components are performing satisfactorily and line interference seems to be at an acceptable level.

When all eight power supplies are operated at full load, the line drop in the TVA system is negligible, but the 161 kV feeder voltage drop at the substation is about 2.3%. Line harmonics are of somewhat greater concern. Operation of one series pair of power supplies into the resistive load with the thyristors

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When all eight power supplies are operated at full load, the line drop in the TVA system is negligible, but the 161 kV feeder voltage drop at the substation is about 2.3%. Line harmonics are of somewhat greater concern. Operation of one series pair of power supplies into the resistive load with the thyristors phased back about 60° (half voltage) causes a peak harmonic amplitude of about 8% of fundamental to appear on the substation secondary. The peak amplitude corresponds to the beat frequency from the 11th and 13th harmonics which one expects for a 12-phase rectifier system. The substation to feeder line impedance ratio is about 15/1; therefore, the harmonic amplitude seen on the 161 kV feeder should be less than 0.5% for the single series pair of power supplies or 2% for the entire system. Efforts are under way to measure line

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harmonics in neighboring facilities, but results are inconclusive at this time.

Test operation has also been accomplished with an an inductive dummy load. Time constants are similar to the ORMAK TF winding, but the maximum allowable current is only 10,000 A. Efforts to generate a flat-top with the control computer were successful using estimated values for thyristor gate timing data and some trial and error fine tuning. It appears that open loop performance is adequate for ORMAK operation.

An interesting problem encountered during the tests with the inductive load was the effects of losing primary ac power during a shot. Normally, the thyristors will commute off when the computer stops supplying gate drive pulses. However, when primary ac power is lost, commutation is not possible and those units which are in conduction become trapped with the full dc load current while the stored energy in the inductor decays. Under some conditions this could overload the thyristor ... take out their protective fuses. (The fuses are quite expensive although much less expensive than thyristors.) Further, this could cause excessive energy dissipation in the TF winding since the load dump circuit cannot conduct until after the fuses clear. We hope to avoid the problem by carefully monitoring ac supply voltage and terminating a shot at the earliest indication that the primary ac power is dropping out. Typically, commutation voltage should be available for at least a few cycles following trip initiation in a feeder breaker.

Conclusions

Installation of the OSSPS is scheduled for completion in March 1976. Design effort is under way to provide a bus switching network that will allow the OSSPS to provide toroidal field excitation for the ISX facility which is to be located near the ORMAK facility. Since the TF power requirements are similar, the two facilities will be able to share the OSSPS on an alternating shift basis.

OSSPS is serving as a design basis for the larger power systems required in the next generation of fusion research equipment. Power levels of up to several hundred MVA have been considered using the OSSPS modules as building blocks.

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References

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2. R. K. Green, Sargent & Lundy Engineers, private communication.

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Figure Captions

Fig. 1. Typical cycle for each sector of the TF windings. The current decay and dumping characteristics between t=0.75 and t=1 sec are shown as desired, although not necessarily practical.

Fig. 2. A simplified schematic of a series pair of power supply modules comprising an equivalent 12-phase rectifier system.

Fig. 3. Data format for a typical shot. Rise time and flat-top duration are about 0.1 sec, respectively.

Fig. 4. Per unit dc current characteristic of a power supply pair as a function of gate delay or time interval from the zero crossing reference to gate pulse (A0).

Fig. 5. A view of the shelter under construction just east of the "ORMAK" building. The steel framing will also support the overhead dc bus between the power supplies and ORMAK.

Fig. 6. A view of the dedicated 40 MVA substation transformer and its primary switchgear. The 161 kV feeder line is overhead.

Fig. 7. A view of 2 rectifier modules. The vented enclosure on top contains the load dumping resistor network. Overall dimensions for each module are 60" width, 48" depth, and 126" height.

Fig. 8. A view of two power transformers with parts of one enclosure removed. Tap connections are visible on the top of each winding. The thyristor fuses are located in the top section of each transformer enclosure.

Fig. 9. A close-up view of one transformer.

Fig. 10. One of the rectifier modules during installation in the test area.

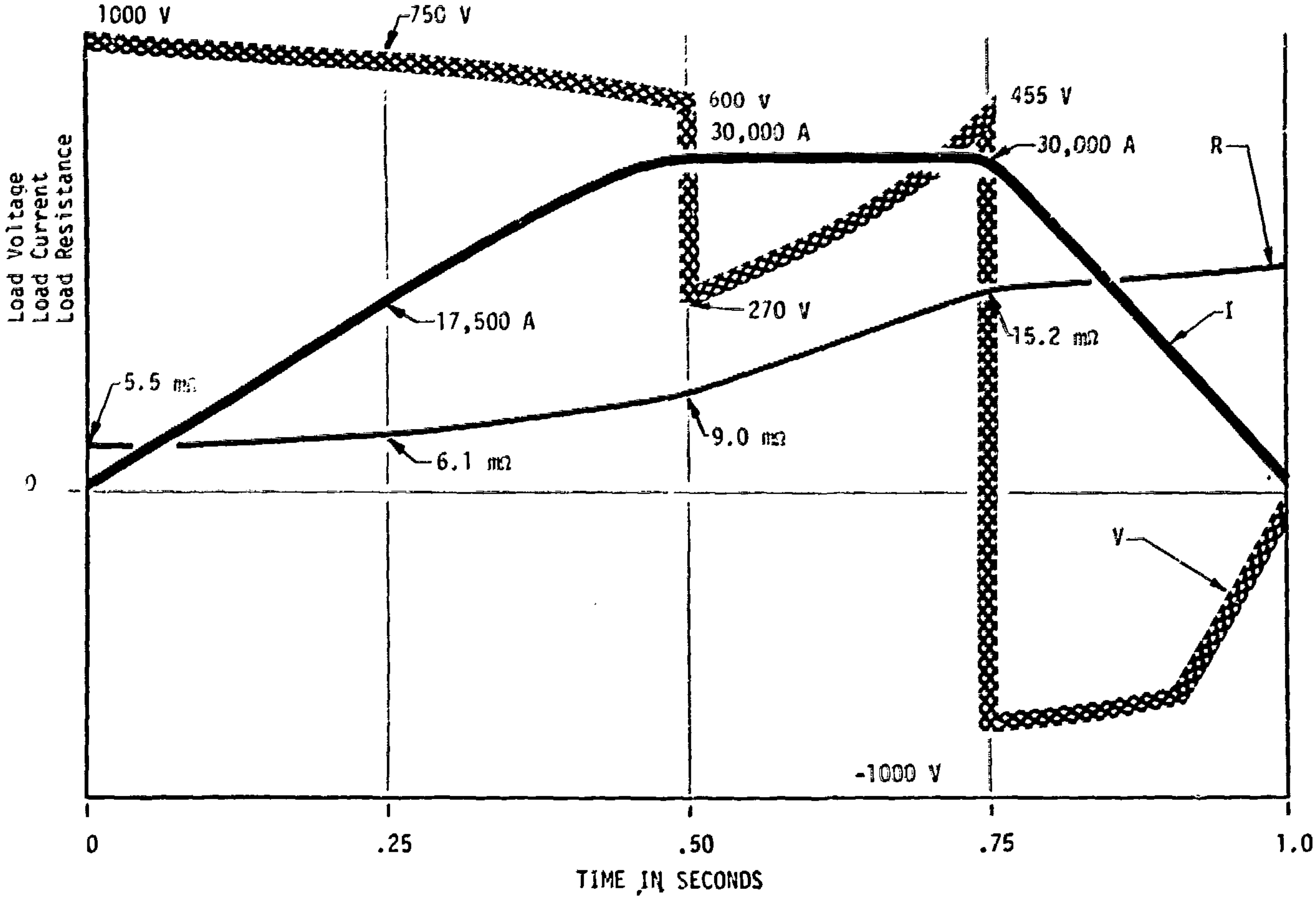

FIGURE 1.[redacted]

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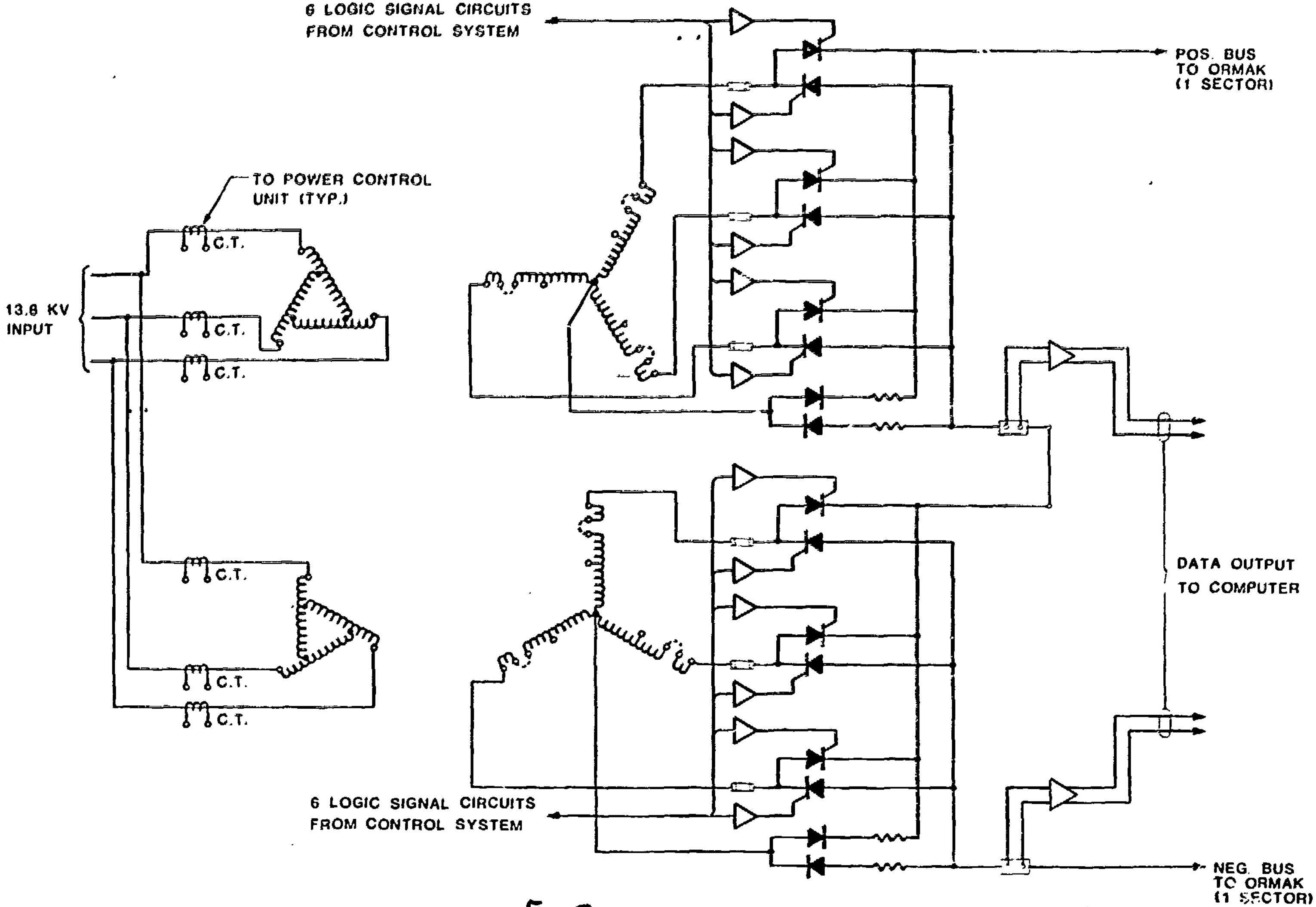


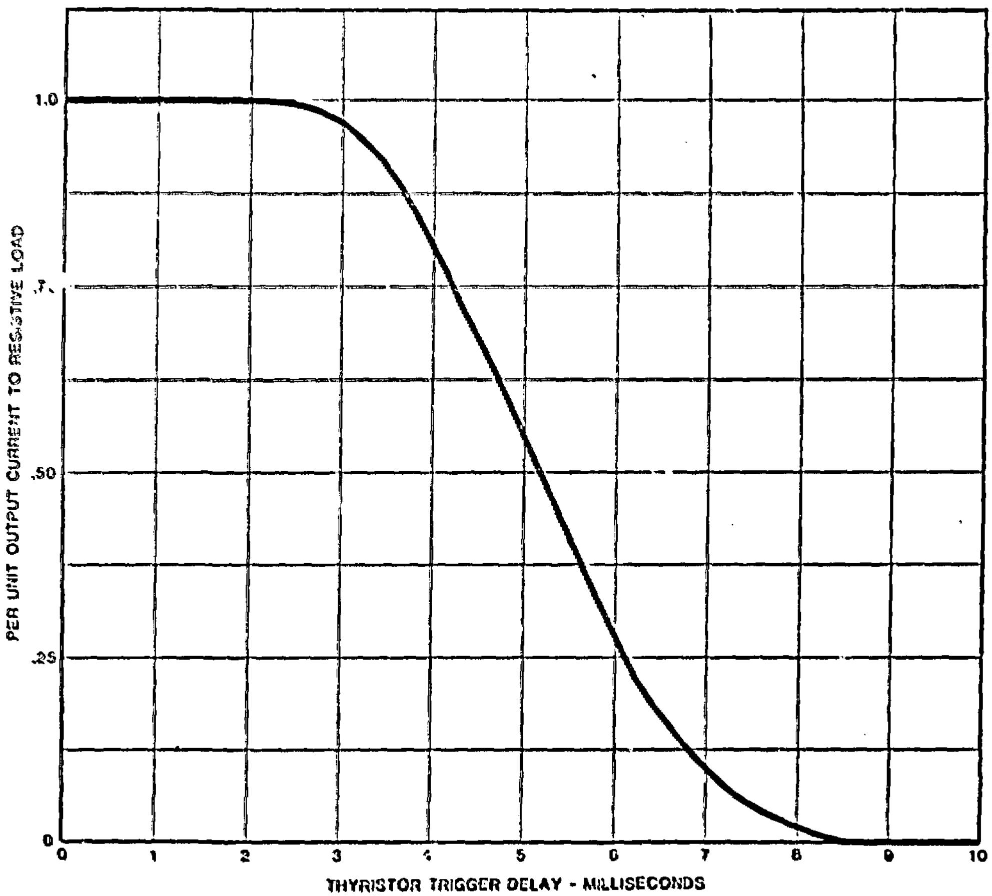
Fig 2

Fig 3

~~Table 3.~~ Data format for a typical shot. Rise time and flat-top duration are about 0.1 second, respectively

Cycle	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11
1)	2.00	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39
2)	2.00	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39
3)	2.00	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39
4)	2.00	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39
5)	2.00	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39	1.39
6)	2.00	1.39	1.39	1.39	1.39	1.39	1.75	1.75	1.75	1.75	1.75	1.75
7)	4.50	1.37	1.37	1.38	1.37	1.37	1.38	1.37	1.37	1.38	1.37	1.37
8)	4.30	1.37	1.37	1.37	1.37	1.37	1.37	1.37	1.37	1.37	1.37	1.37
9)	4.05	1.37	1.37	1.36	1.37	1.37	1.36	1.37	1.37	1.36	1.37	1.36
10)	3.75	1.37	1.36	1.36	1.36	1.36	1.36	1.36	1.36	1.36	1.36	1.36
11)	3.40	1.35	1.36	1.35	1.36	1.36	1.35	1.36	1.36	1.35	1.36	1.36
12)	3.00	1.36	1.36	1.36	1.80	1.80	1.80	1.80	1.80	1.80	1.80	1.80
13)	0.00											

spread out for double column width



PER UNIT OUTPUT CURRENT TO RESISTIVE LOAD
1.0
.50
.25
0
0
1
2
3
5
7
8
10
THYRISTOR TRIGGER DELAY - MILLISECONDS

Fig 4

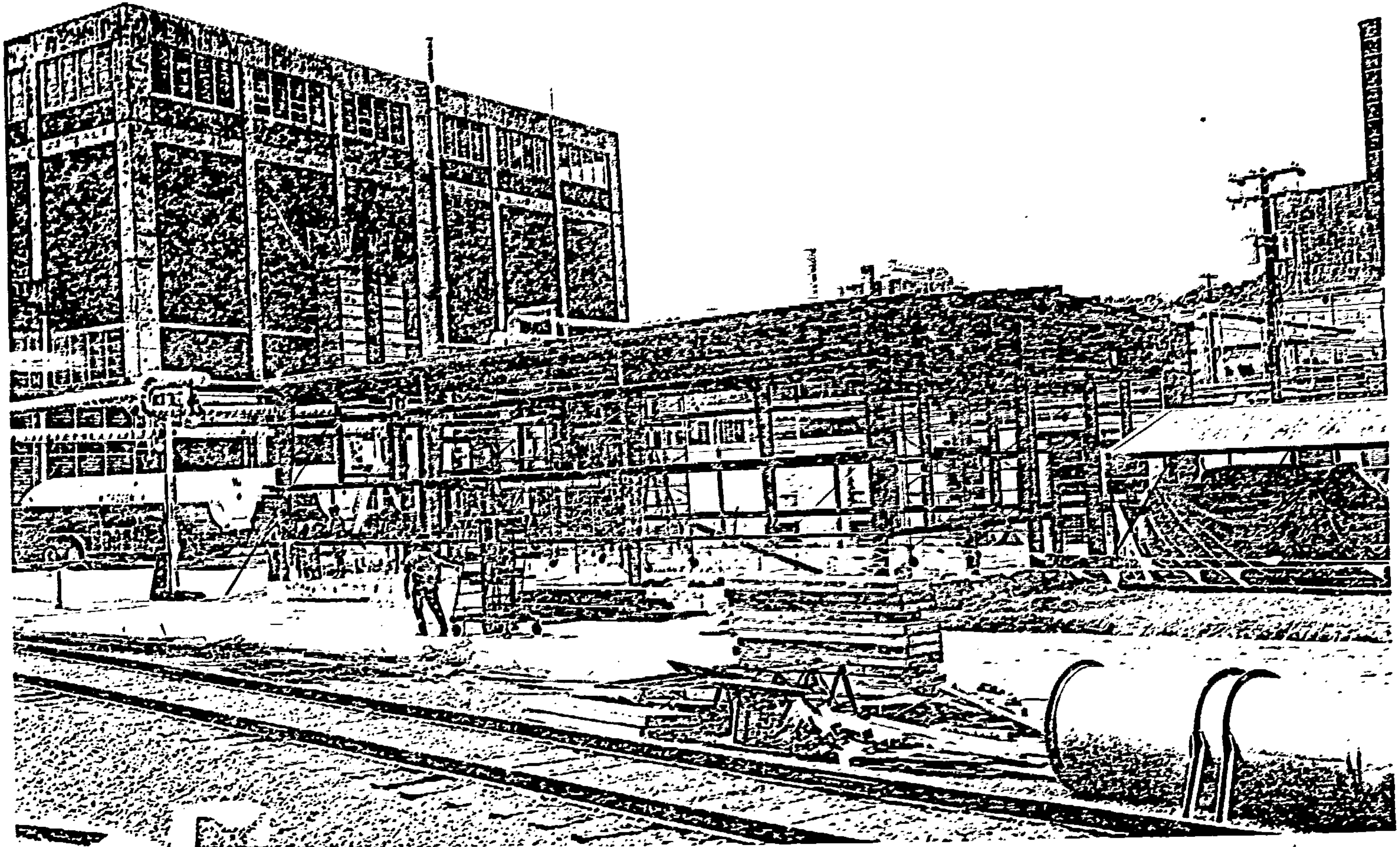


Fig 5: 4340-75

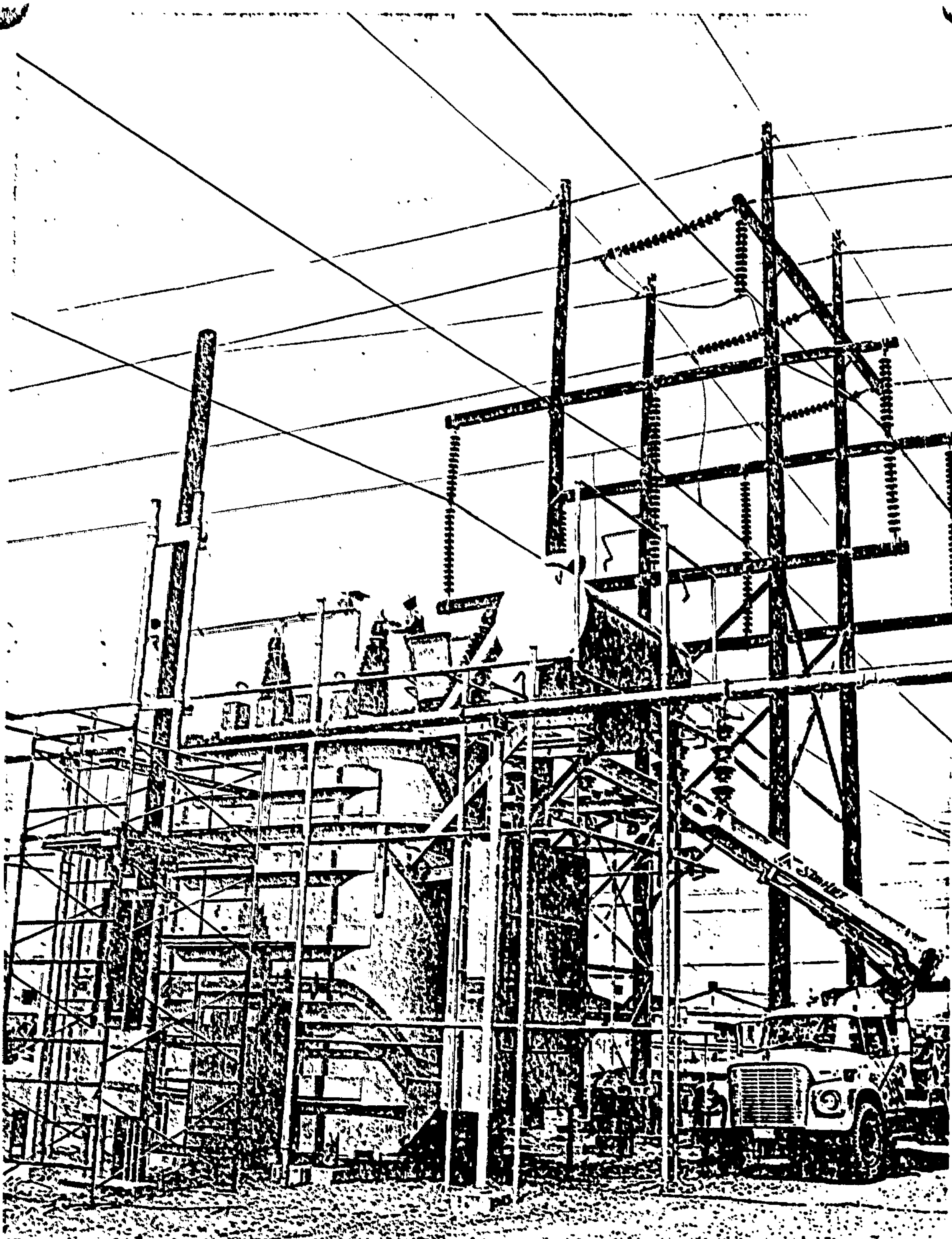


Fig 6 4341-75

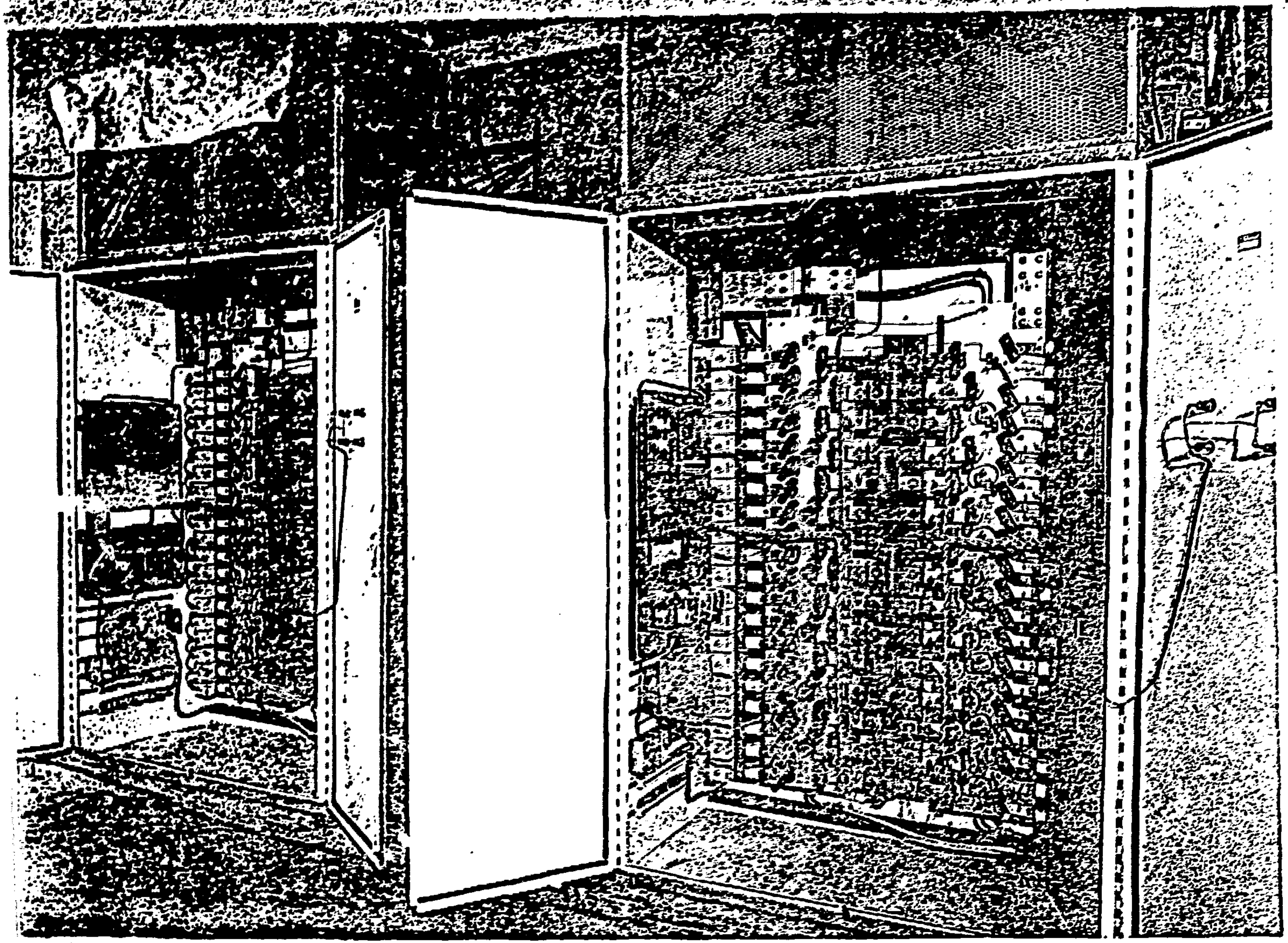


Fig. 7

4722-75

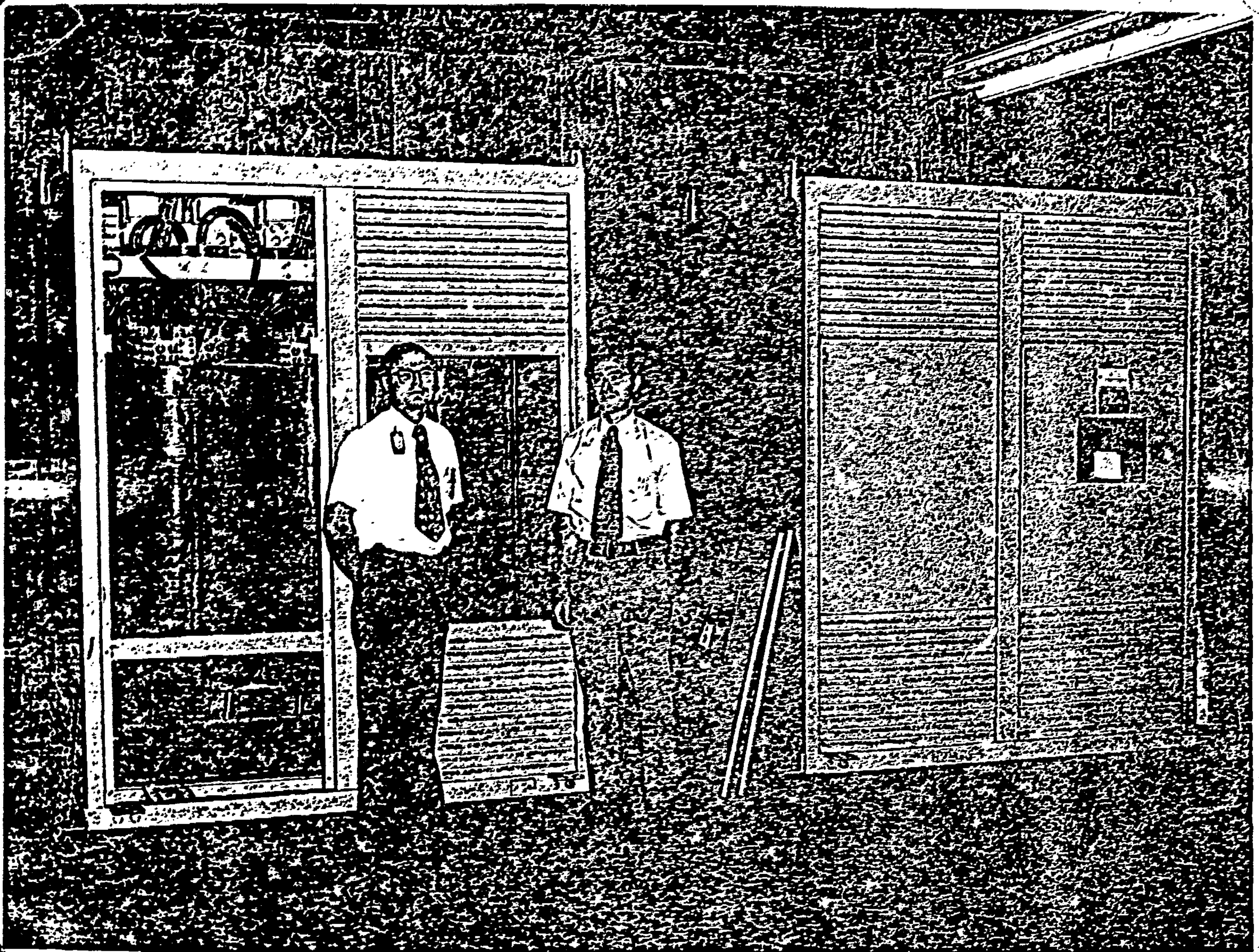


Fig 8 4435-75

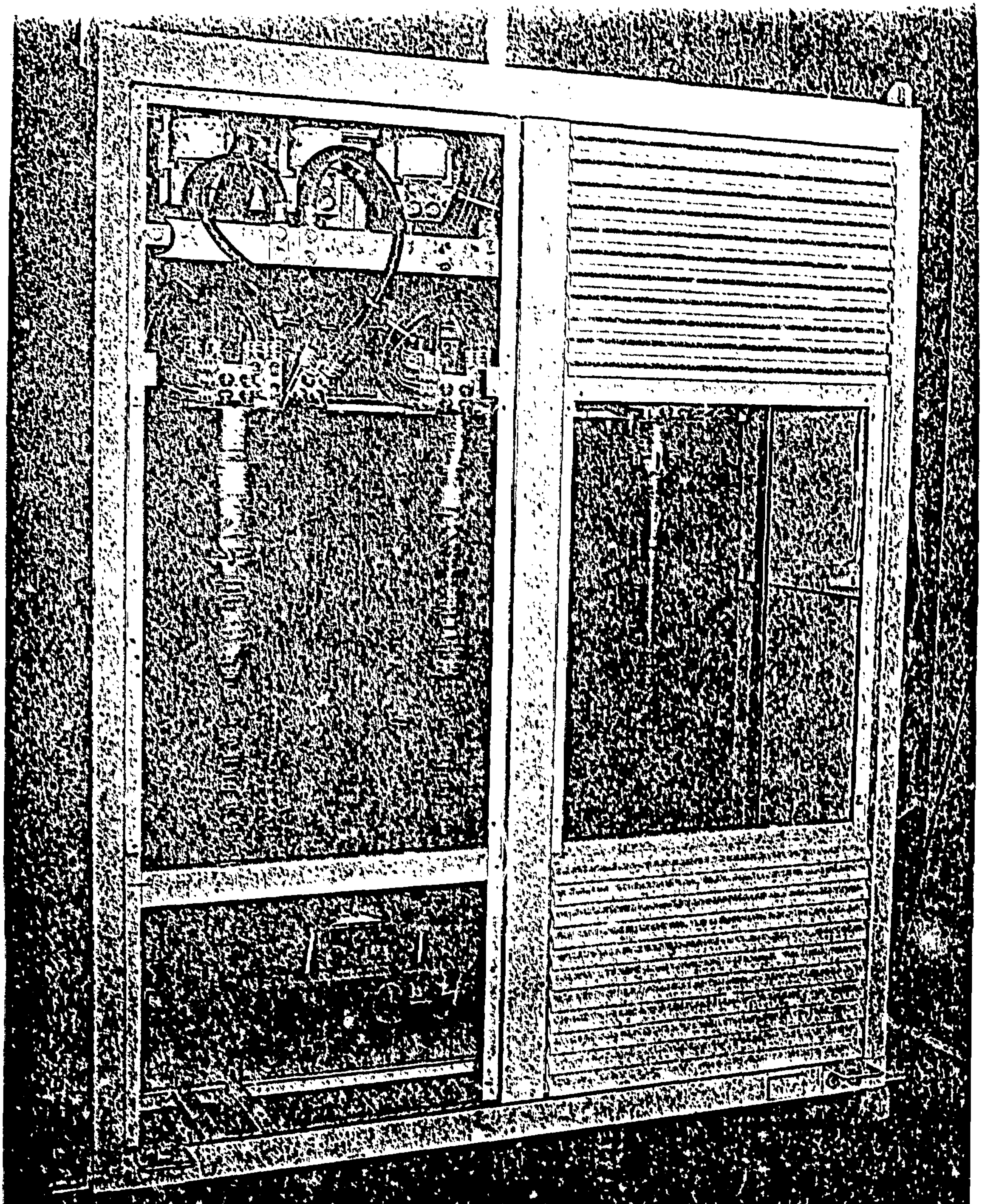


Fig 9 4431-75

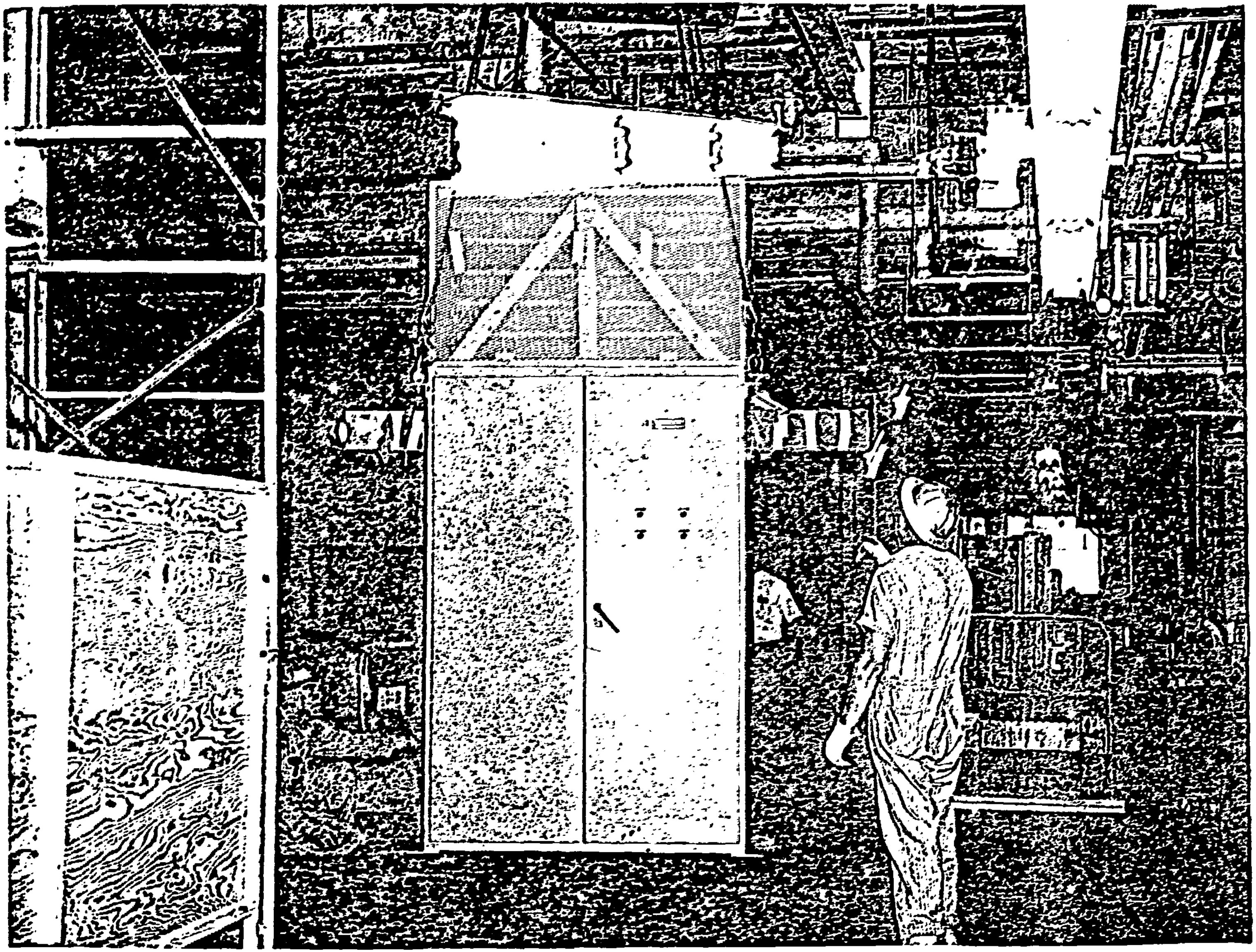


Fig 10

4433-75