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MPS Data Acquisition System

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MPS DATA ACQUISITION SYSTEM

Introduction

Data generated by the various particle detectors in the Multiparticle Spectrometer Facility (MPS) (Fig. 1) are collected by the Data Acquisition System and formatted into 18-bit words. A 16 K-word core memory in the DATA HANDLER buffers these words during the spill and then writes them out onto magnetic tape between spills. The Data Handler also tags selected events for transmission to the on-line computer (PDP-10) for analysis if the computer is available. The MPS and the particle detectors are described in Refs. 1 and 2. A description of the Data Handler will be made available at some future date. This note describes that part of the DATA Acquisition System which connects the detectors to the Data Handler; namely, the Detector Electronics, Device Controller and device port Optical Isolator. See Fig. 2 for a system block diagram.

System Operation

The salient features of the MPS, detectors and the Data Handler are summarized below. The primary detectors used are (going roughly from upstream to downstream):

Beam Drift Chamber

Beam Scintillation Counters (Photomultiplier)

Beam Hodoscopes (PWC)

Beam Cerenkov Counter (Photomultiplier)

Trigger Scintillation Counters (Photomultiplier)

Trigger Chambers (PWC)

Capacitive Spark Chambers

Magnetostrictive Spark Chambers

Recoil Cerenkov Counter (Photomultiplier)

Recoil Trigger Chambers (PWC)

Downstream Trigger Scintillation Hodoscopes

Downstream Cerenkov Counter

Located within the Fast Electronics Trailer at the MPS is an array of high speed NIM logic which determines for each incident beam particle whether or not to trigger an event recording cycle. To do this, prompt signals from the beam detector electronics are combined to define a "good beam particle", i.e. one that fully traverses the incident beam system is of the correct type ($\pi^{\pm}$, $K^{\pm}$, $p^{\pm}$), and one which if it were to trigger a recording cycle would probably be analyzable by the software. The trigger PWC's and downstream trigger hodoscopes provide discrete levels on their respective prompt signals which are directly related to the number of particles traversing each detector. The electronics forms a trigger by requiring a good beam particle and a unique number of particles in various detectors around and downstream of the MPS target. When the fast electronics in the trailer succeeds in forming such a trigger, the event recording cycle is initiated and the gates are disabled until the cycle is complete.

The trigger signal from the fast electronics trailer directly controls numerous latching operations in the fast trailer and the Control Room, and it also initiates the readout cycle of the Data Handler, Digital signals representing the state of each PWC wire, each piece of scintillator in a hodoscope, and each cell of a Cerenkov hodoscope are connected by long delay lines to buffer latches. The hodoscope latches in the Control Room are gated open for a short time by the trigger pulse to accept the photomultiplier

type digitized signals. In the case of the PWC's, the buffers are located in the fast trailer and actually are gated for every good beam particle so that the trigger must disable the strobe gate until the cycle is complete. There are also CAMAC event data gates for recoil Cerenkov pulse height, drift chamber Time-to-Digital information and downstream Cerenkov hodoscope pulse information which are controlled by the trigger signal. Additionally, the trigger signal must fire the High Voltage Pulsers for the Spark Chambers and also generate the signals known as "Quiet Gates" which bracket the electromagnetic disturbance from the sparking to suppress spurious signals in critical electronics circuits.

Meanwhile, the trigger signal is applied to one or more USER PORTS which send an optically isolated pulse to the Data Handler via any (or several) of four triggering bits in each port. The Data Handler can accept multiple sources of this signal and by using switches on the Data Handler, USER PORTS can be favored or treated equally in their ability to trigger the system. The four trigger bits for each USER PORT are wired (by patch boards) in such a way that the devices to be read out during the cycle depend upon which trigger bits were used to initiate the cycle. One can, for instance, trigger the cycle in such a way that PWC's and hodoscopes are read out but spark chambers (which require a longer readout and recovery time) are not.

The devices communicate with the Data Handler over optically isolated busses called DEVICE PORTS. Table I shows the current assignments of the device ports which are reserved for hodoscopes, beam PWC's, trigger PWC's, CAMAC event system, the Cerenkov pulse height system and the capacitive

and magnetostrictive chamber systems. Upon receipt of a trigger, the Data Handler interrogates each device port in sequence beginning with Port 00 and skipping device ports which are either switched out manually at the Data Handler (device port toggle switches) or are to be skipped as determined by the trigger bit patch board. A timing diagram is shown in Fig. 3.

The device ports are actually optically isolated data busses and consequently several device controllers can be attached to each device port by daisy chaining. The device controllers contain the circuitry to recognize an address (group word) from the data handler and then proceed to examine the buffers, scalers, Camac units etc. connected to it and upon command, format the data and transmit it in 18-bit words to the data handler. The group word assignments for each device controller are given in Table I.

The format of the data actually written onto magnetic tape by the data handler is shown in Fig. 4. The device controllers supply the data words. The data handler suffixes the group word. The group word number is the device controller address. There is only one physical magnetostrictive controller, and only one capacitive device controller; however, several group words appear for these devices in order to sub-divide the data. The data handler does not supply group words 33 to 62; these actually come from the magnetostrictive device controller. The 64th group word contains information concerning the trigger bits and so forth and is generated by the data handler itself. At the end of each spill a special word is written by the data handler and it contains the scalers, DVM, etc. which monitor the experiment.

The Device Ports

TABLE I

The following is a list of currently employed devices with their group and port numbers.

DEVICE	PORT #	GROUP #'s
Hodoscope (fast gates)	00	00
Beam PWC's	01	01
Trigger PWC's	02	04
CAMAC System	04	16
Capacitive Spark Chambers	06	24 - 30
Magnetostrictive Spark Chambers	07	32 - 62

The Device Ports

The Data Handler services the device controllers serially, by group number, collecting the data and inserting a group word for each controller. The group word format is:

M.S.B. L.S.B.

# of Data Words * Group #

000 X8 X7 X6 X5 X4 X3 X2 X1 X0 G5 G4 G3 G2 G1 G0

Servicing the controllers is accomplished using optically isolated device ports, one for each group of controllers. In this way ground loops are eliminated. A schematic of a Device Port optical isolator is shown in Fig. 5.

Optical Isolator Module

The optical isolator module is located remotely with the device controllers. Each signal between the data handler and controller is ground isolated with a Hewlett Packard (5082-4360) optical isolator. This circuit is as fast as commercially available (≈ 10MHZ), (65 nsec prog. delay). The output is driven by a differential line driver DM8831. In order to preserve isolation the power supply for the isolators and drivers is supplied from the MPS control room (+12V) and regulated on the module to +5V. A device port wiring diagram is shown in Fig. 6.

Port Signals

The following is a description of the Device Port signals.

Group Address Lines - 6 binary bits for unique addressing of controller

Group Request - pulse that occurs after the address lines have stabilized.

It's use is to prevent incorrect decoding of address.

Handler Ready (HR) - Data handler initiated is sent when handler is ready for transmission of an 18-bit byte of data.

Data Ready (DR) - Controller initiated is sent when controller is ready for transmission of data and after receipt of (HR).

Group Acknowledge (GA) - Signal is generated by controller when correct address has been decoded and is dropped when the controller has completed its data transmission for the complete event cycle.

Data Lines - 18 binary bits of data.

The Device Controllers and Detector Electronics (see Fig. 2) for each Device Port are described in succeeding sections.

HODOSCOPE SYSTEM - PORT 00

Detector Electronics

Electronically, the detectors are photomultiplier tubes (PM). A block diagram of the Hodoscope System is shown in Fig. 7. The base, amplifier and adder/disc are discussed in Reference 1 and schematics are given in Figs. 8, 9 and 10. The Discriminating Coincidence/Buffer (DCB) is a commercial NIM module (EG&G #C142 or C196). The data bits represent the status of a Cerenkov cell or a piece of scintillator. The Adder/disc circuits can add the signals if several PM's are connected to the same cell. The prompt signal is often summed over the entire hodoscope to count the number of hits in the hodoscope, or is put into a matrix logic circuit with other hodoscopes.

HODOSCOPE CONTROLLER

The controller interfaces the DCB's (EG&G's C142 DCB's and C146 strobed coincidence buffers) with the data handler. Each data bit equals one DCB channel. Unlike other controllers it sends only data, the sequence identifying the location. Maximum capacity is 360 fast gates, 180 of each type.

After the correct address is decoded a group acknowledge (GA) is sent to the data handler which in turn sends the first HR. HR starts a timing sequence which delays (200 ns) before sending a DR signal. During this time the first strobe pulse is generated (3 x 74164 shift registers) and opens half the gates (18) on the first multiplexer board. This cycle is continued until the last strobe (pre-selected) is reached. This strobe is not sent to the multiplexer board, instead it generates a STOP which turns off the ON flip-flop and Group Acknowledge. The data handler then goes on to the next device. The fast gates are reset with Quiet Gate routed through the device controller and the multiplexer board. The controller can be tested or used independently of the data handler by switching the internal switch to test. A block diagram is shown in Fig. 11 and a schematic in Fig. 12.

Control Indicators

STOP - The controller has completed the data handler cycle.

GA - The controller has successfully decoded the data handler address.

HR - The controller has received at least one HR signal.

DR - The controller has generated at least one DR signal.

Mechanical Configuration

The controller is located in the MPS control room. It occupies two slots of a CAMAC tray along with the 10 multiplexer modules and one optical isolator. The Detector Electronics is located near the detector.

BEAM PWC SYSTEM - PORT 01

Detector Electronics

Sixteen planes are currently interfaced. There are four planes per Device Controller with four device controllers all daisy-chained to a single device port as shown in the block diagram of Fig. 6. Beam hodoscope H8 uses 50-foot coax, which has a slightly different test pulser network. Schematics for the various circuits are givenin Figs. 14 through 18, and a brief description of each circuit board follows.

1. Test Pulser Networks

These resistor networks fan out a test pulse to each wire of the system. The networks are shown in Fig. 14. This pulser system allows one to study the electronic performance (gain and delay variations from wire to wire, etc.). A separate test system is also available to introduce (differentiated) pulses onto the anode wires of a PWC by pulsing the PWC cathode.

2. Cluster Trigger Board (CT)

Each card contains 8 identical circuits, one per PWC wire. The board remotely receives the PWC signals, many of which are in the MPS magnet, by way of 95Ω ribbon coax. Chambers in and near the MPS magnet have 50 foot lengths of this cable, with the CT boards located in the fast trailer. Beam chambers have 10 foot lengths with the CT's located on the experimental floor, except H8 as noted earlier.

The signals are isolated with 1:2 step-up pulse transformers and effectively terminated in 100Ω. The PWC signals are typically 500 μvolts - 20 nsec. and are amplified using a gain of 100 video amplifier (μa733). The pulses are compared with a threshold voltage using fast, low-jitter comparators (μa760). The comparator outputs trigger monostables (74123) set to 70NS for 26 wires/inch beam PWC's and 100NS for 10/inch trigger PWC's. The standardized pulses are now routed to the strobed buffers along flat cable of several lengths (12NS to 250NS) depending on the trigger timing delay of the particular experiment. A vital feature of the CT is the generation of a prompt trigger signal labled "OR", which determines the number of particles which traverse the chamber in a given event. This is accomplished using high speed logic gates (74S15) which anti all pulses of a cluster except for the highest numbered signal. A 'ock diagram is shown in Fig. 15 and a schematic in Fig. 16.

3. Strobed Buffer Module (SB)

Each module contains 32 identical circuits, one per PWC wire. A double buffer allows for a second candidates trigger's data to be stored while the two triggers are further processed. Each circuit consists of a line receiver (μa710) which compares a negative going signal (from +4 volts to +012 volt) to a 2.4 volt reference. The output is fed to a D-FLIP-FLOP (74S175) which stores the signal on the leading edge of the strobe signal. The output is fed into a 74165 shift register during the "SHIFT" signal. It is held there during the spark chamber firing and eventually shifted out serially to the device controller. The outputs of the D-FLIP-FLOPS are also available as a high speed output (74S04) to allow arithmetic processing, or other high speed logic processes, of the wire location which allows such operations as the momentum of

particles to be determined in a trigger using three PWC's. If these outputs are to be OR'd the 74S04's can be changed to open collector 75S05's. To prevent spark chamber noise from loading and shifting erroneous data an inhibit signal is used to trigger a monostable (50 sec) which gates out the STROBE, SHIFT and CLOCK signals during spark chamber firing. The schematic is shown in Fig. 17.

4. Trigger Isolator F/O Module

Each module consists of three identical channels for the strobe, shift and inhibit pulses. Each is ground isolated with a pulse transformer then amplified with a long-tailed pair and fanned out with a complimentary emitter follower. The input signal is designed to accept T^2L logic (0 to +3 V). A schematic is shown in Fig. 18.

PWC Device Controller

The controller includes all the circuitry to formulate a data word, which identifies the PWC wire location, it's plane number and the beginning or end of a cluster. Each controller can service up to four PWC planes and can be expanded with additional controllers using a TRI-STATE-BUSS arrangement. The 18-bit data word format is as follows:

M.S.B. L.S.B.
Cluster Bit
Plane Number — Wire Number

$1\ [C]\ 0\ [P_4\ P_3\ P_2]\ [P_1\ P_0]\quad [D_9\ D_8 \ldots\ldots\ldots\ldots\ldots\ldots D_0]$

The M.S.B. is always a logical 1. P_4 through P_2 are hard wired at each controller, i.e. 0000 for the master controller, 0001 for the first slave, etc. P_1 and P_0 are the lower order plane number electronically advanced on each controller.

The controller is enabled by decoding the correct address from the data handler, upon which it sends back a group acknowledge (GA) signal. The data handler in turn sends a handler ready signal which initiates the controller clock (≈ 15MHZ), which shifts the data in the strobed buffer module shift registers. For each clock pulse a data counter (three 74193's) is advanced by 1, thereby identifying the wire location (10 binary bits). Upon receipt of a logical 1 at the serial input to the controller (presence of a particle at that location) the clock is stopped and the data handler is serviced. A data ready (DR) signal, the data counter contents and a cluster bit are sent to the data handler. When the data handler is finished processing this data a new HR signal is sent which re-starts the clock. If in the cluster mode the clock continues until the end of the cluster, or if in the case of a cluster of one to the next cluster. At the end of the cluster the data handler is again serviced with the cluster bit set to a logical 1. If not in cluster mode each wire of the cluster is serviced. The last wire in the strobed buffers is hard wired to a 0 and the input to the last shift register is hard wired to a 1, thereby identifying the end of the chamber. This location is called high order bit (HOB). The last location to be serviced is a pre-selected count in the controller (STOP), which is the end of the HOB cluster and will direct control to the next plane or if the last plane to a slave controller or drop the Group Acknowledge line (GA). When the GA is dropped the data handler will pass on to the next device. See Fig. 19 for block diagram, Fig. 20, for schematic. The controller will function without the data handler. An internal switch marked TEST-NORM is switched to TEST. Another switch marked internal-external is switched to external to check a chamber and

to internal to check itself. In test external mode, a 3V pulse to the Front Panel BNL marked START will initiate an event cycle. The controller will continue until the event cycle is completed.

Front Panel Switches

HOB - high order bit places the end of the strobed buffer shift registers either at a 1 or a 0.

CM - cluster mode - the ON position provides a data handler cycle for only the first and last location of a cluster. The OFF position provides a cycle for each location containing a logical 1.

A & B - Mode Switches

A	B	MODE
0	0	Normal Operation
0	1	Data all 0's
1	0	Data all 1's

Internal Switches

ALL-ONE - In the ALL position the controller will service all four planes. In the ONE position it will service the plane designated by the 2^0 and 2^1 switches.

2^0 and 2^1 - Code of plane to be serviced.

TEST - NORMAL -- Normal position when operating with the data handler and test when operating by itself or in testing itself.

internal - external -- internal to test itself, external to test a chamber independent of data handler.

BNC Connectors

Serial out - the output of the strobed buffer shift registers.

Start - To perform an event cycle when in test mode.

Indicators

ON - controller has successfully decoded the data handler address.

HR - controller has received at least one HR signal.

DR - controller has generated at least one DR signal.

STOP - controller has completed entire event cycle.

CL - controller has generated at least one clock pulse.

Mechanical Configuration

The PWC device controllers are located in the MPS fast logic trailer. Each controller occupies two slots of a CAMAC tray. The rest of the tray holds up to 10 strobed buffers, modules, 1 trigger isolator board, and one optical isolator module.

Trigger PWC System - Port 02

This system is read out similarly to the beam PWC system. There are currently two (2) downstream trigger PWC's and one cylindrical PWC around the target. All three chambers are read out with a single Device Controller. The recoil system is under construction at this time and will use an additional Device Controller.

CAMAC System - Port 04

Detector Electronics

Commercial CAMAC modules are used together with a type-A controller for each bin. This system gathers CAMAC data for each event and is distinct from the CAMAC data recorded once per spill in the special word by the data handler.

Device Controller

The CAMAC controller interfaces up to 7 CAMAC TYPE A controllers with the data handler. It includes all the circuitry to formulate a data word, which identifies the data; location of the CAMAC module and the module channel. Since CAMAC's data word is 24 bits long, two controllers - data handler cycles are necessary to identify each piece of data. The data word format is:

First Word Sent

L.S.B.

DATA

D_{17} D_1, D_0

Second Word Sent

M.S.B.

Crate # | Module # | Module Sub Address # | DATA

C_4 C_2 C_1 N_{16} N_8 N_4 N_2 N_1 A_8 A_4 A_2 A_1 D_{23} ——— D_{18}

At present the controller only reads out and clears the CAMAC modules, since its function code is hard wired to F(2). The controller is enabled by decoding the correct address from the data handler, upon which it issues a Group Acknowledge (GA) signal. The data handler now issues a handler ready (HR). The CAMAC address generator is incremented ($\overline{A_{inc}}$) and after a delay a $\overline{BTA}$ signal is sent to the TYPE A controller. Upon receipt of a BTB from the TYPE A controller and a BQ from the addressed CAMAC module, indicating valid data, a data ready (DR) is sent. After the data handler has finished loading the data it sends the second HR. This HR does

not issue an $\overline{A_{inc}}$. The phase is changed $\phi 1$ to $\phi 2$, and the second half of the data word is sent. This is accomplished with 7451 AOI gates. In this case the DR is derived from the HR. If no BTB is received a $\overline{C_{inc}}$ is generated which clears the address generator module and channel portion and advances the CAMAC tray portion by 1. If no BQ is received the channel portion is cleared and the module portion is advanced by 1. These cycles are continued until STOP is reached (BCR + 1). STOP resets the ON flip-flop, GA is dropped, and the data handler goes on to the next device.

The controller can be run without the data handler by switching the internal switch marked TEST - NORMAL, to test. It can be run without CAMAC TYPE A's by switching the BQ and BTB TEST switches to the YES position.

Indicators

GA - controller has successfully decoded data handler address.

HR - controller has received at least one HR.

DR - controller has generated at least one DR.

STOP - controller has completed its event cycle.

BTB - controller has received at least one BTB from a Type-A controller.

BQ - controller has received at least one BQ from a CAMAC module.

Mechanical Configuration

MPS Control Room. See Fig. 21 for block diagram; Fig. 22 for schematic.

Capacitive Spark Chambers - Port 06

Detector Electronics

Each wire of the spark chamber (grounded plane) is connected to a capacitive network on the shift register module shown in Fig. 23. DC power to the shift registers is only applied during the readout cycle. At the instant power is applied, a logical one is stored if the capacitive network for that bit was activated by a spark. Block diagrams and schematics of the Capacitive Readout Spark Chamber System are shown in Figs. 24a, 24b, 24c and 24d. A detailed description of the system will be made available at some future date.

Capacitive Spark Chamber Device Controller (CSCDC)

The CSCDC includes all the circuitry to formulate a data word which identifies the wire location, plane number and beginning or end of cluster. Like the PWC system the controller shifts data through shift registers and assigns a binary number for the location. A different approach from that of the PWC controller was required because:

1. The total number of wires is approximately 10 times that of the PWC (30,000).

2. The shift registers are remote to the controller, and, therefore, the clock frequency cannot be as high (5 MHZ).

In order to save time the shift register modules are grouped into five chains and processed in parallel prior to the data handler cycle. The data is locally stored until all the shifting is done and the data handler is ready.

At the trailing end of Quiet Gate (QG) the CSCDC generates a power gate (PG) which energizes the shift register modules. 2 μsec later the controller clock starts shifting the data from the shift register chains

simultaneously to each memory module. For each clock pulse a data location counter on the memory module is advanced by 1. Whenever the shift register output is a logical 1, a write pulse stores the contents of the data location counter into the current memory location. The memory location is advanced by 1 immediately after the write pulse. Note, that unlike the PWC controller, the clock is not stopped. The memory is a 256 x 14 RAM, composed of Monolithic Memories MM6530; 256 x 1 Schottky bipolar RAMS. Thirteen (13) bits describe the wire locations (0-8192). The fourteenth bit describes the cluster bit, a logical 0 for the beginning of cluster and a 1 for the end of the cluster. The RAM outputs are bussed together using open-collector 7405's. The 18 bit data format is:

M.S.B. L.S.B.

	Cluster Bit	Memory Module #	Wire Location
1	C	P_2 P_1 P_0	D_{12} ---------- D_0

When the data location counter (74193's) reaches a pre-selected location, a STOP signal is generated. This signal drops the POWER GATE and turns off the shift registers.

After the CSCDC decodes the first correct address from the data handler, it sends back a Group Acknowledge (GA) signal. A logical 1 is shifted through a shift register (p222), which enables memory module #1. Each time a correct Group Word is decoded the shift register output enables a new memory module. A group word for each memory module is necessary since each Group Word can handle only 512 data words. Upon receipt of a GA the Data Handler sends a HR signal which is gated with STOP. The resulting pulse generates a sequence of 3 pulses;

1st pulse - stores the contents of the memory address counter in latches (2 x 7475)

2nd pulse - resets the memory location counter.

3rd pulse - sets the Data Ready (DR) start flip-flop.

An enable (en) is generated which enables the memory in module #1 and the DR-HR cycle is started. A DR and the contents of the first memory location are sent to the Data Handler. After the Data Handler has serviced the data a second HR is generated, which increments the memory address counter. The cycle is now repeated. Note that the first HR does not increment the counter. This is done by the flip-flop in p41. DR-HR cycles are repeated until the contents of the memory address counter equals that of the latches. A logic comparator (2 x 7485) senses this equality and produces an END pulse. END prevents a DR generation in the memory module, since there is no data in the last memory address location. END also drops the Group Acknowledge line. The data handler now issues the next group word which will enable the second memory module. The last memory module's END drops the GA line and the data handler goes on to the next device. A block diagram is shown in Fig. 25 and a schematic in Fig. 26.

CSCDC Switches

CM - cluster mode ON will record first and last wire location of chamber; OFF will record all locations of cluster.

HOB - high order bit. It places the end of the shift register chain at either a 1 (ON) or 0 (OFF).

A&B - currently always in normal mode 0 0

CSCDC BNC's

CLOCK OUT - clock to shift registers

CLOCK OUT FOR DELAY - clock to be delayed for CSCDC

CLOCK DELAY IN - above clock after delay

POWER GATE (PG) - present for duration of shift register operation. ON (+5V), OFF (0V).

HOB - output of high order bit switch.

CSCDC Indicators

ON - CSCDC has successfully decoded data handler address.

HR - CSCDC has received at least one HR.

DR - CSCDC has generated at least one DR.

LAST END - CSCDC has completed its data handler cycle.

CL - CSCDC has generated at least one clock pulse.

Memory Bd. Indicators

STOP - module has completed clock operation

WRITE - module has generated at least one write-pulse.

END - module has completed its event cycle.

Mechanical Configuration

The CSCDC is located in the MPS control room. It occupies two slots of a CAMAC tray along with 5 memory modules, and the optical isolator module. The Detector Electronics is located on the chamber.

Magnetostrictive System - Port 07

The magnetostrictive system is described in detail in Reference 1.

Acknowledgements

I would like to thank C. Jacobs and C. Zein for the material they supplied for this report.

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Ref. 2 The BNL Multi-Particle Spectrometer, E.D. Platner et al., Proc. of the 1973 International Conference on Instrumentation for High Energy Physics, Frascati, May 8-11, 1973, 672 (1973).

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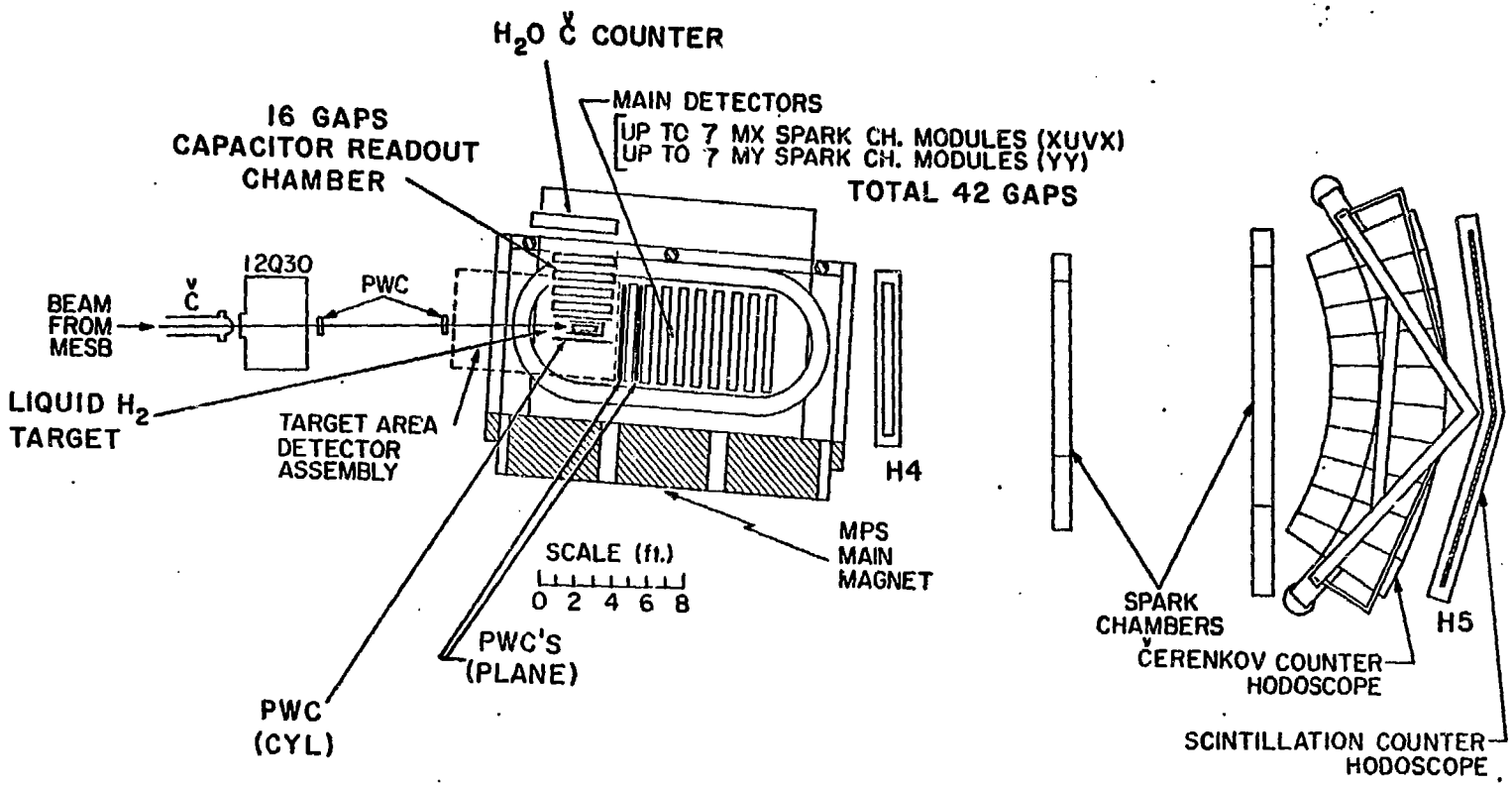

H2O Č COUNTER
MAIN DETECTORS
UP TO 7 MX SPARK CH. MODULES (XUVX)
UP TO 7 MY SPARK CH. MODULES (YY)
TOTAL 42 GAPS
16 GAPS
CAPACITOR READOUT
CHAMBER
12Q30
PWC
BEAM
FROM
MESB
Č
LIQUID H2
TARGET
TARGET AREA
DETECTOR
ASSEMBLY
H4
MPS
MAIN
MAGNET
SCALE (ft.)
0 2 4 6 8
PWC'S
(PLANE)
PWC
(CYL)
SPARK
CHAMBERS
ČERENKOV COUNTER
HODOSCOPE
H5
SCINTILLATION COUNTER
HODOSCOPE

Figure 1

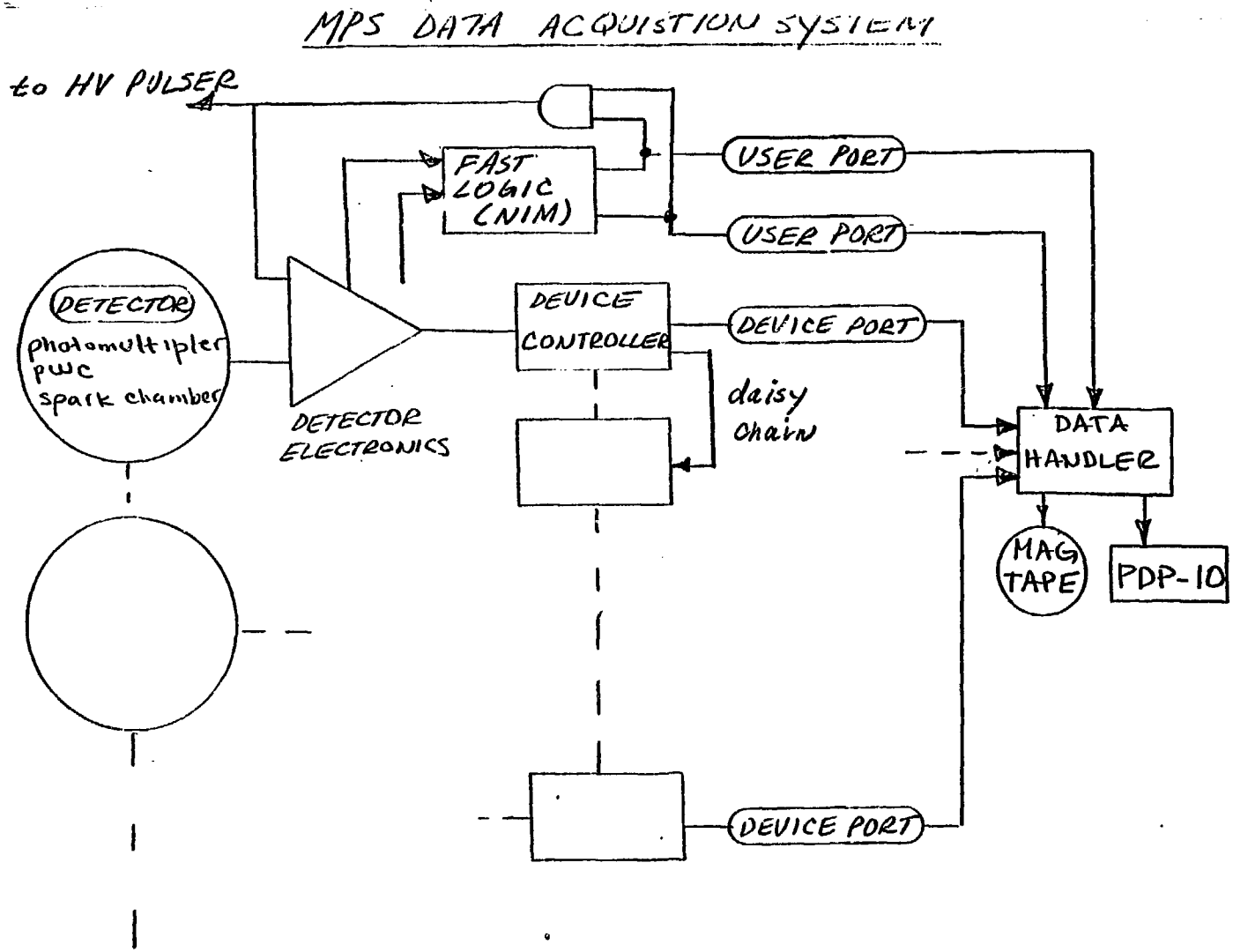

MPS DATA ACQUISTION SYSTEM
to HV PULSER
FAST LOGIC (NIM)
USER PORT
USER PORT
DETECTOR
photomultiplier
PWC
spark chamber
DETECTOR ELECTRONICS
DEVICE CONTROLLER
DEVICE PORT
daisy chain
DATA HANDLER
MAG TAPE
PDP-10
DEVICE PORT

Figure 2

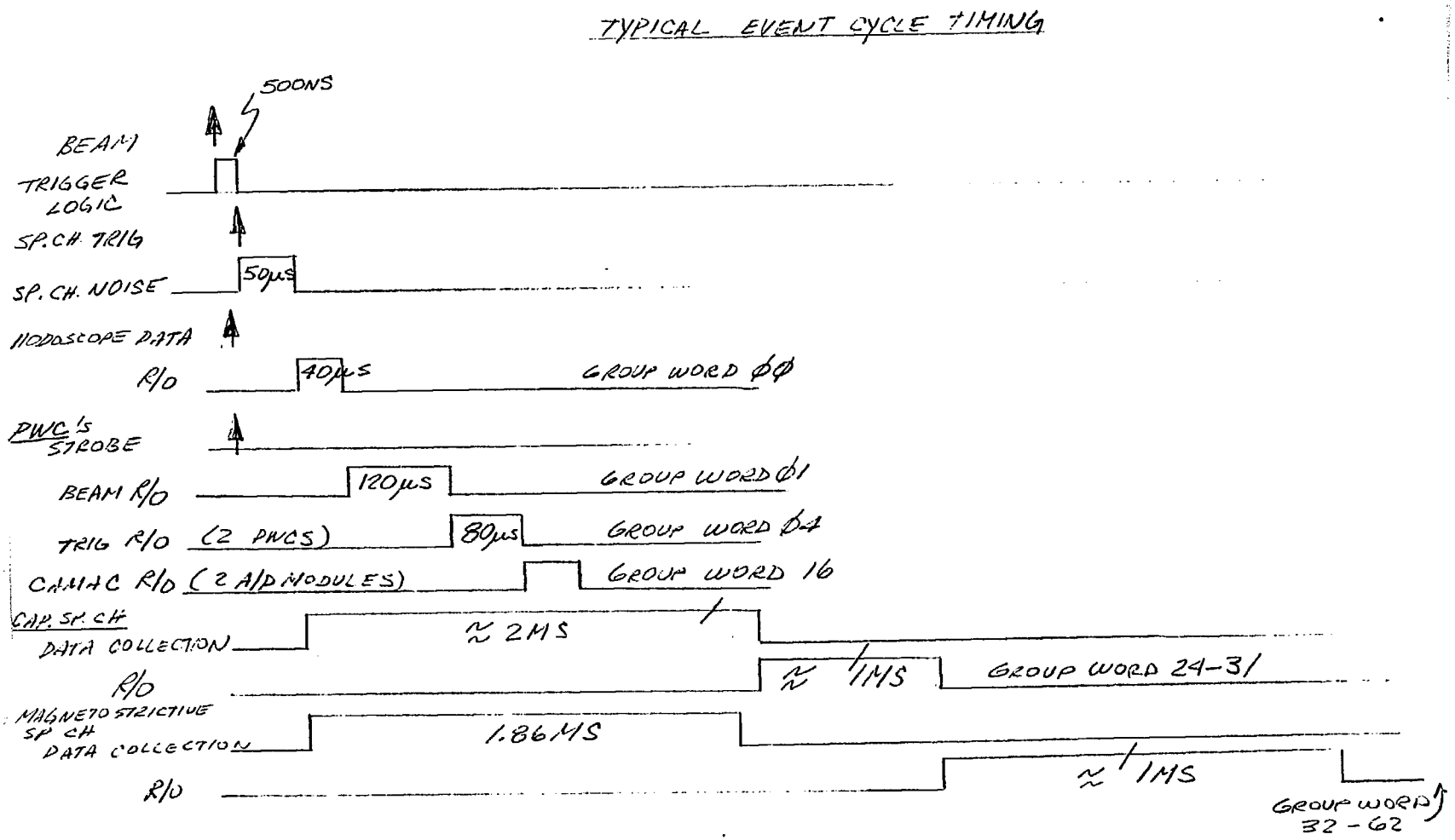
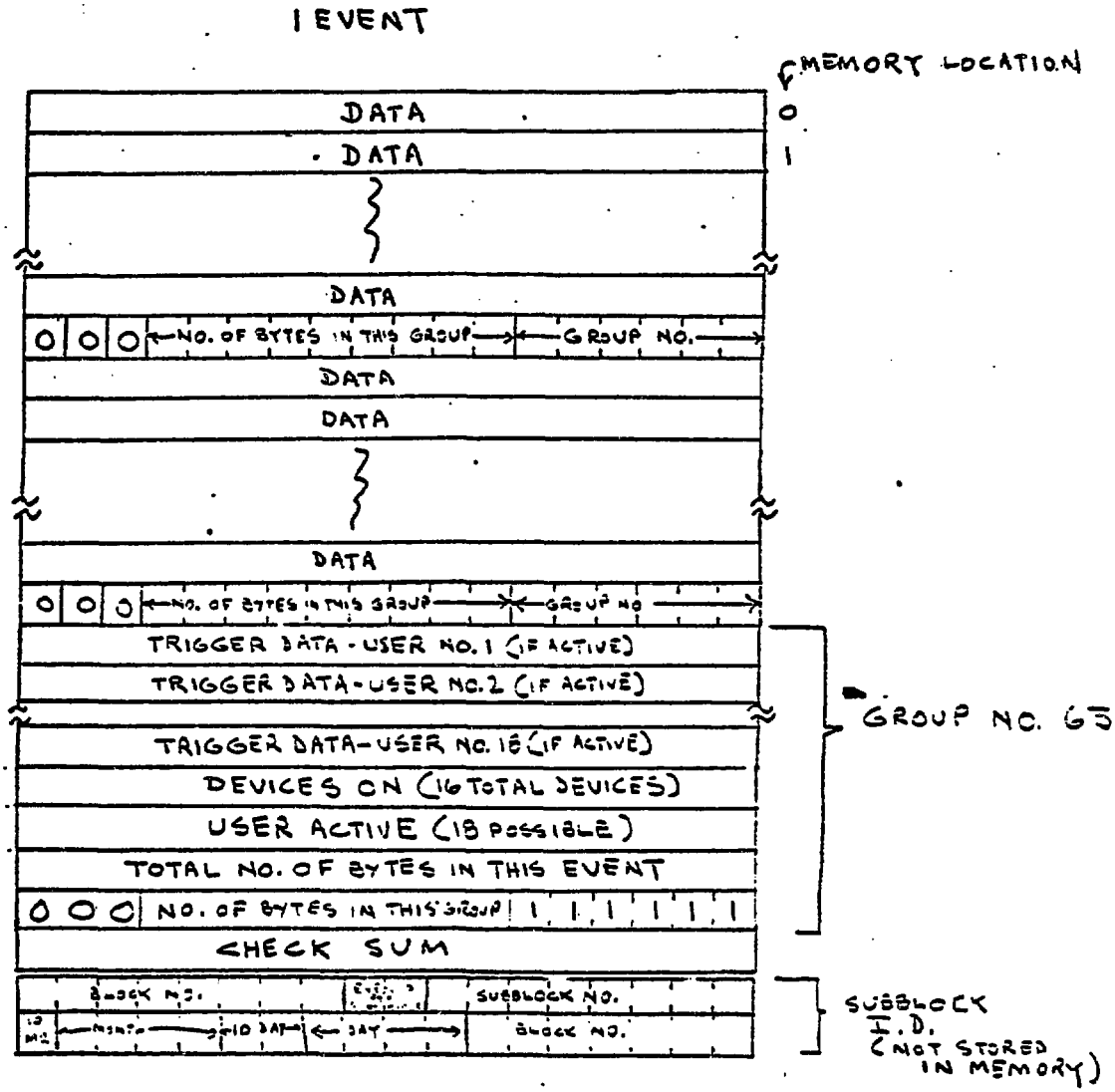

TYPICAL EVENT CYCLE TIMING
500NS
BEAM TRIGGER LOGIC
SP. CH. TRIG
SP. CH. NOISE
50μs
HODOSCOPE DATA
R/O
40μs
GROUP WORD ØØ
PWC'S STROBE
BEAM R/O
120μs
GROUP WORD Ø1
TRIG R/O (2 PWCS)
80μs
GROUP WORD Ø4
CAMAC R/O (2 A/D MODULES)
GROUP WORD 16
CAP. SP. CH DATA COLLECTION
≈ 2MS
R/O
≈ 1MS
GROUP WORD 24-31
MAGNETOSTRICTIVE SP CH DATA COLLECTION
1.86MS
R/O
≈ 1MS
GROUP WORD 32 - 62

Figure 3

BY..... DATE..... SUBJECT..... SHEET NO.....OF.....

CHKD. BY..... DATE..... EVENT STRUCTURE JOB NO.....

REV. 12-30-72 DEPT. OR PROJECT.....



BIT #'S to BE DESIGNATED BIT $\phi\phi$ ⟶ BIT 17

M.S. L.S.

Figure 4a

BROOKHAVEN NATIONAL LABORATORY

BY C. ZEIN DATE 12-30-72 SUBJECT SPECIAL WORD EVENT STRUCTURE SHEET NO. 9 OF

CHKD. BY C.Z. DATE JOB NO.

DEPT. OR PROJECT

SPECIAL WORD EVENT

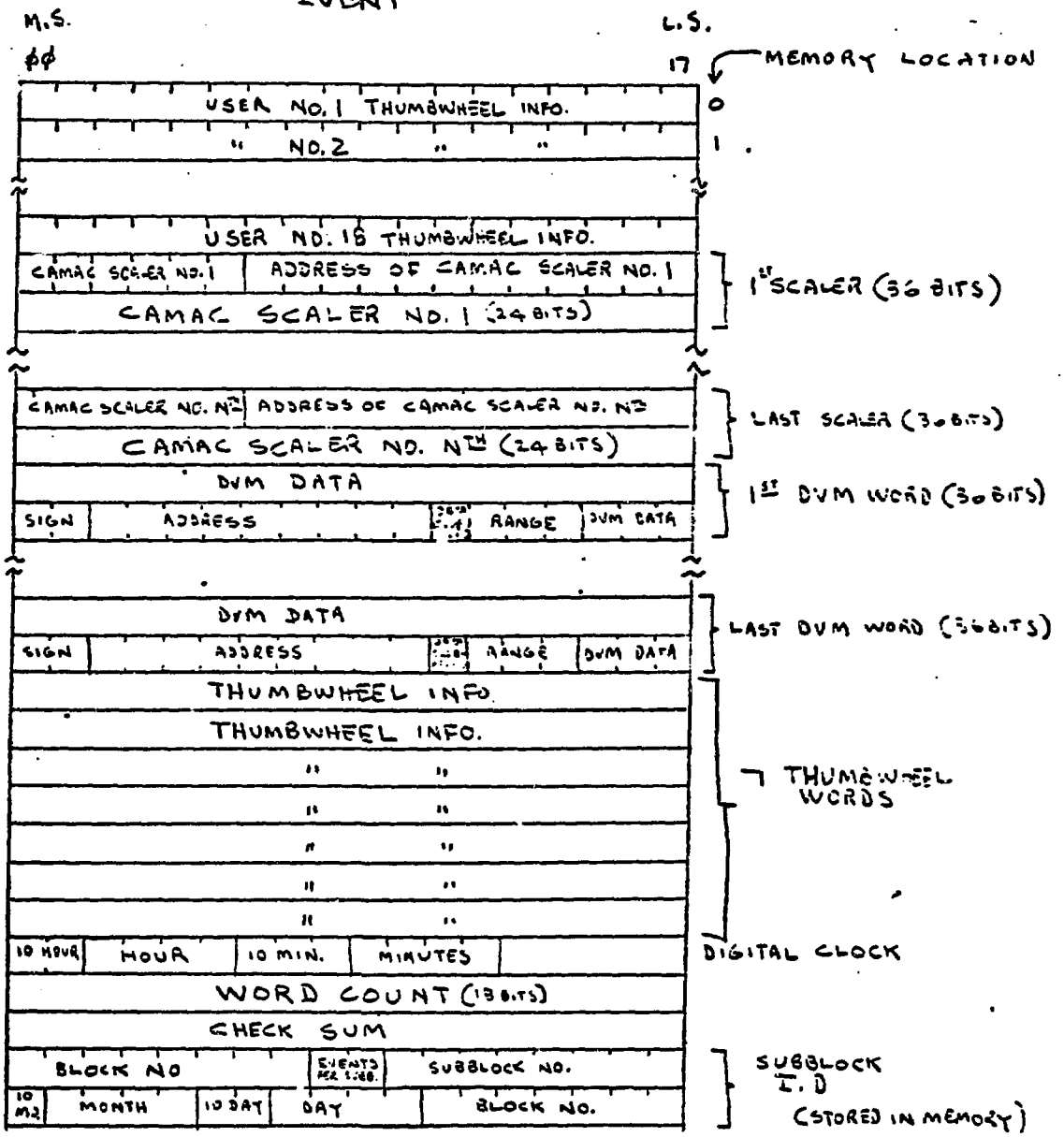


Figure 4b

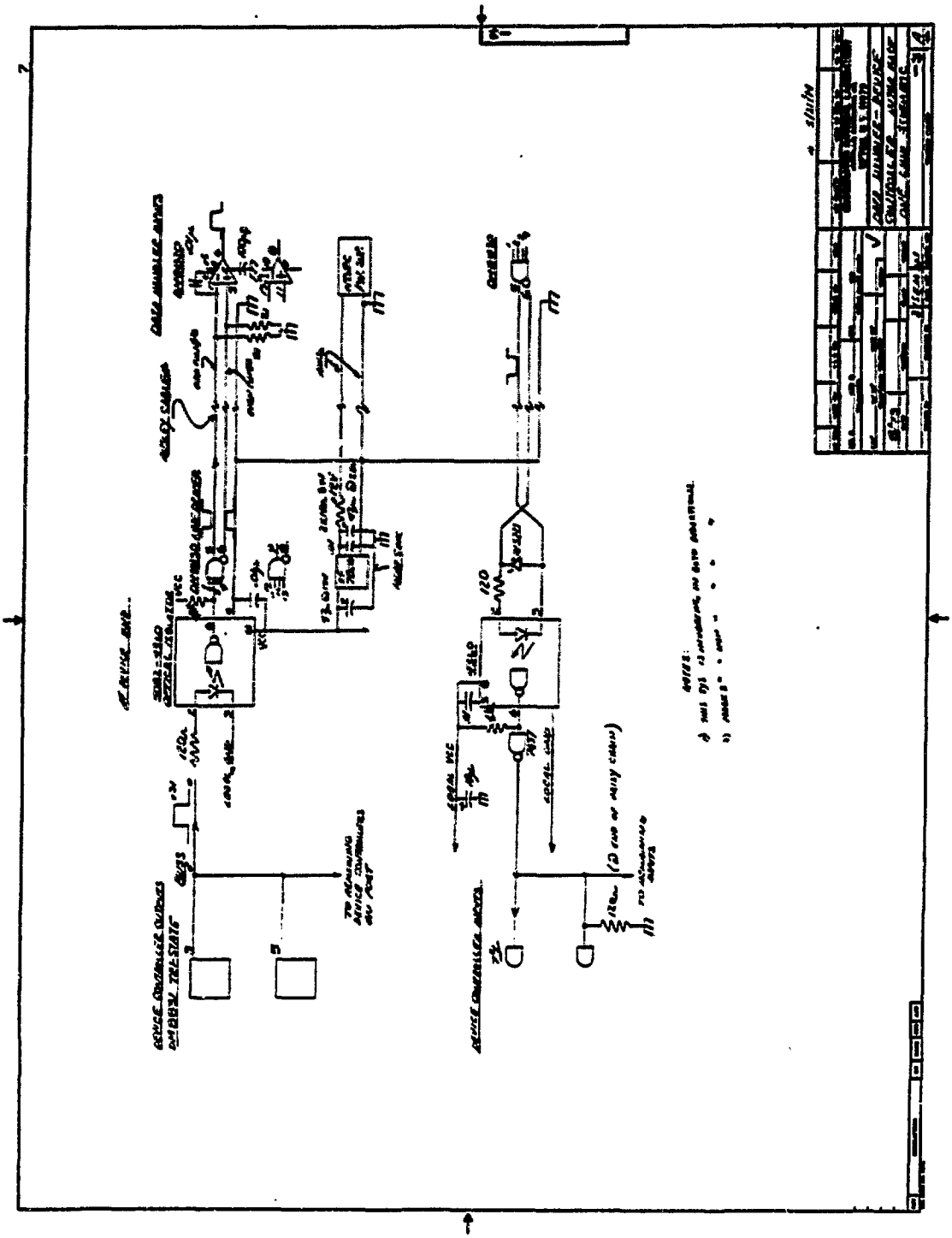


Figure 5

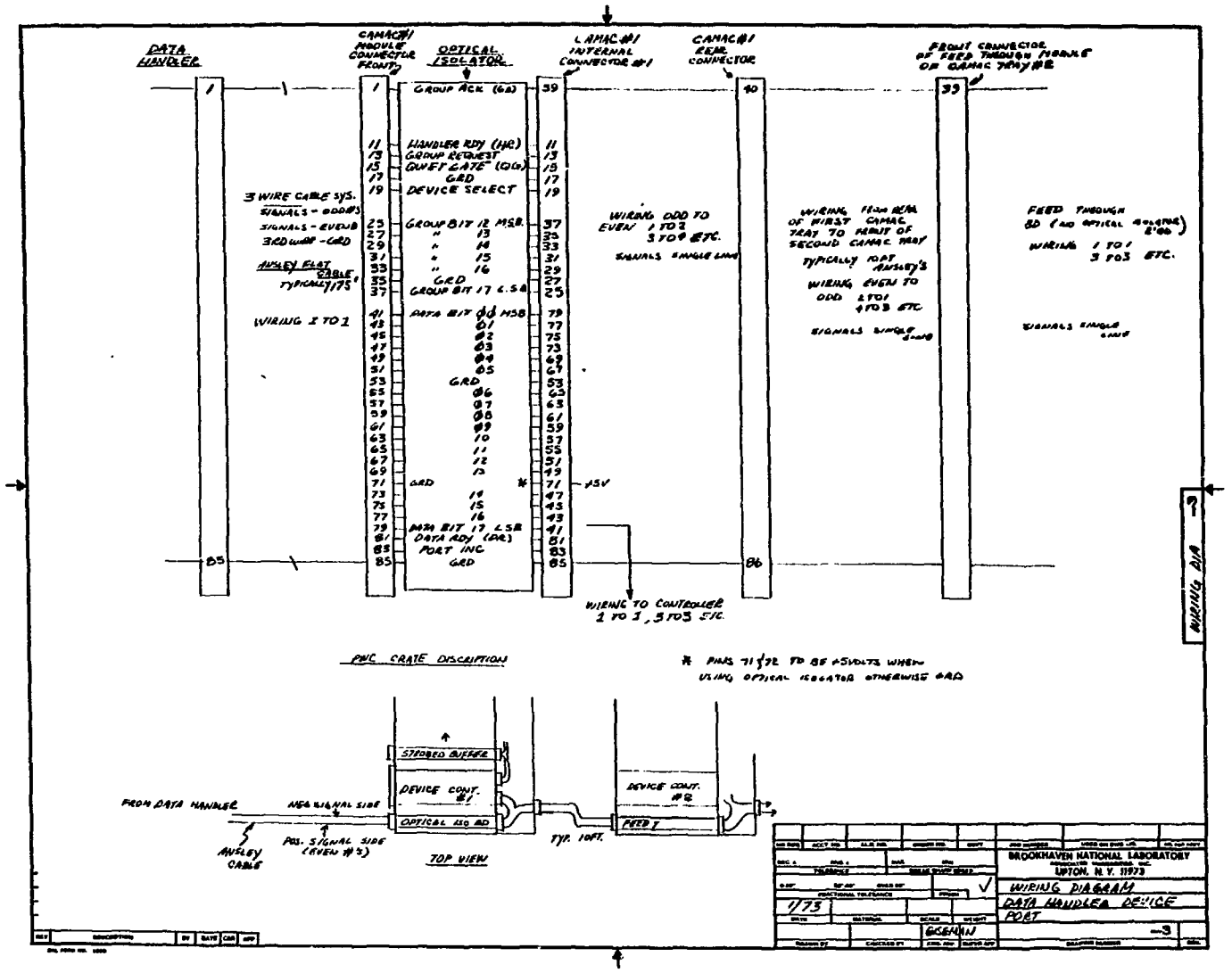

DATA HANDLER
CAMAC #1 MODULE CONNECTOR FRONT
OPTICAL ISOLATOR
CAMAC #1 INTERNAL CONNECTOR #1
CAMAC #1 REAR CONNECTOR
FRONT CONNECTOR OF FEED THROUGH MODULE OF CAMAC TRAY #2
GROUP ACK (GA)
HANDLER RDY (HR)
GROUP REQUEST
QUIET GATE (QG)
GRD
DEVICE SELECT
3 WIRE CABLE SYS.
SIGNALS - ODD #'S
SIGNALS - EVEN #
3RD WIRE - GRD
ANSLEY FLAT CABLE TYPICALLY 175'
WIRING 1 TO 1
GROUP BIT 12 MSB
GROUP BIT 17 LSB
DATA BIT 00 MSB
DATA BIT 17 LSB
DATA RDY (DR)
PORT INC
WIRING ODD TO EVEN 1 TO 2 3 TO 4 ETC.
SIGNALS SINGLE LINE
WIRING FROM REAR OF FIRST CAMAC TRAY TO FRONT OF SECOND CAMAC TRAY
TYPICALLY 10FT ANSLEY'S
WIRING EVEN TO ODD 2 TO 1 4 TO 3 ETC
FEED THROUGH BD (NO OPTICAL ISOLATOR 2'00)
WIRING 1 TO 1 3 TO 3 ETC.
WIRING TO CONTROLLER 1 TO 1, 3 TO 3 ETC.
WIRING DIA
PWC CRATE DISCRIPTION
* PINS 71 & 72 TO BE +5 VOLTS WHEN USING OPTICAL ISOLATOR OTHERWISE GRD
STROBED BUFFER
DEVICE CONT. #1
OPTICAL ISO BD
DEVICE CONT. #2
FEED T
FROM DATA HANDLER
NEG SIGNAL SIDE
POS. SIGNAL SIDE (EVEN #'S)
ANSLEY CABLE
TYP. 10FT.
TOP VIEW
BROOKHAVEN NATIONAL LABORATORY
UPTON, N.Y. 11973
WIRING DIAGRAM
DATA HANDLER DEVICE
PORT
1/73
GISEMAN

Figure 6

HODOSCOPE SYSTEM

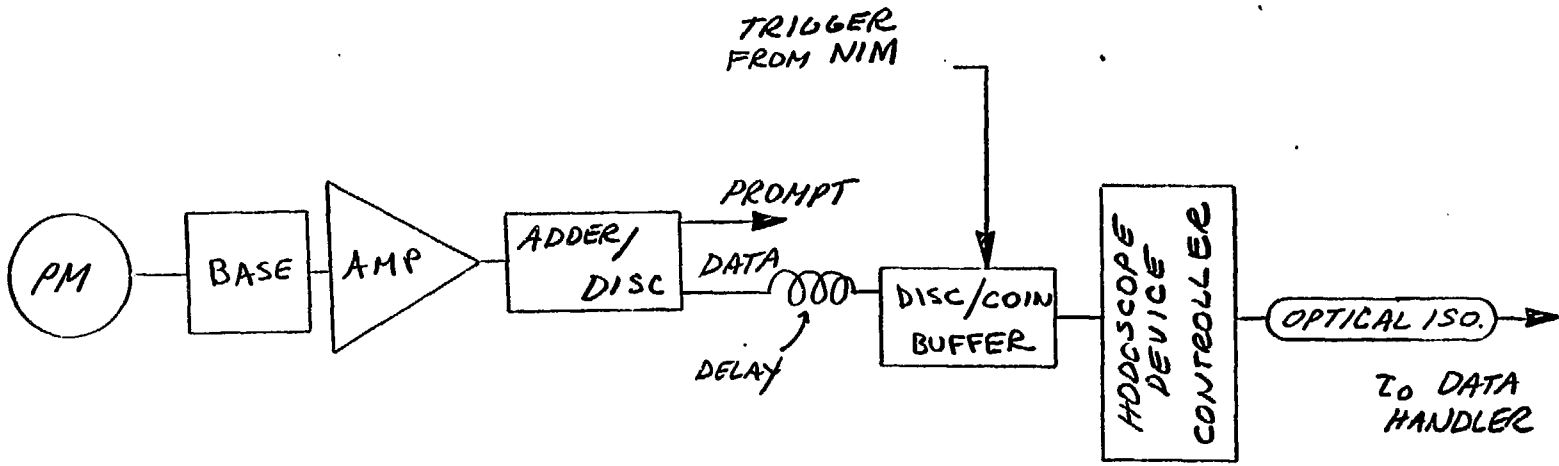


Figure 7

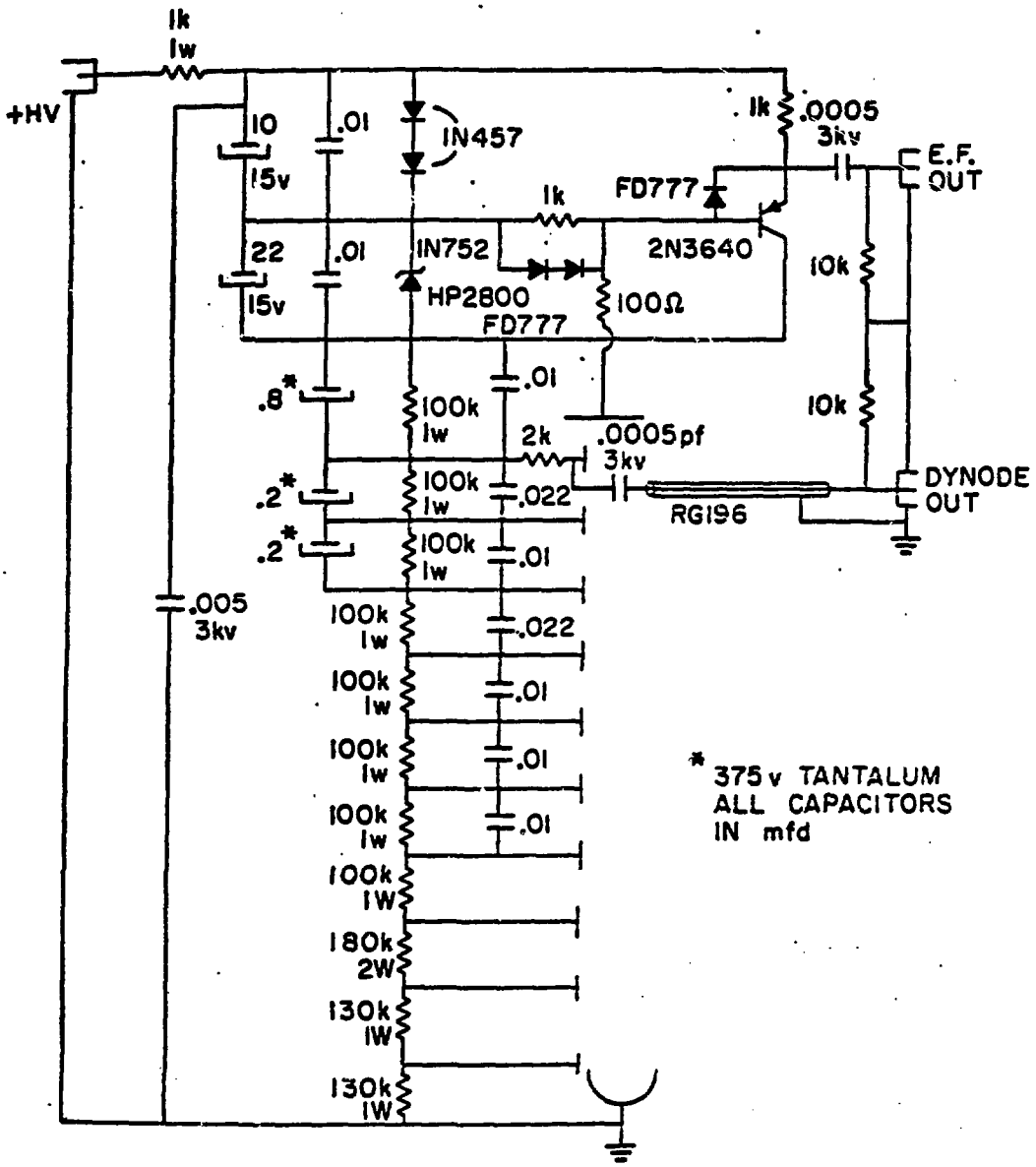
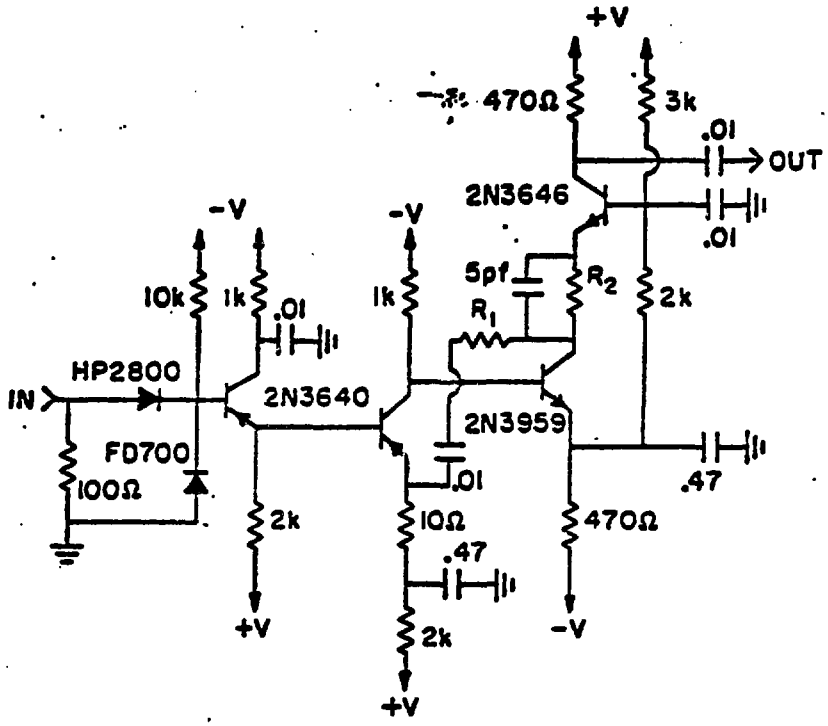

1k
1w
+HV
10
15v
.01
1N457
1k
.0005
3kv
E.F.
OUT
FD777
1k
22
15v
.01
1N752
2N3640
10k
HP2800
FD777
100Ω
.01
.8*
100k
1w
10k
2k
.0005pf
3kv
.2*
100k
1w
.022
DYNODE
OUT
RG196
.2*
100k
1w
.01
.005
3kv
100k
1w
.022
100k
1w
.01
100k
1w
.01
100k
1w
.01
100k
1W
180k
2W
130k
1W
130k
1W
* 375 v TANTALUM
ALL CAPACITORS
IN mfd

Figure 8



R_1: 240Ω FOR X3
100Ω FOR X10, X20

$10 < +V = |-V| < 20$

R_2: 68Ω FOR X3, X10
33Ω FOR X20

Figure 9

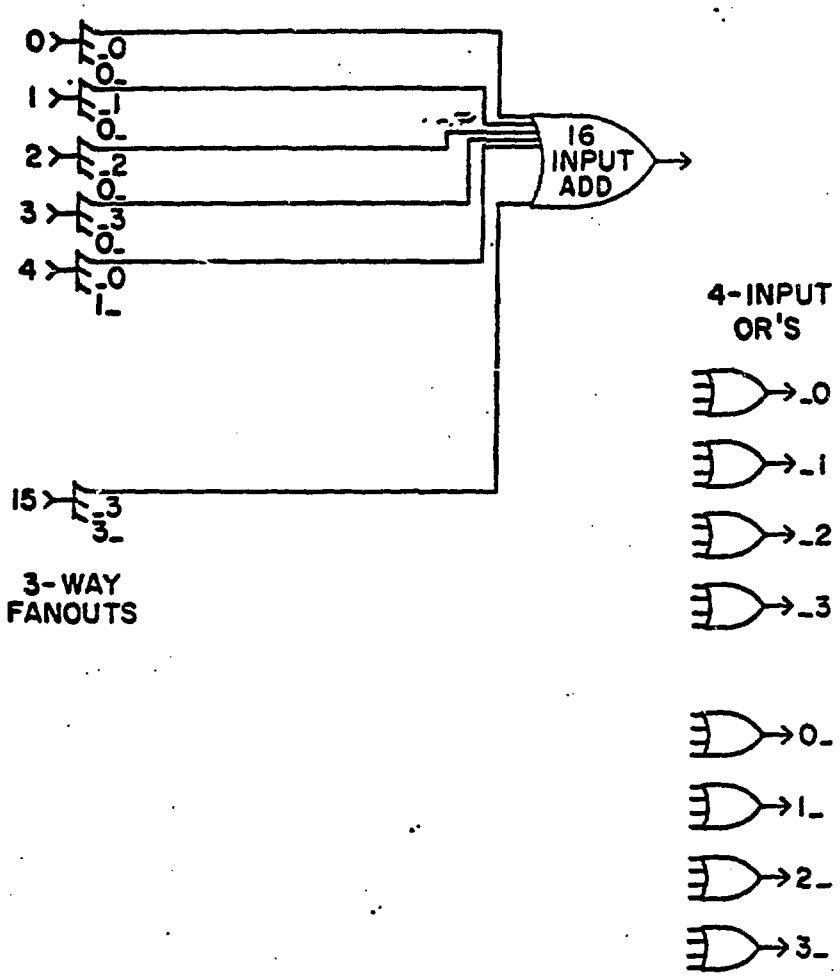

0
_0
0_
1
_1
0_
2
_2
0_
3
_3
0_
4
_0
1_
15
_3
3_
3-WAY
FANOUTS
16
INPUT
ADD
4-INPUT
OR'S
_0
_1
_2
_3
0_
1_
2_
3_

Figure 10a

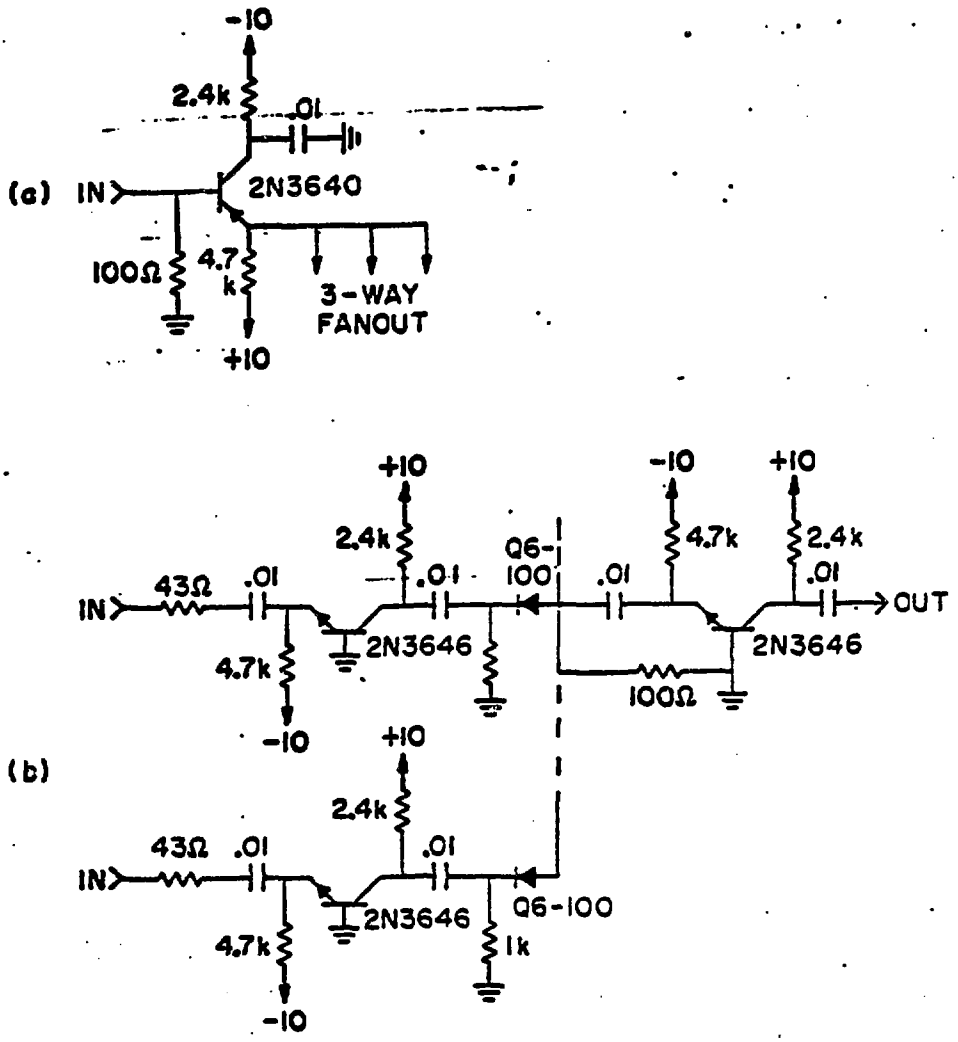

(a)
-10
2.4k
.01
IN
2N3640
100Ω
4.7 k
3-WAY FANOUT
+10
(b)
+10
2.4k
43Ω
.01
IN
4.7k
-10
2N3646
Q6-100
-10
+10
4.7k
2.4k
OUT
100Ω
+10
2.4k
43Ω
.01
IN
4.7k
-10
2N3646
Q6-100
1k

Figure 10b

HODOSCOPE DEVICE CONTROLLER BLOCK DIAGRAM

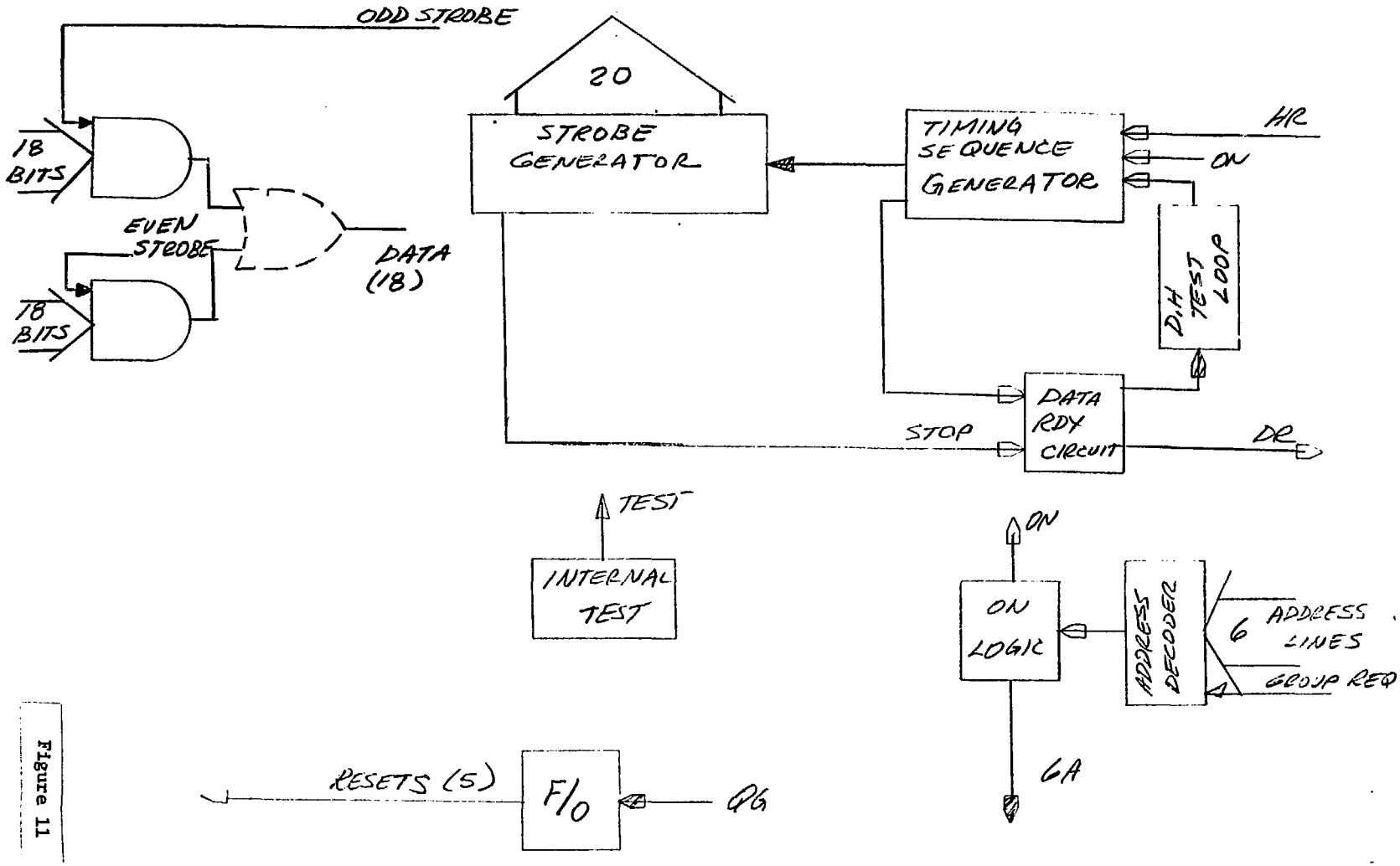


Figure 11

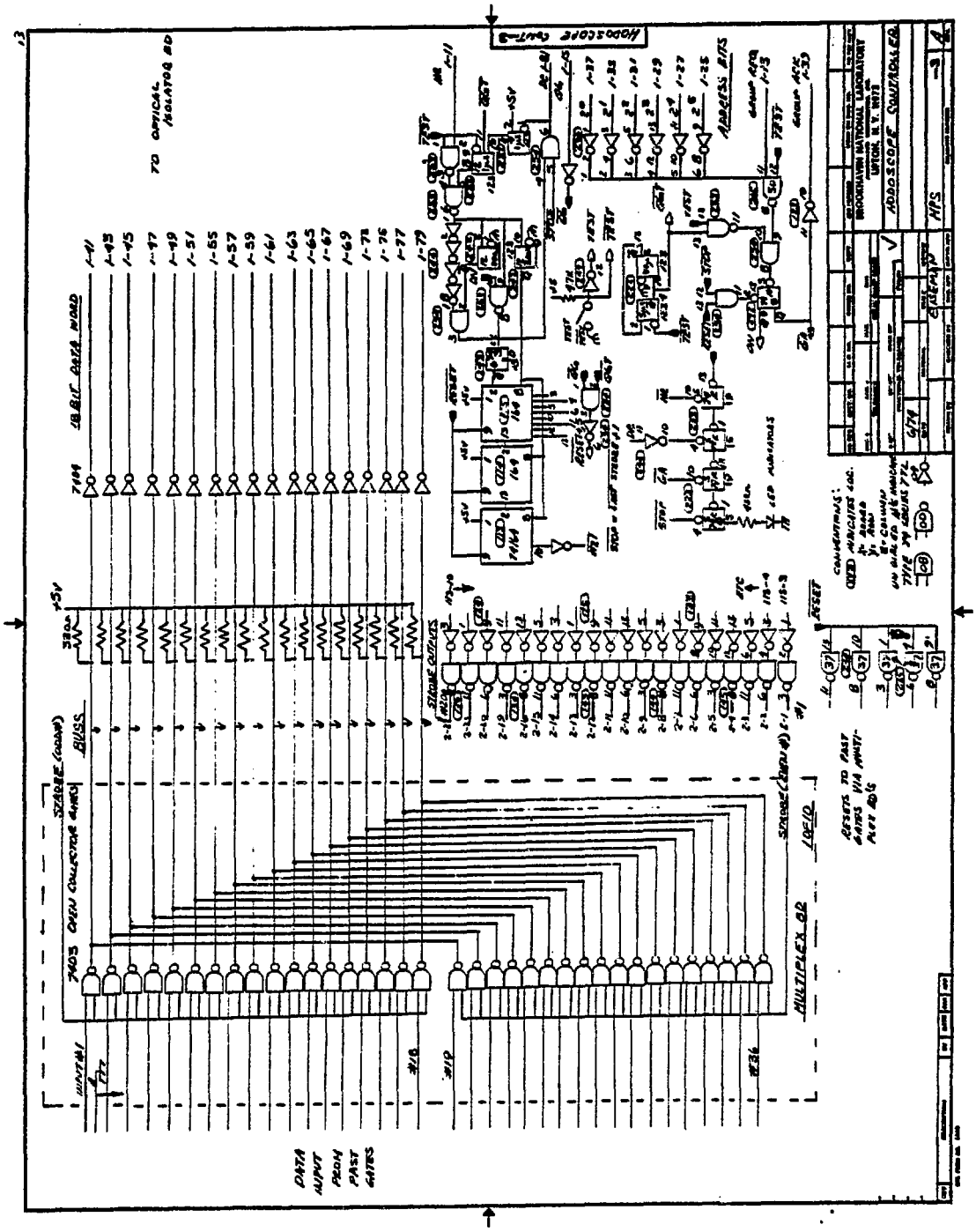

HODOSCOPE CONT-3
TO OPTICAL ISOLATOR BD
18 BIT DATA WORD
STROBE OUTPUTS
STROBE (ODD#)
BUSS
OPEN COLLECTOR GATES
LOFID
MULTIPLEX BD
DATA INPUT FROM PAST GATES
ADDRESS BITS
RESETS TO PAST GATES VIA MULTI-PLEX BD'S
CONVENTIONS:
BROOKHAVEN NATIONAL LABORATORY
UPTON, N.Y. 11973
HODOSCOPE CONTROLLER
HPS

Figure 12

BEAM PWC BLOCK DIAGRAM

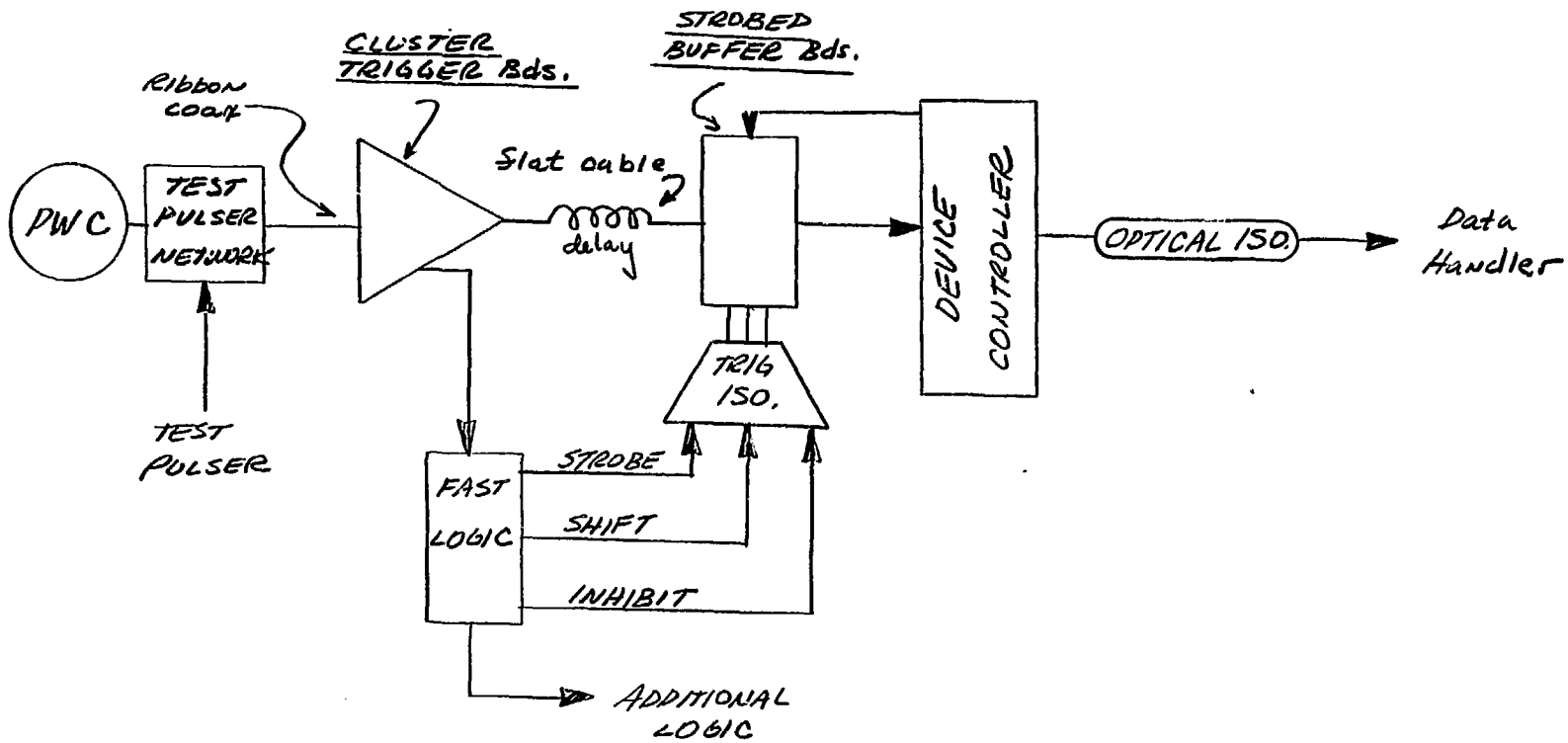
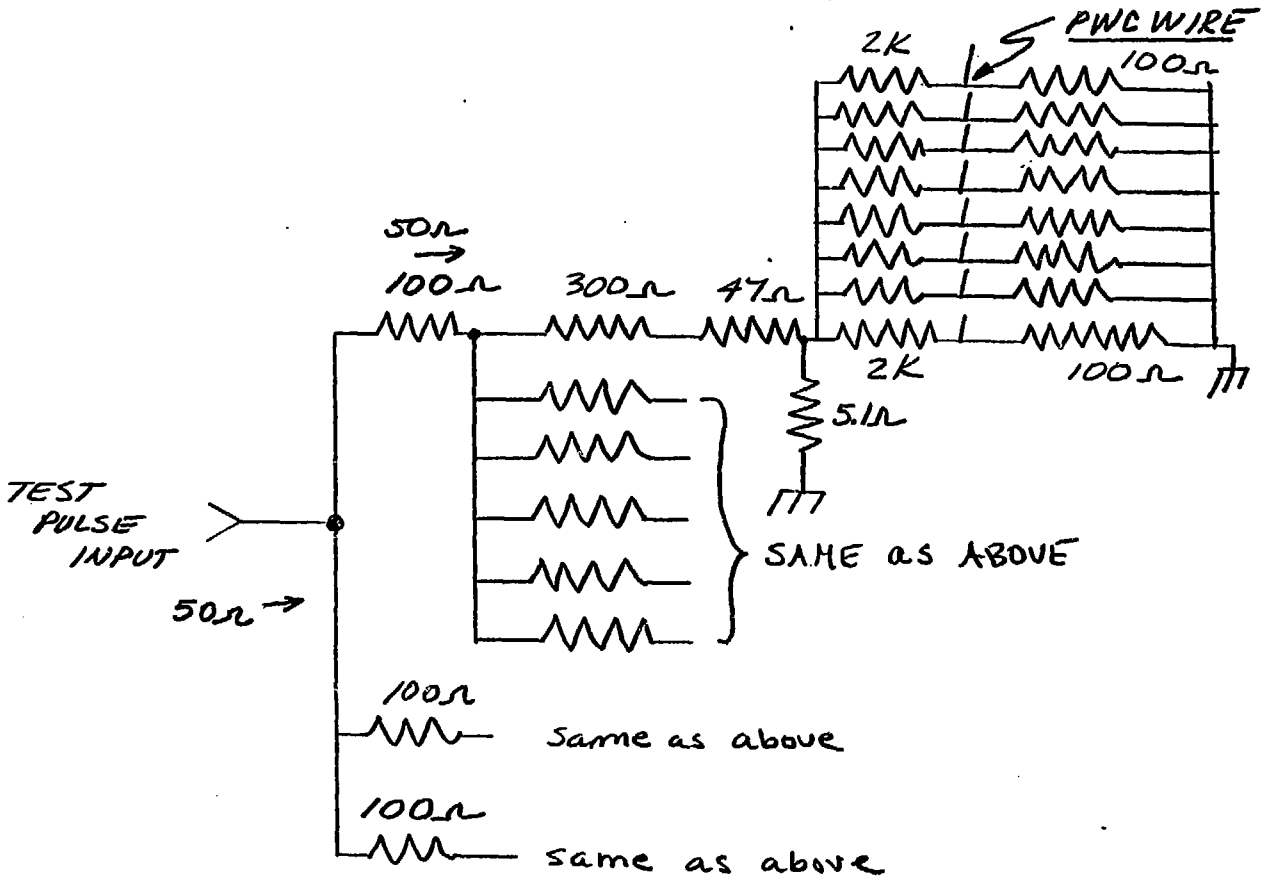


Figure 13

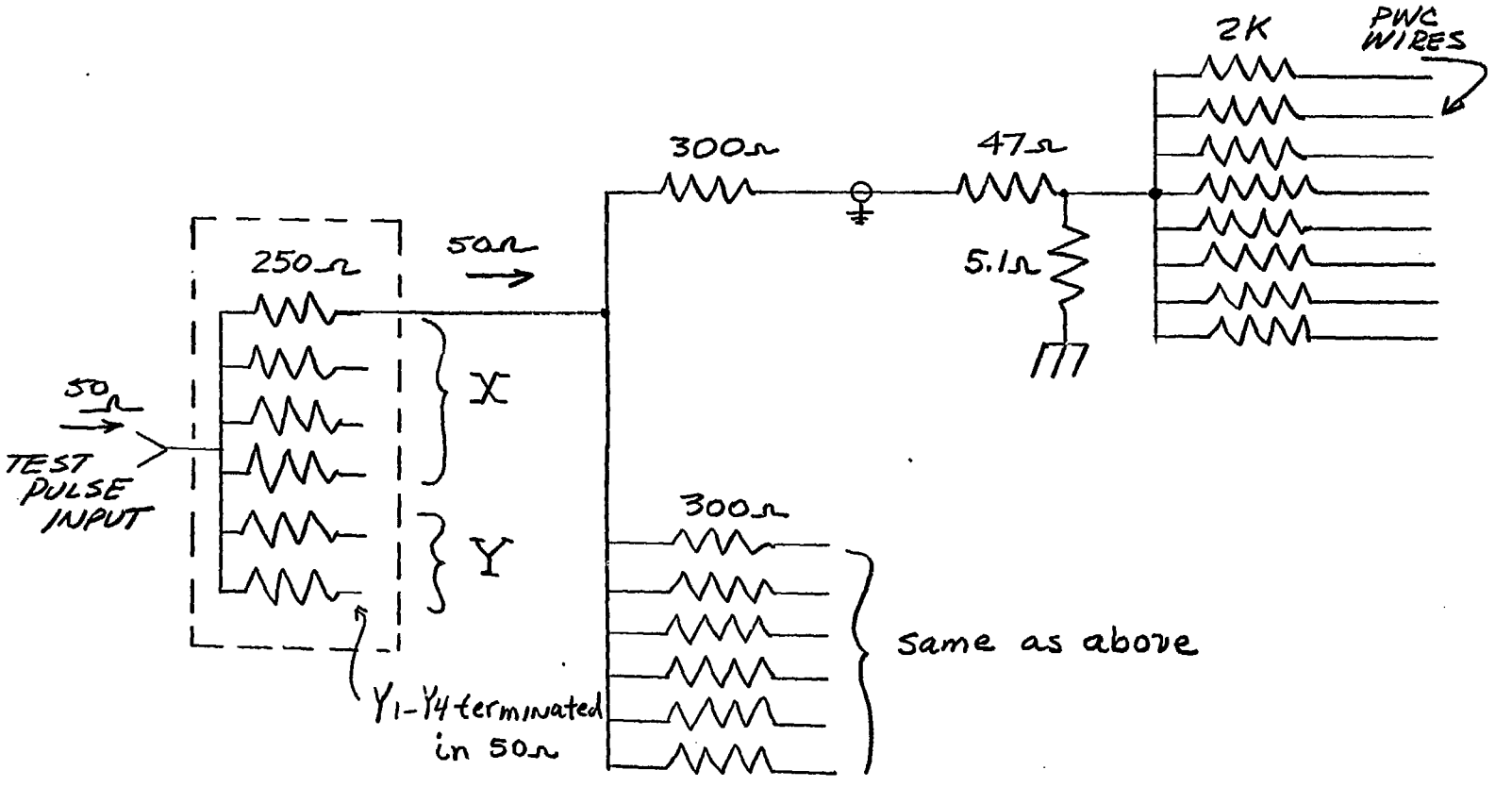
TEST PULSE NETWORK



NETWORK USED FOR 160 WIRES (50' RIBBON COAX cables)

Figure 14a

TEST PULSE NETWORK (BEAM PWC's)



USED WITH 10' RIBBON COAX

Figure 14b

CLUSTER TRIGGER BLOCK DIAGRAM

ONE OF EIGHT IDENTICAL CIRCUITS

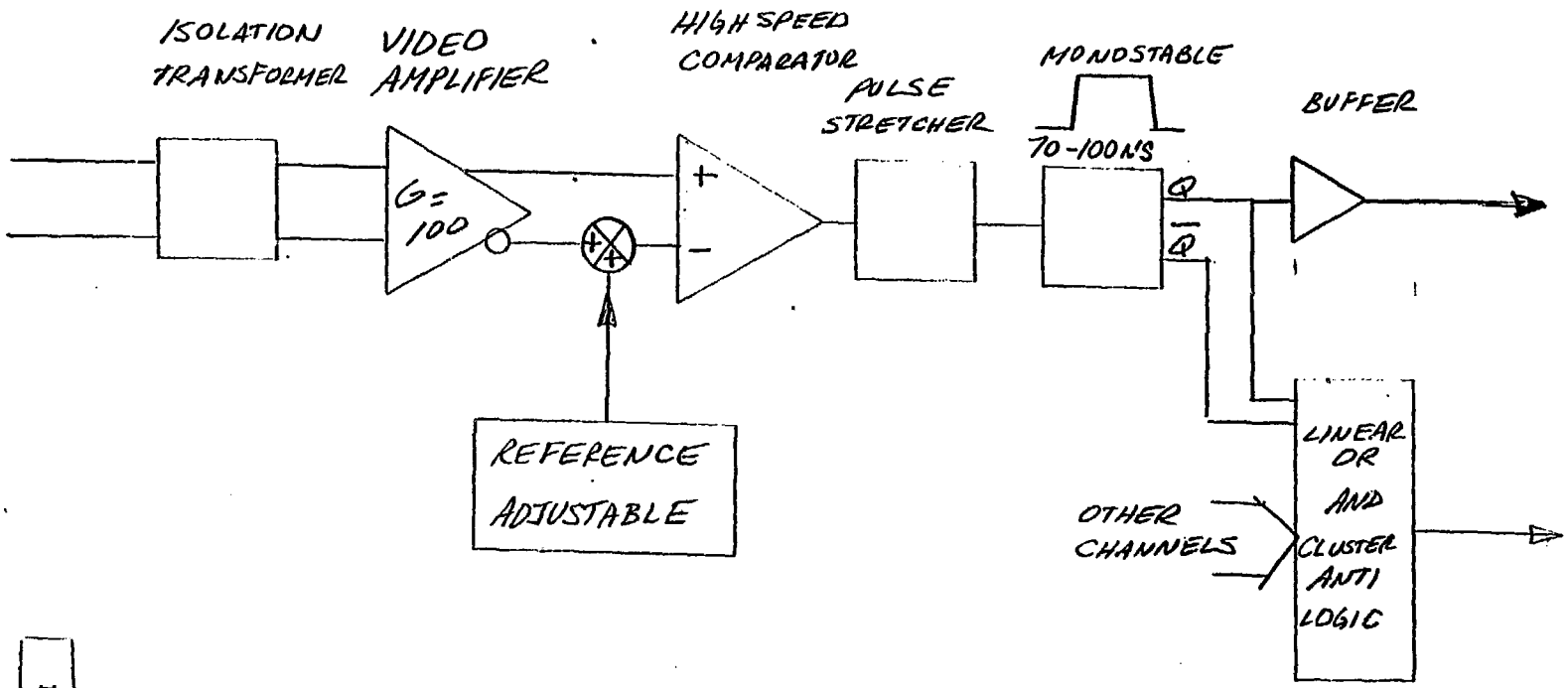


Figure 15

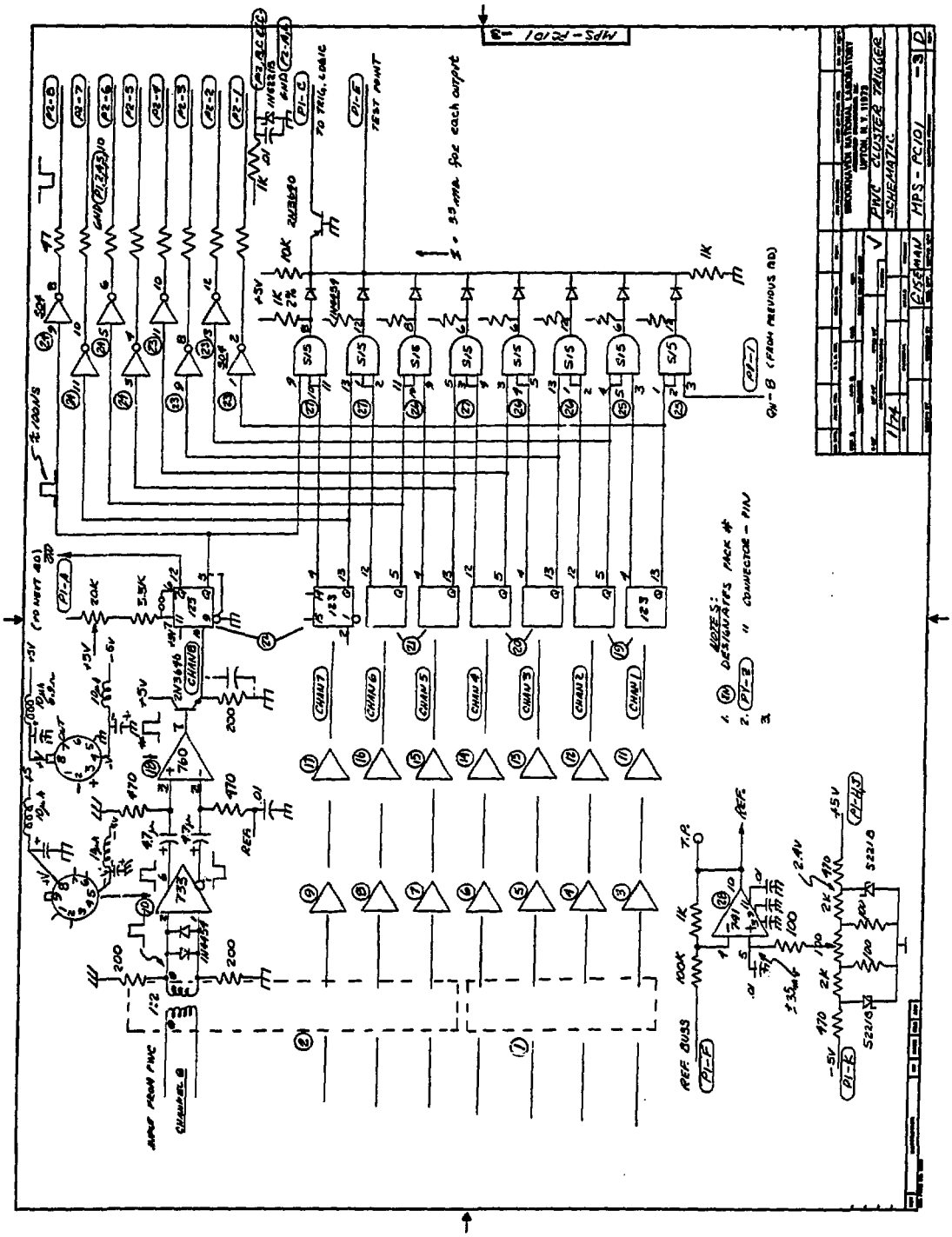

MPS-PC101 -3
PWC CLUSTER TRIGGER SCHEMATIC
MPS-PC101 -3
NOTES:
1. (IN) DESIGNATES PACK #
2. (P1-2) " CONNECTOR - PIN
3.
CHAN 1
CHAN 2
CHAN 3
CHAN 4
CHAN 5
CHAN 6
CHAN 7
CHAN 8
REF. BUSS
CHANNEL 8
TO TRIG. LOGIC
TEST POINT
REF.
T.P.
CISEMAN

Figure 16

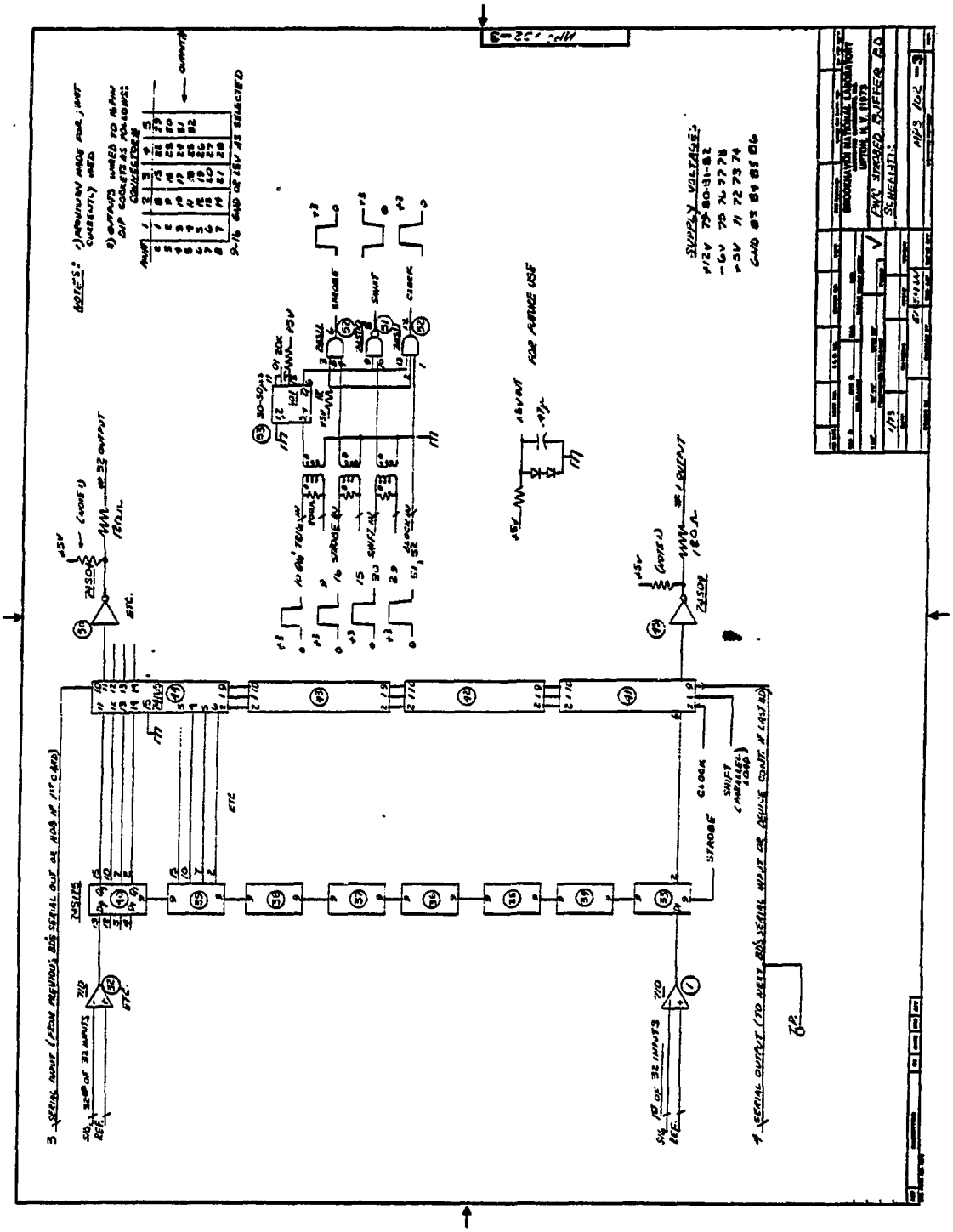
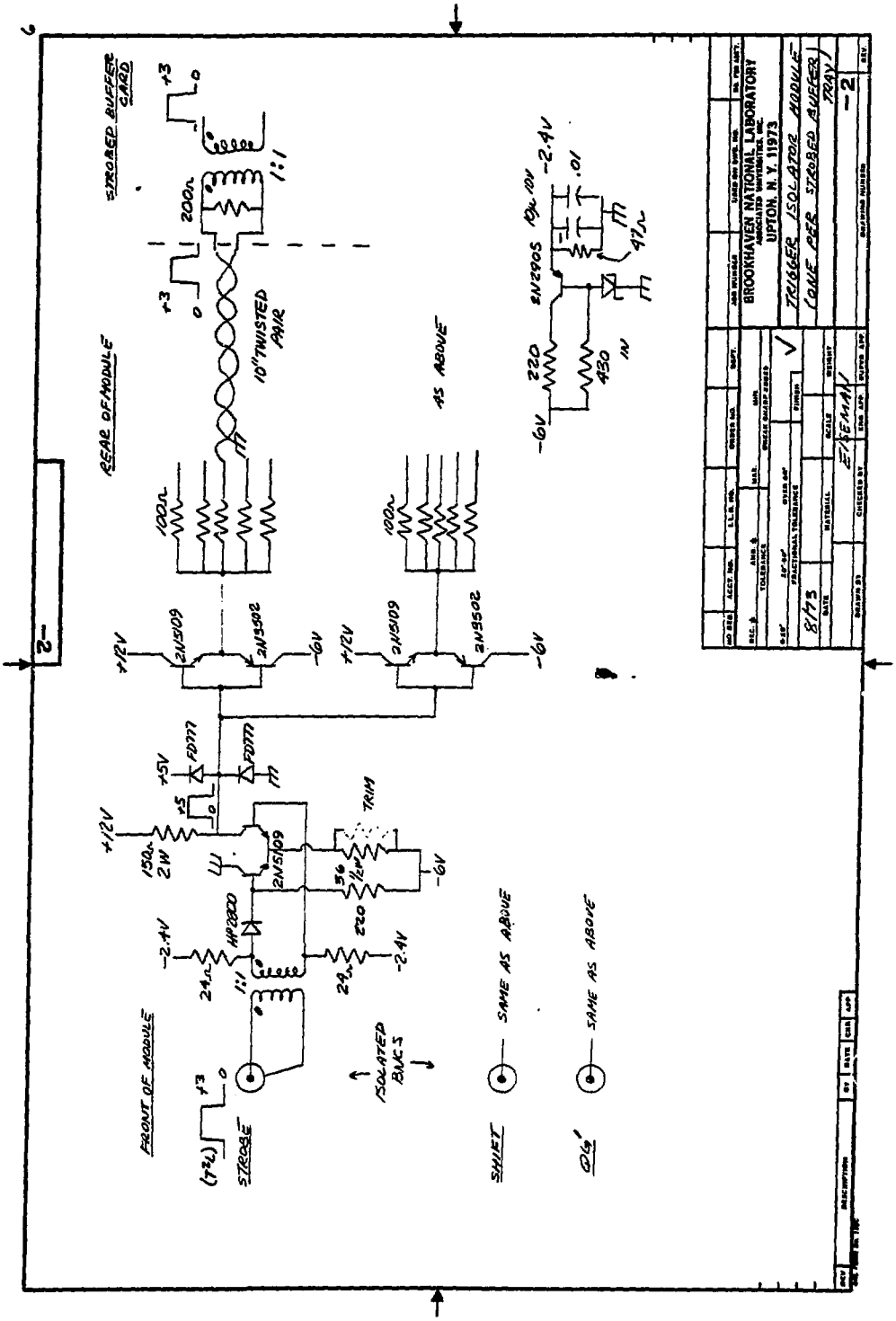


Figure 17



STROBED BUFFER CARD
REAR OF MODULE
10" TWISTED PAIR
AS ABOVE
FRONT OF MODULE
STROBE
ISOLATED BNCS
SHIFT
SAME AS ABOVE
QG'
TRIM
BROOKHAVEN NATIONAL LABORATORY
UPTON, N. Y. 11973
TRIGGER ISOLATOR MODULE
(ONE PER STROBED BUFFER)
TRAY
8/73
EISEMAN
-2

Figure 18

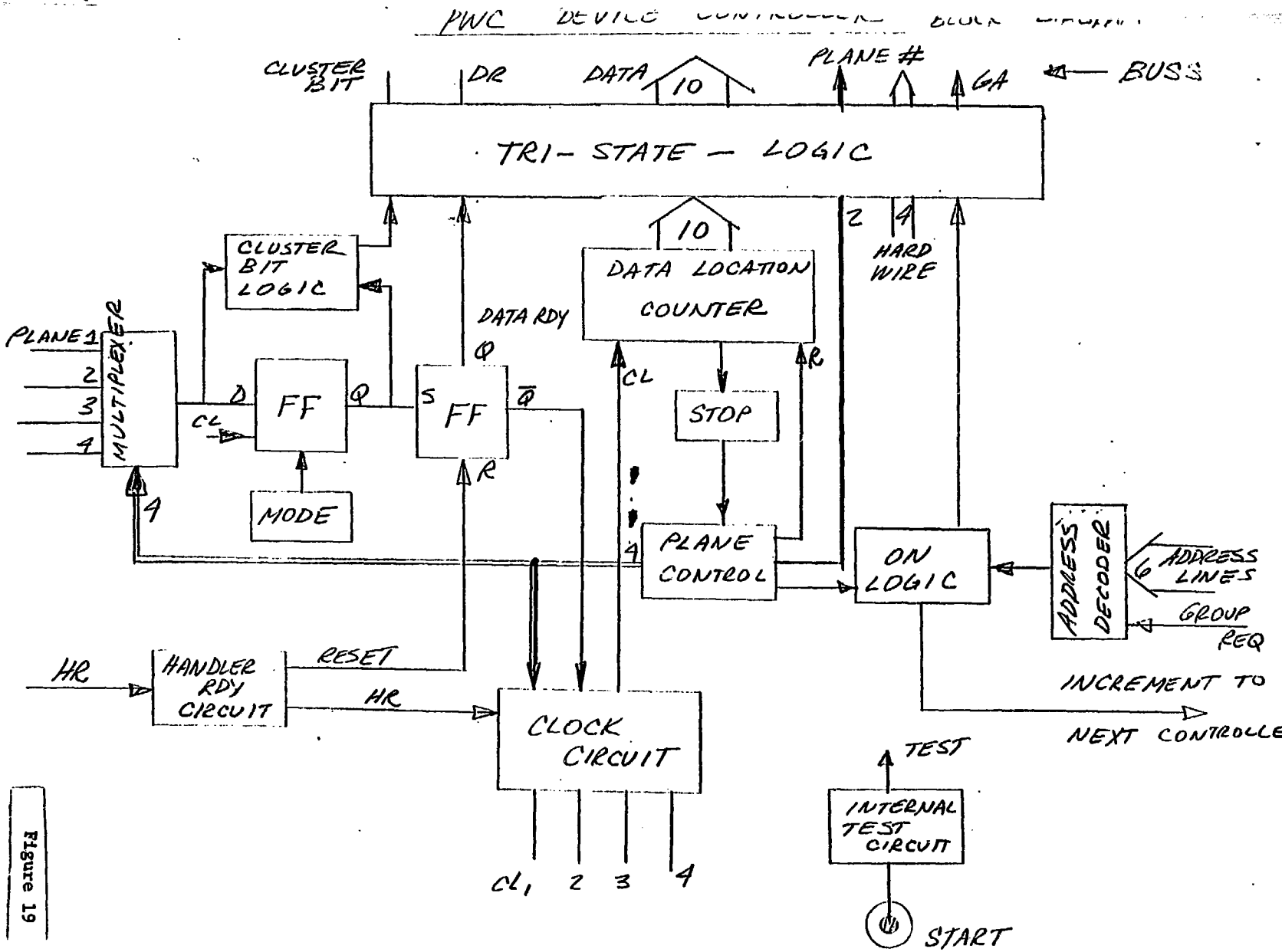

PWC DEVICE CONTROLLER BLOCK DIAGRAM
CLUSTER BIT
DR
DATA
10
PLANE #
GA
BUSS
TRI-STATE-LOGIC
10
2
4
HARD WIRE
CLUSTER BIT LOGIC
DATA LOCATION COUNTER
DATA RDY
PLANE 1
2
3
4
MULTIPLEXER
D
FF
Q
S
FF
Q
$\overline{Q}$
CL
R
CL
R
STOP
MODE
4
4
PLANE CONTROL
ON LOGIC
ADDRESS DECODER
6
ADDRESS LINES
GROUP REQ
HR
HANDLER RDY CIRCUIT
RESET
HR
CLOCK CIRCUIT
INCREMENT TO NEXT CONTROLLE
TEST
INTERNAL TEST CIRCUIT
START
CL1
2
3
4

Figure 19

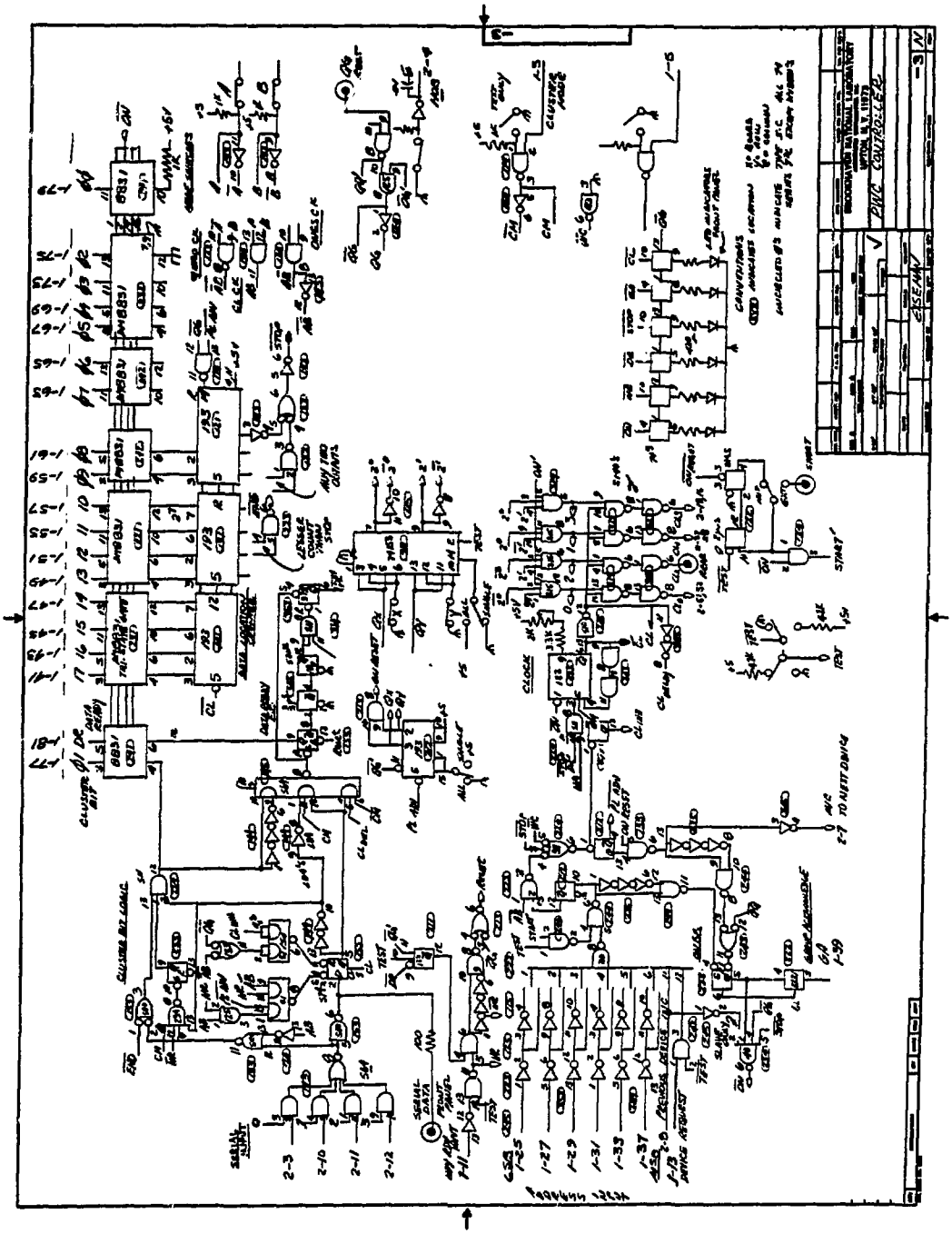


Figure 20

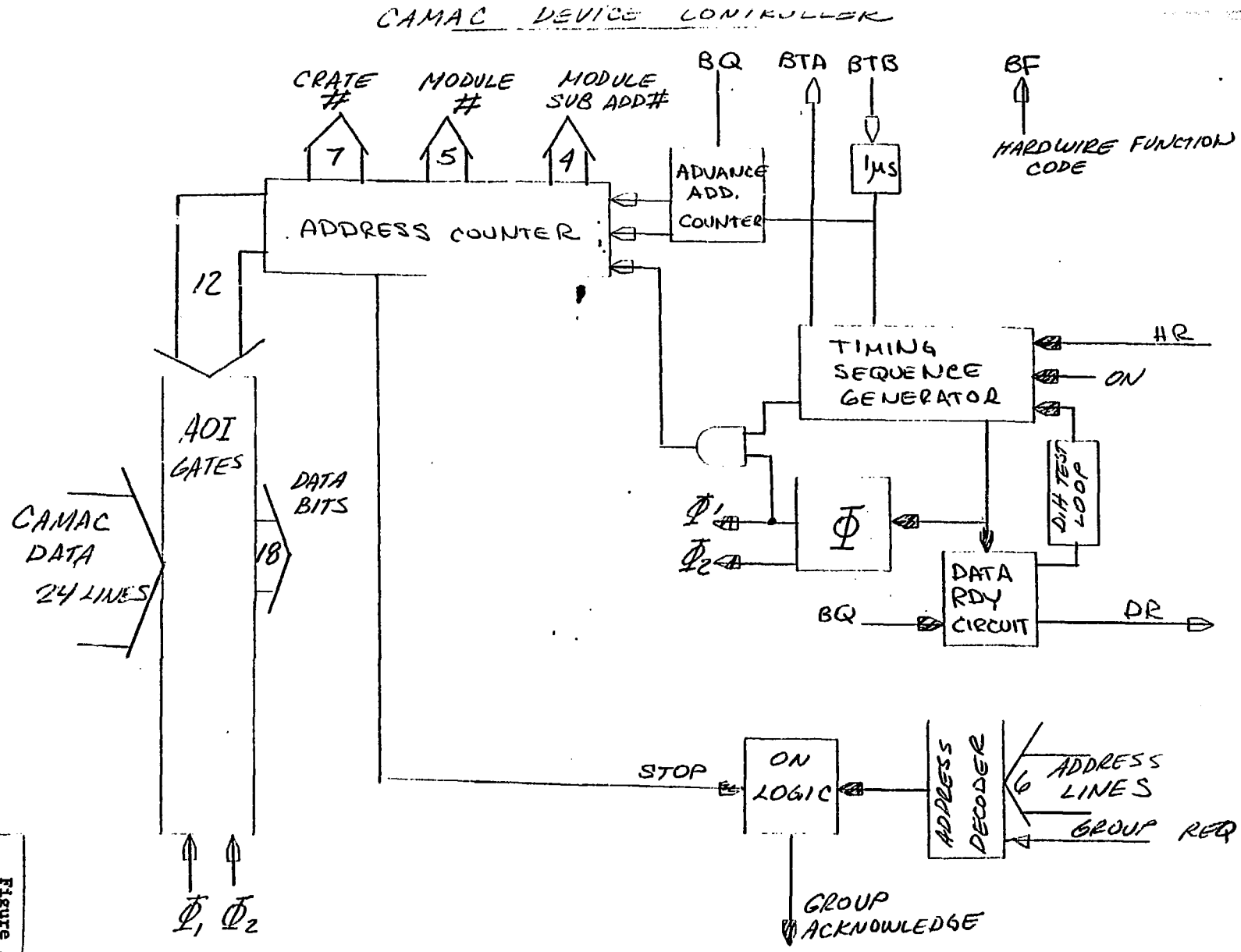

CAMAC DEVICE CONTROLLER
CRATE #
MODULE #
MODULE SUB ADD#
7
5
4
BQ
BTA
BTB
BF
HARDWIRE FUNCTION CODE
ADVANCE ADD. COUNTER
1μs
ADDRESS COUNTER
12
TIMING SEQUENCE GENERATOR
HR
ON
AOI GATES
DATA BITS
18
CAMAC DATA 24 LINES
Φ1
Φ2
Φ
DIH TEST LOOP
DATA RDY CIRCUIT
BQ
DR
STOP
ON LOGIC
ADDRESS DECODER
6
ADDRESS LINES
GROUP REQ
GROUP ACKNOWLEDGE
Φ1 Φ2

Figure 21

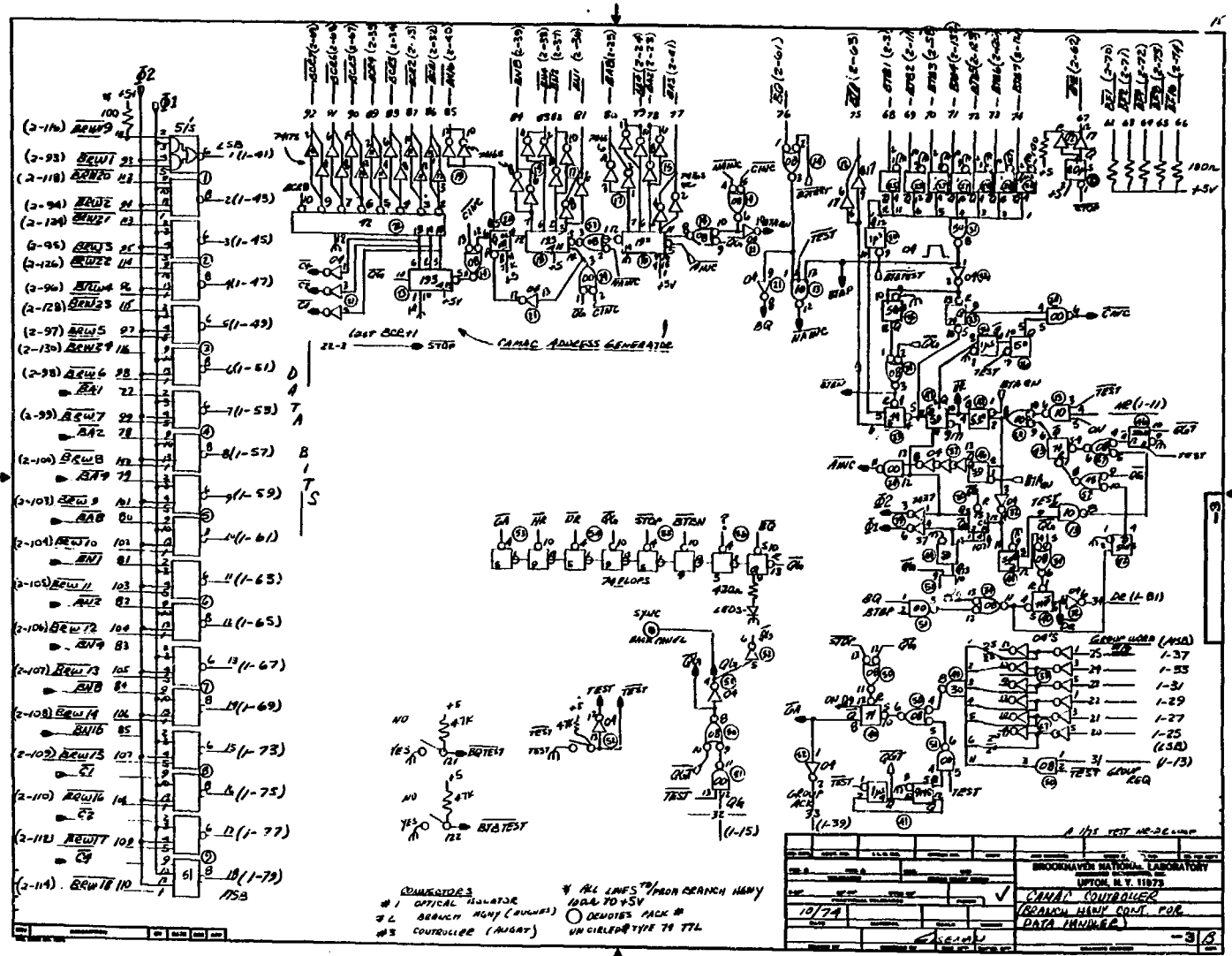

CAMAC ADDRESS GENERATOR
DATA BITS
74 FLOPS
BROOKHAVEN NATIONAL LABORATORY
UPTON, N.Y. 11973
CAMAC CONTROLLER
(BRANCH HWY CONT. FOR DATA HANDLER)
10/74

Figure 22

BY C.L.J. DATE 7/1/73 SUBJECT SPARK CHAMBER CLEARED SHEET No. ____ OF ____

CHKD. BY ____ DATE 6/12/73 CAPACITOR SHIFT REGISTER READOUT JOB No. ____

DEPT. OR PROJECT ____

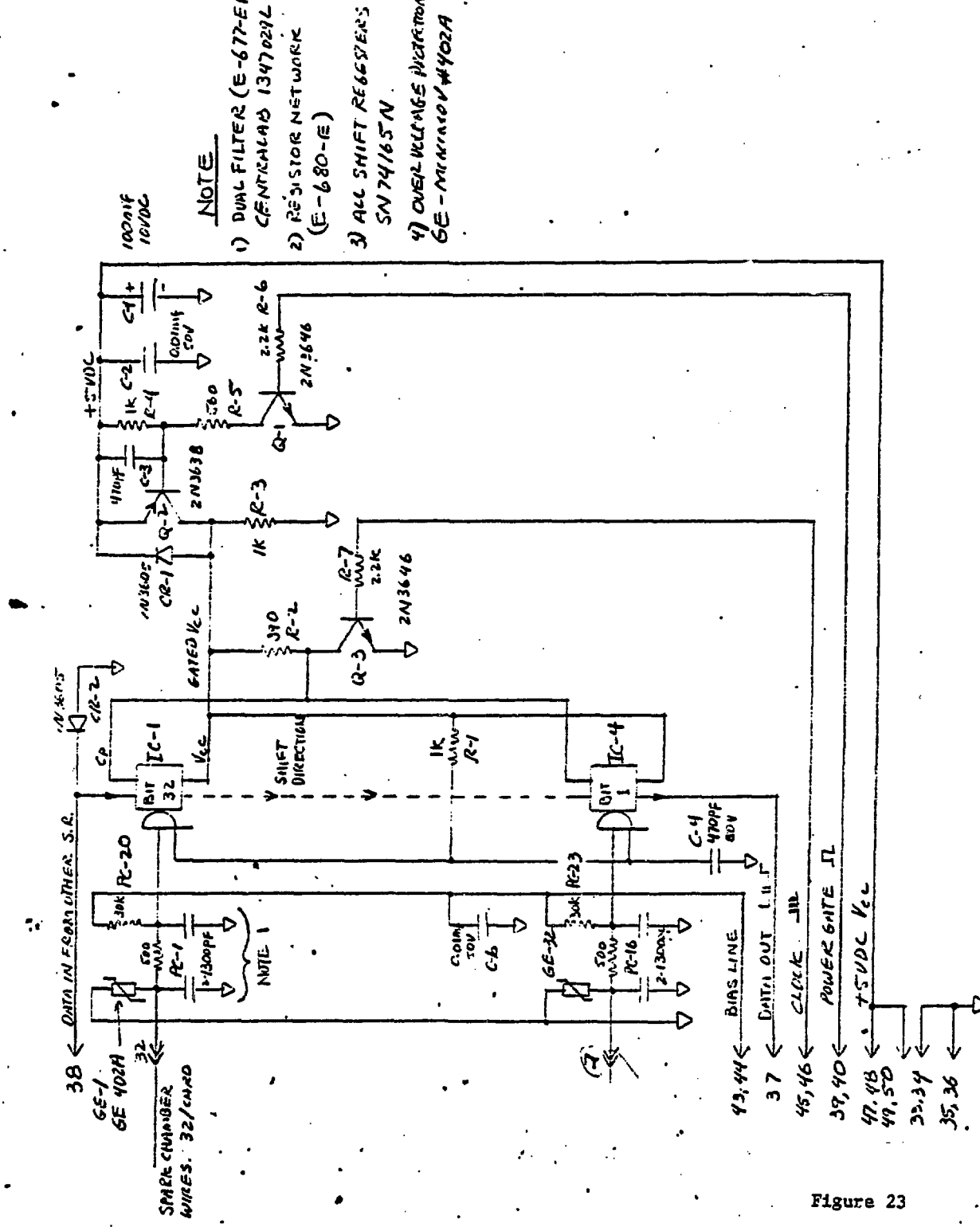


Figure 23

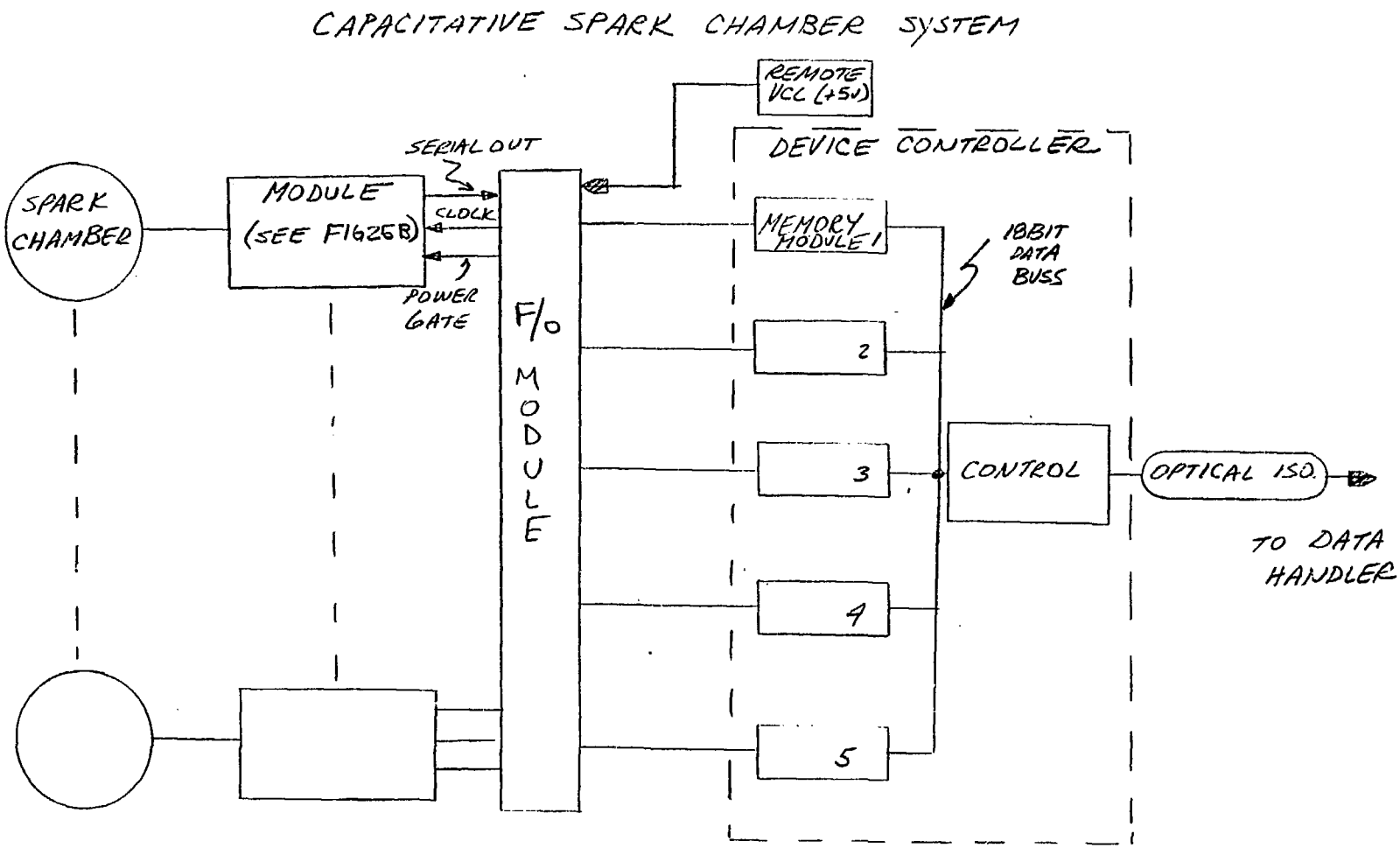

CAPACITATIVE SPARK CHAMBER SYSTEM
REMOTE VCC (+5V)
DEVICE CONTROLLER
SERIAL OUT
SPARK CHAMBER
MODULE (SEE FIG26B)
CLOCK
POWER GATE
F/O MODULE
MEMORY MODULE 1
2
3
4
5
18BIT DATA BUSS
CONTROL
OPTICAL ISO.
TO DATA HANDLER

Figure 24a

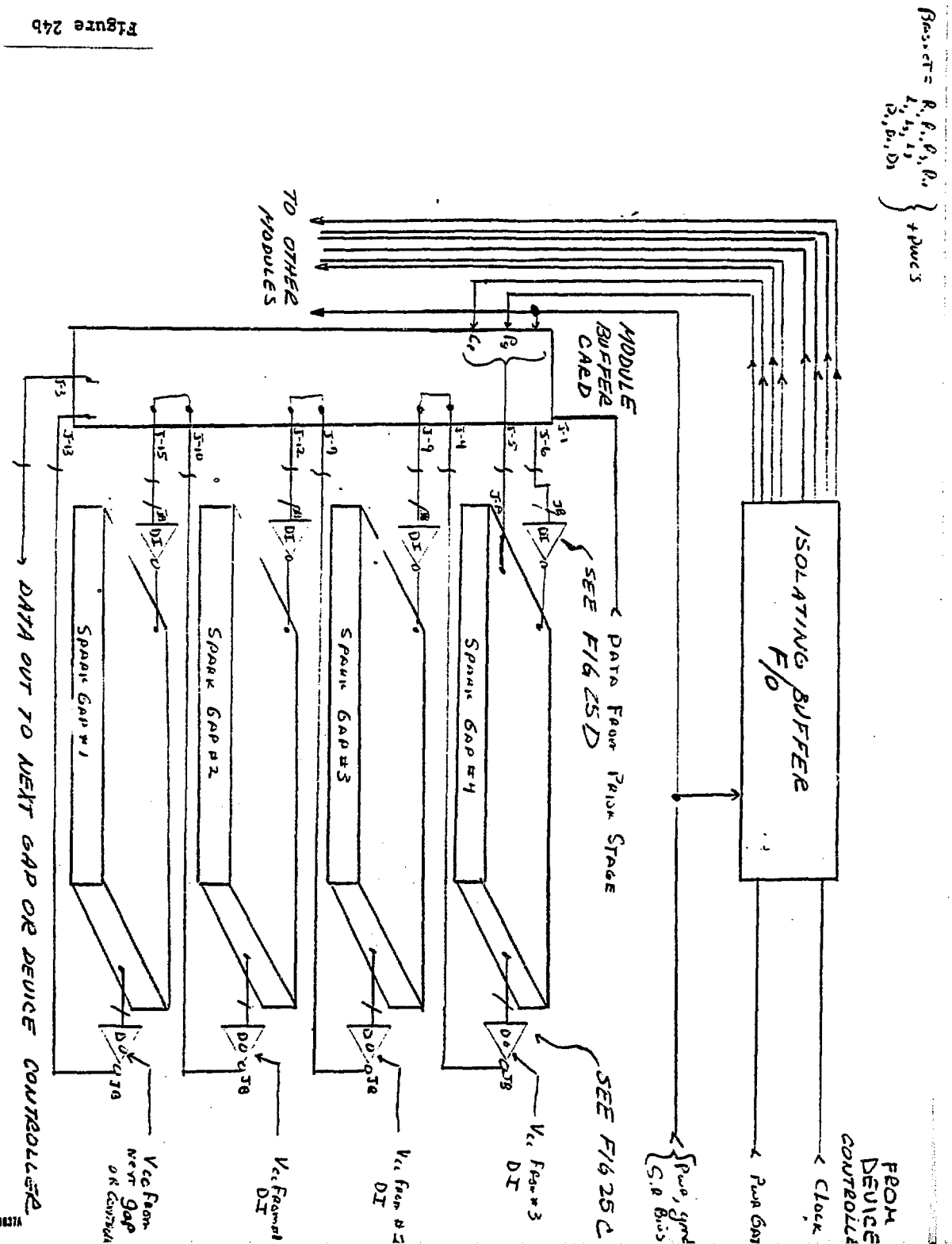
BROOKHAVEN NATIONAL LABORATORY

BY [illegible] DATE _____ SUBJECT Block Diag. Signal Distribution Case Modules SHEET No. 1 OF 1

CHKD. BY _____ DATE _____ JOB No. _____

Tentative Only DEPT. OR PROJECT _____

Figure 24b



SP 11837A

BY CW DATE 5/74 SUBJECT OUTPUT ISOLATOR CROSS-MPS SHEET NO. 1 OF 1

CHKD. BY ..... DATE ..... DEPT. OR PROJECT ..... JOB NO. .....

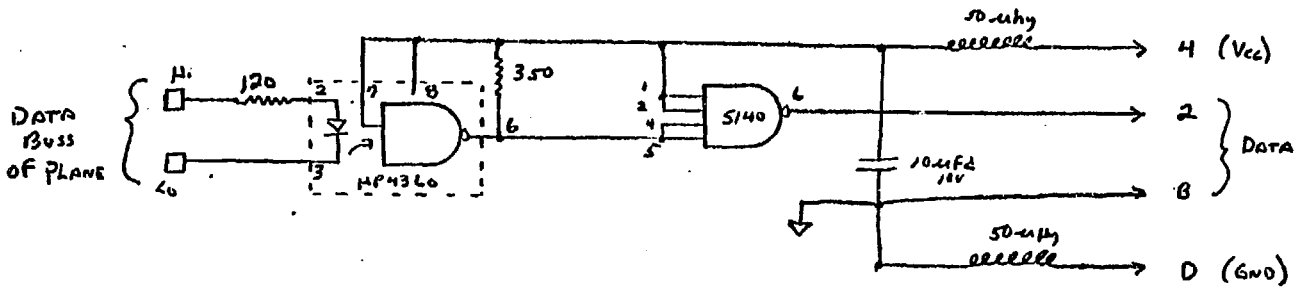


Figure 24c

BROOKHAVEN NATIONAL LABORATORY

BY CLJ DATE 5/94 SUBJECT INPUT ISOLATORS SHEET NO. 1 OF 1

CHKD. BY _____ DATE _____ CROSC MPS JOB NO. _____

DEPT. OR PROJECT _____

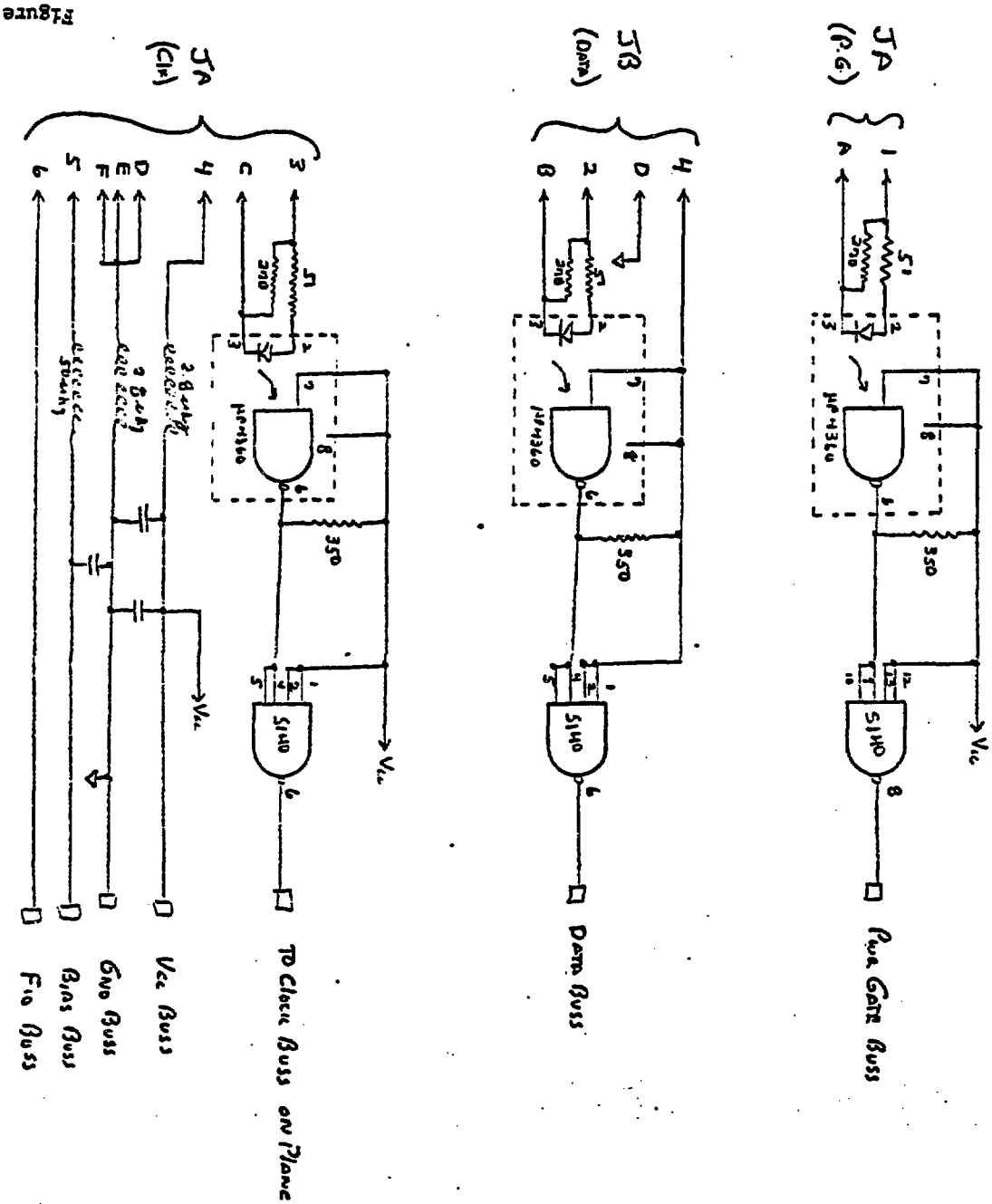


Figure 24d

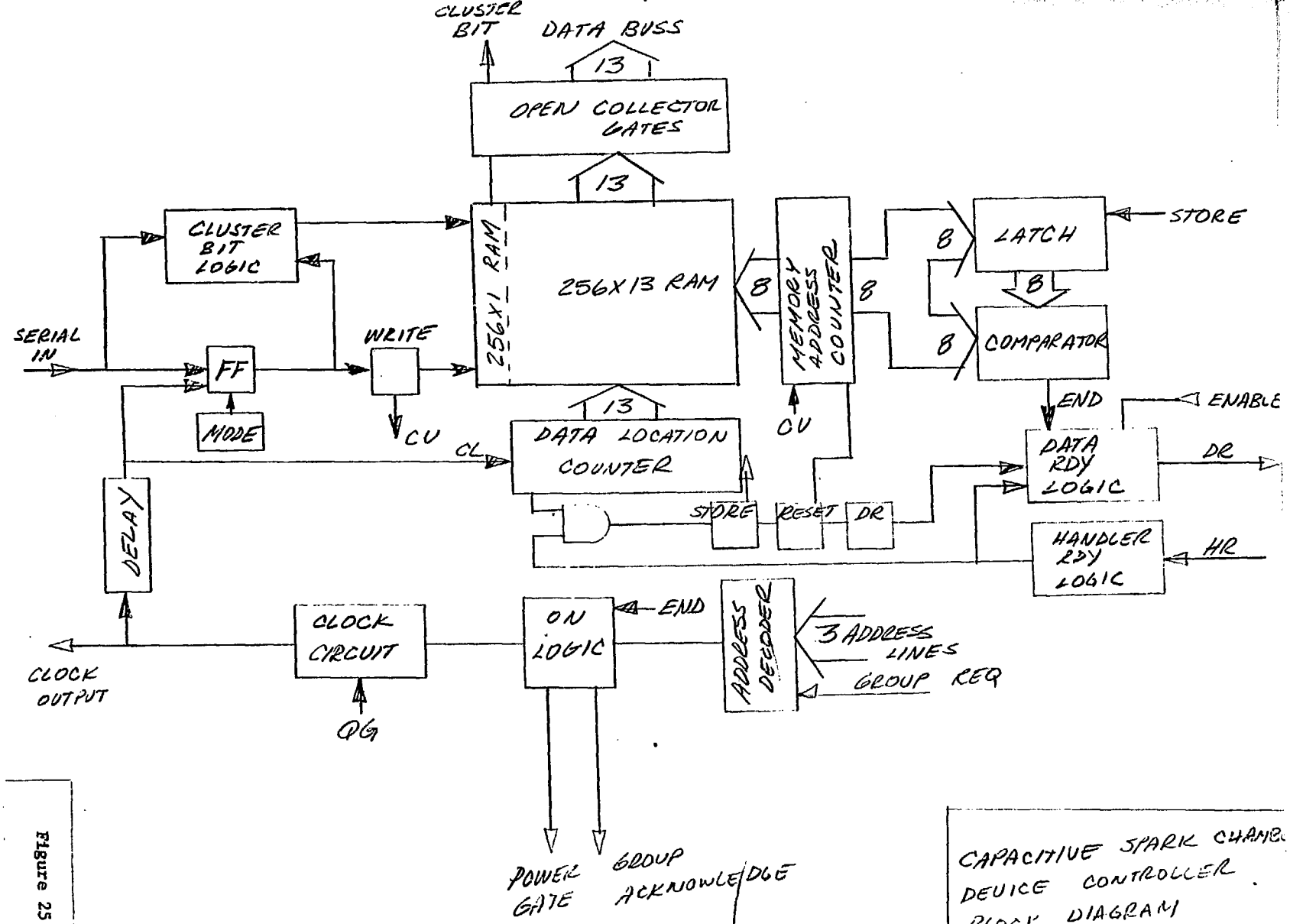


Figure 25

CAPACITIVE SPARK CHAMBER DEVICE CONTROLLER BLOCK DIAGRAM

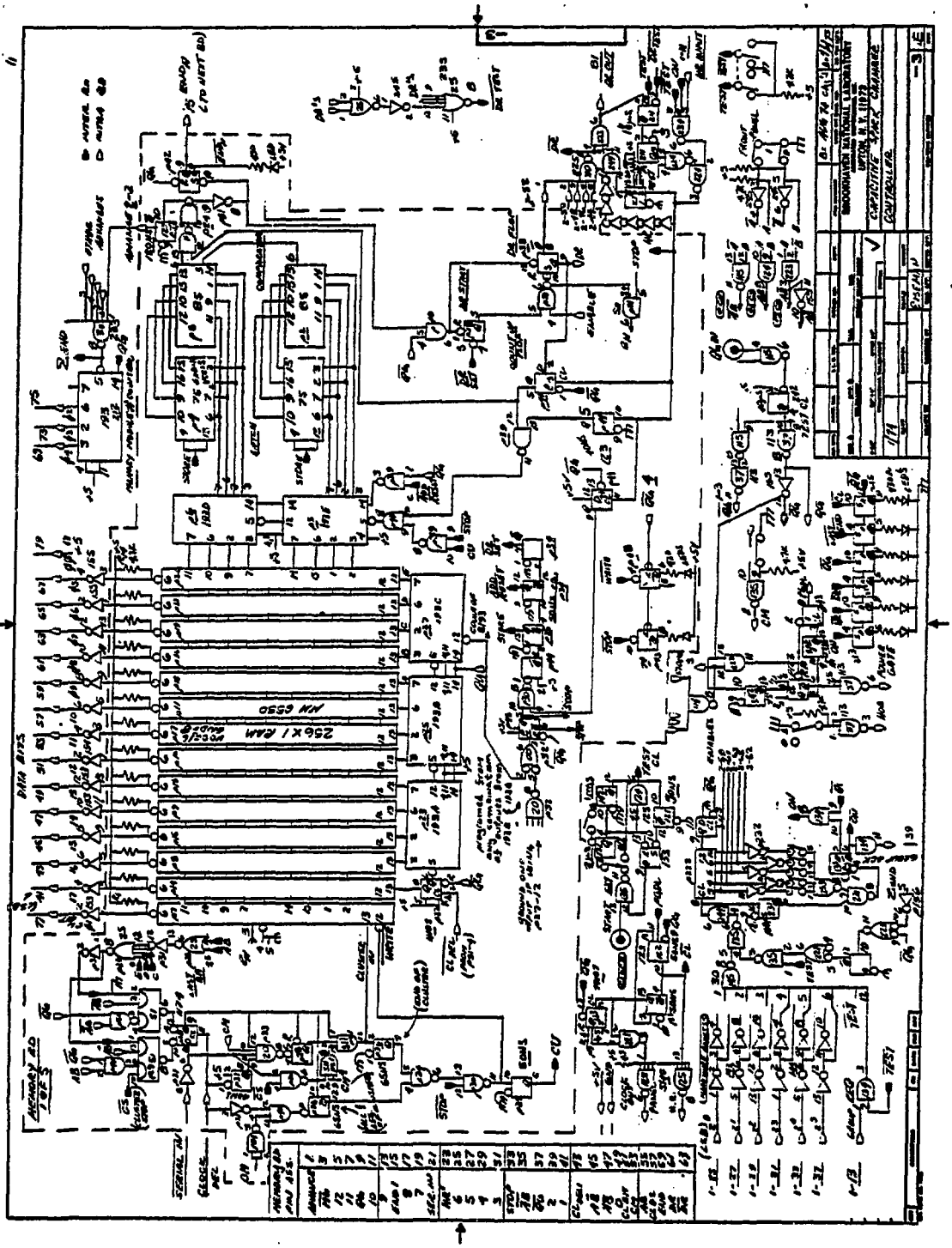

BROOKHAVEN NATIONAL LABORATORY
UPTON, N.Y. 11973
CAPACITIVE SPACE CHAMBER
CONTROLLER
256 X 1 RAM
MM 6550
DATA BITS
MEMORY BD
SERIAL IN
CLOCK
DEL
STOP
SONS
CU
TEST
CLUSTER
WRITE
POWER GATE
ENABLE
STORE
WRITE
CLOCK
DEL
MEMORY BD
PIN ASS.

Figure 26

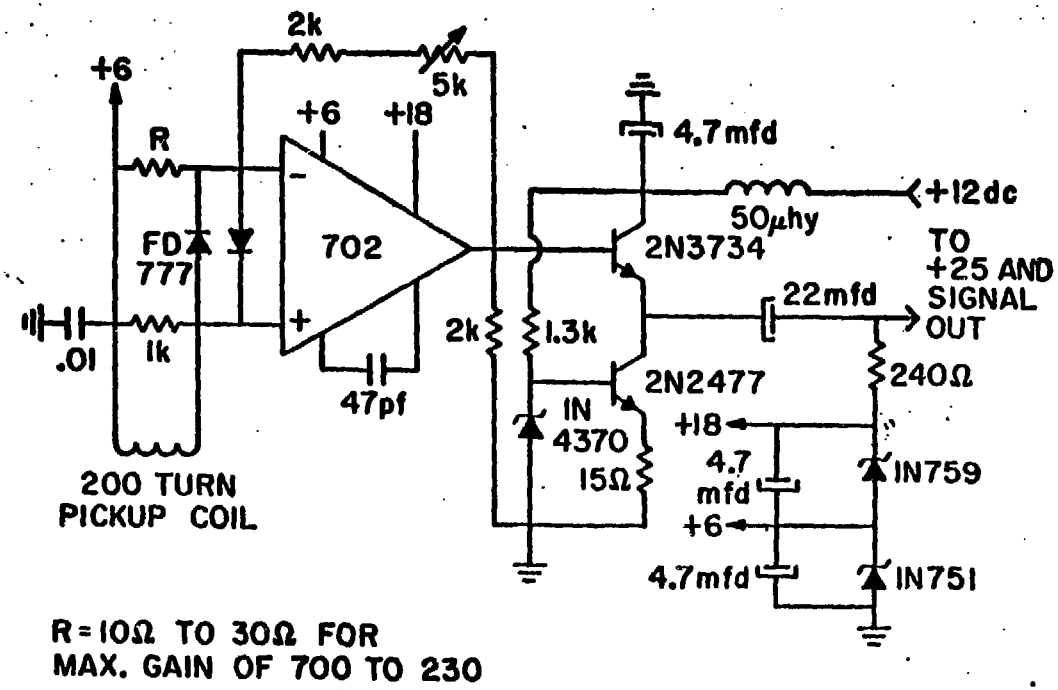

+6
2k
5k
R
+6
+18
4.7mfd
+12dc
50μhy
FD
777
702
2N3734
TO
+25 AND
SIGNAL
OUT
22mfd
.01
1k
2k
1.3k
2N2477
240Ω
47pf
IN
4370
+18
4.7
mfd
15Ω
IN759
+6
4.7mfd
IN751
200 TURN
PICKUP COIL
R=10Ω TO 30Ω FOR
MAX. GAIN OF 700 TO 230

Figure 27

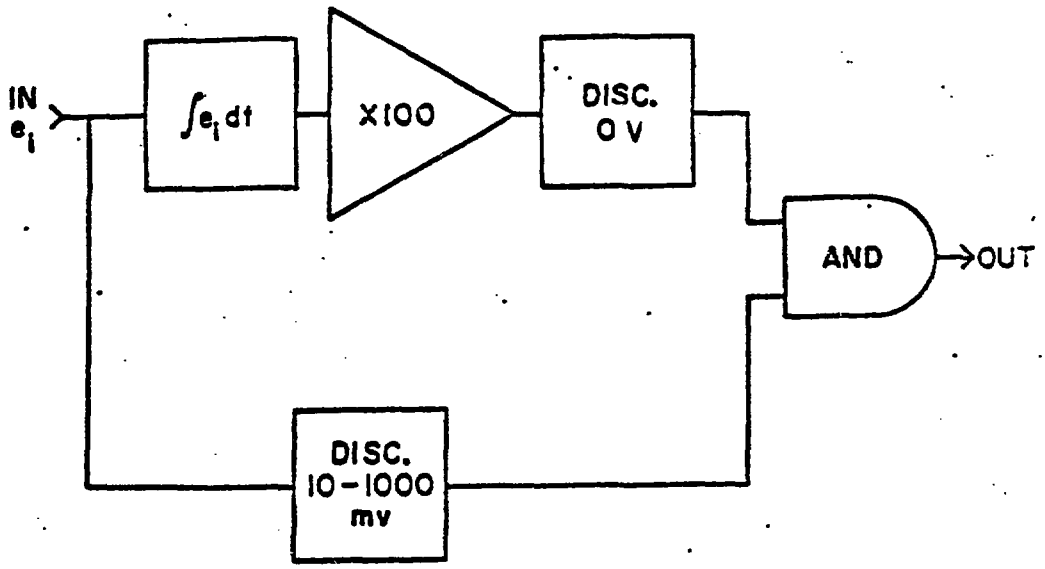


Figure 28a

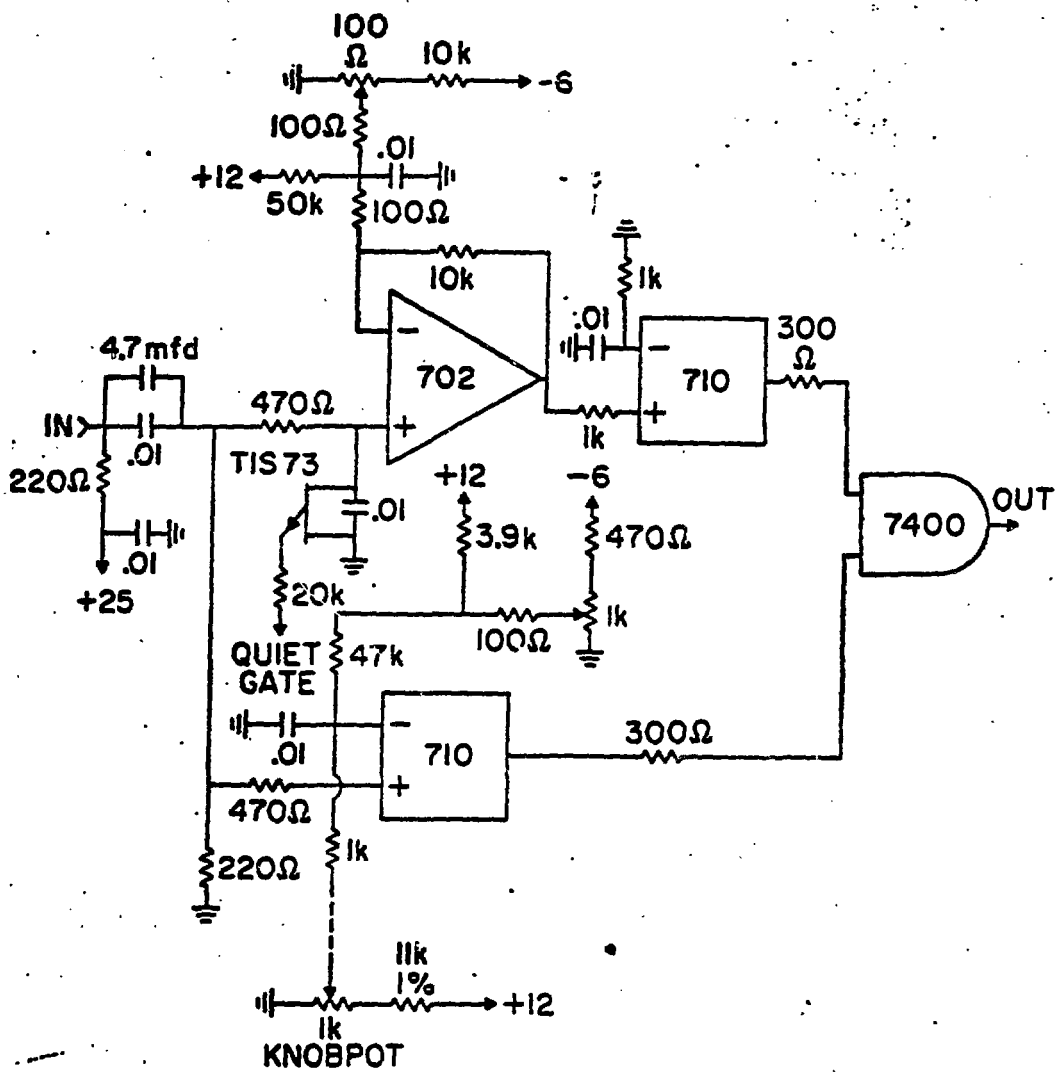

100
Ω
10k
-6
100Ω
.01
+12
50k
100Ω
10k
1k
.01
300
Ω
4.7mfd
702
710
470Ω
IN
.01
1k
220Ω
TIS73
+12
-6
.01
3.9k
470Ω
7400
OUT
.01
+25
20k
1k
100Ω
QUIET
GATE
47k
.01
710
300Ω
470Ω
220Ω
1k
11k
1%
+12
1k
KNOBPOT

Figure 28b

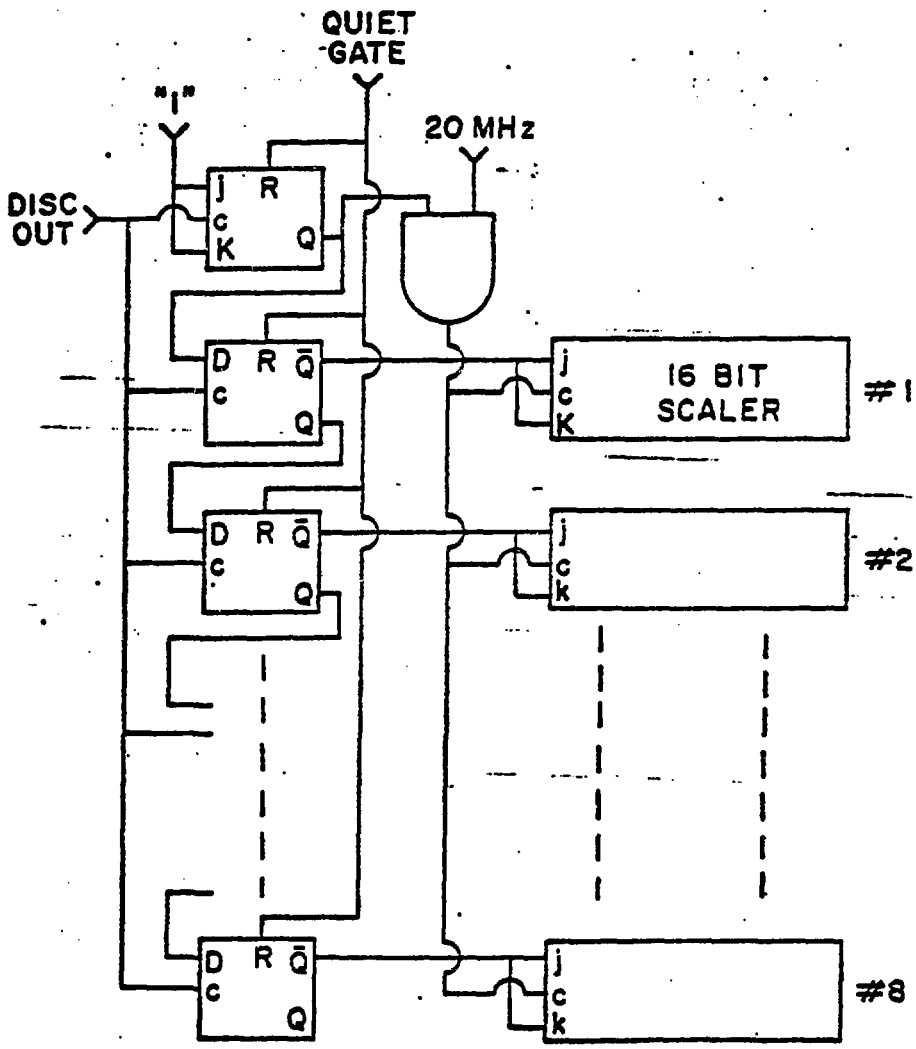


Figure 29