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A LOW-POWER, CMOS PEAK DETECT AND HOLD CIRCUIT FOR NUCLEAR PULSE SPECTROSCOPY*

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A Low-Power, CMOS Peak Detect and Hold Circuit for Nuclear Pulse Spectroscopy[1]

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Abstract

A low-power CMOS peak detecting track and hold circuit optimized for nuclear pulse spectroscopy is presented. The circuit topology eliminates the need for a rectifying diode, reducing the effect of charge injection into the hold capacitor, incorporates a linear gate at the input to prevent pulse pileup, and uses dynamic bias control that minimizes both pedestal and droop. Both positive-going and negative-going pulses are accommodated using a complementary set of track and hold circuits. Full characterization of the design fabricated in 1.2μm CMOS including dynamic range, integral nonlinearity, droop rate, pedestal, and power measurements is presented. Additionally, analysis and design approaches for optimization of operational characteristics are discussed.

I. INTRODUCTION

Several disadvantages associated with the classical peak detect and hold circuit were addressed with the topology introduced by Kruiskamp and Leenaerts [1] (see Fig. 1). This topology uses a MOS current mirror in place of the traditional rectifying diode. Use of this rectifying mirror minimizes the effect of charge injection into the hold capacitor and produces a circuit that is completely compatible with standard CMOS analog integrated circuit fabrication processes.

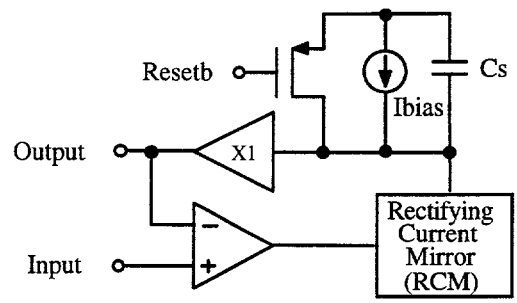

Fig. 1 Peak Detect and Hold Circuit Topology

This paper presents an improved peak detecting track and hold (PDH) circuit designed to address the specific needs of a nuclear pulse spectroscopy system [2] such as the one shown in Fig. 2. In this system, signals from the detectors are amplified and shaped for a peaking time of ~ 7 μs and are input into both the PDH and a discriminator. The

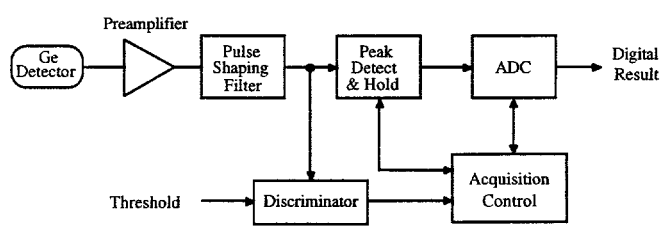

Fig. 2 Nuclear Spectroscopy Pulse Processing and Data Acquisition System Block Diagram

discriminator distinguishes noise from detector events and produces an output signal that indicates that an input pulse has exceeded the set threshold. An acquisition control block receives signals from the discriminator, PDH, and ADC and synchronizes the overall data acquisition operation. The

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intended application requires that the entire system be monolithically compatible, have very low power dissipation, and operate using a single 5-V supply.

The design presented in this work is based on a previously published topology [1] that has been modified for use in a low-power, monolithic spectroscopy system. The improved circuit incorporates a linear gate that allows the input to be disabled while in the hold mode to eliminate pulse pileup. Dynamic biasing of the reset transistor ensures sufficient loop gain during tracking to minimize pedestal voltage, and has a negligible effect during hold operations thus minimizing droop. Two additional circuit blocks were added which promote better circuit operation and system timing: a discriminator and peak detect circuit.

II. PDH CIRCUIT TOPOLOGY

The peak detect and hold topology presented in [1] outlines a significant improvement in the area of monolithic peak detect and hold circuits. The diode used in classical peak stretchers [3] is replaced using a rectifying current mirror. In this topology, an input differential pair compares the input voltage with the fedback output of the amplifier. A negative-going input pulse will be assumed for this example. As an input pulse amplitude becomes increasingly negative, the rectifying current mirror (RCM) sinks current that charges the sampling capacitor (Cs). As the pulse reaches peak value, the fedback voltage and input voltage become equal, the RCM turns off, and the output voltage is unable to follow the input signal back to the baseline since current cannot be sourced to Cs. The circuit at this point is open loop and will hold the pulse peak until droop effects diminish the signal integrity. A current source (Ibias) is used to prevent both undesired charging of the sampling capacitor while in the track mode and its associated instability. Removal of the rectifying diode and closer control of the current source switching amplitude reduce the errors due to charge injection. Additionally, all circuit components are compatible with common analog CMOS integrated circuit processes.

III. IMPROVED PDH CIRCUIT TOPOLOGY

The improved PDH circuit topology is shown in Fig. 3. The circuit shown is designed to detect and hold negative-going pulses referenced to 2.5 V. Several circuit additions have been made to improve the overall operation and accuracy. A linear gate consisting of two differential input stages is used to prevent pileup of incoming pulses. In the track mode the input signal is input into differential pair DP1. Once a peak has been detected, the hold loop is switched to a second differential pair, DP2, whose input is tied to the minimum channel input voltage (2.5 V in this case). This prevents a second incoming pulse from further charging Cs while in the hold mode and acts to keep the loop open. When the circuit is reset, DP1 is reenabled, and the circuit is ready for another peak detect and hold operation. Control of the linear gate input stages is accomplished using the complementary LIN-G and LIN-GB signals.

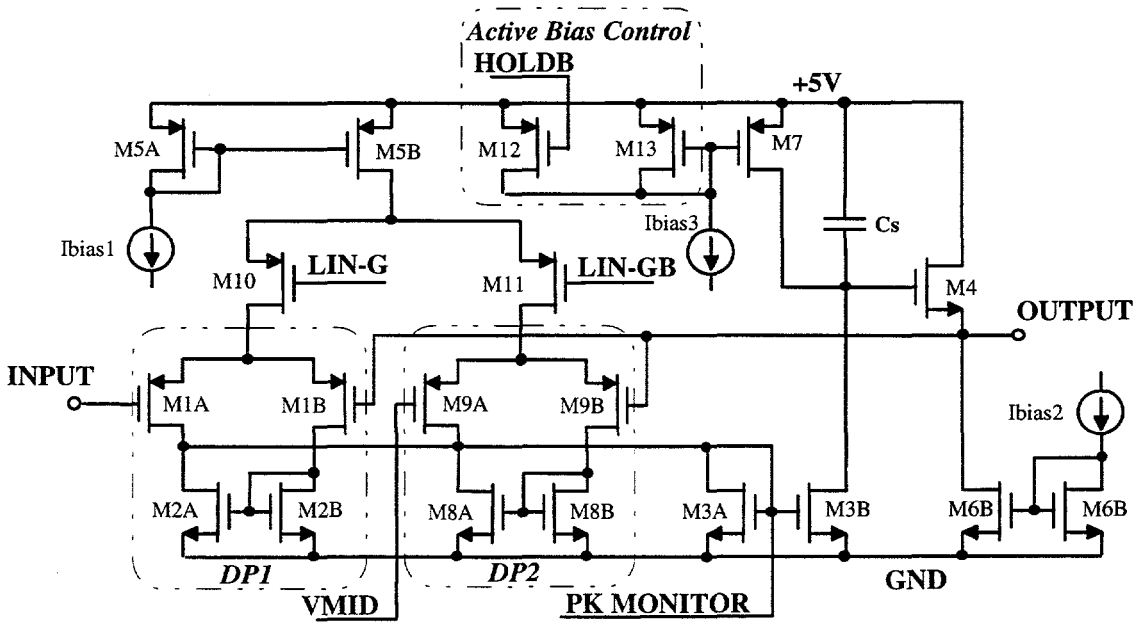

Fig. 3 Improved PDH Circuit Schematic - Negative Pulse Channel

Droop errors are reduced in the improved circuit by using an active biasing circuit. The current source (Ibias3) is required to maintain closed-loop operation while in the track mode by biasing M3 to prevent instability. However, during the hold operation, this current simply charges the hold capacitor (Cs), increasing the error due to droop. Elimination of this effect is accomplished by sensing existence of a pulse and turning off the current sourced by M7 while in the hold mode. Control of this disabling function during a hold operation is accomplished using a discriminator with latched output. Pulses over a set threshold set the discriminator output that asserts the HOLDB line. The threshold level has minimal effect on the circuit accuracy as long as HOLDB is activated by the time the pulse reaches maximum amplitude. Proper active biasing of M7 will result in reduced droop related errors since less current will be available for charging/discharging Cs during the hold operation.

Control of the linear gate input to prevent pulse pileup is accomplished using a peak detect circuit. Pulse peaks are detected by monitoring the bias condition of the rectifying current mirror M3B. Using a simple comparator designed to operate near the appropriate rail, the gate-to-source voltage (*Vgs*) of M3B is monitored and compared to a fixed reference voltage. As an input pulse is nearing peak, the differential pair that is comparing the output voltage (source followed voltage on Cs) to the input signal begins to turn off M3A, resulting in a sharp decrease in M3B *Vgs*. In addition to input control, use of the peak detect signal can provide useful timing information in some applications.

The pedestal in the improved topology can be attributed to two primary factors: input differential pair mismatch, and quiescent current at Cs due to M3B and M7. The quiescent current is maintained in normal operation such that a small amount of current flows into Cs. This is accomplished by the biasing of M7 using Ibias2 as previously described. The resulting change in the output voltage due to this current mismatch can be reduced by increasing the transconductance gain of the input differential pair by either transistor sizing or control of the bias current (Ibias2). Input device mismatch can be minimized using larger input devices with common centroid layout. Pedestal due to these sources tends to be somewhat independent of pulse amplitude and can be corrected for analytically if desired.

Another advantage of this general topology is its inherent duality. Inverting and resizing the devices and bias circuits allows the basic design to be directed toward either polarity operation (i.e. positive- or negative-going input pulses).

IV. DESIGN CONSIDERATIONS

One of the primary design goals for this circuit development was low-power operation using a single 5-V supply. With this requirement, the trade-offs associated with minimizing the current bias levels while retaining acceptable performance were paramount. Three bias currents are associated with this implementation. Ibias1 biases the input differential pair and can be used to tailor the closed loop characteristics while operating closed loop (tracking mode). Ibias2 is used to bias the output stage and must be sized according to loading requirements. Finally, Ibias3 is used to prevent undesired charging of the hold capacitor and can also affect the closed-loop gain as it sets the tracking current level in M3B.

The threshold set for monitoring *Vgs* of M3B is somewhat arbitrary since it swings at least several hundred millivolts in a short period of time relative to the pulse shaping time. The range M3B *Vgs* swings can be somewhat affected by the current amplitude sourced by M7. A small level of hysteresis built into the comparator circuit provides some noise immunity but is not essential for proper operation. Obtaining very small amounts of hysteresis using cross coupled drains is difficult if small geometry devices are desired due to the large required ratioing of device sizes [4].

The chosen value of Cs has an effect on several circuit characteristics. The closed-loop characteristics are affected by the value of Cs since it can become a dominant pole in the transfer function [1]. Cs should be selected large compared to the gate-to-source capacitance of M3B to minimize the effect of charge injection when M3B is turned off. Additionally, larger values of Cs will also act to further reduce the droop rate. The primary limitations to the size of Cs are the physical size limitations and the effect on system bandwidth and loop characteristics.

V. EXPERIMENTAL RESULTS

Complementary versions of the PDH circuit were designed and fabricated in 1.2-μm N-well CMOS. A discriminator circuit was also designed and included with each PDH design. A single ASIC with two channels, each optimized for one pulse type, was tested with the input pulses referenced to 2.5 V. The results of these measurements are summarized in the following sections.

A. Dynamic Range and Integral Nonlinearity (INL)

Pulses shaped using a 6-μs semigaussian shaping filter were input to the circuit, and the INL was calculated from data taken using a Trecor Northern TN-7200 multichannel analyzer (MCA). An example plot showing an input waveform and PDH output for a positive input circuit is shown in Fig. 4. The results of the dynamic range and INL tests are summarized in Table 1. Note that all pulse amplitudes are referenced to 2.5 V.

INL as a function of input pulse amplitude is demonstrated in Fig. 5 for both positive and negative PDH circuits. Linearity errors associated with the endpoints are largely due to pedestal error for small input pulses and circuit nonlinearity associated with operation near the power supply rails for large input pulses.

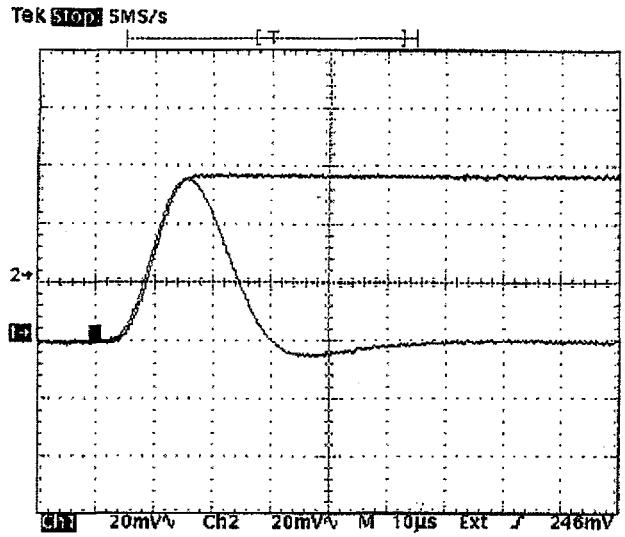

Fig. 4 Sample Input/Output Waveforms for Positive Input PDH Channel

Table 1. Dynamic Range and INL Results for PDH Circuits

	Negative-Pulse PDH Circuit	**Positive-Pulse PDH Circuit**
Pulse Amplitude Range	-25 mV to -2.50 V	+25 mV to +2.50 V
Dynamic Range	100/1	100/1
INL	< ±0.05%	< ±0.16%

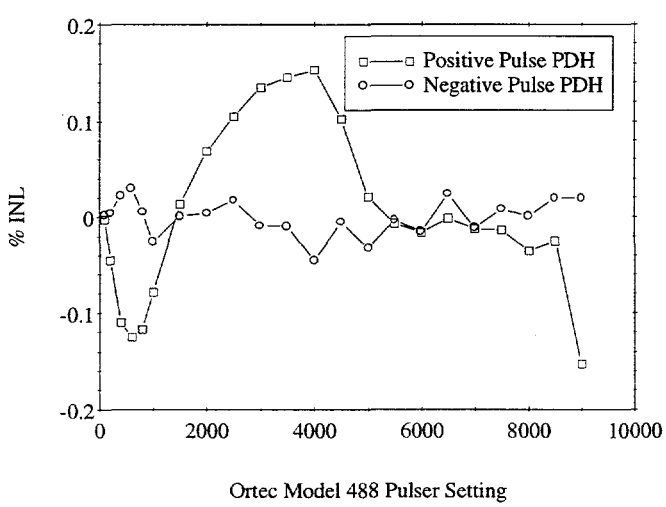

Fig. 5 INL Measurement Results for Positive- and Negative-Pulse PDH Circuits

B. Pedestal

The pedestals were determined for each of the PDH circuits by extrapolation of the measured transfer characteristic shown in Fig. 6. The pedestals were found to be < 5 mV for the positive-pulse channel and < 35 mV for the negative pulse channel.

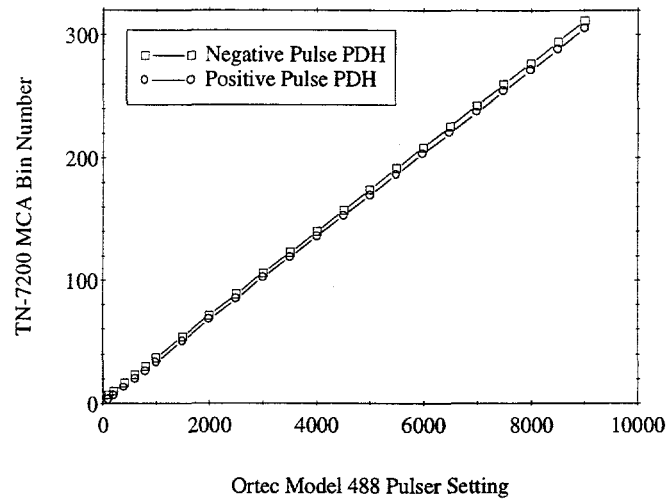

Fig. 6 Extrapolation of Pedestal Values from the Transfer Characteristic Curves

C. Droop Rate

The droop rate was measured over a 6-ms time interval for each of the PDH circuits. The droop was measured to be less than 6.67 µV/µs for both positive- and negative-pulse circuits. As expected, the droop rate was found to be dependent on the pulse amplitude, as demonstrated in Fig. 7.

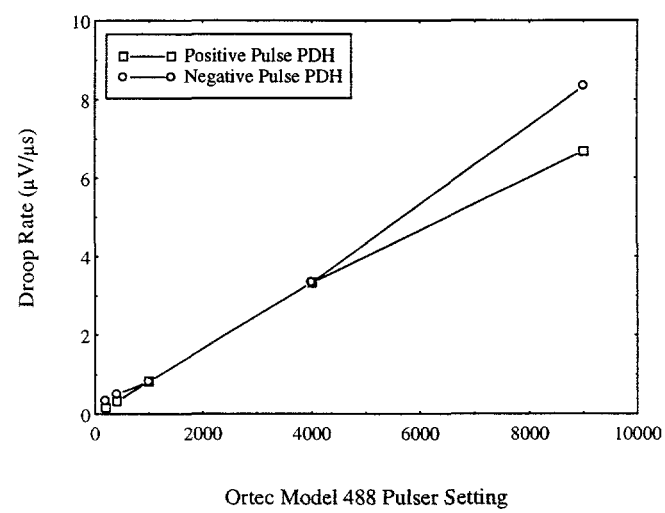

Fig. 7 Droop Rate vs Pulse Amplitude for Negative and Positive PDH Channels

D. Power Measurements

All circuit characterization was performed using a single 5-V supply. The total power dissipation per channel including the PDH circuit, discriminator, and peak detect circuits was 1.2 mw. Excess power was required both in the output stage (Ibias2) and for the closed-loop bias (Ibias1) to compensate for the load capacitance associated with the chip package and test system. Both PSPICE and HSPICE verify that for designs with load capacitance on the order of 0.1 pF, comparable circuit performance can be obtained using less than 200 μw per channel.

V. CONCLUSIONS

A pair of complementary, low-power, monolithic peak detecting track and hold circuits have been fabricated in 1.2-μm CMOS and fully characterized. The designs are optimized to minimize measurement errors associated with droop, pedestal effects, and pulse pileup. Measured data demonstrate that each channel is capable of 100/1 dynamic range with less than ±0.16% INL. Low power, 5-V operation, and CMOS compatibility make this circuit ideal for use in a variety of monolithic data acquisition systems, including spectroscopy applications.

VI. ACKNOWLEDGMENTS

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VII. REFERENCES

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