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THIN-FILM DECOUPLING CAPACITORS FOR MULTI-CHIP MODULES

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Abstract: Thin-film decoupling capacitors based on ferroelectric lead lanthanum zirconate titanate (PLZT) films are being developed for use in advanced packages, such as multi-chip modules. These thin-film decoupling capacitors are intended to replace multi-layer ceramic capacitors for certain applications, since they can be more fully integrated into the packaging architecture. The increased integration that can be achieved should lead to decreased package volume and improved high-speed performance, due to a decrease in interconnect inductance. PLZT films are fabricated by spin coating using metal carboxylate/alkoxide solutions. These films exhibit very high dielectric constants ($\varepsilon \geq 900$), low dielectric losses ($\tan\delta \approx 0.01$), excellent insulation resistances ($\rho > 10^{13}$ Ω-cm at 125°C), and good breakdown field strengths ($E_B \approx 900$ kV/cm). For integrated circuit applications, the PLZT dielectric is less than 1 μm thick, which results in a large capacitance/area (8-9 nF/mm^2). The thin-film geometry and processing conditions also make these capacitors suitable for direct incorporation onto integrated circuits and for packages that require embedded components.

Introduction

High-performance decoupling capacitors are a critical part of integrated circuit systems (ICs) and multi-chip modules (MCMs). As the clock rates for MCMs increase, improvements in signal decoupling will be required since the inductance associated with interconnecting decoupling capacitors and ICs will limit operational frequency. One strategy for improving signal decoupling in high-speed MCMs is to integrate thin-film capacitors into the package, which may involve embedding the capacitors into one of the interconnect layers.[1,2] This approach not only has the potential of minimizing the inductive parasitics, but should also permit a reduction in the size of MCMs. Replacing multi-layer ceramic (MLC) decoupling capacitors with thin-film capacitors that can be fully integrated in ICs and MCMs requires the use of thin films with high dielectric constants.

Lead zirconate titanate (PZT) and lead lanthanum zirconate titanate (PLZT) thin films are good candidate materials for decoupling capacitor applications since these materials have high dielectric permittivities and low dielectric losses up to about 1 GHz.[3,4] In addition to their excellent dielectric properties, PZT and PLZT films are being evaluated for a wide range of applications based on their ferroelectric, piezoelectric, pyroelectric, and electrooptic properties.[5-8] The lead zirconate titanate system ($Pb(Zr_xTi_{1-x})O_3$) is a compositional solid solution with a peak in the dielectric constant of $\varepsilon \approx 1100$-1200 for thin films with a composition of $Pb(Zr_{0.5}Ti_{0.5})O_3$ (i.e., PZT 50/50).[9,10] Higher dielectric constants ($\varepsilon > 5000$) have been attained in ceramic samples for certain PLZT compositions, where La is substituted for Pb.[11] La doping imparts additional benefits, such as suppressing ferroelectric hysteresis and improving the elevated temperature leakage resistance and breakdown strength of PZT films.[12] A high leakage resistance, especially at elevated temperatures, is important since 1) leakage current measurements are often used to monitor the electrical "health" of integrated circuit systems and 2) poor leakage resistance in capacitors tends to be associated with bad aging characteristics and premature device failures.[13]

PZT and PLZT films can be fabricated using a variety of thin-film deposition techniques. One method that has been used extensively is sol-gel processing, since this approach allows for excellent compositional control, which is especially important for multicomponent systems. In addition, solution deposition is a relatively simple, low-cost approach to fabricating thin films that is compatible with standard semiconductor processing techniques, such as spin coating and photolithography. Finally, sol-gel techniques can produce PZT and PLZT films at relatively low firing temperatures (≤ 650°C), which makes their processing compatible with a variety of substrates.

The electrode material and configuration are also important since they primarily determine the parasitic series inductance and resistance of the capacitor. In fact, reducing the parasitic components of MLC capacitors has primarily been achieved by improving the electrodes. The choice of materials for the base electrode of our thin-film capacitors is limited since few metals are chemically compatible with the PZT process. The top electrode is also annealed, but the annealing temperature is lower; this permits consideration of a wider range of top electrode materials. Currently, platinum is used for both electrodes since it is relatively inert to the fabrication process and has a reasonable conductivity ($\rho \approx 10$ μΩ-cm). However, the possibility of incorporating high-conductivity metals, such as copper, is being considered to provide additional design flexibility.

Experimental Procedure

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Materials Fabrication

PZT and PLZT films were prepared by a previously published sol-gel processing method.[14-16] This method uses alkoxide and carboxylate precursors, along with methanol, acetic acid, and water as solvents. The starting solutions are fabricated by first mixing the appropriate ratio

then added, followed by methanol after another 5 minutes. Finally, the lead (IV) acetate and lanthanum acetate, if desired, are added. The solution is then heated to ~ 85°C to dissolve the acetates. Preparation is completed with further additions of methanol, acetic acid, and water, which yields a 0.4 M solution. The solution batches were prepared with 10 mol % excess Pb, as compared to the stoichiometric ABO_3 formula, to compensate for Pb loss due to volatilization during the crystallization anneal.

The PZT or PLZT films are formed by spin coating the solution onto a substrate using a photoresist spinner. Silicon wafers are used as the substrates. The wafers are first prepared with a 400 nm thick SiO_2 diffusion barrier, a thin Ti adhesion layer, and a Pt layer which serves as the base electrode. The Ti and Pt films are sputter deposited. Each PZT or PLZT layer is spin cast at 3000 rpm for 30 seconds. After spin casting, the wafer is heat-treated on a hot plate at ~ 300°C for 5 minutes to pyrolyze organic species in the precursor film. The wafers are fired at 650°C in air for 30 minutes using a 50°C/min ramp rate. This technique yields films that are single-phase perovskite and have columnar microstructures, where the lateral grain size is 100-200 nm. Individual, spin-cast layers are 90-100 nm thick after pyrolysis and crystallization; therefore, a multilayering approach was used to obtain thicker films. The crystallization anneal was done after every three to four layers were deposited and pyrolyzed to avoid film cracking.

To form the parallel-plate capacitor structure, Pt top electrodes are sputter deposited through a shadow mask. A post-deposition anneal of 500°C for 30 minutes is used to improve the adhesion of the top electrode. The PZT film is then photopatterned and etched. For simplicity a circular capacitor pattern is being used; however, this geometry is not a restriction. A schematic diagram of the cross-section of a thin-film decoupling capacitor is shown in Fig. 1. The

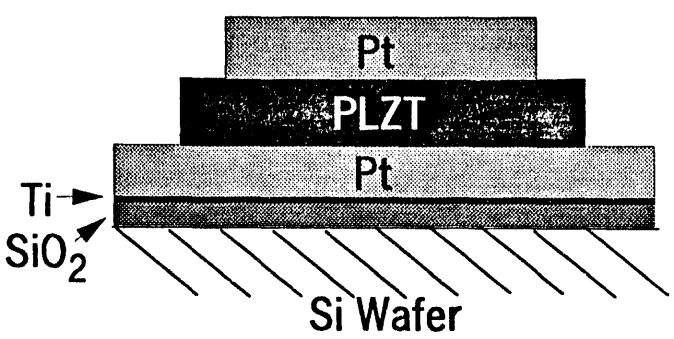

Figure 1. Schematic diagram of capacitor cross section.

dielectric pattern is larger than the top electrode to avoid edge effects. Discrete capacitors are then obtained by dicing the wafer. Both the photopatterning and dicing operations permit great flexibility in specifying the value of the capacitance and the shape and size of the capacitor pieces. Furthermore, since the active part of the capacitor is only a few microns thick, the thickness of the part is primarily determined by the thickness of the starting substrate, which adds additional flexibility in specifying the end product.

Electrical Characterization

Dielectric constant and dielectric loss were characterized using an HP 4194 impedance analyzer. A small oscillation voltage (ΔV = 20 mV p-p) was used to minimize any contributions due to ferroelectric hysteresis. Dielectric properties were measured with and without an applied dc bias. The dielectric properties were evaluated as a function of temperature using a Signatone hot stage.

Leakage resistance was characterized by measuring leakage currents at constant voltage as a function of time using a Keithley source-measurement unit (model 236) connected to a data aquisition system. Monitoring the leakage current as a function of time was important, since a steady-state was attained only after extended testing times (~ 1 hr.).[10,12] The temperature dependence of the leakage resistance was investigated up to 125°C using the Signatone hot stage, which controlled the temperature of the film to ±1°C. For these measurements it was important that the hot stage utilized a dc power supply, which minimized electrical noise, and was contained in a grounded metal enclosure, which provided electrical shielding and a dark test environment.

Dielectric breakdown strengths were determined using a voltage staircase program. In this case, the source-measurement unit was used to increase the applied voltage in 2V increments and to constantly monitor the current as a function of time. In the voltage staircase measurements, dielectric breakdown was indicated by a large (> an order of magnitude) and sudden increase in the measured current. A time interval of 5 minutes between voltage increments was used since this time interval was previously shown to minimize the time dependence of the measured breakdown strength.[10] Dielectric breakdown was verified by optical microscopy, since the resultant breakdown craters were easily observable. For each test condition, 4 to 10 capacitors were used to obtain a statistically significant value for the average breakdown strength.

The impedance response of the capacitors to high-speed switching events was characterized with a fast transient impedance test. For these tests, the capacitors were wire bonded into a transmission line fixture, such that the top electrode of the thin-film was bonded to the stripline and the base electrode was bonded to the ground plane. A fast current transient was simulated by using an HP8082A analog pulse generator (50Ω output impedance) to produce a 10 V step with a 6 ns rise time. This signal was roughly equivalent to a current step of 200 mA (≡ 10V/50Ω), since the voltage drop across the sample was small for short times. The HP 8082A was used since it has a very "clean" output and small reflection coefficient. The voltage drop across the capacitors was measured with a Textronix 602 digital oscilloscope that has a 400 MHZ analog bandwidth.

Results

Since the $(Pb_{1-y}La_y)(Zr_xTi_{1-x})_{1-y/4}O_3$ system comprises a wide compositional space, the initial focus of

this work was to identify a suitable composition for decoupling capacitors. The primary objective of this effort was to optimize both dielectric properties and leakage resistance. Since the dielectric constant for PZT films exhibits a peak near the composition $Pb(Zr_{0.5}Ti_{0.5})O_3$ (PZT 50/50),[9,10] we focused on film compositions with a Zr/Ti ratio of 1. While PZT films, with various Zr/Ti ratios, typically exhibit a high effective leakage resistivity at room temperature (> 10^{13} Ω-cm), their leakage resistance at elevated temperatures (> 100°C) can be orders of magnitude smaller.[10,12,17,18] However, studies using PZT ceramics showed substantial improvements in the elevated temperature leakage resistance through doping with donor impurities, such as La and Nb, which are A-site and B-site donors, respectively.[19]

The effect of La concentration on the steady-state leakage resistance of films (Zr/Ti = 1) is shown in Fig. 2. Leakage current densities (at a given electric field) are plotted, rather than the calculated resistivities, since the current-voltage response is not linear, as discussed later. Figure 2 demonstrates that substituting La for Pb leads to an improvement of nearly three orders of magnitude in the leakage resistance at 125°C, which is roughly the upper temperature limit for device operation. Figure 2 also indicates that leakage resistance improves as the La concentration increases up to at least 5 at. % La. Although the I-V characteristic is non-linear, an effective value for the film resistivity (ρ_{eff} = E/J) can be defined. For the 5 at. %

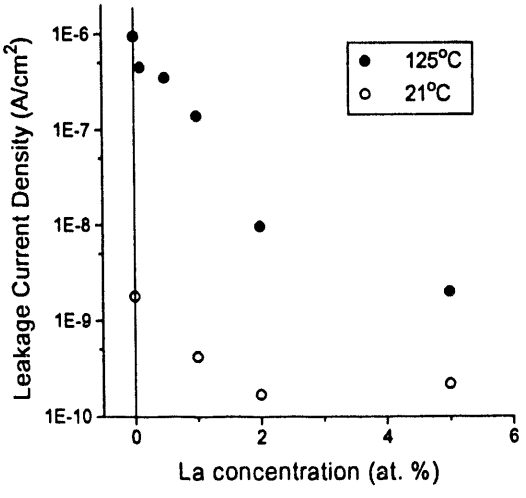

Figure 2. The effect of La doping level on steady-state leakage current density at 21° and 125°C. All the films were approximately 0.8 μm thick and were tested at 5V.

La film at 125°C, ρ_{eff} = 3.5x10^{13} Ω-cm, which is higher than the resistivity of comparable ceramic samples. In addition, Fig. 2 shows that La doping results in some improvement in the room-temperature leakage resistance.

The improvement in leakage resistance due to La additions can be qualitatively accounted for by considering the point defect chemistry. Considering only the major defects, the charge neutrality equation, using Kroger-Vink notation, is given by

$$[La_{Pb}^{\bullet}] + 2[V_O^{\bullet\bullet}] + [h^{\bullet}] = 2[V_{Pb}''] + [A_B'] \quad , \quad (1)$$

where [] denotes concentration, $La_{Pb}^{\bullet}$ is a La^{3+} ion on a Pb^{2+} site, $h^{\bullet}$ is an electron hole, A_B' is an acceptor impurity, such as Fe or Cu, on a B (Ti, Zr) site, and $V_O^{\bullet\bullet}$ and V_{Pb}'' are oxygen and lead vacancies, respectively. Without La additions, Pb loss due to volatility and/or the unintentional incorporation of impurities generates defects that can increase conductivity, since holes and possibly oxygen vacancies are expected to be mobile over the investigated temperature range.[20] However, $La_{Pb}^{\bullet}$ defects can charge compensate the acceptor defects (V_{Pb}'', A_B'), which results in a dramatic decrease in the concentration of the "mobile" defects ($h^{\bullet}$,$V_O^{\bullet\bullet}$) and, therefore, in the leakage current density.

The temperature dependence of the dielectric constant, mesured at 1 kHz, for the PZT 50/50 and the PLZT 5/50/50 (5 at. % La) films is given in Fig. 3. In this case, La doping results in a lower dielectric constant since the PLZT 5/50/50 composition is further from the tetragonal-rhombohedral phase boundary than the PZT 50/50 composition.[11] The dielectric constant of the PLZT film also exhibits a smaller temperature dependence over this temperature range. This result is consistent with the

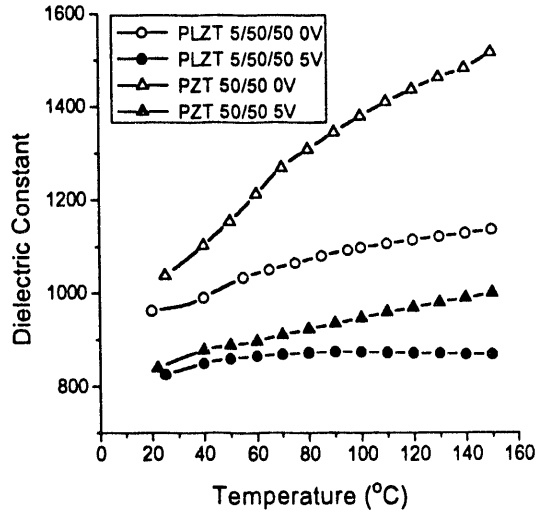

Figure 3. Temperature dependence of the dielectric constant for PZT 50/50 and PLZT 5/50/50 films at 0V and 5V. Both films were roughly 0.9 μm thick.

fact the La doping suppresses ferroelectric hysteresis.[12] In fact, ε at 5V for the PLZT 5/50/50 film shows only a 6% variation from 20°C to 150°C. Furthermore, the dielectric loss for both the PZT 50/50 and the PLZT 5/50/50 films are characterized by tanδ = 0.010-0.015, which remains approximately constant over this same temperature range.

The PLZT 5/50/50 composition yielded films with good dielectric properties and good leakage resistance. We have also demonstrated a significant improvement in the breakdown strength at elevated temperature (> 100°C) due to La substitution.[12] Although other PLZT compositions

may have comparable, or even superior properties, our results indicated that PLZT 5/50/50 was a suitable baseline composition for developing thin-film decoupling capacitors.

After selecting an appropriate composition, the next step was to optimize the dielectric thickness. Although decreasing the thickness increases the capacitance/area (C/A) of the device, it also increases the leakage current density and decreases the breakdown voltage. As exhibited in Fig. 4, the steady-state leakage current is a non-linear function of voltage. The I-V response can be roughly described by a power-law dependence, such that $I \propto V^n$; in this case, $n \approx 2.1$. Due to this non-linear dependence, the improvement in leakage resistance due to an increase in the dielectric thickness can be significantly greater than the resultant loss in C/A ratio. In addition, the capacitor yield increases dramatically with increasing film thickness.

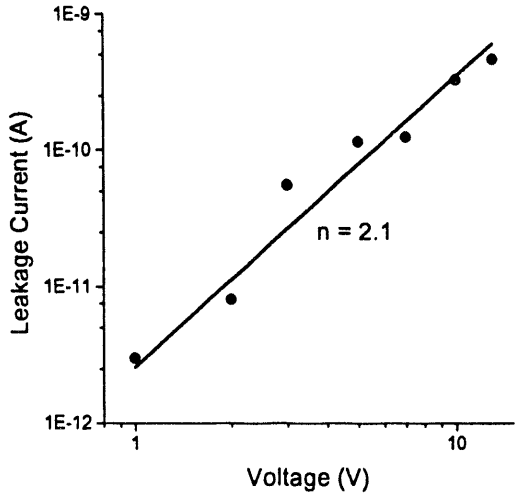

Figure 4. Steady-state leakage current as a function of voltage at 100°C for a PLZT 5/50/50 film (0.9 μm thick). The results were fit to the power-law relationship, $I \propto V^n$. The contact area was 4.91 mm^2.

For 5V decoupling capacitors, a suitable compromise between C/A ratio, leakage resistance, and yield was reached with a film thickness of ≈ 0.8 μm. This thickness leads to C/A(5V) ≈ 8-9 nF/mm^2. Furthermore, the steady-state leakage current of a 50 nF decoupling capacitor with this thickness, based on Fig. 2, would be only about 0.1 nA at 125°C. In addition, the breakdown voltage of PLZT films at this thickness is roughly 65 V (> 800 kV/cm) and is essentially independent of temperature for T ≤ 125°C.

One consequence of using 0.8 μm films is that 8 sol-gel layers are needed, which requires two crystallization anneals at 650°C. While thinner films might simplify the fabrication process and would lead to higher C/A values, they would be used only if the leakage resistance, yield, and capacitor lifetime are acceptable. Given the potential tradeoffs in performance, it may be appropriate to optimize the film thickness for specific applications.

The other critical design issue is optimizing the metallization to minimize the inductance and resistance of the capacitor. By restricting the initial choice of electrode materials to Pt, the only relevant design parameters were the thickness of the metallization and the capacitor geometry. A circular geometry was chosen partly to minimize spreading resistance effects in the electrodes. While increasing the thickness of the Pt electrodes reduces the series resistance, increasing the electrode thickness increases the film stress, which leads to adhesion problems. A compromise between adhesion and high-frequency impedance response was achieved with 1 μm thick electrodes.

Figure 5 compares the fast-transient impedance responses of a PLZT thin-film capacitor to a commercial MLC capacitor with a similar capacitance. The contribution of the stripline fixture and cabling was eliminated by subtracting the response of a short-circuited stripline from the data for each device; consequently, these curves correspond essentially to a zero lead length condition. Clearly, the impedance characteristics of the two devices are comparable on this time scale.

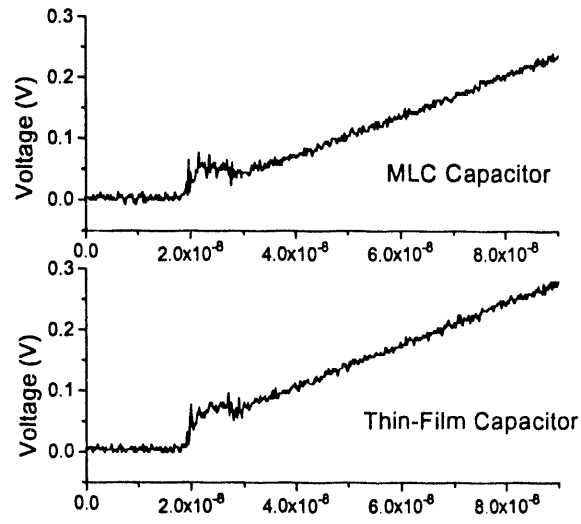

Figure 5. Voltage drop across the test capacitor as a function of time for the fast-risetime, transient impedance measurements. The upper curve is for a commercial multi-layer ceramic capacitor (AVX 05085E683ZA7050, 50V DC) and the lower curve is for the PLZT thin-film device.

The transient impedance response can be analyzed using an equivalent circuit consisting of an inductor, a resistor, and a capacitor in series.[21] The transient responses have been fit to this equivalent circuit using SPICE modeling. The values obtained for the equivalent series inductance (ESL), equivalent series resistance (ESR), and capacitance from the traces in Fig. 5 are given in Table I. Based on the derived values of the circuit elements, thin-film capacitors are suitable replacements for MLC capacitors. Although the MLC capacitor has a slightly smaller ESR value, the thin-film device will achieve a clear advantage if integration permits a substantial reduction in interconnect length.

Table I - Transient Impedance Characteristics

	ESL	ESR	C
Thin-Film	1.5±0.5 nH	250±10 mΩ	58±1 nF
MLC	1.5±0.5 nH	100±10 mΩ	61±1 nF

Discussion

The previous results demonstrate that the properties of PLZT 5/50/50 thin-film capacitors make them suitable for signal decoupling in integrated circuit applications. Based on these results, thin-film decoupling capacitors have been developed for use in prototype multi-chip modules. An array of six decoupling capacitors that have been mounted in an MCM for digital signal processing is shown in the center of Fig. 6. Four other sections with thin-film capacitor arrays are also visible. For each capacitor, the inner circle is the Pt top electrode, the larger ring is the part of the PLZT film that extends beyond the top electrode (see Fig. 1), and the rest of the part is the exposed Pt base electrode. The active area is defined by the 2.5 mm diameter top electrode; this area results in a value of approximately 40 nF at room temperature and 5V. The thickness of the capacitor array piece, which is essentially defined by the substrate thickness, has been matched to the thickness of the

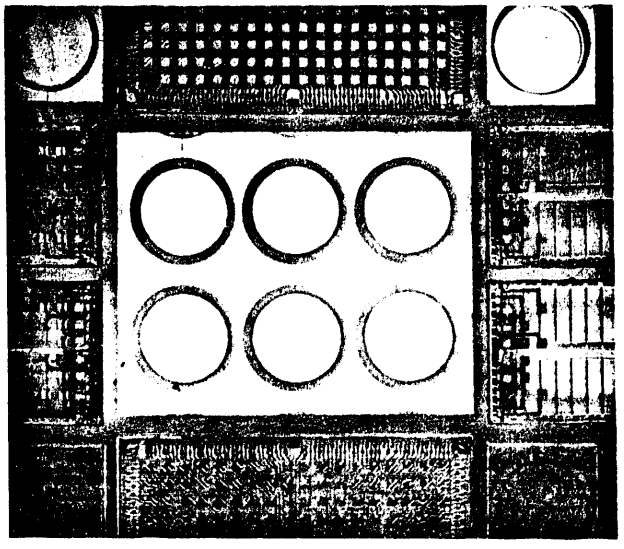

Figure 6. Thin-film capacitor arrays mounted in a multi-chip module. The MCM also contains SRAMs, ASICs, and digital signal processing chips.

surrounding ICs. The size of the decoupling capacitor arrays have also been defined to fill the space between the different sized ICs. The result is a space-filling, planar array of ICs and capacitors that is, therefore, compatible with an overlay interconnect technology. This result could not be achieved using commercial multi-layer ceramic capacitors. In this context, it is also important to note that both electrodes are accessed from the top.

While the ability to fabricate capacitor parts with a specific thickness or area was critical for the MCM shown in Fig. 6, the full potential of a thin-film capacitor technology will only be realized by fully integrating the capacitors into the packaging architecture. One approach, which we are investigating, is to fabricate the thin-film capacitors directly on the surface of a finished package or on one of the interconnect layers of a multi-layer package to produce an embedded component. Because of the relatively high firing temperature (600°-650°C) that is required, this approach is probably only compatible with a multi-layer ceramic (MCM-C) technology. Another approach, also being investigating, is it to develop free-standing, thin-film (< 1 mil thick) capacitors. Such capacitors could be embedded in an interconnect layer of either a deposited (MCM-D) or laminated (MCM-L) architecture. Alternatively, a free-standing, thin-film capacitor could be attached directly to an IC to provide on-chip decoupling. All of these approaches should lead to improved interconnection, with a resulting improvement in high-speed performance, and a reduction in package volume.

The potential benefits associated with utilizing integratable thin-film decoupling capacitors in MCMs are clear. However, additional development and proof testing of these capacitor designs will be required before achieving this integration. Furthermore, the increased manufacturing complexity associated with capacitor integration and the possibility of increased costs suggest that thin-film decoupling capacitors will be primarily put to use in high-end MCMs, where performance is at least as important as the cost per part. This prognosis is not unnecessarily restrictive since high-performance MCMs will benefit the most from employing integrated passive components.

Conclusions

Thin-film decoupling capacitors have been developed using sol-gel derived PLZT 5/50/50 films. The films have a very high permittivity of $\varepsilon \geq 900$ that is essentially constant up to 1 GHz and is roughly independent of temperature over the range 21°-150°C. The films are also characterized by a low dielectric loss, high leakage resistance, and relatively high breakdown strength. The decoupling capacitors have a dielectric thickness of approximately 0.8 μm, which is a compromise between high capacitance/area (8-9 nF/mm^2), low leakage and good reliability. In addition, the transient impedance characteristics of the thin-film devices are comparable to commercial MLC capacitors. Consequently, the thin-film capacitors appear to be suitable replacements for MLC capacitors. However, the ultimate benefit of a thin-film capacitor technology is to be able to integrate the passive components into the packaging architecture. This increased integration should improve the high-speed performance of MCMs and permit volume reductions, but this type of integration will require further development.

Acknowledgement

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