Implementation of an EPICS IOC on an Embedded Soft Core Processor Using Field Programmable Gate Arrays *

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Abstract

At Jefferson Lab, we have been evaluating soft core processors running an EPICS IOC over µClinux on our custom hardware. A soft core processor is a flexible CPU architecture that is configured in the FPGA as opposed to a hard core processor which is fixed in silicon. Combined with an on-board Ethernet port, the technology incorporates the IOC and digital control hardware within a single FPGA. By eliminating the general purpose computer IOC, the designer is no longer tied to a specific platform, e.g. PC, VME, or VXI, to serve as the intermediary between the high level controls and the field hardware. This paper will discuss the design and development process as well as specific applications for JLab's next generation low-level RF controls and Machine Protection Systems.

Introduction

At present, to be accessible to the accelerator's distributed control system, our field hardware must be designed to operate with a VME or VXI based single board computer Input/Output controller (IOC). Frequently, this requires long cable pulls and in some cases a new VME crate installation. During the initial design cycle, typically we must choose between the VME platform, serial communication, or blind stand-alone units. Stand-alone units provide no feedback to the control room and there is no convenient way to verify that the devices are functioning correctly. Serial devices are severely band limited and require expensive serial interface equipment when the standard IOC ports have been fully utilized. The VME based systems are expensive and often do not accommodate available space constraints. The ability to integrate the IOC directly into our custom hardware provides enormous flexibility and provides significant enhancements to our operating capabilities.

Field Programmable Gate Arrays (FPGAs) are very attractive for implementing digital designs. They have high component counts and are relatively low cost. Their highly configurable platform provides enormous design flexibility, allowing changes to take place during the development process and even well after the board design has been completed. Typically modern digital designs are generated and simulated using a standardized hardware description language such as VHDL or Verilog, synthesized, and then routed for a particular device.

Generally, embedded systems follow the master/slave approach to integrating system designs. However, with the advent of soft core processors, an FGPA can host the application logic and the processor core running a fully featured operating system within a single package. Embedding the processor core within the logic fabric offers tighter integration with the application design logic and greater flexibility in the overall system architecture, and, in many cases, it is expected to have higher performance by avoiding master-slave communication bottlenecks [1].

Occasionally our equipment must be installed and operated in radiation environments in order to support end-station experiments and accelerator operations. Therefore it is reasonable to expect single event upsets (SEUs) in the configuration memory of the FPGA [2]. Modern FPGA families include the ability to perform CRC checks on the configuration memory while the device is in operation [3]. The device can be set up to reconfigure itself after the detection of a soft error if desired. Reconfiguration times are fairly quick on the order of a few milliseconds. It should be noted that device operation is unavailable during this period of time. However, the overall benefit provides significant advantages over manually resetting the device especially when it is located in a controlled environment.

Soft Core Processors

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