19980330 092

ORNL/CP-94465

CONF-9509265--

A Radiation-Hard Analog Memory In The AVLSI-RA Process

C. L. Britton, Jr., A. L. Wintenberg, and K. F. Read, M. L. Simpson, G. R. Young
Oak Ridge National Laboratory

L. G. Clonts, E. J. Kennedy, R. S. Smith, B. K. Swann
The University of Tennessee

J. A. Musser
Physics Department, Indiana University

RECEIVED
OCT 08 1997
OSTI

Abstract

A radiation hardened analog memory for an Interpolating Pad Camber has been designed at Oak Ridge National Laboratory and fabricated by Harris Semiconductor in the AVLSI-RA CMOS process. The goal was to develop a rad-hard analog pipeline that would deliver approximately 9-bit performance, a readout settling time of 500ns following read enable, an input and output dynamic range of +/-2.25V, a corrected rms pedestal of approximately 5mV or less, and a power dissipation of less than 10mW/channel. The pre- and post-radiation measurements to 5MRad are presented.

I. Introduction

Deadtimeless, pipelined, radiation resistant readout is required for use in experiments at the LHC. The requirements of high speed, low noise, low power, and radiation resistance present important challenges to be addressed. The requirements for the GEM Central Tracker Interpolating Pad Chamber (IPC) included not only high resolution (50mm in r/f), but also radiation hardness of up to 2.5MRad[1]. The pads in the IPC connected to preamplifiers which utilized a peaking time of approximately 30ns. The signal was stored in a switched capacitor analog memory unit (AMU) every 16ns. After receipt of a trigger, the pads were read in groups of three consecutive samples. This allowed the peak of the signal to be approximated from multiple samples of the preamplifier output and allows the peaking time of the preamplifier to be longer than the actual sampling time of 16ns. The output of the SCA went to a 16-1 multiplexer which was in turn connected to an 8-bit flash ADC (FADC).

The analog pipeline designed at Oak Ridge National Laboratory and fabricated by Harris Semiconductor in the AVLSI-RA process consists of storage cells, readout amplifiers, and control logic. The goal was to develop a rad-hard analog pipeline that would deliver approximately 9-bit performance, a readout settling time of approximately 500ns after receipt of a read enable, an input and output dynamic range of +/- 2.25V, an rms pedestal variation of approximately 5mV or less, and a power dissipation of no more than 10mW/channel. In order to gain an understanding of the process and obtain a useful prototype circuit, the pipeline was implemented in two functionally identical but spatially different topologies. Both types of pipeline were fully functional on first silicon and differed only in the logic interconnect. Each memory ("D" chip for the "digitated" layout and "S" chip for the "sectioned" layout) are 8-channel pipelines that are 128 cells (approximately 2.05ms) deep and contains 4 channels of voltage-write-voltage-read (VWVR) topology and 4 channels of voltage-write-charge-read topology (VWCR). Alternative topologies were prototyped to gain insight into their characteristics in case one did not prove satisfactory for a radiation environment. Also fabricated were a test structures chip, and a preamplifier for the IPC, with the preamplifier being designed at Brookhaven National Laboratory.

This paper will discuss the design requirements of the memory and its associated components (storage cell, readout amplifiers, logic, etc.). In particular, the bandwidth and noise requirements of the opamps and the memory cells are described in addition to drive-related requirements of the logic and layout. Some pre-and post-radiation measurements have been presented[2], but this paper will present some measurements not previously published. The measurements were performed at 47.5MHz and 10MHz writing rates and show that the memories have corrected pedestals of less than 4mV rms, integral linearity of less than +/- 0.5%, and readout settling time of approximately 500ns. The power dissipation was approximately 8mW. Ionizing radiation of up to 5MRad was found to have little effect on the basic function of the chips. The pipeline was intended for simultaneous read-write operation as the trigger latency was to be up to 40ms. However, testing for this paper was limited to stop-and-read as the project ended too soon for a true deadtimeless readout controller to be completed. The read and write controllers in the memories are completely independent of each other.

[1] Research sponsored by the U. S. Department of Energy and performed at Oak Ridge National Laboratory, managed by Martin Marietta Energy Systems, Inc., for the U. S. Department of Energy under contract DE-AC05-84OR21400.

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

MASTER

DTIC QUALITY INSPECTED 3

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, make any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

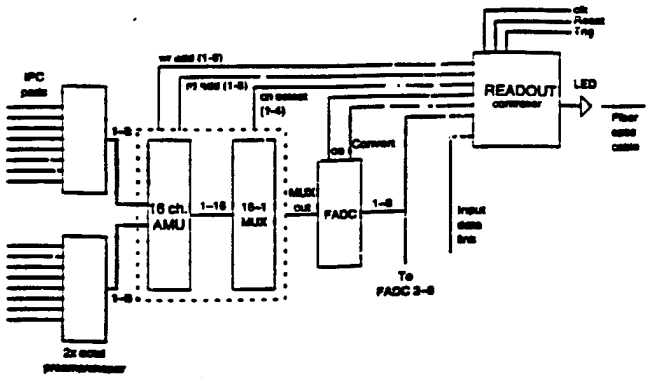

Fig. 1 Proposed Interpolating Pad Chamber (IPC) Electronics Architecture

II. MEMORY REQUIREMENTS

1. Linearity

It was determined from the basic detector resolution requirements that the integral non-linearity (INL) required for the analog memory be on order of 0.5% or better over a range of 0.5V to 4.5V for the semi-Gaussian pulse output from the pad preamplifier. This was due primarily to the inherent measurement accuracy of the IPC concept being approximately 1%[1].

2. Readout

The settling time of the output readout amplifier represents the largest factor in obtaining a minimal readout time. It was desired to achieve a 9-bit settling time of approximately 500ns for a 10pF load capacitance, while maintaining an amplifier power dissipation of less than 6mW. The IPC detector required approximately 400,000 channels of preamplifier, AMU, and MUX channel. One FADC would be shared by 16 AMU channels through the MUX. With the required linearity, it was decided that the power budget for the AMU would be 10mW/channel, maximum. This would result in approximately 4kW power dissipated due to the memories for the entire detector.

3. Addressing

The decision was made to allow all control for the preamplifier and the memory to be handled by a state machine controller on a separate chip. Since the pipeline was to be 128 cells deep, a seven-bit decoder was required. In order to ease the requirements of having cell enable logic able to settle every 16ns due to the beam crossing clock of the SSC, it was decided to configure the decoders as two separate six-bit decoders, each controlling 64 cells in a pipe. A block diagram of the memories is presented in Fig. 2

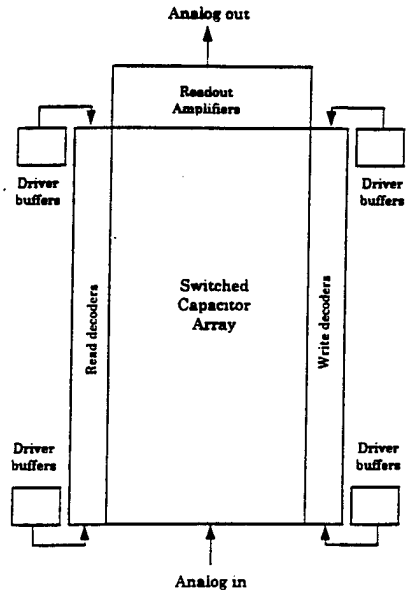

Fig. 2. BlockDiagram

II. MEMORY DEVELOPMENT

1. Topologies

a. Voltage-read The Harris Semiconductor AVLSI-RA process was chosen for this development for two reasons. First, the process had high-density capacitors as part of the standard processing steps. Second, ORNL had developed a good working relationship with Harris during a prior development that utilized the VHF bipolar process[3, 4]. The availability of two-plate discrete capacitors, allowed for the pursuit of some level of development in voltage-write voltage-read (VWVR) memory. This topology, shown in Fig. 3, has been widely used[5, 6] and has the advantage of reading a voltage and writing a voltage so that, to a first order, there is no component-dependent conversion-gain to introduce uncertainty in the measurement. Additionally the switching action reduces common-mode noise effects.

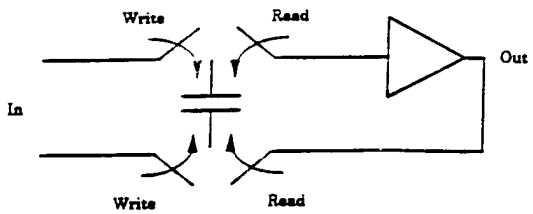

Fig. 3, VWVR

b. Charge-read In contrast to the VWVR topology, the voltage-write-charge-read (VWCR shown in Fig. 4) topology output risetime depends not only on the values of the bus and

sample capacitors, but also on the ratio of the sum of these to the value of the feedback capacitor. To achieve a unity gain inverting memory, the feedback capacitor must equal the sample capacitor.

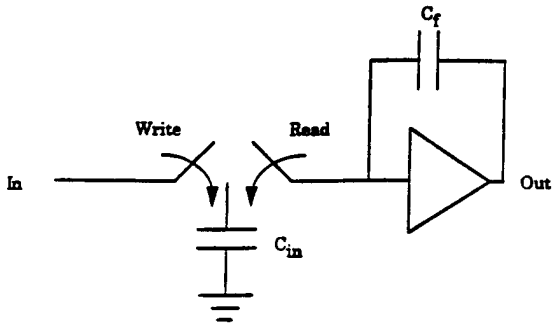

Fig. 4 VWCR

c. Digitated vs. Sectioned With an internal array length of approximately 4mm, two address topologies were implemented to test the effects of driving long enable lines. In the sectioned, or S-chip, one 6-bit decoder drives the upper 64 cells and one drives the lower 64 cells. In the digitated, or D-chip, the decoders are like the S-chip except one decoder addresses every other cell (odd cells) while the other decoder addresses the remaining cells (even cells). For the purpose of radiation testing of off-resistance, both the VWVR and the VWCR cells had two different gate lengths.

2. *Capacitor Size*

Because the resistance of the sampling switch is non-linear, it can be shown[7] that

$$\tau_{effective} \approx [\max R(v_{in})] \cdot C_{sample} \qquad (1)$$

where $t_{effective}$ is the effective time constant of the switch-capacitor combination, $R(n_{in})$ is the peak resistance of the switch within the operating range, and C_{sample} is the sample capacitor value. With this relationship, the transistor switch peak resistance and the capacitor size can be determined for a given sampling precision. The chosen capacitor size was 1pF.

3. *Readout Amplifiers*

The readout amplifier topologies were chosen for drive capability. In general, single pole amplifiers give the best settling time. However, the expected load capacitances of 5-15pF did not allow for a single-pole design that was relatively independent of load capacitance. Two topologies whose schematics are presented in Figs. 5 and 6, were fabricated in the memory. The first, IPC5C, was a modification of the standard two-stage CMOS amplifier.

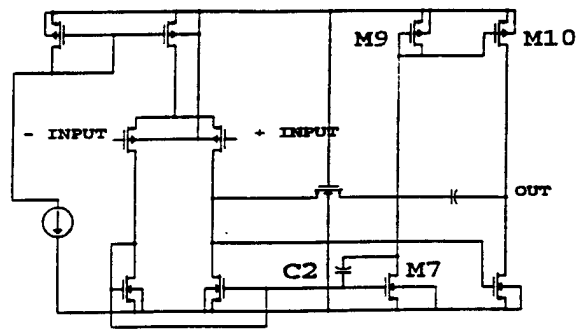

Fig. 5 IPC5C Schematic

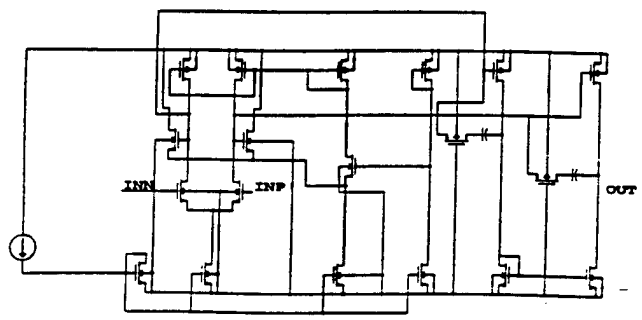

Fig. 6 IPC4B Schematic

It is similar to that found in many textbooks[8] except that the drive was extended to be push-pull. The feedforward path generated by transistors M7, M9, and M10 was compensated by C2 to improve the phase margin[7, 8]. The remaining topology, IPC4B, was similar to one previously published[9] except that it was optimized for improved settling at faster risetimes[7]. Both of these designs provide linear outputs to within approximately 0.2V of the supply rails.

The pipeline-amplifier combinations for both digitated and sectioned chips are presented in Table 1. The final die sizes were 5.05mm x 5.9mm and were packaged in 68-pin ceramic packages.

Table 1. Analog memory pipeline components

PIPELINE	MEMORY TYPE	AMPLIFIER	SWITCH LENGTH
0	VWVR	IPC4B	short
1	"	"	long
2	"	IPC5C	short
3	"	"	long
4	VWCR	IPC4B	short
5	"	"	long
6	"	IPC5C	short
7	"	"	long

IV. EXPERIMENTAL RESULTS

To evaluate the suitability of both the process and candidate topologies for use in the central tracker, a set of tests was designed. Although these tests were by no means exhaustive, over 70Mbytes of data was generated. Six packaged die from three wafers were irradiated at approximately 82kRad/hr. to 1MRad and 5MRad total dose. Utilizing both binary addressing and Gray-code addressing, measurements were taken at 0-, 1-, and 5MRad intervals. The writing rate of 47.5MHz was selected based on the maximum speed of the pattern generator for a 190MHz external clock. During radiation exposure the chips were powered but not operating. The test setup is shown in Fig. 7. Channels 0-3 are VWVR, while channels 4-7 are VWCR. A summary of some of the test results are as follows:

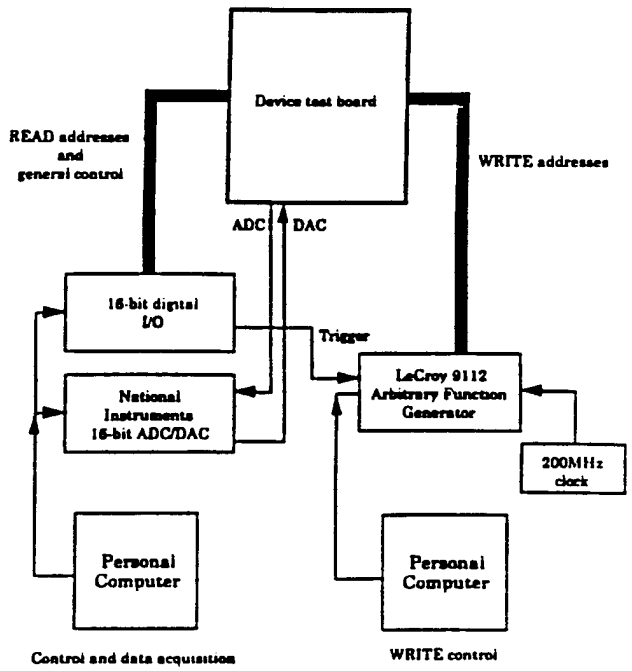

Fig. 7 Block diagram of test system

1. Readout Amplifier Measurements

The prerad IPC4B mean offset voltage was -1.4mV with a s of 1.8mV and the IPC5C mean was 0.2mV with a s of +2.1mV. The worst case change at 5MRad was 5mV with the average change being approximately 3mV. The pre-rad measured dc gain of the IPC4B was approximately 10K and the IPC5C was approximately 12.5K. A summary of the dynamic behavior of the amplifiers is presented in Table 2. From the table the IPC5C amplifier appears to have the fastest and most radiation resistant response of the two designs.

Table 2. Measured slew-rates and risetimes for the IPC4B and IPC5C amplifiers.

	IPC4B0 MRad	IPC4B 1MRad	IPC4B 5MRad	IPC5C 0MRad	IPC5C 1MRad	IPC5C 5MRad
+Slew (V/ms)	15.3	15.3	15.7	17.3	17	16.9
-Slew (V/ms)	15.6	15.7	16.7	16.8	17	16
VWVR $+t_r$ (ns)	157	166	185	132	134	134
VWVR $-t_r$ (ns)	183	188	205	145	142	145
VWCR $+t_r$ (ns)	192	209	225	187	187	184
VWCR $-t_r$ (ns)	193	218	242	186	190	187

2. AC INL

The 5MRad INL for a 50ns semi-Gaussian pulse similar to that from a real preamplifier is presented in Fig. 8. There was little change between 0- and 5MRad.

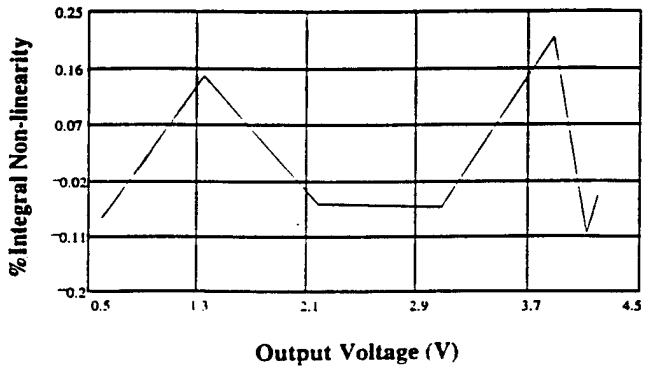

Fig. 8 Chip S4A, pipe 4 even cell 6, 5MRad

3. Droop Rate

To obtain a measure of droop in the analog memories, cell voltages were written and then measured after 0.5s and 1s delays. The cells exhibited a droop of much less than 1V/s at pre-rad and after 5MRad. These results are much better than needed for a trigger latency in the few tens of microseconds.

4. Pre- and Post-correction Pedestals

For the detector pedestal correction a correction method was chosen which stored a "pedestal table" in off-line computer memory. This table was generated by reading each

cell many times and obtaining an average value characteristic of each cell in the memory. To remove the systematic error on a cell-by-cell basis and leave only random variations, the raw event data for a given cell was then subtracted from the desired cell table value. The pre- and post-correction pedestals of chip D4A are presented for 47.5MHz clock rate, even addresses in Fig. 9. The data consists of pre-correction cell values for 1.5V input subtracted from the pedestal tables for 1.5V, 2.5V, and 3.5V inputs. The pedestal table for 1.5V is the desired operating voltage for the system because this represents the quiescent output of the preceding preamplifier-shaper. The remaining input voltages were included to study correlation of pedestal vs. voltage. As can be seen, the voltage-read channels have much better correlation than the charge-read channels and were adequate for the tracker. The data presented are for binary addressing. Although the pre-correction patterns were different for binary and Gray, both exhibited approximately the same post-correction behavior.

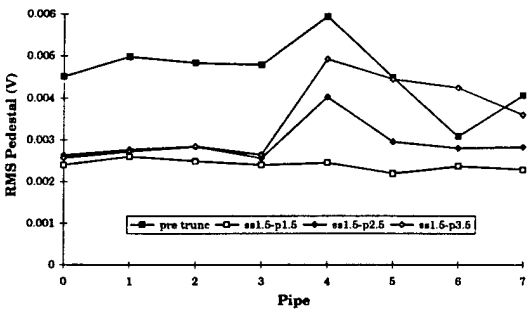

Fig. 9. D4A, 5MRad, Even, 1.5 Volt Input, 47.5MHz Binary Write

5. Nearest-neighbor channel interaction

The purpose of this test was to investigate the interaction of one channel on its neighbors. Each channel was written 1.5V, 2.5V, and 3.5V while all other channels remained at 2.5V. The voltage-read channels showed no systematic effect while the charge-read neighboring channels exhibited a deviation of approximately 4mV for a 2V span of channel 5. This was thought to be due to the large error signal at the input of the readout amplifier when the sampling capacitor is connected for readout. Under these conditions the input reference line is disturbed in adjacent channels. Individual amplifier reference lines might solve this but would represent a cumbersome layout.

V. Conclusions

Testing indicates that the process appears to be very resistant to radiation damage. Both operational amplifiers worked well but the simplicity of the IPC5C would make it the amplifier of choice. The 9-bit settling time of the IPC5C was approximately 500ns for the VWVR topology and 560ns for the VWCR topology. Both exhibited only minor change after radiation. The measured power dissipation (pre- and post-rad) was approximately 8mW/channel for a clock rate of 47.5MHz. The voltage read exhibited a better overall linearity and consistency, particular for pedestal correction. The even-odd effects of cell addressing would indicate that the digitated layout is preferable to the sectioned. The uncorrected pedestal is somewhat higher than expected because of measurements made on a similar but smaller ORNL memory in a soft process. Some consultation with the manufacturer would be in order to resolve these differences.

VI. Acknowledgments

The authors would like to thank Tim Johnson, John Fakiris, and Nick VanVonno of Harris Semiconductor for their involvement, Dan Marlow and Bob Wixted of Princeton University, Bill Sippach of Nevis Laboratories, and Paul O'Connor of BNL for many hours of helpful discussions.

VII. References

[1] GEM Technical Design Report, GEM-TN-93-262, July 31, 1993

[2] Ibid, p. 7-3.

[3] C. L. Britton, Jr., E. J. Kennedy, R. A. Todd, A. L. Wintenberg, and G. R. Young, " A Four-Channel Bipolar Preamplifier for RHIC Dimuon Pad Readout", IEEE Trans. Nucl. Sci., Vol. 39, No. 5, Oct. 1992 (1302-1306).

[4] R. A. Todd, et al, "Monolithic Systems Design for the Silicon Electromagnetic Calorimetry Collaboration", 1993 NSS Conference Record, pp. 592-596.

[5] S. A. Kleinfelder, "A 4096 Cell Switched Capacitor Analog Waveform Storage Integrated Circuit", *IEEE Trans. Nucl. Sci.*, Vol. 37, No. 3, 1230-1236, June, 1990.

[6] A. L. Wintenberg, T. C. Awes, C. L. Britton, L. G. Clonts, M. S. Emery, M. N. Ericson, F. Plasil, M. L. Simpson, J. Walker, and G. R. Young, "Monolithic Circuits for the WA98 Lead Glass Calorimeter", to be presented this symposium.

[7] C. L. Britton, Jr., "Studies on Analog Memories for Physics Experiments with Design Towards Radiation Hardening", Ph. D. Dissertation, The University of Tennessee, Knoxville, May, 1995.

[8] P. E. Allen, and D. R. Holberg, CMOS Analog Circuit Design, Jolt, Rinehart, and Winston, 1987.

[9] J. N. Babanezhad, "A Rail-to Rail CMOS Op Amp", IEEE Jour. Solid State Circuits, Vol. 23, No. 6, December, 1988, pp. 1414-1417.

M98000322

Report Number (14) ORNL/CP--94465
CONF-9509265--

Publ. Date (11) 199509
Sponsor Code (18) DOE/ER, XF
UC Category (19) UC-400, DOE/ER

DOE