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CAPATTERY DOUBLE LAYER CAPACITOR LIFE PERFORMANCE

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ABSTRACT

Double layer capacitors (DLCs) have received increased use in computer memory backup applications for consumer products during the past ten years. Their extraordinarily high capacitance density along with their maintenance-free operation makes them particularly suited for these products. These same features also make DLCs very attractive in military type applications. Unfortunately, lifetime performance data has not been reported in the literature for any DLC component.

Our objective in this study was to investigate the effects that voltage and temperature have on the properties and performance of single and series-connected DLCs as a function of time.

Evans model RE110474, 0.47-farad, 11.0-volt Capatteries were evaluated. These components have a tantalum package, use welded construction, and contain a glass-to-metal seal, all incorporated to circumvent the typical DLC failure modes of electrolyte loss and container corrosion.

A five-level, two-factor "Central Composite Design" was used in the study. Single and series-connected Capatteries rated at 85°C, 11.0-volts operation were subjected to test temperatures between 25 and 95°C, and voltages between 0 and 12.9 volts (9 test conditions). Measured responses included capacitance, equivalent series resistance, and discharge time. Data were analyzed using a regression analysis to obtain response functions relating DLC properties to their voltage, temperature, and test time history. These results are described and should aid system and component engineers in using DLCs in critical applications.

INTRODUCTION

Double layer capacitors (DLCs) have features that make them very attractive energy storage devices. Their high cycle-life and charge/discharge characteristics resemble conventional capacitor behavior. However, DLCs typically have over 100 times higher energy density. Thus, they are finding widespread use as bridge power sources in CMOS memory backup applications for consumer products. In contrast with most secondary batteries that are now used for memory backup, DLCs need no maintenance, are inherently safe, require a much simpler charging circuit, and do not present disposal problems. These same features make DLCs attractive for military applications.

Until recently, DLCs have been used only in non-critical applications. In part, this has been due to their crimp-seal case, which does not effectively guard against electrolyte loss over time, particularly at higher temperatures. Also, this type seal, as well as the construction materials commonly used in the package, do not provide adequate protection in high humidity environments.

The Evans Capattery double layer capacitor is designed to circumvent these limitations. It has a tantalum package, uses welded construction, and contains a glass-to-metal seal to prevent the typical DLC failure modes of electrolyte loss and package corrosion. Unfortunately, reliability and lifetime property/performance information, like that found in MIL-HDBK-217, has not been published for the Capattery or for any other DLC.

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MASTER

DLC properties versus time are usually reported in product literature at maximum rated temperature and voltage conditions. But such aging data is not adequate for optimal design purposes, particularly when the component will be used at lower temperature and/or with derated voltage. This situation greatly impedes effective use of the important DLC technology in critical military applications.

The objective of this work was to determine the effects that voltage and temperature have on the lifetime properties and performance of Capattery DLCs. Single devices and series-connected systems were evaluated in this joint study. Our goal was to obtain and develop the information needed for optimal use of the Capattery throughout its rated voltage/ temperature range, thus allowing DLC technology to be used effectively in critical applications.

DLC COMPONENTS/SYSTEMS

The design and construction of the Evans Capattery double layer capacitor used in this study has been previously described (1). The capattery was a model RE110474, having a nominal capacitance value of 0.47 farad, with an 11.0-volt rating, and a specified operating temperature between -55 and 85°C. A previous study showed essentially normal behavior under stress conditions of 95°C-11.0 volts and 85°C-13.75 volts (2). At the maximum rated voltage and temperature conditions, Capattery properties have been measured past 10,000 hours in an extended life test (Figures 1 and 2). Over this test period, capacitance values show a 25% decrease while the equivalent series resistance (ESR) is stable to within 10%. This life data was the starting point for the present aging study aimed at learning the effects that both voltage and temperature, individually and together, have on device properties and performance.

Figure 1
Capacitance vs Time of Capattery under 11.0 Volts, 85C Test Conditions

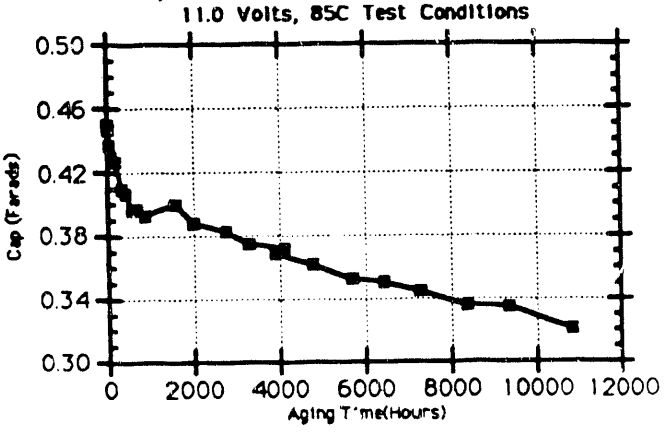
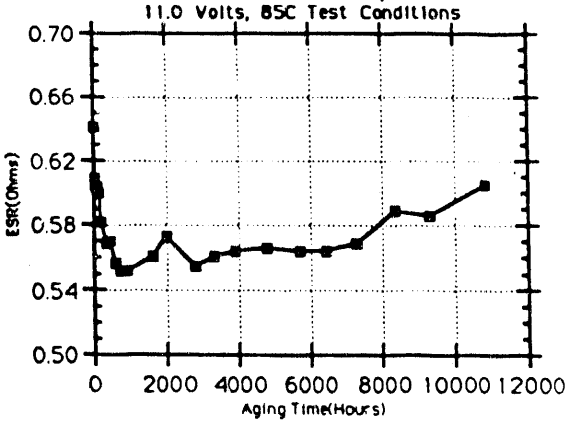


Figure 2
ESR vs Time of Capattery under 11.0 Volts, 85C Test Conditions



Single and series-connected capacitor systems were used in the study. The systems were comprised of three capacitors held in an aluminum package that was filled with urethane foam. No voltage balancing means were employed. The reason for studying the systems was to gain property and performance information for a particular 34-volts application that was of interest to Sandia. Results from the single component and system tests could then be compared to identify any changes brought about by packaging and by the series stacking.

EXPERIMENTAL DESIGN

For expensive components and/or test methods and in situations where extensive time is required for the testing, it is costly to run trials at every possible combination of parameter space. In such cases, it is cost effective to utilize experimental designs that systematically take samples from the test space to deliver the desired information.

In the past ten years, through the efforts of Taguchi, the field of engineering has shown considerable interest in the use of experimental design techniques adapted to what has become known as "Robust Design" (3). With this methodology, the goal is to find the design set points that can withstand manufacturing-tolerance-induced variation as well as field-use variation and still have a product that performs to the targeted application requirements.

In this DLC aging study, we have concentrated on the field use-induced variations of voltage and temperature. Manufacturing variation has been consciously left out of the study. The DLCs were selected for uniformity before the testing began.

Earlier aging tests showed that Capatteries experience the greatest property changes when maintained at elevated temperatures. Thus, the sample test space of this study was restricted to temperatures of 25°C and above. Table 1 lists the voltage-temperature sample test space investigated in this study, which was 0 to 12.9 volts and 25 to 95°C. The voltages shown are single capacitor values--voltages three times these values are used for the series-connected system.

TABLE 1

Sample Space Investigated in this Study

VOLTAGE (V)	TEST TEMPERATURE (C) 25	35	60	85	95
0	--	--	XX	--	--
1.9	--	XX	--	XX	--
6.4	XX	--	XX	--	XX
11.0	--	XX	--	XX	--
12.9	--	--	XX	--	--

XX = Test Point

With five levels for each of the two factors, the total number of combinations amounts to twenty five, as shown in Table 1. The statistical experimental design structure that samples from this space is called the Central Composite Design (CCD) (4). The nine positions marked "XX" in the Table are the test points selected for this DLC study. By using the methods of regression analysis based on least squares curve fitting principles, the "missing" data points may be estimated under the assumption of continuous functional relationships. As mentioned in the previous section, Capatteries exhibit normal aging behavior at the temperature and voltage extremes of this design, therefore the assumption appears valid.

The CCD provides the basis for empirical models that relate capacitor properties and performance (capacitance, ESR, and discharge time) to the field use conditions (temperature and voltage). It also permits the investigation to be accomplished with the least expenditure of resources.

EXPERIMENTAL PROCEDURE

Properties were measured at 25°C on single DLCs and DLC systems at periodic intervals during the study. Measurements included capacitance and ESR per methods described in DOD-C-29501. All capacitance measurements were made using a 100-ohm series resistor. Devices had an average capacitance of 0.46 ± 0.01 farad, and an ESR of 0.56 ± 0.02 ohms. Measurement gage error for the capacitors studied, which were all from the same production lot, was essentially equal to the capacitance standard deviation (0.01 farad), and one-third the ESR standard deviation (0.006 ohms).

Discharge time performance was also measured. For the system, this involved charging it to 34 volts for 60 seconds, then measuring the time required to reach 17.5 volts when discharged by a 7- watt load. These measurements were made using a tester designed and built by Sandia.

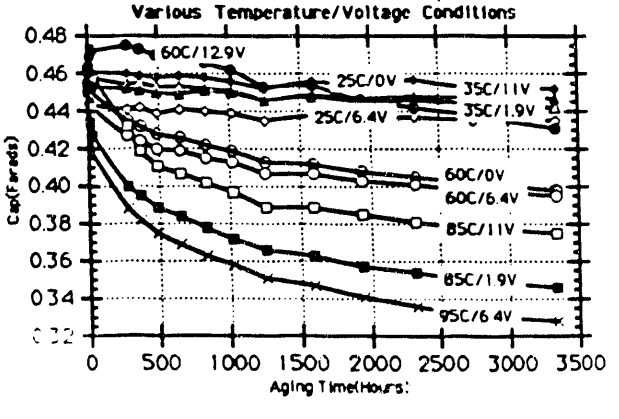
Discharge times were measured for single capacitors by charging them to 11.3 volts for 60 seconds, then measuring the time to reach 5.8 volts under a constant 300-milliamp discharge load. A storage oscilloscope was used for the time measurements. Although not equivalent, the single-component test approximates the actual constant-power discharge conditions. As of this writing, single component tests extend to 3336 hours (15 measurements) and system tests to 1314 hours (9 measurements).

Because all of the capacitors were from one production lot, a single capacitor or system is assumed to be sufficient at each test point to accomplish the goal of this investigation. However, for a related time-to-failure study, three capacitors were used at each of the single-capacitor study points. One series-connected assembly was used at each point for the system study.

RESULTS AND ANALYSIS

Figure 3 shows the average capacitance of three single DLCs versus time at each of

Figure 3
Capacitance vs Time of Capattery under Various Temperature/Voltage Conditions



the nine temperature/voltage test points. Some of the measured responses exhibit rather stable behavior, while others show a rapid decline followed by a more gradual capacitance decrease. At 3000 hours, the largest change is seen at the higher temperatures. High voltage at a given temperature does not, in all cases, produce more capacitance loss, as seen for the 60°C test points.

ESR data for the single capacitors are shown in Figure 4. Again, the values are averages of the three components at each test point. As shown, after an initial decrease of varying size in the first 500 hours, a slight decrease is exhibited during the first three thousand test hours for all conditions except the 60°C, 12.9 volts test point. This condition produced a monotonic ESR increase. In general, higher temperature leads to lower absolute ESR values, at least out to 3300 hours.

Figure 4
ESR vs Time of Capattery under Various Temperature/Voltage Conditions

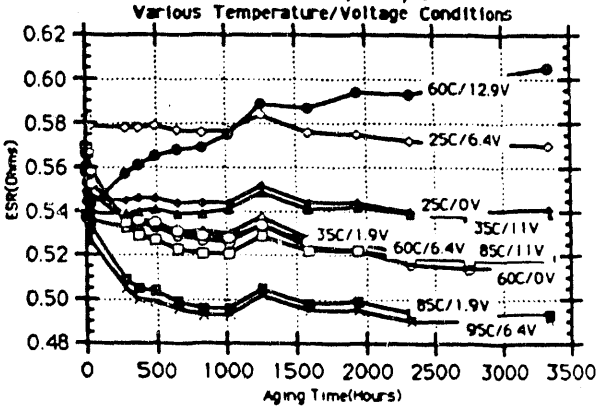
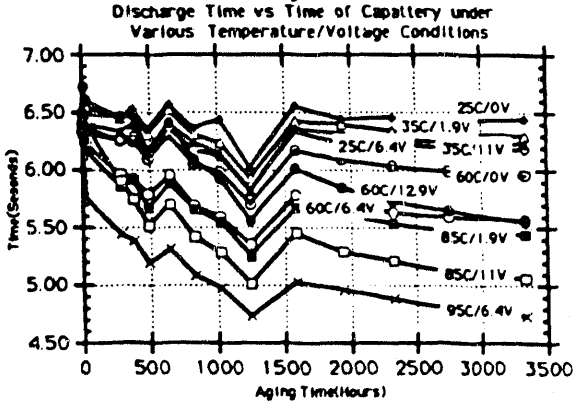


Figure 5 shows the average discharge time versus aging time for the single capacitors at each of the nine test conditions. High temperature along with high voltage leads to the largest change in discharge time. Essentially no change is seen out to 3000 hours for the 25 and 35°C test conditions, while the 95°C, 6.4 volts condition shows a 25% capacitance decrease. The "blips" seen in the data at times less than 1600 hours are attributable to instrumentation difficulties.

Figure 5
Discharge Time vs Time of Capattery under Various Temperature/Voltage Conditions



This rather complicated and somewhat unexpected interplay of voltage and temperature on DLC responses was analyzed using least squares regression methods. For the single capacitors and the series-connected capacitor systems studied, the capacitance, ESR, and discharge times were fit to the variables of temperature, voltage, and time. Based on the statistics of the fit, the equations derived from the test data show good to excellent correlation and should provide reasonable predictive power for the ESR, and excellent predictive power for the capacitance and the discharge time. Table 2 lists the statistics for each of the three responses for both the single capacitor study and the series-connected system study. A perfect fit would give R^2=100%.

TABLE 2

Regression Analysis Statistics for the Response Functions

RESPONSE	SINGLE CAPACITOR		CAPACITOR SYSTEM	
	Std. Error	R^2	Std. Error	R^2
Capacitance (F)	0.009	93.5%	0.011	95.5%
ESR (Ohms)	0.018	59.2%	0.021	99.8%
Discharge Time (s)	0.176	86.7%	0.191	99.2%

The properties and performance of capacitors and systems that were not a part of the regression derivation are compared to response equation predictions in Table 3. These capacitors and systems were in a companion shelf-life study, and were maintained at 0 volts, 25°C conditions. As shown, the single capacitor equations make a better prediction than do the system equations, and come very close to the actual observed values. The single capacitor equations were based on data that extended about three times longer in duration than the system data. It is expected that the system equations will become better predictors as their test time increases.

TABLE 3

Equation Predictions Compared with Measurements
1000 Test Hours at 25°C and 0 V Conditions

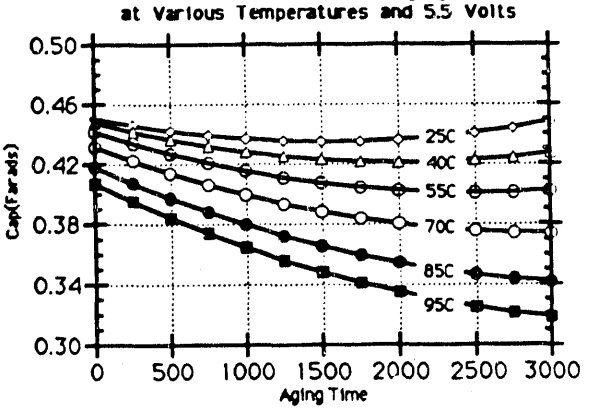
(Predicted/Actual)

	ESR (Ohms)	Capacitance (F)	Discharge Time (s)
Single Capacitor	.55/.54	.47/.46	6.5/6.4
Capacitor System	.58/.55	.39/.41	5.8/6.2

DISCUSSION

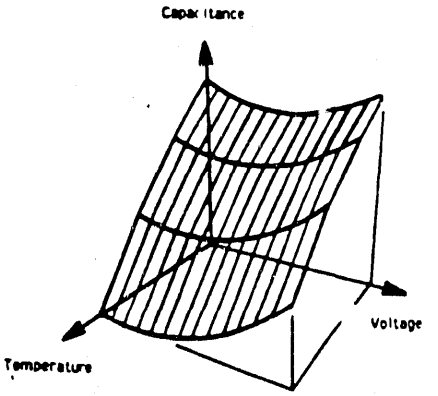
Figure 6 displays the predicted capacitance versus time for single capacitors at various temperatures and at 5.5 volts (50% voltage derating). Higher temperatures increase the magnitude of the capacitance change. The family of curves in Figure 6 also do not start at a common point at zero time. The response equations do not accurately predict the rapid capacitance change experienced during the first 50-100 hours.

Figure 6
Predicted Capacitance vs Aging Time
at Various Temperatures and 5.5 Volts



A snap shot in time of the response functions is useful for identifying the relative significance that temperature and voltage have on capacitor properties and performance. Figures 7, 8, and 9 are, respectively, the predicted response surfaces of capacitance, ESR, and discharge time for single capacitors at 3000 hours. The voltage grid lines are shown in 1 volts increments from 0 to 13 volts, and the temperature grid lines are at 25, 50, 75, and 100°C. Each response axis begins at a non-zero value in order to magnify the response surface shape.

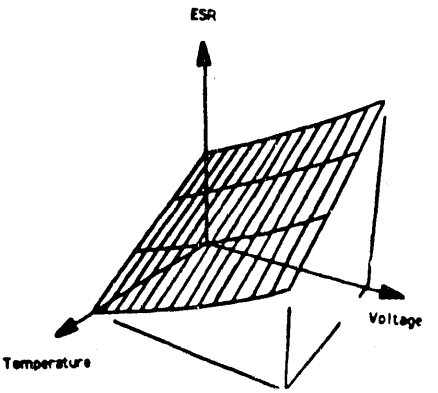
Figure 7
Predicted Capacitance Voltage-Temperature
Response Surface at 3000 Hours
(Temperature 25C-100C, Voltage 0V-13V)



As shown in Figure 7, the largest capacitance change is predicted to occur at the maximum temperature with approximately 3 volts. In other words, operating the capacitor at 100°C and 3 volts will create the largest capacitance loss after 3000 hours Surprisingly, 100°C, 13 volts operation is predicted to be less strenuous, at least from the absolute capacitance view point. At 25°C, the capacitance is a weak function of voltage with the strongest influence near 6.5 volts.

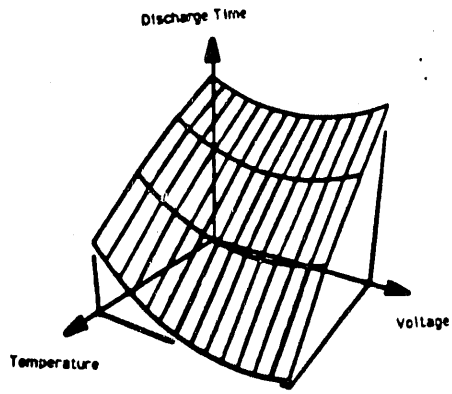
The predicted ESR response surface is shown in Figure 8. It is nearly planar and tilted slightly downwards towards higher temperatures and lower voltages. For most DLC applications, problems are created only when large ESR increases occur. At 3000 hours, no significant change is predicted over the studied temperature-voltage parameter space.

Figure 8
Predicted ESR Voltage-Temperature
Response Surface at 3000 Hours
(Temperature 25C-100C, Voltage 0V-13V)



The predicted discharge time response surface (Figure 9) is more complex than the previous two. It is saddle shaped, with minimum values occurring at about 8 volts and 25°C. At 0 volts, the discharge time is only weakly influenced by temperature. Predicted conditions that provide the greatest discharge time retention are 25-75°C at low voltages, and 25-50°C at maximum voltage.

Figure 9
Predicted Discharge Time Voltage-Temperature Response Surface at 3000 Hours
(Temperature 25C-100C, Voltage 0V-13V)



An explanation for the observed and projected DLC performance and property changes is beyond the scope of this paper. For convenience, collected data in this study was fit to polynomial equations with time, temperature, and voltage factors. This response function form does not lend itself to physical interpretation of property changes arising from temperature or voltage activation processes. It is also risky to use in making predictions outside of the investigated sample space. Further work that includes data fits to physically realistic model equations should increase the confidence levels of predictions at other conditions, for instance, at longer time periods.

CONCLUSIONS

The effects that temperature and voltage have on the properties and performance of Capattery DLCs and DLC systems were investigated over the space 25 - 95°C and 0 - 12.9 volts using a five-level experimental design. Data was collected and analyzed to develop empirical response functions. The statistics of the fit were good to excellent. Some differences were found between the single capacitor and system equations, but additional test hours are needed to draw conclusions.

Response surfaces of capacitance, ESR, and discharge time were shown at 3000 hours. Capacitance change was largest at high temperatures, and for a given temperature, at voltages between 3 and 6.5 volts. Voltage-temperature effects on ESR are small and rather uniform, except near the highest voltage. A saddle-shaped response surface was seen for the discharge time, with the largest changes at high temperature and voltages. We plan to continue this study to be able to develop response functions for much longer times.

ACKNOWLEDGEMENTS

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