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Printed Wiring Board Design and Manufacture in Electronic Instrumentation Department 8450

D. J. Hardin, H. E. Schoeppe, R. L. Franssen, G. W. Kirchner

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Abstract

In order to successfully and efficiently produce printed wiring boards, the full progression from design concept through fabrication must be understood. Within Department 8450, this includes the utilization of Valid Logic Systems Computer-Aided Engineering (CAE) tools to perform schematic capture, circuit simulation, and board layout. If the appropriate functions are not performed in the proper sequence, or if the essential materials are not available when needed, the time required to produce a printed wiring board will grow inordinately. This report details the process flow within Department 8450, starting with the initial design requirements and concluding with a completely fabricated and tested circuit board. Recommendations for improving the system are also presented. Design and manufacturing considerations that impact the process are identified, as are the input and output requirements for each stage. With this information as a guide, a design engineer will be able to utilize the CAE tools available for circuit board design more effectively and minimize the time interval from concept to final product.

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Scope

The pathway for the design and manufacture of printed wiring boards can diverge into many alternate routes at various points throughout the process. To investigate all of these alternatives would be very time consuming and somewhat counter-productive to the idea of developing a process flow within Department 8450. For that reason, this report focuses *primarily* on the steps required to produce printed wiring boards utilizing the resources within this Department. This does not mean that all routes other than the one presented were blindly ignored, it simply means that a detailed study of the process flow for each of these avenues was not conducted.

The process described here is the implementation of the Valid Allegro system in Department 8450 to perform the design and layout of printed wiring boards for eventual fabrication by the Electronics Prototype Laboratory Section (Div. 8451-1). To that end, the sequence of each stage of the design process will be detailed, followed by the recommendations for improvement by the Design Quality Team.

Introduction

To achieve a quality printed wiring board, the design must reflect the needs of the customer. For this to happen, the customer (in this case, the design engineer) must understand the process that needs to occur for a printed wiring board to be produced. This provides a basis for making decisions affecting the design, and a commitment to those decisions.

The purpose of the study which led to this report was twofold: determine what constitutes the process flow for printed wiring board fabrication, and improve the quality of that process. Although there are many ideas as to what the word "quality" entails, in this instance it refers to the ability to progress through the system (from the initial concept to a finished, tested, *usable* product) with as little delay, rework, and disorientation as possible. The consequences of doing otherwise results not only in slipped schedules and lost effort, but with the compromise of entire projects.

The design and fabrication of a printed wiring board requires the efforts of numerous individuals and organizations working in concert. Too often, the design engineer is not aware of all the steps necessary to complete the journey from design concept to a completed board. This leads to a communications breakdown that can leave a design languishing in the printed wiring board pipeline, or can cause needless iterations of activity with a corresponding loss of time. In reality, there is no "pipeline" into which a designer can submit a sketch and have a finished product miraculously appear, unattended, at the other end. It is the engineers responsibility to assure that all materials and information are provided for each stage of the concept-to-fabrication process.

As can be seen in Fig. 1, the process of producing a printed wiring board consists of three distinct activities: the logical design, the physical design, and manufacturing. The logical design phase includes the establishment of the design requirements, forming the design concept, and considering the impact on the design by external concerns. The physical design involves the drawing of schematics, circuit simulation, and the physical board layout (component placement, routing of traces, etc.). The last stage is the actual manufacturing, testing, and loading of the final product. Each of these stages are still driven by design requirements and each have particular documentation criteria associated with them. This report will detail each of these stages in a hierarchical fashion, and will identify the input and output requirements from each section.

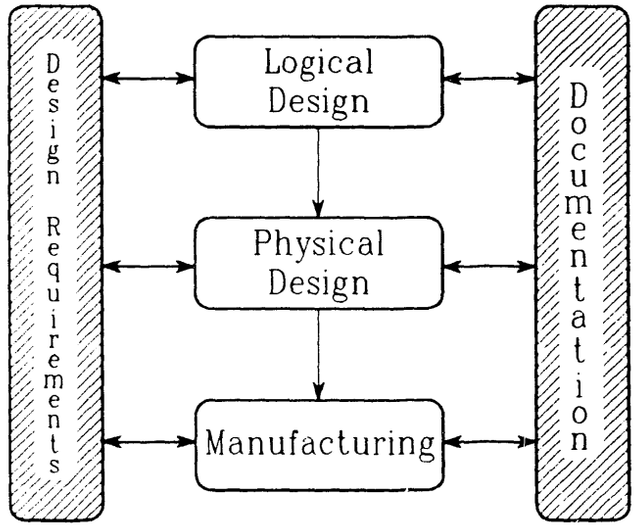

Figure 1: Basic Process Flow

The most efficient avenue for the design and documentation of a printed wiring board is to maintain all aspects of that design on a single system. Within Department 8450, the system of choice is the Valid Allegro system, and the intent is to utilize the capabilities of Valid and Allegro to accomplish the design, circuit simulation, board layout, and documentation of all printed wiring boards required by this department. The primary focus of this design process flow will be just that: the flow through the Valid system and Department 8450. The true process flow, however, is not restricted to this approach. There are logical check-points where the design, or portions thereof, could be translated to different systems if the need should arise. Although these branch points do exist, they can easily lead to a duplication of effort, as well as introduce confusion and a source of error.

Expanding on the basic process activities of logical design, physical design, and manufacturing, an overall process flow from design requirements to finished product can be derived (Fig. 2). Although this illustration does not show the possible branch-points in the flow, or the iterative loops that may be encountered, it does present the linear progression of activities required to produce a printed wiring board.

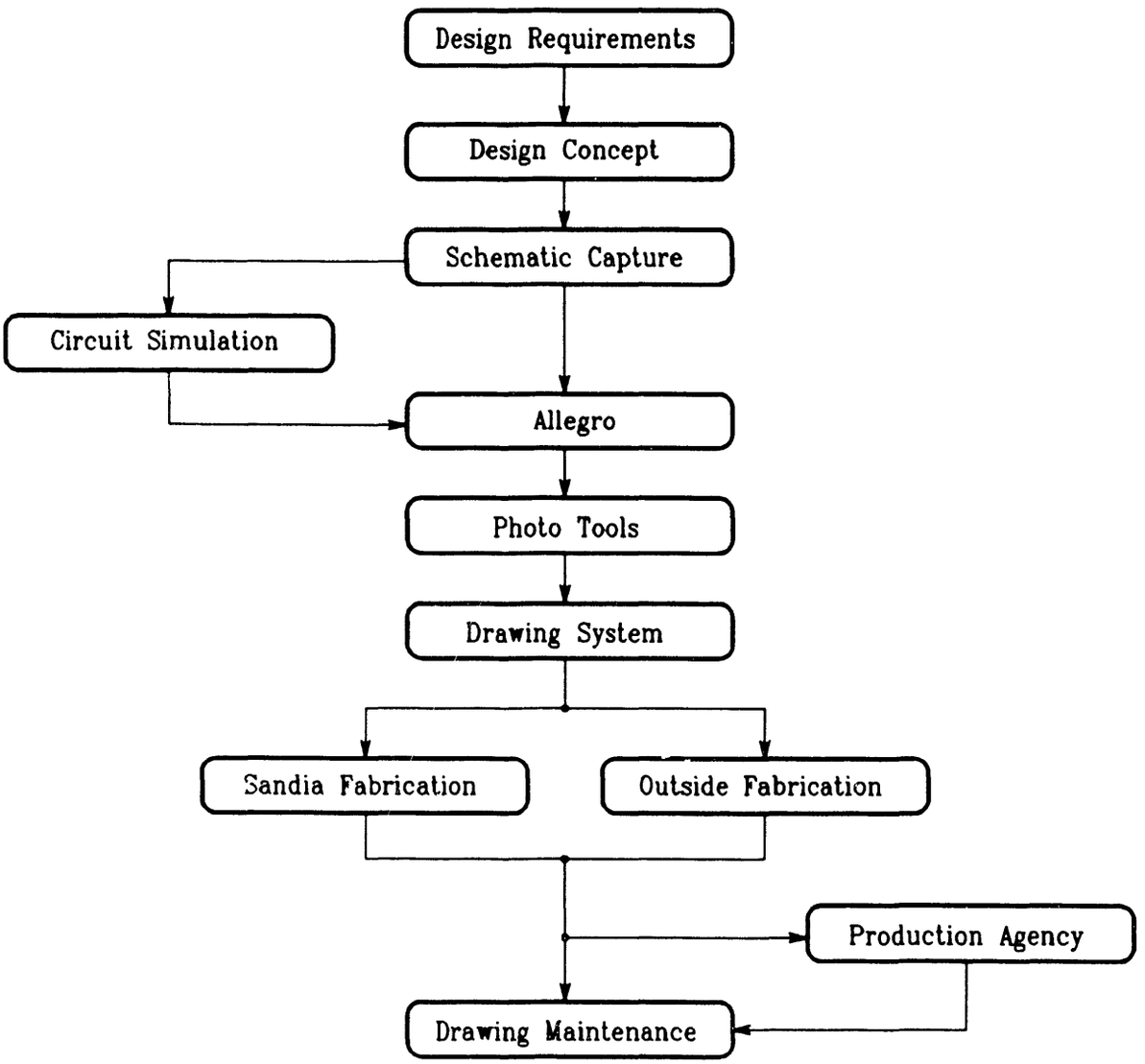

Figure 2: Overall printed wiring board process flow

The design requirements and design concept stages should be performed by the engineer *before* trying to utilize the Valid system. The attention that is paid to detail at this stage of the design can save weeks, or even months, of effort later. The first step of the design

actually involving the Valid system is the schematic capture (the drawing of the circuitry utilizing a graphics editor). This, in conjunction with the component libraries, forms the basis upon which the rest of the system relies.

When the schematic is complete, circuit simulation is an optional, but highly recommended, activity. In addition to validating the design, the simulation process provides the engineer with a better understanding of how the finished printed wiring board will function. Again, any time spent simulating the design can result in enormous savings of time and money if a flawed design is discovered before a circuit board is designed and fabricated.

Following the successful compilation of data from this phase, the engineer proceeds to the physical layout of the board by employing Allegro (still on the Valid system). This involves the definition of the board itself, the placement of components, and the routing of circuit traces. Once this has been achieved, the design phase is essentially concluded. The pertinent files and drawings are now submitted to photo-tooling.

The particular functions of producing photo-plot films, contour routing files, and other additions required for manufacturing are not performed within Department 8450, but instead are accomplished by Div. 8284-2 (Outside Fabrication and Numerical Support Section). After these plots and files are produced, the package is now available for release to drawing control, and assuming all materials are available, fabrication of the board can proceed.

The fabrication of printed wiring boards will generally be accomplished by Div. 8451-1 (Electronics Prototype Laboratory Section), but could be performed by a commercial fabricator or by one of the production agencies if necessary. The impact on the process flow of not having the board built within Department 8450 should be minimal from the standpoint of the Valid system output requirements, but could severely affect the time required to receive a finished product.

Long after a printed wiring board has been designed and fabricated, it may be necessary to build new boards or modify the design. This requires a drawing maintenance system in association with drawing control to ensure that the file types and formats saved today can be accessed in the future. Also, enough information should be saved in a readable form to permit the reconstruction of the original design regardless of the computer system used.

The first step toward the design of a printed wiring board is to determine what the final product will be and how it will function. As can be seen below, this determination is made based upon the design requirements. This is the most basic, yet undoubtedly the most crucial phase of the entire design cycle. Each step of the process should be carefully considered, with as much information gathered as possible, to ensure that the requirements being used to drive the design are accurate, necessary, and unlikely to change. The importance of this process cannot be overstated.

Generally, the design requirements will provide a functional description of what the design is to accomplish and any prerequisite knowledge such as system interfacing, standards, or specifications that need to be met. This information is made available through the system engineer via data lists, design guides, control documents, etc. The final application of the design, whether it be for JTA, reimbursable project, or lab use must be taken into consideration as well, particularly during component selection.

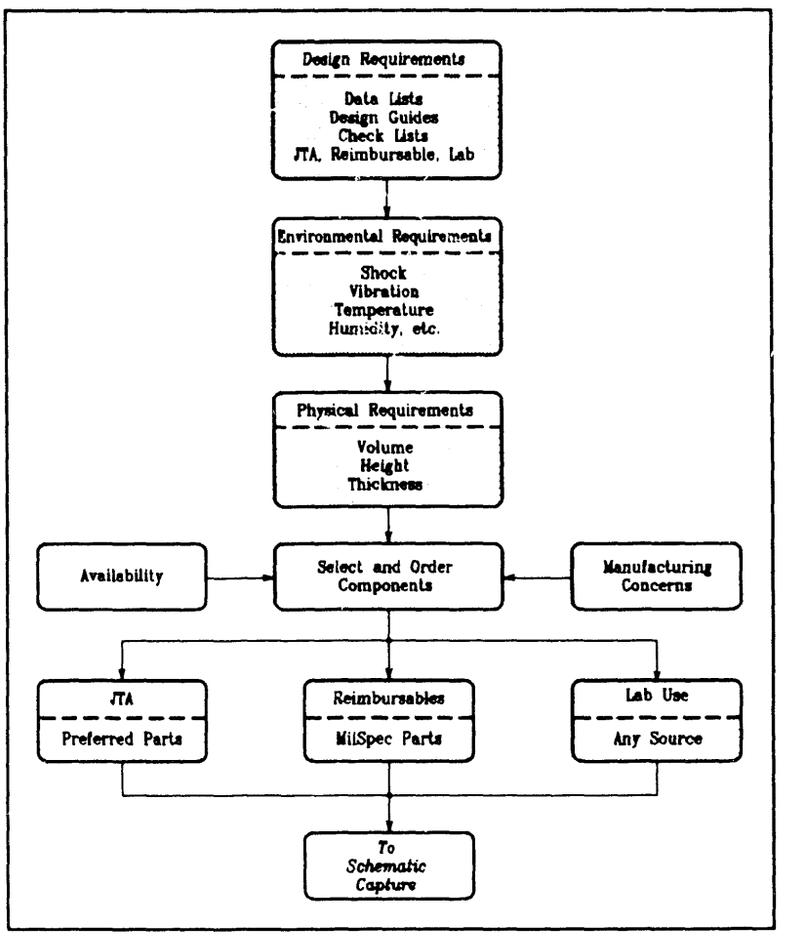

Figure 3: Design Requirements and Design Concept

The selection of components is, by no means, a trivial issue. A design that may not function or cannot be manufactured due to component failure or lack of availability can disastrously impact the quality of an entire program. Again, apply careful and thorough consideration.

Environmental concerns, often overlooked during component selection, may affect the decisions made. Are there any system requirements for the design to function under extremes of mechanical shock, vibration, or temperature? Consider the effects of humidity and contamination on the design, as well. There will normally be physical constraints pertaining to the volume and/or height the design may occupy, so make certain the components selected do not violate these limitations.

This is also the point in the design where manufacturability should be determined. For instance, if surface-mount devices are to be utilized, assure they are necessary as per the design requirements. Leaded components are generally cheaper, more readily available, and easier to implement in the design process. *Involve manufacturing in the design process!* If a component change must occur, it is far more efficient to do so before the design, layout, and fabrication has been performed.

Investigate the availability of the components being considered; don't assume they are sitting on a shelf waiting to be used. Some components can have lead-times of many months, and others are produced only once or twice a year. Even if the part is carried as a stock item by Sandia Laboratories general stores, there is no assurance that the quantities required are on hand or are attainable. As a general "rule-of-thumb," the graph in Figure 4 can be used to estimate the time required for the procuring of components, but the engineer should verify the lead-time for all parts that are essential to the design.

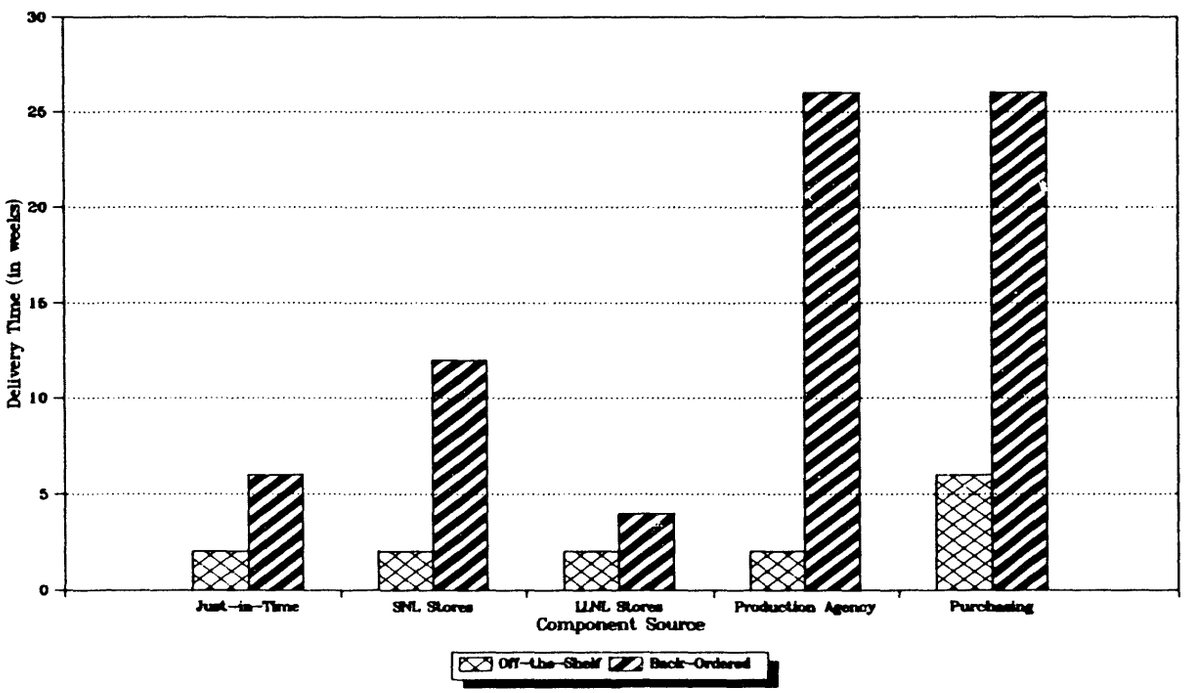

Figure 4: Component Lead-Time

As previously discussed, the final application of the design may determine the source for the components selected. If the design is part of a JTA weapons system, the components will generally be selected from a preferred parts list, while a reimbursable project may use parts meeting the Military Specifications. A printed wiring board that is intended for laboratory

use, on the other hand, might not have any restrictions on the components, and any commercial source would suffice. If possible, identify suitable substitutes for the components selected. Once all of these determinations are made, the components necessary to complete the design should be placed on order to ensure they will be on-hand when required. This will help prevent the needless interruption of the process flow waiting for long lead-time items to appear.

Inexperience and lack of familiarity with the basic requirements for designing and building a printed wiring board is a major stumbling block to the successful implementation of a design. The items discussed above are but a few of the issues that need to be considered during the design concept stage; there are still many other considerations that can affect the design process. A Preliminary Design Definition Check List, such as can be found in Appendix A (pg. 39), should be utilized to assist the engineer in the design requirement and design concept stage. This will assist the designer in appraising the number of layers, any unique requirements, noise-generating components, resistor wattage and type, current requirements, heat sinks, voltage planes required, and so on.

The transition from design concept to circuit design is made by drawing the circuit schematic, an act referred to as schematic capture. Schematic capture (Fig. 5) is performed on the Valid system using a Graphics EDitor (GED) to add the component symbols and interconnections that form the circuitry.

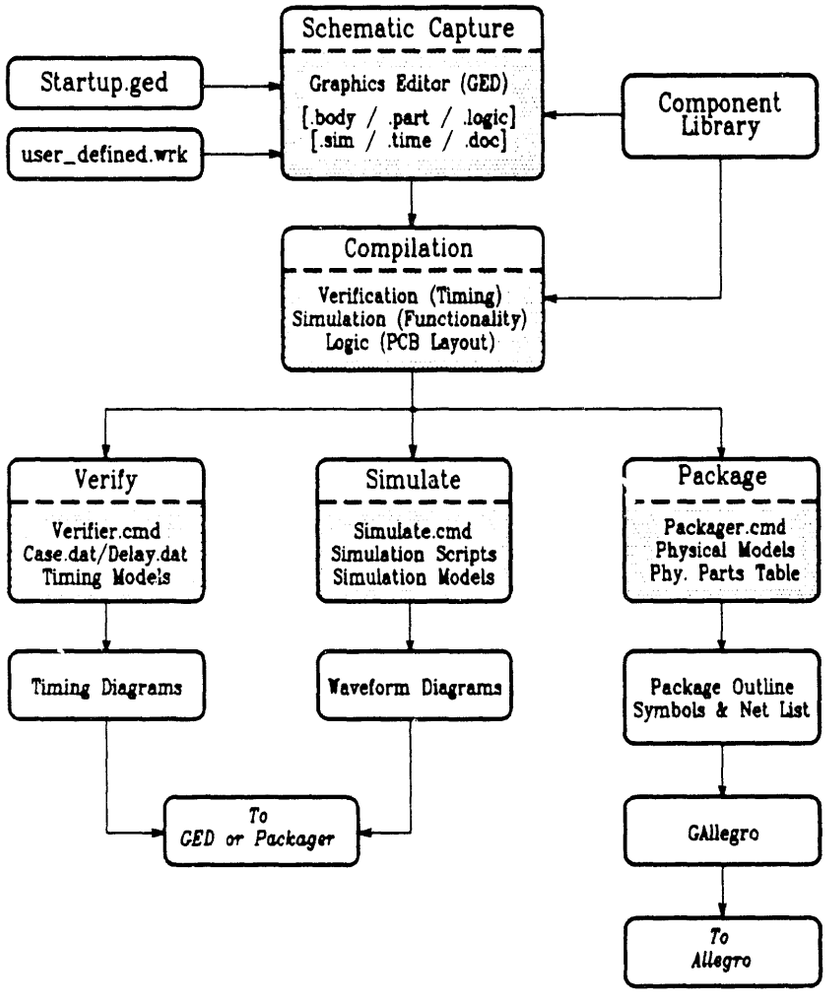

Figure 5: Schematic Capture and Circuit Simulation

The significance of this stage involves more than just drawing the circuitry; Valids' methodology of "Rules Driven Design" places the source of the designs functionality at the schematic level. This means that *only* the schematic defines, or can modify, the design. No other portion of the design cycle, such as Allegro, can modify the functionality without violating the design.

In preparation for this stage of the design, the engineer should make certain that the appropriate libraries exist on the Valid system for the parts to be used. This includes the libraries for schematic capture (GED), as well as for circuit simulation and Allegro (printed wiring board layout). If they don't exist, they will have to be created to reflect the correct component values and properties. The files "startup.ged" and "*.wrk" contain system defaults and user definitions, and should be customized by the user.

As mentioned above, the system libraries required for the components to be used must exist, but the library system can be very confusing. Where are the libraries and what are their contents? What format do new library entries need to conform to? If each engineer creates his or her own library figures in a separate directory, a great deal of duplication of effort and non-standardization occurs. The efficiency and implementation of the system would be enhanced with the addition of a system librarian to maintain a global component library. The engineer would still be responsible for gathering all of the pertinent information concerning a new component, but the addition of that part to the library should be standardized.

Unless crucial to the design, do not define specific pin numbers, package designations, or any other physical references at the schematic stage. This can severely restrict the capabilities within Allegro when it is time to perform the printed wiring board layout. Leave these items to be defined by the "packager" portion of Allegro.

Once schematic capture has been completed, a plot file of the schematic can be generated, along with intermediate files for compilation, which is the process of extracting the necessary information from the GED graphic files to form the properly formatted logical files for the next phase. The path of the compilation (defined in the "*.wrk" file) can be for timing verification, circuit simulation, or packaging. Timing verification provides worst-case analysis of synchronous circuits, but is rarely used due to the timing features available through the functional simulator and the lack of necessary timing models. Functional circuit simulation and packaging are the common routes to follow.

Simulating the design, or portions of it, can highlight problems that would otherwise not be found until the design was fabricated and tested. While not required, the proper use of these tools can definitely reduce the overall number of design iterations and subsequent loss of time that would normally occur. For this reason, it is *strongly* recommended that circuit simulation be included in the design process for all but the simplest of designs.

Once the schematic reflects an operational design, the next step is to invoke the Packager. This step converts the logical output files of the compiler into a combined logical/physical representation. Reference designators are now assigned and physical package names are attached, thus preparing the files for input into Allegro, and the infamous (but all-important) "net list" is produced at this point. In addition, the Packager is also the hub of the back-annotation process from Allegro to GED, maintaining the files that are used to keep track of the current state of the design.

Printed Wiring Board Layout via Allegro

Allegro is a Computer Aided Engineering (CAE) software tool which is used to perform the physical layout and analysis of a printed wiring board. The process of designing the printed wiring board is, in essence, the building of an Allegro database. When Allegro is active, it operates on a copy of the database file ("*filename*".brd), which must be saved between editing sessions. Once complete, this database becomes the source for performing analysis on the design (thermal, signal-to-noise, etc.) and for the creation of manufacturing files (artwork files, ncdrill files, drawings, etc.). Allegro is also used to create the various symbol libraries (package, format, and printed wiring board) used in the layout process. The scope of this section will be to present the block-level flow through the Allegro system. An in-depth dissertation on the use, and caveats, of the Allegro PCB Editor can be found in Appendix B (pg. 45).

When starting a new design, a preliminary database is established with Allegro system defaults. These defaults should be modified to conform to the actual design requirements. The physical shape of the printed wiring board, "keep-in/keep-out" areas, layer definition, and specific design rules are all part of the database initialization. For future compatibility outside of Department 8450, standardized database file-naming conventions should be developed and implemented.

As can be seen in Figure 6 (pg. 20), the inputs to Allegro are the net-list and device files from the previous stage. While the net-list defines the interconnection of the parts, the device files describe the functionality and name of the Allegro package symbols to be used. These device files, having been generated by the Packager, should be checked for compatibility with the Allegro package symbols. Once verified, the net-list can be input to Allegro, and the net-list functions can be assigned to Allegro functions.

Component placement is a very critical and time consuming task. Although Allegro has an "autoplace" capability, it will not automatically and perfectly place all of the components without any designer intervention. A combination of automatic and manual placement must be used in an iterative process, because once placed, the traces connecting components must be routed. Expertise in this area will only come with experience. To avoid difficulties, do not attempt to perform any of the routing until all of the components have been placed.

The evaluation of the placement of components is primarily a visual task, although several tools are available to minimize the confusion (function swapping and pin swapping, for instance). Thermal analysis can also be performed at this point to highlight "hot spots" which might modify component placement. Once the designer is satisfied with the placement, it is imperative that back-annotation be accomplished. Pin and gate swapping, reassigning reference designators, and other related activities which don't affect the functionality of the design can effect the net-list and, in turn, the schematic. Back-annotation ensures this information is relayed back to GED so that the schematic reflects the current design state.

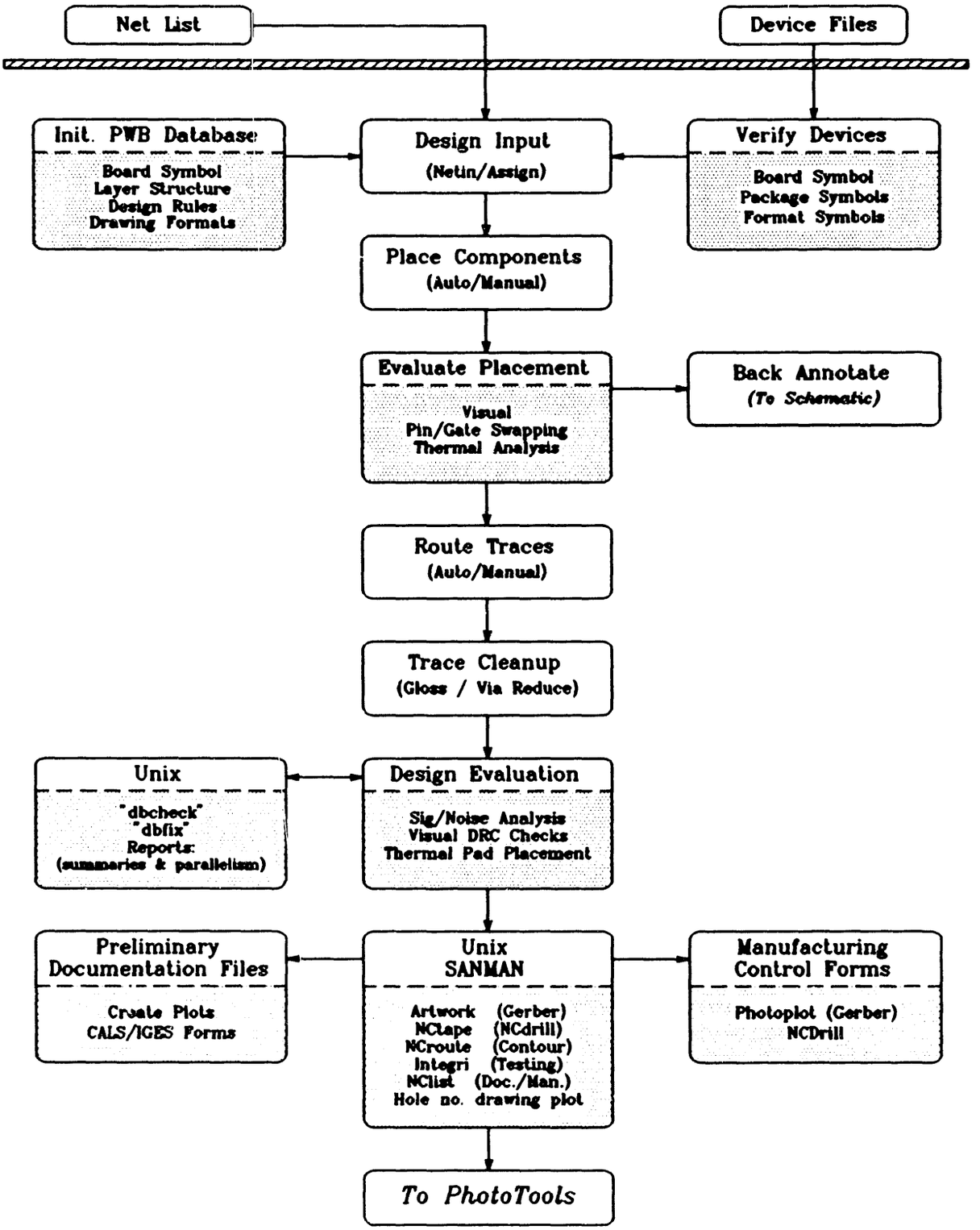

Figure 6: Printed wiring board layout via Allegro

After the components are placed, the logical connections defined in the net-list are displayed as a "rats-nest" of lines. Routing of a printed wiring board consists of converting this rats-nest into the actual trace connections to be used when the board is fabricated. Routing is generally performed using both manual and autorouting procedures, similar to the component placement operation.

Following the complete routing of the board, there are a number of functions to be performed to prepare the layout for eventual manufacturing. These functions fall under the categories of clean-up and design evaluation, and include such items as glossing (trace and via reduction, line smoothing, centering, etc.), restoring pads sizes, and the addition of thermal pads.

None of the files required for manufacturing are created directly by Allegro. Instead, the required information is tagged within Allegro by the use of forms, and the actual manufacturing files are generated at the UNIX level by routines that extract the necessary information from the Allegro database. The output from this phase includes: the Gerber files, the NCdrill file, contour routing information, "Integri" test vectors, and hole number drawings. At this point, the hole numbering routine has not been completed, but is in process.

The function of the photo-tooling stage in the printed wiring board process is essentially to provide the interface between the design stage and the manufacturing stage. As shown below (Fig. 7), this is where the photo-plots are made for all the layers of the circuit board, and the final manufacturing files (drill, contour routing, listing, etc.) are produced.

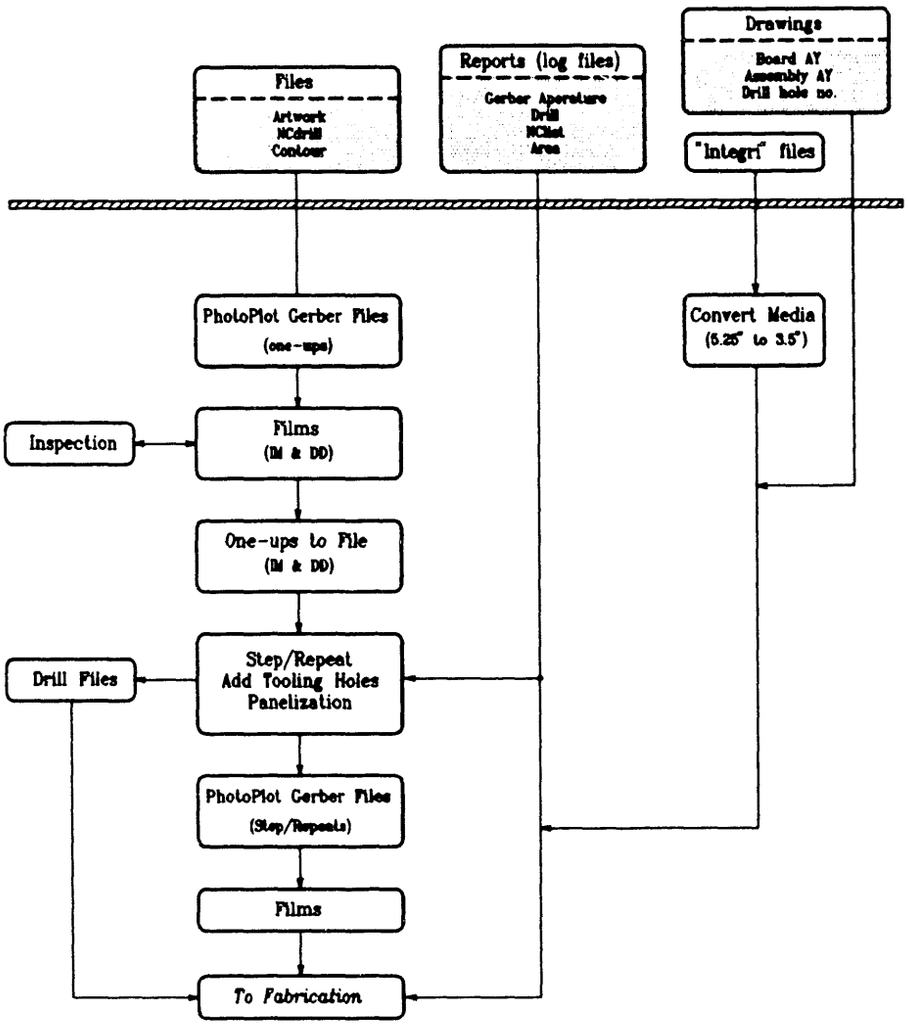

Figure 7: Photo-Tooling Process Flow

This particular step in the overall process flow is one that is not performed within Department 8450 because the tools and expertise required for this task are found in Div. 8284-2 (Outside Fabrication and Numerical Support Section). Since all such work must flow through this one section, it is vital that sufficient time be allocated for this step in the process.

All of the files and drawings that are inputs to the photo-tooling process originated on the Valid system from the Allegro database. The first task is to photo-plot the Gerber files as"one-ups," meaning that no panelization or step-and-repeat operations (multiple copies of a printed wiring board on a single panel) have been performed. The films issued by this process (IM and DD files) are then returned to the design engineer for inspection. If the inspection reveals no errors, and the engineer is confident that the photo-plots accurately reflect the design, then the "one-ups" are again plotted and, this time, released to the drawing system.

Within the Department 8450 process, the plots are now taken to the Electronics Prototype Laboratory Section (Div. 8451-1) for the determination of physical layout information concerning panelization or step-and-repeat procedures. After this has been accomplished, the package is once again returned to photo-tooling for the actual process of plotting the required panelization or step-and-repeats. The appropriate tooling holes and "S/T" (origin) holes are now added, and a new drill file is produced to include these new holes.

The hole numbers that were assigned in the board layout stage still apply, as far as the hole-number plot and the NC listing are concerned, but the sequence of the NCdrill file will no longer bear any resemblance to that generated from the Allegro database. This, however, should cause no great problems; holes on the board can still be identified or located with the use of the NC coordinate list and the hole-number plot, it is only the sequence in which the holes will be drilled that has been changed.

The contour routing information for the physical board shape is currently presented to photo-tooling in the form of a plot or drawing of the board shape. This plot is then manually converted to the proper coordinate information for the router. A method of transferring this data in a more meaningful form, such as another database file, should be investigated.

Some of the files produced at the termination of the Valid Allegro stage are needed for fabrication, but are not used for photo-tooling. These files include the "AY" drawings of the board and the board assembly, hole-number plots, and "Integri" test vector files. While most of these merely pass directly through photo-tooling, the Integri test file does undergo a media conversion (from 5.25" diskette to 3.5" diskette) while in the photo-tooling stage.

The final films can now be plotted and all pertinent manufacturing information generated to prepare the design for fabrication, but this should only be done <u>after</u> completing the full release of information to Drawing Control.

Drawing Control

Before a printed wiring board can be fabricated, the associated package of drawings and files must be released to Drawing Control. This ensures that all parties involved are working with the same revision of data. If the drawing system is circumvented, it is all too easy to end up with drawing issues out of synchronization with the various design process stages. This, in turn, can lead to a considerable loss of time if a board is manufactured to out-of-date information. For the purpose of printed wiring board manufacture within Department 8450, it is recommended that a full release to the drawing system be executed after the inspection phase of photo-tooling.

Whether or not to release to the drawing system is not an issue...that function has to occur if boards are going to be manufactured, or if the design is to be transmitted to a Production Agency. How best to achieve that release from the Valid system is a different story, however, since a path does not yet exist that will accomplish it. There are two possibilities that will be discussed in this section: using drafting as a drawing release agent, or interfacing directly with Drawing Control.

Obviously, drafting has the ability to release their own drawings from the Computer Vision (CV) system to Drawing Control with little difficulty. However, to make use of their ability to release documents would entail a significant amount of development time and effort to establish some sort of compatibility for *intelligent* file transfer between the Valid system and the CV system. This does not appear to be a viable link, not only because of the effort involved, but also because it would possibly create another bottleneck in the process flow by removing the release action from the engineer's hands. It is, therefore, recommended that the ability to interface directly with drawing control be instituted. Figure 8 (pg. 26) shows the steps involved in the release process, and how to get there from the Valid Allegro system.

The key intersection that will now allow Department 8450 to communicate directly with drawing control is the "Sun" system of Department 8270. This is the system to which the files from drafting are copied as part of the process for releasing documents, but it does not require compatibility with the CV system for access. By hand-carrying a 9-track digital tape (or in the future, by utilizing the Random Access Network) the files generated by the Valid Allegro system can be loaded onto the Sun system. This action, accompanied by an Engineering Release form and an Electrical Drawing Information form, will allow Department 8450 to release drawings to drawing control without having to utilize Drafting.

Once the aforementioned tasks have been completed, the rest of the operation is the same for information from either source; drafting or Department 8450. Drawing Information (Div. 8273) transfers the files from the Sun system, performs file comparisons, creates drawing control information (latest issue, etc.), and establishes an index file with drawing numbers, names, and other system data. A Unix based program, TAR (*T*ape *AR*chive), is then used to complete the release action.

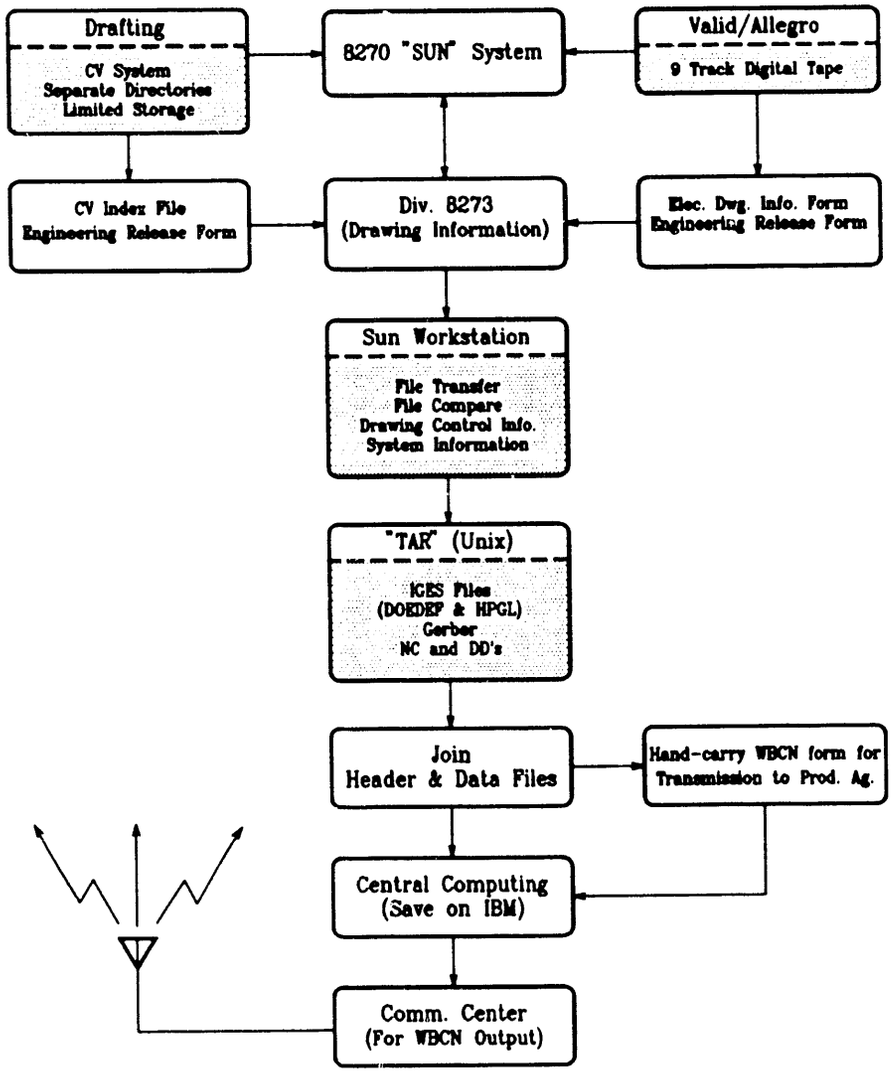

Figure 8: Drawing Control Process Flow

The TAR system is used as a means of transferring the hardware related IGES files, whether they be DOEDEF (Department of Energy Definition, a subset of IGES) or HPGL plot files, and the necessary electronic files, such as Gerber, NC's, DD's, etc., to tape. These files, having been joined with the appropriate header and datafile information, are then saved as a set on the IBM system in the Central Computing Facility (CCF).

If it has been requested that the drawings and information be sent to a Production Agency, Div. 8273 will hand-carry a WBCN form (Wide Band Communications Network) to the CCF. The CCF will then, in turn, relay the information to the communications center for subsequent transmission.

In order to have a printed wiring board fabricated, the entire package of drawings, films, and files must first be submitted to Fabrication Liaison (Div. 8284-2, Outside Fabrication and Numerical Support Section). A determination will then be made as to where the board will be fabricated; either in-house (by Div. 8451-1) or by an outside manufacturer. This requires a little foresight on the part of the engineer, because if the job is to be performed in-house, only a single set of drawings are necessary, but if it is to be sent outside, *five* sets of drawings must be supplied.

The process flow for fabrication within Department 8450 begins when the design package is delivered from liaison. The multi-step process of manufacturing the printed wiring board is shown at right. In addition to the steps detailed in Figure 9, there are numerous inspections performed throughout.

It cannot be expressed too strongly that it is the responsibility of the requester, not the fabricator, to ensure that *all* materials required to complete the assembly are on hand. If the circuit board is to have the components loaded after fabrication, do not assume that Div. 8451-1 (Electronic Prototype Packaging Section) will stock or procure any special parts that are needed; this can lead to very long delays in the completion of the job. Lastly, attempting to short-circuit the system by bypassing liaison is not the path to successful printed wiring board fabrication.

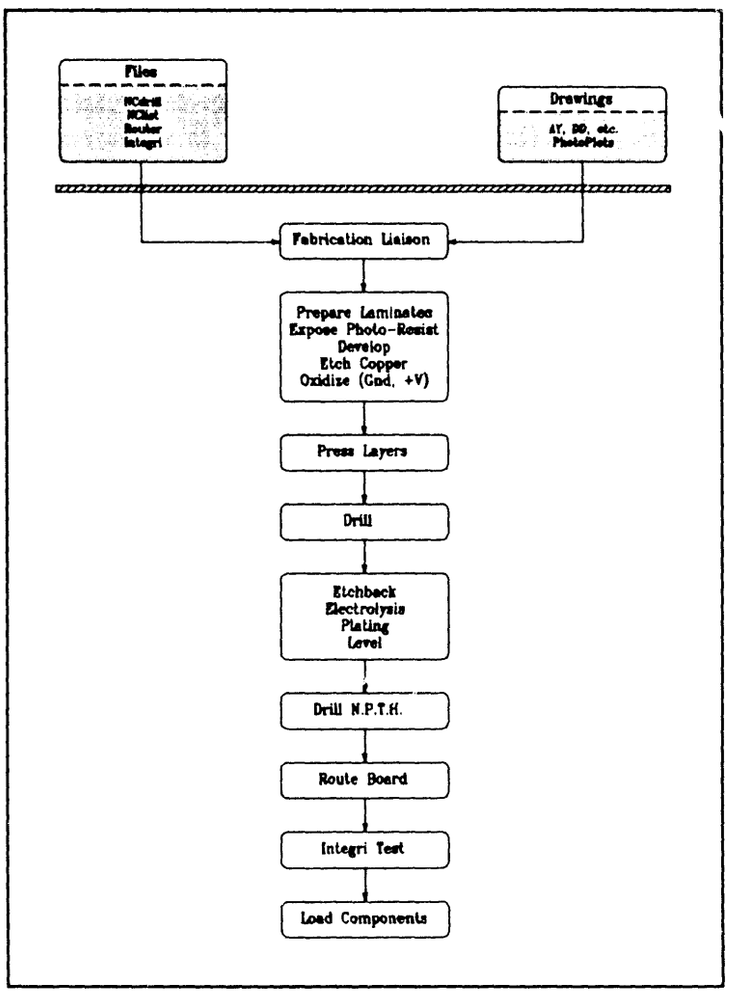

Figure 9: Printed Wiring Board Fabrication

If the printed wiring board will be fabricated by an outside manufacturer, the format of the files and information provided may need to be different from those required in-house. As yet, there doesn't exist a standardized path for outside manufacturing. This avenue will be explored, in conjunction with the purchasing department, to see if there are merits to establishing a link with known vendors.

Training Requirements

To effectively complete the journey through the entire process flow described herein, the designer will have to be proficient in a number of diverse areas. Much of this proficiency, particularly concerning design requirements and design concept issues, will only come with experience. This also applies, to a different extent, for the utilization of the Valid Allegro system.

Most engineers now have considerable experience with computers and their ability to generate graphics. Except for becoming familiar with the operating system used on Valid (Unix), and ensuring all of the proper files exist for access by GED, the process of becoming adept at schematic capture should not be difficult. The consensus among current Valid users is that sitting down and using the system, in conjunction with the GED tutorial, is the best way to learn.

Unfortunately, this same ease of use does not apply when discussing the use of Allegro. With Allegro, a significant amount of user training may be required, as there are a large number of tools and a great deal of flexibility provided by Allegro for the design of a printed wiring board. While the operation of Allegro is relatively straightforward, the designers' knowledge of what tools are available will dictate the efficiency with which it is used.

More important, yet more difficult to acquire, is the required manufacturing knowledge. A printed wiring board must be defined in accordance with established design guidance procedures. This is especially true with the increased usage of surface-mount technologies. The problem in this area is the lack of formalized documentation, thereby introducing the possibility of the designer getting different "correct" answers depending on the source. While most engineers are trained in the area of logic design, few have the specialization required for printed wiring board design.

There isn't a tutorial for Allegro, as there is for GED, and there is a dearth of digestible information concerning the design rules that must be followed for the layout of the board. Training for the Allegro system should consist of gaining familiarity with the system through use, followed by some level of formalized instruction. Until proper documentation exists, however, learning the design rules can only be accomplished by relying on more experienced peers.

Process Flow Time Requirements

The estimated time required to move through the process flow, beginning with the original design concept stage and ending with a completed printed wiring board, has far too many variables to permit any degree of accuracy. The number of design iterations, the complexity of the layout, the availability of parts, and the designers level of expertise with the Valid system are but a few of the factors which could significantly affect the duration of the overall process.

One engineer who recently utilized the Valid Allegro system for the design and layout of a circuit board was logged onto the system for a cumulative total of 11½ hours. The breakdown of this total can be seen below (Fig. 10). It should be stressed that, while this individual is experienced in the use of Valid Allegro, there was no formal training involved. The design in question included eight integrated circuit packages and approximately 30 discrete components on a two-sided printed wiring board.

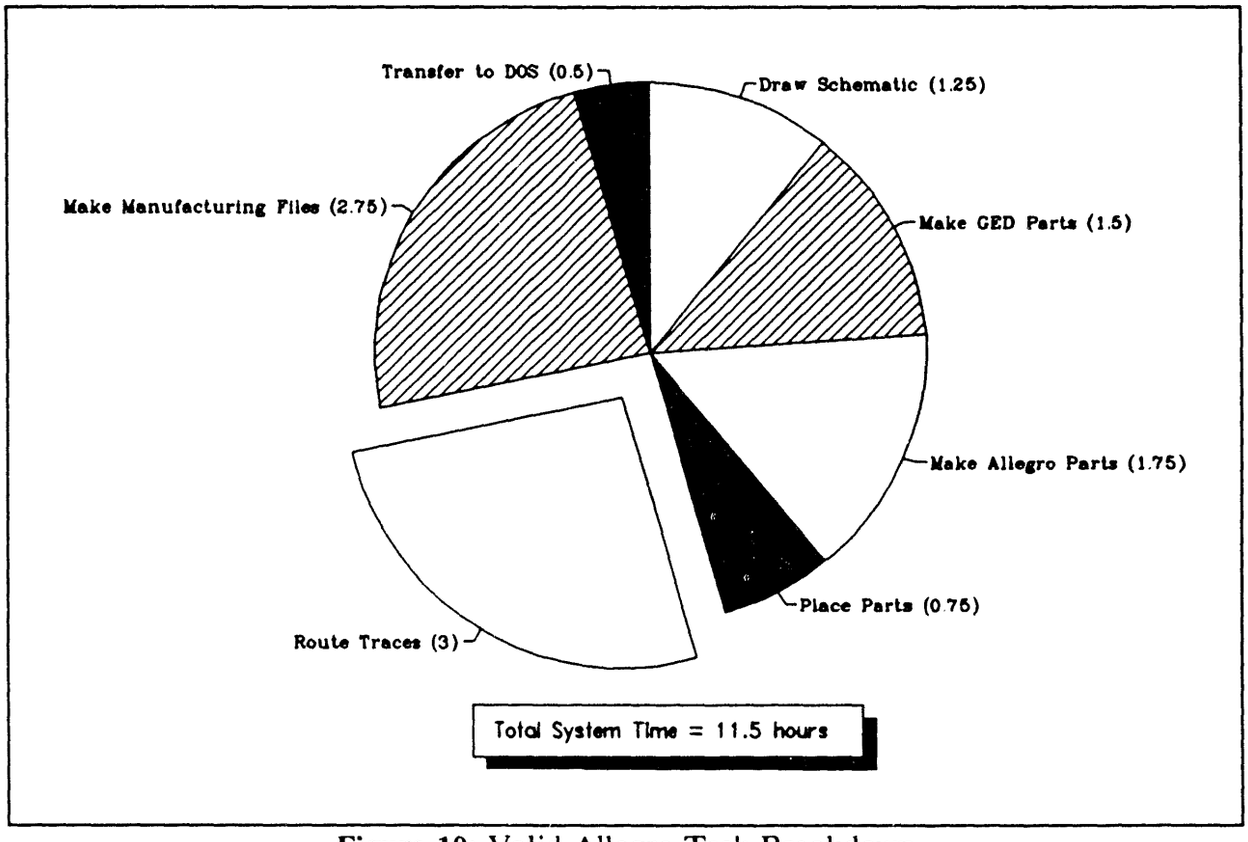

Figure 10: Valid Allegro Task Breakdown

As can also be seen, the largest amount of time for a single task was spent performing the routing of circuit traces, although the creation of library parts to support GED and Allegro

actually consumed a greater portion of the total time. These were followed closely by the generation of required manufacturing files.

This, at least, provides a relative benchmark for what an engineer experienced on the system can accomplish in a relatively short time. Of course, this is only the time required for the design stage, and does not include the time necessary for travel through the photo-tooling process, nor the fabrication and test stage.

Best estimates for photo-tooling is to allow approximately 4-5 days for that process, and another 7-10 days for the fabrication and testing of the finished board. Loading of the bare board can take from 2-5 days depending on density and component type. Remember, these are only estimates...some tasks can be accomplished much more quickly, others much slower. If, however, the design requirements and design concept were sound and all materials are available when required, the turn-around time for the entire process can be quite impressive.

Problems and Recommended Solutions

The process flow described in this report is the recommended path for the design and fabrication of printed wiring boards within Department 8450, but the process is not entirely in place nor without a few problems that need to be surmounted. The following list highlights what are perceived by the Design Quality Team to be obstacles to the smooth progression from design concept to finished product, and recommended solutions.

I. Proper definition of design requirements:

If the design requirements are not sufficiently defined or, worse yet, are in a state of flux, the design process cannot begin on a solid foundation. The design concept and component selection procedures can only be considered in vague terms. It would be pointless, and very costly, to continue very far along the design path if the basic design requirements are subject to change.

The solution to this problem appears easy, but will be very difficult to implement or enforce: all design requirements must be firmly established before beginning the printed wiring board design. In reality, this seldom occurs because of system interfacing conditions that are dictated by outside sources. If these conditions change, as they often do, there is little choice but to reiterate the design process. The engineer's involved must be made aware of the impact on this process.

II. Valid and Allegro system libraries:

Presently, each of the user on the Valid system develops their own library figures for special components and keeps those figures in their own system directories. This leads to significant duplication of effort, as well as non-standardized library figures and naming conventions. The standardization issue may not be a problem, unless it is desirable to someday form a link with drafting.

It is recommended that the services of a system librarian be made available for the creation and maintenance of a *global* library. It should remain the responsibility of the designer to ensure that all pertinent information has been gathered concerning the component in question, but the system librarian would perform the creation of the library figure and update the applicable files to reflect the addition for <u>all</u> users. Standardization of the library entries could then be easily achieved.

III. Proficiency with the Allegro system:

The time flow through the system will be anything but efficient for new users due to the complexity of Allegro and a lack of familiarity with design guidance procedures. Even experienced users have difficulty staying current with the ever-changing design rules; the infrequent user will inevitably have to be versed in these rules each time they want to use the system. While some engineers will relish the thought of having total control of the entire design process, others will

not be so inclined. Few designers will want to take time from other responsibilities to perform such a time consuming function. The time required for a casual user to find their way through the maze of tools and rules presents a major bottleneck to the desired smooth progression through the system.

The recommended solution for this problem is to have drafting personnel experienced on the Allegro system available to assist the engineer during this phase or, preferably, to perform the actual board layout for the designer. If a permanent assignment cannot be arranged, it would certainly be advantageous as an interim solution until more engineers are skilled in the use of the system.

IV. Generation of hole numbers:

Although there is some debate as to the relative merit and necessity for the assignment of hole numbers, it is required by Div. 8451-1 and by the Production Agencies. The generation and assignment of these hole numbers is a post-Allegro routine that has not been completely developed, although it is in process.

This routine should be completed as soon as possible, although the requirement for the hole numbers warrants some investigation.

V. Photo-tooling operation and requirements:

Even though the process performed during the photo-tooling stage has been documented in this report, it is still an obscure and cryptic operation. No one, save for one individual, is cognizant of *all* the steps required to accomplish the production of manufacturing files and films. Since this area of expertise is outside the department, it represents a very real potential for a breakdown in the process flow.

It needs to be determined what files, formats, forms, machinery, etc., are required to fulfill this task; more than one person should know how to provide this vital service. It should also be determined what alternatives, if any, exist in case of a disruption in the photo-tooling capability.

VI. Release of information to Drawing Control:

The options concerning the release of drawings was discussed in the section on the drawing system (pg. 25), with the recommendation that Department 8450 interface directly with Drawing Control. The problem is that the mechanism described to permit this transfer of information has not been tested, and some key components of that interface may not exist.

A test of this system should be conducted at the earliest possible time. This should involve the release of the drawing set, the ability for those drawings to be retrieved for use on the Valid system, and the compatibility of the released

package with the Production Agencies. This is a vital link in the establishment of an intradepartmental design and manufacturing capability.

VII. In-house fabrication vs. outside fabrication:

Thus far, it has been assumed that the final product would be fabricated by the Electronics Prototype Laboratory Section (Div. 8451-1). If, for any reason, a printed wiring board had to be sent to an outside manufacturer, little is known as to what changes in data format or other conditions might be required. The procurement process could easily result in a quagmire each time it was necessary to use an outside manufacturer, adding considerably to the turn-around time.

The possibility of pre-establishing a link with one or more outside vendors should be explored. If the capabilities and requirements of such a vendor were known, it would permit the process flow to account for a known diversion, resulting in minimal interruption to the process.

Conclusion

The design and fabrication of a printed wiring board involves the collaboration of a variety of personnel and organizations dealing with an incredible number of details. This seemingly herculean effort has, in the past, been performed by the Design Definition Divisions (Div. 8271 and 8272). With the advent of increasingly sophisticated Computer Aided Engineering stations, the capability for this design process is now available to a broad spectrum of users. The Valid Allegro system utilized by Department 8450 is a system fully capable of accomplishing the design of highly complex printed wiring boards, as well as the simulation and analysis of circuit parameters before the board is ever built.

The process flow described in this report will permit the complete design and fabrication of printed wiring boards within this department by the design engineers themselves. Not only will this reduce the time required to move from the initial design requirements to a fabricated and tested circuit board, but will allow the engineer to maintain control over the design throughout the entire process. This enables both a quick response to changing needs and a reduction in the number of design iterations incurred.

Although there are serious concerns relating to user training for Allegro, and the linkage to Drawing Control and the Production Agencies must still be established, seldom does the opportunity exist to drastically alter design and fabrication procedures *and* realize an increase in design control and productivity. The potential of the Valid Allegro system provides such an opportunity and should be utilized.

Appendix A

Preliminary Design Definition Check List

Before starting the design definition, the following questions should be answered by the engineer. These questions have been roughly grouped according to design phase.

Overall Electronic Package Design

1. What is the intended use and function of the design?

2. Will the design become a production item? Consider starting in the metric system (ML-AY), as opposed to an A-series drawing.

3. What is the operational environment?

   a. Heat
   b. Vibration
   c. High g's
   d. Weight restrictions

4. Are there space limitations?

5. Are there any mechanical or electrical interfaces to maintain?

6. Any unique system requirements?

7. Are there any noise-generating components which must be isolated from noise-sensitive components?

8. Approximately how many printed wiring boards will be required?

   a. What type?
   b. How many layers?
   c. Any specific separation of circuitry desired?

9. What components will be used? What mounting technology is required?

Schematic

1. Is the information necessary for the schematic design complete?

2. Are the common values and types identified for the components listed below?

   a. Resistor wattage and type
   b. Polarized capacitors
   c. Common TTL and CMOS integrated circuits
   d. diodes
   e. transistors

3. Are all special components identified?

4. Will there be decoupling capacitors used for the IC's? What size and value?

5. Will it be necessary to pre-assign pins on connectors or components?

6. Are there any circuits that must be in close physical association?

7. How will unused gates be terminated?

PWB Design Layouts and Assemblies

1. Is the schematic complete enough to design a printed wiring board?
2. What are the power requirements? Will the power traces need to be wider than the signal traces?
3. Will test points be required? Where will they be located?
4. Are there any heat-sensitive components? Will they require heat-sinks?
5. Are voltage and/or ground planes required? Will they be internal or external layers?
6. Are there any critical circuits requiring high-speed, shielding, etc.?
7. Are there any variable components that need to be placed for access?
8. Do any components require sockets?
9. What is the board configuration? Any special dimensions or keep-out zones?
10. Is there a height requirement or limitation for the board with components?
11. Will wires be soldered to the board? If so, what size?
12. Are jumper wires permitted?
13. Will the board require conformal coating?

Appendix B

Allegro PCB Editor

Database Initialization:

When starting Allegro on a new design, the user is prompted for a filename and a drawing sheet size. A preliminary database is then established with Allegro system defaults. Those defaults should be modified to the actual designs' requirements. Once complete, the database is saved as "filename".brd.

Design Procedures:

- "filename"
  Standardization of filename conventions is in process, but is not implemented as yet.

- "drawing size"
  It is advisable to keep the documentation separate from the physical design. Establish the size to accommodate the board size plus an inch or more for a border.

- Add Board Outline and Features
  Enter the physical shape of the board along with tooling and mounting holes. The bare board should have been previously defined using the Allegro Board Symbol editor. The board symbol is then added as a single entity to the database rather than being comprised of all the individual lines and arcs which make up the board.

  Define route and component "keep-in/keep-out" areas, and any other physical characteristics of the board. These can also be predefined as part of the board symbol.

- Establish Board Layer Structure
  Allegro defaults to a double sided board, so add routing layers as required. Also, add copper areas ("shapes") to layers which will be used as imbedded planes, and don't forget to define which signal (Gnd, V_{cc}, etc.) will be connected to these planes.

- Design Rules
  Specify minimum pad-to-pad, line-to-line, and line-to-pad spacings, as well as routing trace widths. Allegro's default values will probably not be acceptable. Even though these parameters will not be required until component placement and routing, the net-list may contain additional information specified at schematic capture. Specifying these items now may avoid some confusion later, after the net-list is entered.

Design Input:

Allegro requires both a net-list and a set of device files, with elements contained in the net-list pointing to a particular device file (*.txt). The device files describes the functionality (pin and gate swapping, pin-counts, power pins, etc.), and the name of the Allegro package symbol to be used. Both the net-list and device file information is generated from Valid's "Packager" output files by the appropriate interface utility ("Gallegro" for versions of Allegro before 4.0). Prior to reading the net-list, the device files should be checked for compatibility with Allegro package symbols. This is accomplished with "dev_check," which verifies the existence of the symbols called out in the device files, then determines if the pin-counts match. Once completed, the net-list can be input to Allegro, and the net-list functions can be assigned to Allegro functions.

- NetIn / Assign

  A pre-4.0 Allegro procedure, this is currently used for 3rd party software and for compatibility with previous Allegro versions.

- GED2PCB (Ver 4.0 and up)

  Icon driven within Allegro, it prompts the user for the GED source directory and filenames, and the Allegro directory. It combines gallegro, dev_check, netin, and assign into one integrated command.

Component Placement:

Component placement is probably the most critical and time consuming aspect of designing a printed wiring board. Allegro has both manual and autoplace capabilities, with which components can be placed on top of the board, mirrored to the bottom, and can be rotated in 90 degree increments (future versions will have 1 degree rotation capability). Regardless of the method used, remember that these components will soon have to be routed. It is recommended that the user pause here and run "insight" in the autoroute etch section of Allegro. This will indicate the most probable grids to be used during the routing phase. Component placement which aligns with the via grid will generally yield the cleanest finished product.

All grids emanate from the design origin (0,0). The 'S' tooling hole of the board should be set to (0,0) *prior* to placement.

- Autoplace

  Contrary to its' name, autoplace is not a magic switch which, once flipped, will iterate component placement until perfection is achieved. Unfortunately, user intervention is required. First, a placement grid must be established. Components which are to be auto placed must be "tagged," and placement parameters must be established (i.e.- allowable rotations, preferences, and mirroring). A placement weight of zero should also be set for nets which will be on embedded planes. Since Autoplace bases its decisions on minimum net

lengths between components already placed and the next component to be considered, critical items such as connectors and large multi-pin devices should be manually pre-placed. Imbedded plane nets should also have a weight of zero applied so as not to affect the placement calculations. If "rooms" were setup in GED, corresponding placement rooms should be established.

Once all parameters have been established, autoplace can be executed, in either an automatic or interactive mode. In the interactive mode the system pauses after each component is placed, thereby allowing the operator to modify placement before proceeding to the next.

- Manual Placement

  As the name implies, this is a totally manual procedure. Components "snap" to the visual grid, and *not* to the autoplace grid which may have been previously established.

- Placement Evaluation

  The obvious placement evaluation is visual. This entails looking at both dense and very vacant areas, and possibly at the "rats-nest" display. It may be useful to execute function and pin swapping in an effort to minimize net lengths. This may also allow more efficient placement of some components. Another Allegro feature is Thermal Analysis of the placed board. This may highlight possible "hot spots" on the board which may, in turn, dictate modifications to placement.

  In any event, all components should be placed before attempting to route the board. Once a printed wiring board is even partially routed, adding or moving components, although possible, can become quite cumbersome.

Back-Annotate:

While this is a very simple process, the importance of this process cannot be overestimated. The process of placing components, performing pin and gate swapping, or reassigning reference designators, while not affecting the functionality of the design, can effect the net-list and, therefore, the schematic. This information must be relayed back to GED in order to ensure the schematic reflects the most current design state. Changes (ECO's) to an out-of-date schematic can wreak havoc on the entire printed wiring board process.

- Implementation

  1. Select the Back-annotate Icon. This creates the file "pstfnet.dat".
  2. Modify the "packager.cmd" file to process for back-annotation. Package to update the system design state files.
  3. In GED: "Backannotate pstback.dat" to update the schematic itself.

Back-annotation should be performed at the end of placement and reference designator modification sessions. It is also advisable to perform back-annotation after any manual routing sessions (because of the potential for modifying the pin and gate information), as well as at the completion of the printed wiring board design. If functional design changes need to be made at the schematic level, back-annotate to ensure the schematic is up to date, save the Allegro database, and **QUIT** until the new changes have been implemented. Further work in Allegro may cause the design to be out of sync. Once the schematic has been updated and re-packaged, the updated net-list can be read into Allegro, and the printed wiring board design can continue.

Routing the Board:

Routing a printed wiring board consists of converting the "rats-nest" lines, which display logical connections defined in the net-list, into the actual trace connections which will define the final printed wiring board. Once the routing parameters are established, routing is generally performed using a combination of manual and autoroute operations.

Preparation for Routing:

Verify the values for Design Rules Checks (DRC) and line widths, then run "insight" to set the routing grids and parameters. Allegro's autorouter operates by splitting the job into a maximum of six different phases. Each pass phase performs a specific function, briefly described below. Insight will invoke multiple executions of each pass, with different routing parameters between executions.

- PASS 0: Attach pin escapes to surface mount devices (vias for possible connections to other layers).
- PASS 1: Horizontal layer connections. No vias allowed.
- PASS 2: Vertical layer connections. No vias allowed.
- PASS 3 & 4: Like Pass 1 & 2. Pos/Neg diagonal routers. Usually not used.
- PASS 5: This is a full blown autorouter with the capability to rip up and retry, slide traces to make room, bubble traces around vias, etc. It will attempt to route traces using up to 12 layers simultaneously.

Temporarily modify padstacks of high density connectors so autoroute can succeed in those areas. Autorouter will not automatically neck down traces to route in dense areas.

Routing the Board:

Manually pre-route large non-imbedded plane traces. It is easier to find room later for smaller traces as opposed to large ones. Vias should be specified one size larger

than the trace being routed. For example, specify 62 mil vias for 50 mil traces. This will make inspection of the circuit masters much easier to accomplish.

If the design has surface mount devices, perform one execution of the Pass 5 router, allowing one via and limiting the trace length to 100 mills or so. This will connect all short nets, as well as connect surface-mount device (SMD) pads to the proper planes. If this is not done, Pass 0 will place a pin escape on each and every pin of all surface mount devices, even if adjacent pins are connected to the same net.

Invoke the Pass 0 router to add pin escapes to the remaining SMD pins. While some manual assistance may be required, it is important to make certain that all routable pins have pin escapes attached. This will help to ensure higher completion rates when routing the remainder of the board.

Re-enable Pass 1 through Pass 5 and execute, periodically examining the routing progress. A blocked area, which might be easily corrected manually, could cause some rather bizarre looking route patterns if left unchecked.

Clean-up:

Once the printed wiring board is 100% routed, there can still be a significant number of operations, both manual and automatic, to be performed. These procedures are required in order to prepare and/or improve the layout for manufacturing.

- Glossing

  The goal of the glossing routine is to improve the quality of the etch by attempting to re-route each net in order to achieve trace and via reductions. It will also try to perform line smoothing, centering lines between pads, etc. Because each pass through Glossing evaluates each net once, a minimum of two passes should be performed. This can be a very time intensive procedure, taking many hours; especially for very large and complex designs.

- Restore Pads

  Restore any modified pads back to their original size. This can cause a large number of DRC errors, but it is easy to manually neck down the traces to clean them up.

- Add Thermal Pads

  Allegro assumes the industry standard practice of flashing wagonwheel patterns for thermal pads. Sandia Laboratories, however, requires a 'C'-shaped pattern. These must be manually generated and positioned on the appropriate planes and through-hole pins. While the procedure is mundane and somewhat error prone, it is not overly cumbersome to implement. Several hundred can easily be placed in an hour or two. Missing a pad will

only affect the solderability and reworkability of that site; the connection will still be made to the plane.

Pre-Manufacturing:

None of the files required for manufacturing are created directly by Allegro, but the required information is tagged in Allegro with the use of forms. The actual files are generated at the UNIX level by routines which extract the forms-specified information from the Allegro database.

Manufacturing file generation and procedures:

- NCTAPE: (Standard Valid utility)
  Produces the ncdrill file according to the filename and parameters specified by the user in Allegro, with the drill information produced in order of increasing or decreasing size. This drill ordering, while format compatible, may have to be re-ordered to meet Sandia Laboratories' requirements.

- CORD_LST: (special utility, written in-house)
  This is an interim routine which generates a human-readable coordinate listing of the ncdrill information. This may be required by local printed wiring board manufacturing vendors if they are unable to read Sandia supplied distribution media (usually DOS compatible floppy disks).

- NCLIST: (special utility, under development in-house)
  This routine will supply a full ncdrill listing in the form required by the Nuclear Weapons Complex (NWC). This includes drill hole numbers, coordinates, drill sizes, and reference pad sizes. Once completed, it will also satisfy outside vendor requirements. See "SANMAN" for more information.

- ARTWORK: (standard Valid utility)
  Produces artwork files, one per layer, according to the filenames and parameters specified by the user within Allegro. These files are used to produce circuit masters in photo-plotting.

- COPPER: (special utility, written in-house)
  The "High Reliability Pattern Plating Process" is used at Sandia Laboratories for fabricating the etch patterns on printed wiring boards. This process selectively builds up the outside layer traces at the same time holes are being plated through. A calculation for the total amount of copper which will be plated is required. This calculation by the "copper" routine examines the artwork files for the top and bottom layer, and totals all the lines and dots to calculate the area. This routine assumes the standard apertures currently used by the NWC. Modifications to these standard apertures will invalidate the results of this calculation.

- INTEGRI: (special utility, written in-house)

  Automatic bare board testing at Sandia is implemented on the "Integri" 4500 Bare Board Tester. This system checks each component pad and via for every net for continuity, shorts, and opens to all other pads and vias on the board. If all nets are not accessible from the top side of the board, as is the case when surface-mount components are located on the bottom layer, separate test files are generated for both the top and bottom layers. The ASCII test files, which contain as a minimum the coordinates of each pad/via and netname node numbers, are extracted from the Allegro database. See "SANMAN" for future enhancements.

- SANMAN: (special utility, under development in-house)

  SANMAN, an acronym for **SAN**dia **MAN**ufacturing, will perform the generation of all the above manufacturing files with the execution of a single command. The need for this is twofold; first and foremost, it assures that all files are generated at the same point from the same data base, thereby avoiding possible out-of-date conflicts later on. Secondly, the NWC requires matching hole numbers to be assigned in the ncdrill listing and integri test files, as well as a hole number drawing. This information, which is not required by industry, must also be generated at the same time as the other files. SANMAN, as a single utility, will also perform some confirmation of the validity of the files generated, thus relieving the user of that responsibility.

Distribution:

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R. J. Detry, 8200
P. L. Mattern, 8300
P. E. Brewer, 8500
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8271 A. J. Hayes
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