

CONF-971147--

DESIGN AND PROCESSING OF VARIOUS CONFIGURATIONS OF SILICON  
PIXEL DETECTORS FOR HIGH IRRADIATION TOLERANCE UP TO  
 $6 \times 10^{14}$  n/cm<sup>2</sup> IN LHC APPLICATION\*

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\*Work supported in part by the U.S. Department of Energy: Contract No.  
DE-AC02-76CH00016.

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# Design and Processing of Various Configurations of Silicon Pixel Detectors for High Irradiation Tolerance up to $6 \times 10^{14} \text{ n/cm}^2$ in LHC Application\*

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**Abstract**-Various new configurations of silicon pixel detector have been designed and are in prototype production. The material selection and detector design are aimed to produce silicon detectors with radiation tolerance up to  $6 \times 10^{14} \text{ n/cm}^2$  (or  $4 \times 10^{14} \text{ } \pi/\text{cm}^2$ ) in LHC environment, which corresponds to a net increase (with long term anneal) of space charge of about  $4.2 \times 10^{13} \text{ cm}^{-3}$ . The configuration of  $\text{n}^+/\text{n}/\text{p}^+$ , with multi-guard-rings structure for high voltage (up to 300 volts) operation, has been used for the purpose to make the detector insensitive to space charge sign inversion. The material selection of medium resistivity (1.9k  $\Omega\text{-cm}$ ) n-type silicon has been made to try a new solution in extending detector lifetime: it should be the first step toward the use of low resistivity silicon, to prevent type inversion. The traditional configuration of  $\text{p}^+/\text{n}/\text{n}^+$ , with multi-guard-ring structure and n-type material, has also been used with the same layout, to get a comparison. It is shown as the fabrication of  $\text{n}^+/\text{n}/\text{p}^+$  pixel detectors requires eight mask steps, while just four mask steps are required for the  $\text{p}^+/\text{n}/\text{n}^+$  configuration.

## I. INTRODUCTION

Due to extremely high radiation level at LHC (up to  $6 \times 10^{14} \text{ n/cm}^2$ ), silicon detectors may be required to operate at very high biases (hundreds of volts) to obtain full depletion, or otherwise a partial depletion. These requirements demands new directions in detector design and material selections. There have been a number of recent papers in the literature dealing with non-irradiated high resistivity detectors operating at high biases using multi-guard-rings structures [1-3]. Our approach for solving the problem is carried out in multi-fronts [4].

In this paper, we present the design and fabrication of a  $\text{n}^+/\text{n}/\text{p}^+$  detector configuration insensitive to space charge sign inversion (SCSI). Multi-guard-rings structures are designed for high voltage (up to 300 volts) operation. Material characteristics, chosen to increase hardness, are:

a) medium resistivity (1.9k  $\Omega\text{-cm}$ ) n-type silicon wafers to

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\*Work supported in part by the US Dept. Of Energy: Contract No:DE-AC02-76CH00016.

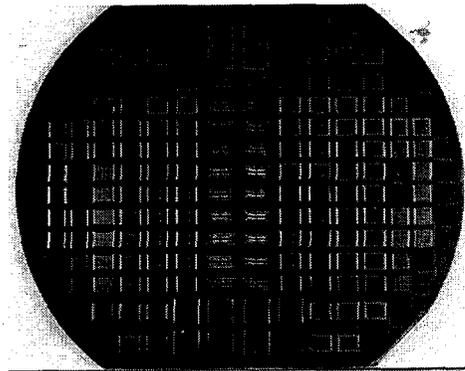


Fig. 1 Photograph of one of the wafers used for measurements (they have all the same layout). N-side is shown.

extend detector lifetime; it should be the first step toward the use of low resistivity silicon, to further delay type inversion. b) smaller wafers thickness (200  $\mu\text{m}$ ) to reduce full depletion voltages.

The traditional configuration of  $\text{p}^+/\text{n}/\text{n}^+$ , with multi-guard-ring structure and n-type material, has also been used with the same layout to get a comparison. The  $\text{p}^+/\text{n}/\text{n}^+$  configuration greatly simplifies the processing.

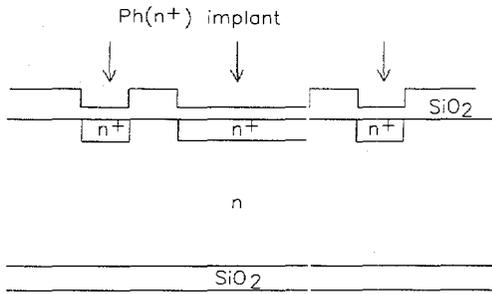
The second section presents briefly the design and fabrication of  $\text{n}^+/\text{n}/\text{p}^+$  and  $\text{p}^+/\text{n}/\text{n}^+$  configurations. The third section presents the testing results from fabricated devices and comparison to the simulation results.

## II. DESIGN AND FABRICATION

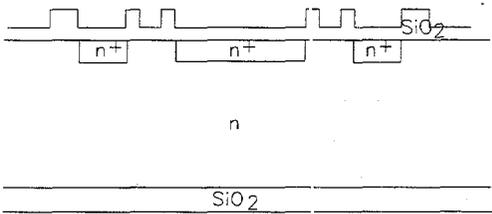
The design and material selection of the silicon pixel detectors have been aimed to produce devices with radiation tolerance up to  $6 \times 10^{14} \text{ n/cm}^2$  (or  $4 \times 10^{14} \text{ } \pi/\text{cm}^2$ ) in LHC environment, which corresponds to a net increase (with long term anneal) of space charge of about  $4.2 \times 10^{13} \text{ cm}^{-3}$ . Medium resistivity (1.9k  $\Omega\text{-cm}$ ) n-type silicon wafers, with 4 inch in diameter and 200 to 250  $\mu\text{m}$  in thickness, have been used to produce  $\text{n}^+/\text{n}/\text{p}^+$  pixel detectors. The  $\text{p}^+/\text{n}/\text{n}^+$  pixel detectors configuration has also been made using medium and high resistivity (4-6k  $\Omega\text{-cm}$ ) n-type silicon wafers with 4 inch in diameter, their thickness are 250  $\mu\text{m}$  and 400  $\mu\text{m}$  respectively.

Processing Steps for the n+/n/p+ Pixel Detectors

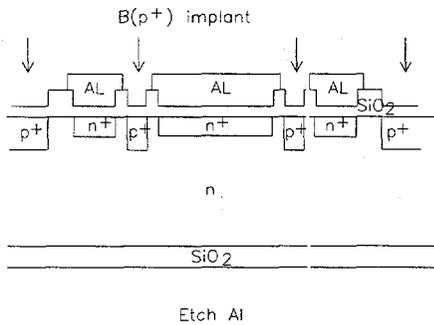
1) Oxide-cut for n+ pixels and GR's



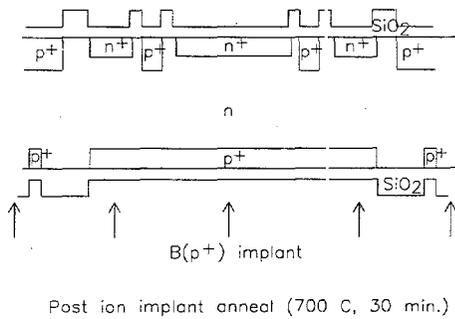
2) Oxide-cut for p+ ch-stopper



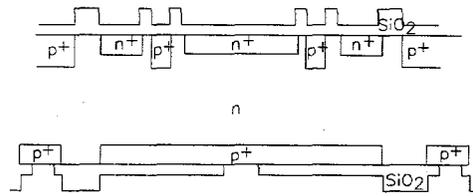
3) Al-cover for n+ pixels and GR's



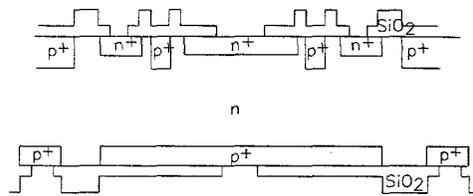
4) Oxide-cut for the back side p+ contact and GR's



5) Oxide step cut for back-side p+ contacts and GR's

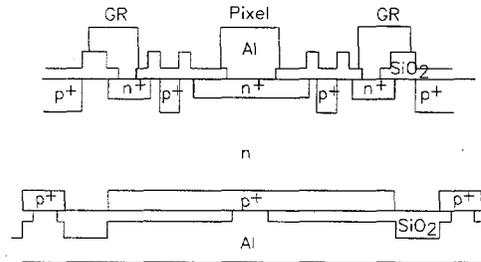


6) Oxide step cut for front-side n+ pixels and GR's



Deposit Al on both sides

7) Al-cut on the front side



8) Al-cut on the back side

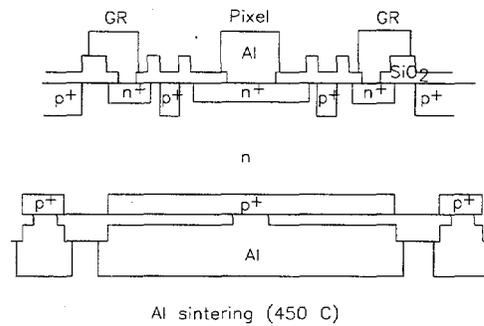


Fig. 2. Processing steps for n+/n/p+ pixel detectors.

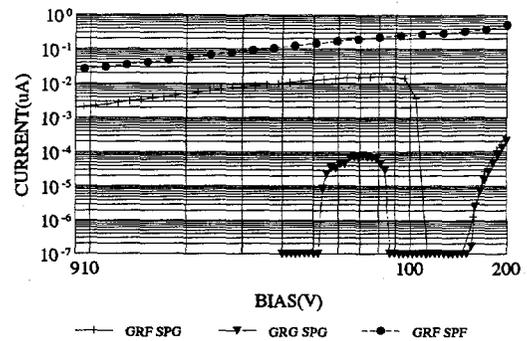
Fig. 1 presents a photograph of the n-side of a wafer with n<sup>+</sup>/n/p<sup>+</sup> pixel detectors design. Fig. 2 shows the processing flow chart of the n<sup>+</sup>/n/p<sup>+</sup> pixel detectors, which requires as many as eight mask steps. Since the rectifying junction in an n<sup>+</sup>/n/p<sup>+</sup> pixel detector is on the back side (p<sup>+</sup>-side) before irradiation, care has to be taken to protect the junction near the cutting edges by introducing multi-guard-rings structure surrounding p-junction on the back side as well. This requirement makes the fabrication of an n<sup>+</sup>/n/p<sup>+</sup> pixel detector a two-side process. The device works as long as n<sup>+</sup> pixels are isolated by space charge region; oxide positive charges can induce electrons near the surface, so p<sup>+</sup> channel stopper implants (step 3) are necessary to ensure the isolation. Before irradiation the junction is on the p-side, and a full depletion of n-bulk is required to separate n<sup>+</sup> pixels. After being irradiated beyond SCSI, the junction would shift to the pixel side (n<sup>+</sup>-side), and the detector should still work with relatively high charge collection efficiency (can be higher than 70%) as long as it is biased at full depletion. Even after high fluence of irradiation (> 2x10<sup>14</sup> n/cm<sup>-2</sup>), when the detector is no longer fully depleted by a bias of 300 volts, the device may still be good with substantial charge collection efficiency (CCE) working at partial depletion mode.

The processing of p<sup>+</sup>/n/n<sup>+</sup> detectors is much simpler since it does not require a channel stopper implant and is a one-side process. It requires as few as four mask steps.

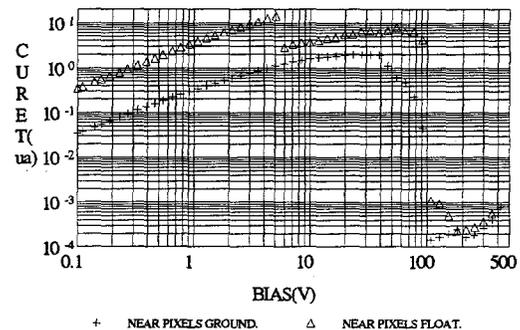
Various pixel detectors with n<sup>+</sup>/n/p<sup>+</sup> and p<sup>+</sup>/n/n<sup>+</sup> configurations have been fabricated in Brookhaven National Laboratory, Instrumentation division.

### III. RESULTS AND DISCUSSION

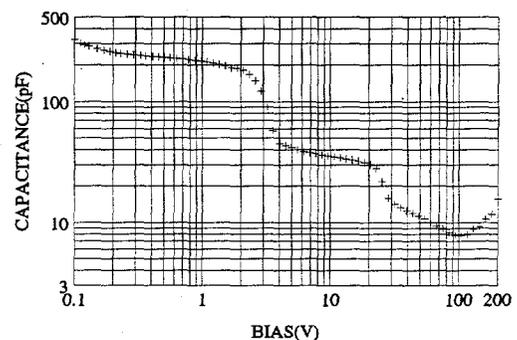
Fig. 3 shows testing results of an n<sup>+</sup>/n/p<sup>+</sup> detector using a probe station. In Fig. 3a), several I-V characteristics, measured with different guard ring connections, are presented. Here electric current flowing through a single pixel is detected. It is observed that pinch off effect arise around the depletion voltage (90V), if guard-ring or surrounding eight pixels are grounded. Currents lower than 10<sup>-7</sup> μA cannot be distinguished from noise. Fig. 3b) shows the I-V characteristic of another single pixel, with inner guard ring grounded; surrounding 8 pixels are floating and grounded respectively. In this case the sample presents a higher leakage current, but no breakdown takes place up to 500V. Pinch off at full depletion is also observed. Fig. 3c) shows the C-V characteristic of the same structure. For very low voltages (bias < 0.3V) the main contribution to capacitance is due to the junction capacitance. Up to 20V the Al-SiO<sub>2</sub>-Si MOS capacitance becomes dominant, where a flatband age of about 3 volts is observed. With increasing bias, the Al-SiO<sub>2</sub>-Si MOS capacitance contribution ceases, probably because surface charge are removed by the field, which is



a) Several I-V characteristics of same single pixel device with different set up. GRF(G) means "guard ring floating (grounded)", while SPF(G) means "surround eight pixels floating (ground)"



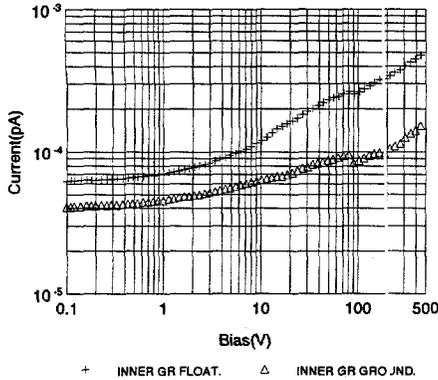
b) I-V characteristic of single pixel device with inner guard ring grounded. Pinch off occur at full depletion (90V).



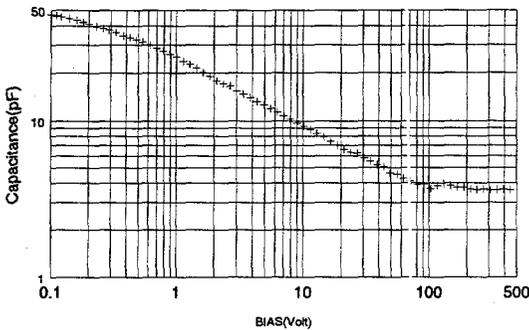
c) C-V characteristic of test structure with all guard rings floating. Flat band voltage is about 3V. Depletion occur at 90V.

Fig. 3. Probe station test results of n<sup>+</sup>/n/p<sup>+</sup> configuration with medium resistivity material.

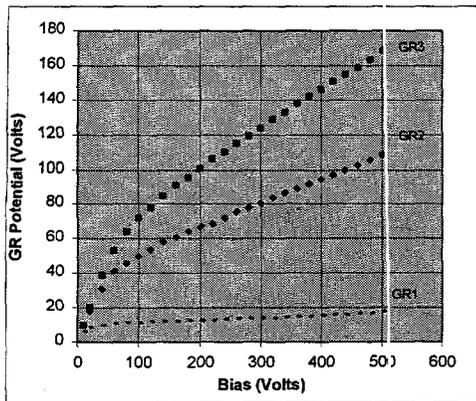
increased at large depletion; so the junction capacitance dominates again. The bulk is fully depleted at 90V, where the capacitance reaches its geometrical value. At higher voltages the capacitance increase is due to rising leakage current. Since the n<sup>+</sup>/n/p<sup>+</sup> pixel configuration is designed to be insensitive to SCSI, further radiation tests using high fluence of neutrons and pions are planned to verify the design considerations and simulation results. Here we can further look at the results of p<sup>+</sup>/n/n<sup>+</sup> pixel configuration



a) I-V characteristics with inner guard ring floating or grounded. No breakdown is observed up to 500V.



b) C-V characteristic with all guard rings floating. The bulk full depletion is about 90V.



c) Guard rings potential versus bias. Label GR1 corresponds to the inner guard ring, GR3 to the outer one.

Fig. 4. Probe station testing results of  $p^+/n/n^+$  configuration with high resistivity material.

operated at high reverse biases and compare them with simulation results.

Fig. 4 shows the probe station testing results of a  $p^+/n/n^+$  detector made of high resistivity silicon. Active area and thickness are respectively  $A=0.25\text{cm}^2$  and  $W=400\mu\text{m}$ .

This detector is a three guard-ring test structure with a single boron implant to define the  $p^+$  area that have the same size of a whole pixel array detector (about  $0.15$  to  $0.16\text{cm}^2$ ). Fig. 4a) is the I-V characteristic of the detector with the inner guard ring floating or grounded. No breakdown is observed up to 500V. Fig. 4b) is the C-V characteristic of the same device with all guard rings floating. The full depletion of the detector is reached at 90V, and bulk current corresponds to a generation lifetime of  $\tau_g=80\text{ms}$ . In Fig. 4c) the guard ring potential versus biases is presented. Note that positive bias was applied to the  $n^+$  -side, which made potential of the detector's  $p^+$  contact at zero. It is clear that the potential is nicely stepped "down" (from 0 to a potential close to the bias applied on the  $n^+$  side) through the three guard rings. At high biases though, the potential difference between the third guard ring and the  $n^+$  contact becomes larger and larger. This result indicates that more guard rings may be needed for better potential distributions and therefore better breakdown protection.

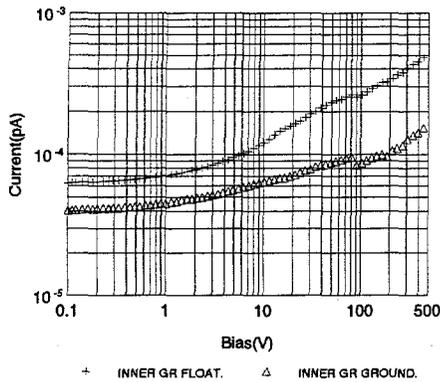
Fig. 5 Shows the testing results of a  $p^+/n/n^+$  detector similar to the previous one except it has seven guard-rings and is made of medium resistivity silicon. Active area is  $A=0.25\text{cm}^2$  and thickness is  $W=240\mu\text{m}$

Fig. 5a) shows the I-V characteristics, 5b) is the C-V characteristics, and 5c) represents the guard-ring potentials versus bias. Measurements with inner guard ring floating and grounded are presented in both cases. No breakdown is observed up to 500V, the bulk full depletion is reached at 70V, and the bulk current corresponds to a generation lifetime of  $\tau_g=48\text{ms}$ . It is obvious that the potential distribution is much better as compared to that of a three-guard ring detector.

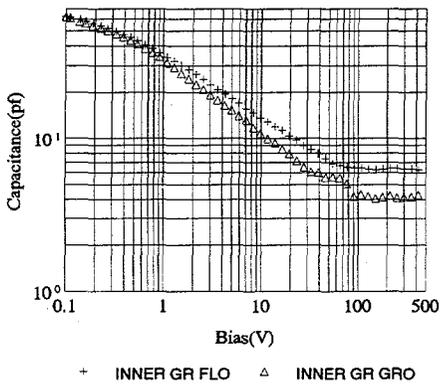
Numerical simulations of the potential distribution of a detector with 7 guard rings have been carried out, and the resulting guard-rings potential versus bias plot has been shown in Fig. 6. In order to obtain a better agreement with experimental data, which has shown the inner guard-ring having a very low potential, the inner guard ring was set to zero potential in the simulation. Although there are some differences between the data (Fig 5c)) and simulation, the potential distributions are similar.

#### IV-SUMMARY

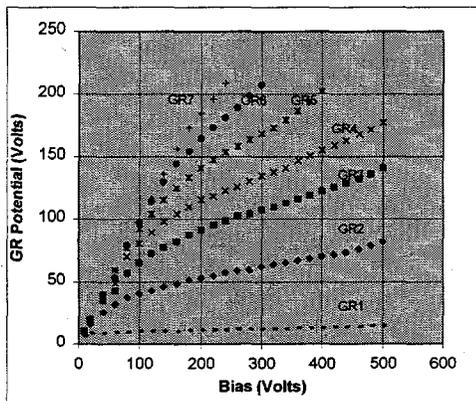
Experimental results for traditional  $p^+/n/n^+$  structure are really satisfactory. Extremely low leakage current have been achieved and no breakdown up to a bias of 500V has been observed, indicating that the multi-guard-ring design is working. Low bulk leakage current as processed  $n^+/n/p^+$



a) I-V characteristic with inner guard ring floating or grounded. No breakdown is observed up to 500V.



b) C-V characteristic with inner guard ring floating or grounded. The bulk full depletion is about 70V.



c) Guard rings potential versus applied bias. Labile GR1 refers to inner guard ring, GR7 to the outer one.

Fig. 5. Probe Station testing results of p<sup>+</sup>/n/n<sup>+</sup> configuration with medium resistivity material.

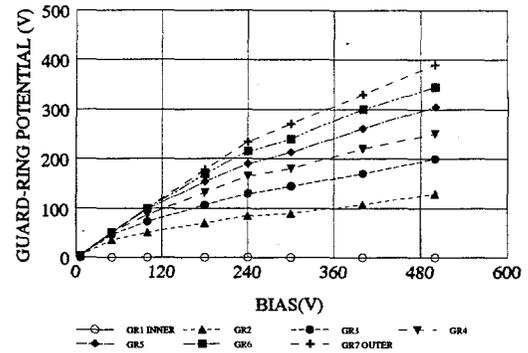


Fig. 6. Simulated guard ring potential versus bias for a 7 guard-rings p<sup>+</sup>/n/n<sup>+</sup> test structure. Inner guard ring is set at zero potential.

detectors is also achieved, although lower breakdown voltages have been observed. This effect may be caused by the breakdown of the junction of the p<sup>+</sup> channel stopper and the n bulk. This breakdown, however may disappear after the detector is irradiated beyond SCSI. Since the n<sup>+</sup>/n/p<sup>+</sup> structure is designed to operate beyond SCSI and an initial operation bias of 200-300 volts for as processed n<sup>+</sup>/n/p<sup>+</sup> detectors can be produced in current design, we can declare that the design and processing is a success.

It has been demonstrated that good n<sup>+</sup>/n/p<sup>+</sup> detectors can be made on medium resistivity silicon. The next step is to push for low resistivity p<sup>+</sup>/n/n<sup>+</sup> as well as n<sup>+</sup>/n/p<sup>+</sup> detectors for extended life time and radiation hardness[4].

Some design modifications are underway to improve the breakdown voltage for n<sup>+</sup>/n/p<sup>+</sup> detector. Neutron irradiation up to 1x10<sup>15</sup> n/cm<sup>2</sup> for n<sup>+</sup>/n/p<sup>+</sup> detectors has been carried out recently and measurement results of those irradiated detectors will be reported in a late paper.

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