SAND77-1145

UNLIMITED RELEASE
PRINTED FEBRUARY 1978

ACTIVE DEVICES FOR HIGH TEMPERATURE MICROCIRCUITRY

D. W. PALMER, B. L. DRAPER,*
J. D. MCBRAYER, K. R. WHITE

NOTICE
This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Department of Energy, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

ABSTRACT

As part of a program to develop high temperature electronics for geothermal well instrumentation, a number of solid state diode and transistor types have been characterized from room temperature to 300°C. The temperature dependence and aging stability of transport and leakage properties were measured. Included in the study were silicon diodes, bipolar transistors, JFETs, MOSFETs, and GaAs MESFETs and JFETs. In summary the results are: diodes and bipolar transistors became extremely leaky at high temperature and are therefore of limited use; silicon MOSFETs and GaAs devices showed unacceptable aging instabilities at high temperatures; silicon JFETs from certain manufacturers were sufficiently stable and had suitable temperature dependent characteristics so that operational circuits could be made.

Comparisons were made of experimental device characteristics and those predicted by theory. The theoretical calculations were done using standard equations revised to include appropriate temperature dependent parameters. Close agreement between theory and experiment was found, indicating that unexpected high temperature effects were insignificant.

In order to facilitate the use of devices in high temperature hybrids, it was necessary to develop bonding and prescreening techniques. A large variance of JFET 300°C operating parameters was found even within a single production lot. Consequently, high temperature prescreening allowed each circuit to be specifically "pretuned." Standard solder, epoxy, and chip and wire attachment technologies were not functional at 300°C. Gold-germanium solder, aluminum wire to DuPont 9910 gold film, and diffusion barrier pads were developed to allow high temperature attachment.

*Currently a graduate student at Princeton.

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

Table of Contents

	Page
Introduction	3
Chapter 1 - MOSFETs	8
Chapter 2 - Junction Field Effect Transistors	41
Chapter 3 - Bipolar Devices	61
Chapter 4 - GaAs Field Effect Devices	70
Chapter 5 - Bonding	88
Chapter 6 - Prescreening Active Devices	98
Conclusion	102
Appendix	103
References	113

ACTIVE DEVICES FOR HIGH TEMPERATURE MICROCIRCUITRY

INTRODUCTION

This report on active devices is the second in a series of four Sandia Laboratory reports concerning high temperature microelectronics. The need for high temperature geothermal electronics has become more immediate and well defined since this work began after the first geothermal logging workshop in 1975.[1] Two distinct modes of instrumentation requirements are now apparent. First, periodic logging of uncased exploratory wells during drilling, and secondly the long term monitoring of cased production wells. The first utilization requires mechanically rugged, small volume electronics capable of repeated 5-hour measurements up to 300°C. The second mode demands continuous, low drift electronics operating at maximum temperature for 100-1000 hours. All the active devices, bonding methods, and prescreening procedures tested in this study were chosen and analyzed with these performance criteria in mind.

In addition to these performance specifications, the further restriction of only incorporating commercial parts and technology in these high temperature electronics was imposed. This approach guarantees that such microcircuitry can be straightforwardly adopted by logging service companies and circuit fabrication houses.

From the time of the first report on passive components[4] at high temperature in December 1976, many additional materials and parts have been found acceptable for geothermal circuitry use. This inventory expansion has somewhat simplified high temperature circuit design and fabrication. To date several logging tools have been fabricated using both hybrid and printed circuit board technology. These circuits have performed for hundreds of hours at high temperatures in ovens and geothermal wells.

Scope of Study

This study is not intended to be the only word on high temperature active devices. In particular, only solid state silicon and gallium arsenide devices are described. At the beginning of this research, commercial General Electric miniature ceramic vacuum tubes were studied with great success up to 500°C, and the progress of Los Alamos Labs[3] with integrated thermionic devices was followed closely. In addition, literature searches revealed many experimental large band gap

semiconductor devices had been fabricated using SiC, GaP, InP, and diamond crystals.

Commercial ceramic tubes were not pursued at Sandia because of their basic incompatibility with the low voltage microcircuitry which was deemed possible. Tubes, although miniaturized, are still at least a cubic centimeter in volume, plate voltages range from 75 to 300 volts, filament power is necessary, and unit cost is high. All this is not to say that ceramic tubes cannot be used in high temperature circuitry. In fact, a parallel effort fabricating geothermal circuits using such tubes is supported by DOE.[30]

As an improvement over ceramic tubes, integrated thermionic devices promise the necessary small size and packing density for microcircuitry but are not yet commercially available. Development of this technology is proceeding rapidly at Los Alamos Laboratories, but was not judged a mature enough technology to commit to Sandia's circuitry in 1976.

The many experimental studies with large band gap semiconductors can only be viewed as future promise for high temperature circuitry. Even if such test devices could be replicated within Sandia on a time scale to benefit the current geothermal exploration, they could not become commercially available for many years.

There is a trend in logging electronics to increase the complexity of the circuitry and to mount several measurement circuits with one housing. To accommodate this complexity and multiplicity of circuits it becomes necessary to miniaturize the circuitry. Two approaches are currently apparent in industry: integrated chips have replaced discrete transistors, and hybrid circuits have replaced printed circuit boards. Aware of this trend, high temperature tests were performed on small scale integrated circuits. In general these integrated circuits failed above about 200°C. Sometimes this failure was due to some particular device on the chip that was not designed to allow high temperature operation, but generally the junction isolation, which is intended to prevent devices from directly affecting one another, became ineffective above 200°C. As a consequence, this study dwells on discrete devices only. Two facts allow hope of high density microcircuitry. First, with hybrid technology it is possible to form circuits with transistor chips at 50 mil centers, a sufficient device density for most circuitry. Secondly, preliminary tests of integrated circuits with dielectric isolation show promise of 300°C operation. However, presently dielectrically isolated integrated circuits are not commercially common.

A considerable part of this report deals with device bonding and qualification. As this research proceeded it was found that a prominent high temperature failure mode for commercially packaged devices was bonding related. In addition, as Sandia's first high temperature circuits were manufactured, yield and lifetime were vastly improved with increased high temperature prescreening of the devices. It is not enough to only know which device types function at high temperature, the chip bonding and sorting are equally important insurance.

A considerable percentage of this report involves computer modelling of devices. Our original interest in this modelling was to guarantee the experimentally measured high temperature characteristics were indeed predictable from straightforward device physics and were not instead due to some peculiarity of fabrication. It also became clear that these computer models allowed device redesign for improved high temperature performance. A basic tutorial approach is taken in several chapters to clearly point out the assumptions placed in the models. In this way future researchers will be better able to amend these programs to their needs. If interest in microcircuitry in the 250 to 325°C range continues to grow, then redesign of existing devices will become advantageous and commercially practical.

This study gave equal emphasis to device types that failed to function usefully at high temperature (Si bipolars, GaAs MESFETs) as to devices that showed satisfactory high temperature performance (Si JFETs and MOSFETs). Although such a report format may slow down the engineer looking simply for the list of "good" devices, at this early stage in evaluation it does not seem prudent to categorically brush away device types. It is hoped by detailing all the results, other researchers with different circuit requirements or access to devices of different geometry or doping profile will find some benefit from this report.

Anticipated Device Limitations

There are at least two categories of failure for high temperature operation. The most obvious is destruction, that is, the device melts or irreversibly degrades after a short time at an elevated temperature. The second category is nonfunctionality, that is, at high temperatures the device no longer supplies its function (rectify or amplify), even though upon cooling the device resumes normal operation. High temperature solid state diffusion provides the main mechanism for irreversible failure. Increased generation of current carriers at high temperatures is the basis for most device functional failures.

Since solid state devices consist of bulk semiconductors with discrete patterned layers of metal and oxides, plus well defined regions of carefully diffused impurities, it is possible that high temperature operation will cause further bulk diffusion or surface migration resulting in degradation and eventual failure. It is the rate of such degradation processes at 300°C that is important. Four diffusion related problems will be listed here along with their general impact on this study. (1) In manufacture many doping diffusion steps take place for about 1 hour at 1000°C.[2] During this controlled diffusion the induced impurities typically penetrate the silicon for several microns. To achieve a diffusion length equal to this at 300°C for Al, B, and Sb in silicon would require more than 10^8 hours of aging. Thus, a dopant redistribution process provides no problem to high temperature operation. (2) A more formidable threat exists from gold diffusion from the back of the silicon die. With 400°C die down temperature and 300°C operation the gold backing begins to reach the front surface within a few hundred hours.[2] Although the solubility of gold in standardly doped silicon is low at 300°C ($<10^{11}$ cm^{-3}), there is still an opportunity for concentration at the surface, interfaces, and at defects. Some of the irreversible changes in conductivity and leakage seen during this study are tentatively assigned to gold diffusion. (3) Surface migration constants are not as predictable as bulk diffusion constants. Post-failure visual inspection of GaAs devices showed surface migration of metal electrodes became a problem above 250°C. In addition, the electrical properties of silicon MOSFET at times demonstrated drifts symptomatic of mobile ions crossing the gate oxide. (4) Conventional wire bonding of silicon die involves an aluminum wire attached to the gold metallization of the substrate or package. Upon 300°C aging such a gold-aluminum interface can cause weak, highly resistive bonds.

Functional failure due to high temperature can also occur. For example, one fundamental limitation occurs when the semiconductor becomes intrinsic, that is, when the thermally generated carrier density exceeds the impurity doping carrier density. Not all active regions of a device must remain extrinsic in order for the device to function; for example, if only one side of a diode becomes intrinsic, rectification can still occur. Nonetheless, at some temperature, no matter how heavy the doping, the device becomes intrinsic, behaving as a resistor. For most commercial silicon devices this occurs at less than 350°C, whereas for GaAs this limit is around 500°C. Chapter 4

deals with this ultimate limitation analytically. Even before this intrinsic transition is reached the device can cease practical operation due to the increase of thermally generated carriers.

Report Outline

Active devices were looked at from 25 to 300°C primarily to find operational bias ranges which had small changes with temperature (zero temperature coefficient regions). Aging tests under bias were performed for 1000 hours at 275 or 300°C with periodic monitoring of characteristics.

Chapter 1 will discuss silicon metal-oxide-semiconductor field effect transistors (MOSFETs), computer model, and oven test results. Chapter 2 contains similar information on silicon junction field effect transistors (JFETs).

Chapter 3 has a discussion on bipolar silicon devices and their shortcomings. Chapter 4 consists of the theoretical expectations and results of tests on commercial GaAs devices. New bonding techniques for active devices are enumerated in Chapter 5. Methods for high temperature pretesting of devices follow in Chapter 6. The computer models are in the Appendix. A short conclusion ends this report.

CHAPTER 1 - MOSFETs

INTRODUCTION

The high temperature functionality of the silicon metal-oxide-semiconductor field effect transistor (MOSFET) was ascertained early in this program by several simple oven tests. The immediate question then became, can MOSFETs be fabricated which are less temperature variable. To answer this question a computer model of a MOSFET was assembled using the standard device physics equations with all temperature dependent terms. This model was then used to confirm that indeed the experimental devices were behaving according to standard theory and not being deviated by some manufacturing peculiarity which was not intended for high temperature operation. Next, this model was used to redesign MOSFET geometry and doping profile in an attempt to temperature stabilize chosen device characteristics.

In this chapter the computer model for an n-channel MOS transistor will be presented first, itemizing the temperature dependence of all parameters. Next, several examples of computer runs are compared with observed transistor characteristics at high temperatures. With few exceptions this NMOS model was adapted to p-channel MOS structures by changing the signs of the terminal voltages and currents. The differences between expected n- and p-channel MOS transistor performance will also be discussed. Lastly, results of high temperature aging tests will be presented.

COMPUTER MODEL

N-Channel MOS Transistor

A simplified view of a typical NMOS transistor is shown in Figure 1.

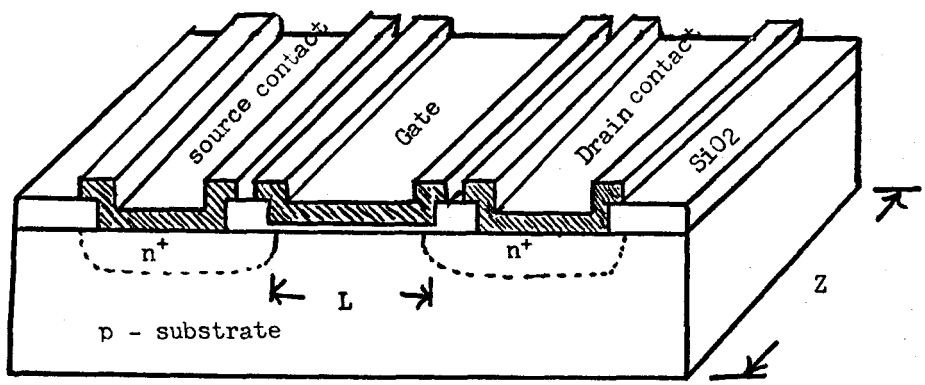


Fig. 1. Schematic of n-channel metal-oxide-semiconductor transistor. Conductivity of the region under gate oxide, the channel, is effected by voltage applied to gate.

If a sufficiently large voltage is applied to the gate, the underlying surface of the p-type silicon substrate will be inverted to form an n-type channel between the diffused source and drain regions (see Fig. 2). The resistance of the channel is inversely proportional to Q_n, the mobile charge density in the inversion layer, the magnitude of which depends on the field at the silicon surface. Hence, the resistance of the channel varies inversely with the potential difference between the gate and the silicon surface.

If the drain voltage is increased from zero to some positive voltage, for a fixed gate voltage, the channel resistance will increase due to a decrease in Q_n brought about by a decrease in the average gate-to-surface potential. If the drain voltage is raised to a sufficiently high value, the surface field near the drain will not be adequate to support an inversion layer--the channel will then disappear at that end. The voltage at which this occurs is called V_{DSAT}, the <u>saturation</u> voltage. As the drain voltage is increased still further, the point which marks the end of the inversion layer will move slightly toward the source but the potential at that point will remain constant. This also means that the current will remain essentially constant for voltages greater than V_{DSAT} since it depends on the potential drop across the channel. The drain characteristics of a typical n-channel MOS device are shown in Figure 3. The two regions--linear and saturation--are easily distinguished.

The current-voltage characteristics presented in standard semiconductor device texts[5,6] form the basis of much of the model

$$I_D = \frac{z}{L}\mu_n C_i \left\{ \left(V_G' - 2\psi_B - \frac{V_{DS}}{2} \right) V_{DS} - \frac{2\sqrt{2\varepsilon_s q N_A}}{3C_i} \left[(V_{DS} + 2\psi_B)^{3/2} - (2\psi_B)^{3/2} \right] \right\}$$

valid for

$V_G' \geq V_T$, the turn-on voltage,

$V_{DS} \leq V_{DSAT}$, the drain saturation voltage.

N_A is the acceptor concentration in the substrate, ψ_B is the bulk (substrate) Fermi potential, μ_n is the electron mobility in the channel, C_i is the capacitance per unit area ($C_i = \varepsilon_{ox}/x_d$ where ε_{ox} is the oxide permittivity, and x_d is the oxide thickness), ε_s is the semiconductor

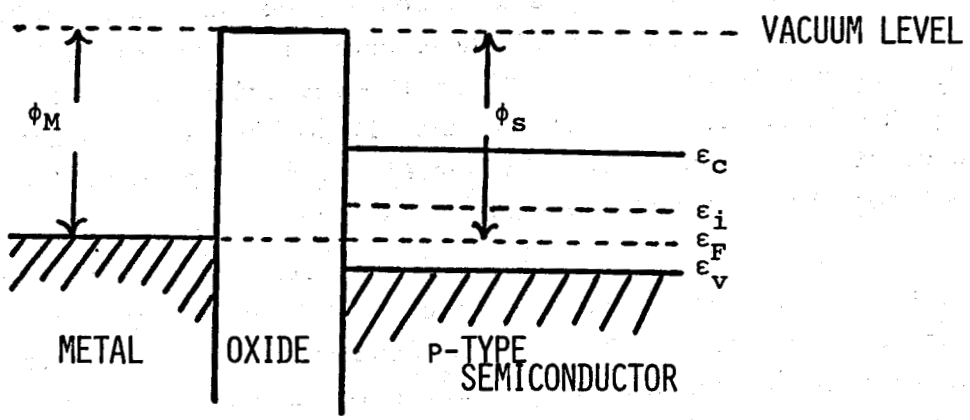


FIG. 2A. IDEAL MOS BAND STRUCTURE. NO BIAS APPLIED. (ϕ_{MS} = 0, NO OXIDE CHARGE, NO SURFACE STATE CHARGE)

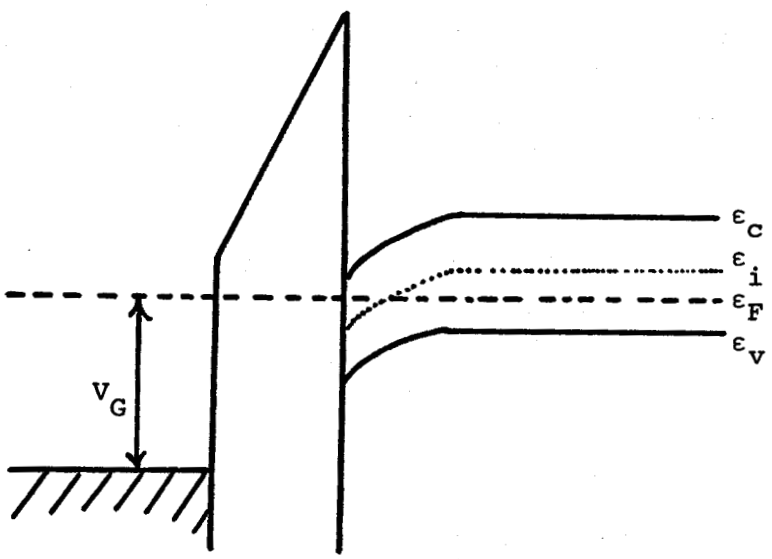


FIG. 2B. IDEAL MOS BAND STRUCTURE WITH LARGE POSITIVE BIAS, V_G, APPLIED TO THE METAL GATE. THE ENERGY BANDS IN THE SILICON ARE BENT DOWNWARD ENOUGH THAT THE INTRINSIC LEVEL, ε_i, IS BELOW THE FERMI LEVEL, ε_F, AT THE SEMICONDUCTOR SURFACE. HENCE, THE NUMBER OF ELECTRONS IS LARGER THAN THE NUMBER OF HOLES (THE MAJORITY CARRIERS) AT THE SURFACE. THIS CONDITION IS CALLED INVERSION.

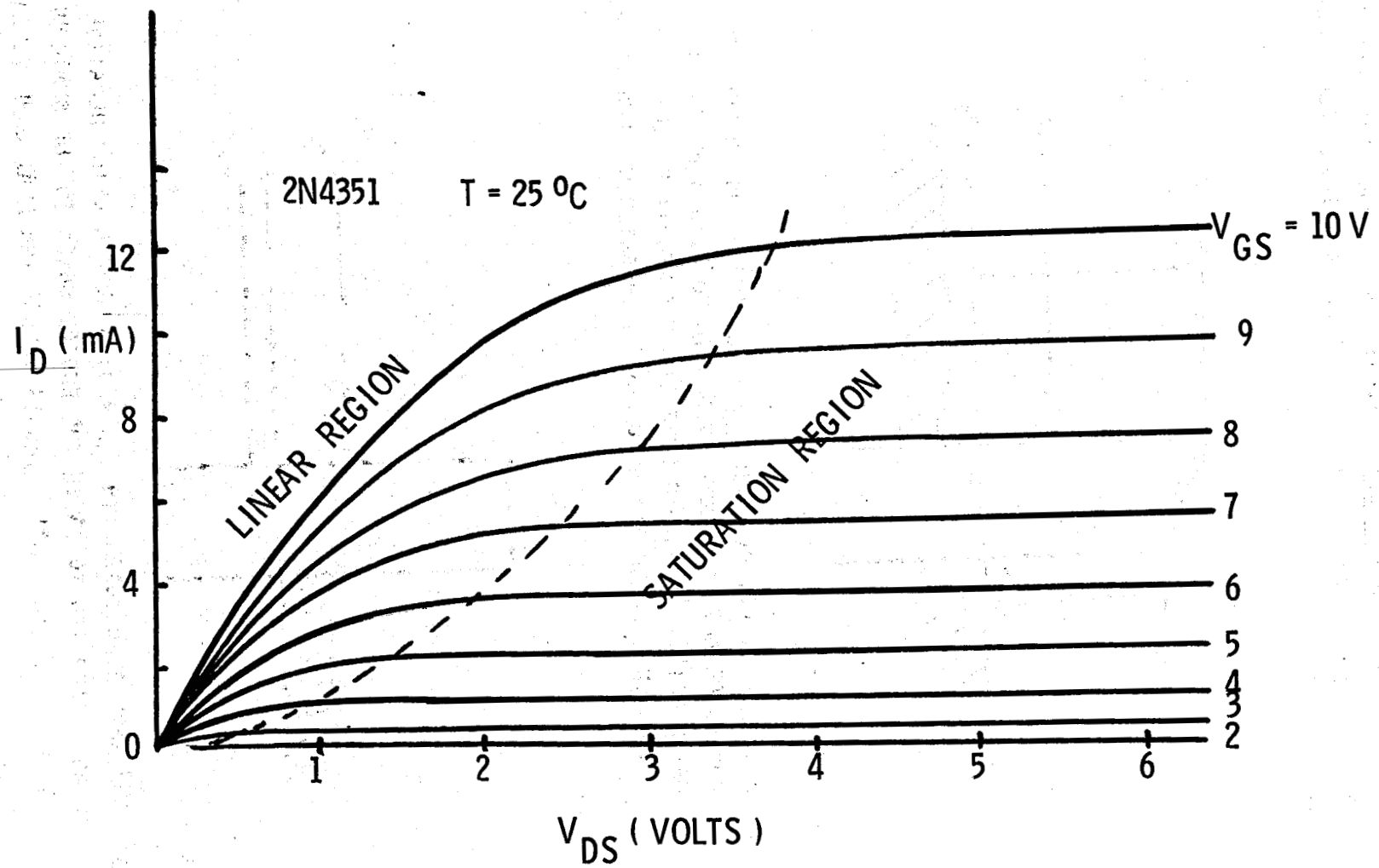


Fig. 3. Typical drain characteristics of an enhancement mode MOSFET. Two operational modes exist: the linear region with drain current increasing with the drain-source voltage, and the saturation region with constant drain current.

permittivity, and q is the electronic charge. V_G', the <u>effective</u> gate voltage, is equal to the <u>terminal</u> voltage minus the flat-band voltage of the MOS structure, $V_G' = V_G - V_{FB}$. Figure 4 illustrates flat-band voltage.

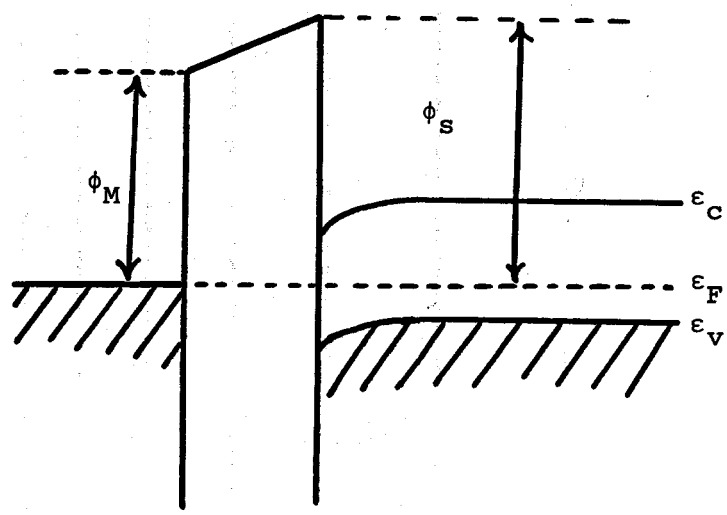


FIG. 4A. MOS BAND STRUCTURE WITH $\phi_{MS} < 0$. THE BANDS IN THE SEMICONDUCTOR ARE BENT DOWN EVEN WITH NO BIAS APPLIED TO THE METAL GATE. IF ϕ_{MS} IS SUFFICIENTLY NEGATIVE, THE SEMICONDUCTOR SURFACE MAY ACTUALLY BE INVERTED WITH NO GATE BIAS.

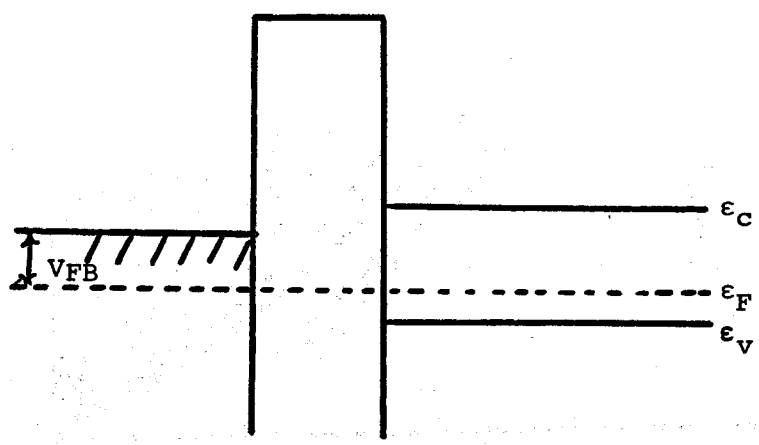


FIG. 4B. MOS BAND STRUCTURE WITH $\phi_{MS} < 0$; A SUFFICIENTLY NEGATIVE GATE BIAS IS APPLIED TO CAUSE THE ENERGY BANDS IN THE SEMICONDUCTOR TO BE <u>FLAT</u>. THIS GATE BIAS IS CALLED THE <u>FLAT BAND VOLTAGE</u>, V_{FB}.

Turn-On Voltage

The turn-on voltage, V_T, is the effective gate voltage needed to invert the p-type material below the gate oxide and therefore create a conducting channel between the drain and source regions:

$$V_T = 2\psi_B + \frac{2\sqrt{\varepsilon_s q N_A \psi_B}}{C_i} .$$

Obviously, this parameter relates to the effective gate voltage described above. The threshold voltage for the terminal gate voltage is $V_{T_{term}} = V_T + V_{FB}$.

Bulk Fermi Potential

A simplified band diagram of the p-type substrate is shown below.

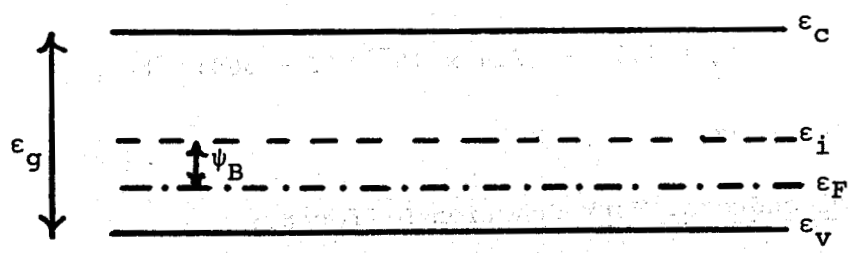


Fig. 5. The energy gap ε_g, fermi level ε_F, and fermi potential ψ_B.

The bulk Fermi potential, ψ_B, is given by the expression

$$\psi_B = \frac{KT}{q} \ln\left\{\frac{N_A + \sqrt{N_A^2 + 4n_i^2}}{2n_i}\right\},$$

where n_i is the intrinsic carrier concentration:

$$n_i = \sqrt{N_c N_v}\, e^{-\varepsilon_g/2KT} .$$

In silicon the effective densities of states in the conduction and valence bands are given by

$$N_c = 12\left[\frac{2\pi m_r^* KT}{h^2}\right]^{3/2} \quad \text{and} \quad N_v = 2\left[\frac{2\pi m_p^* KT}{h^2}\right]^{3/2} .$$

The density-of-states effective masses for holes and electrons are $m_p^* = 0.58\ m_o$ and $m_n^* = 1.06\ m_o$, where m_o is the electron rest mass.[2] A graph of n_i vs. temperature is given elsewhere in this paper.

The bulk Fermi potential vs. temperature is plotted in Figure 6 for several values of substrate doping. It is evident that as the temperature increases the Fermi level moves toward the middle of the band gap, causing a decrease in ψ_B and, hence, V_T.

Band Gap

In the temperature range of interest the band gap of silicon is, with reasonable accuracy, given by

$$\varepsilon_g = 1.12 - (2.4 \times 10^{-4})(T - 300) \quad [\text{eV}] ,$$

where T is in °K.

Metal-Semiconductor Work Function Difference

The metal-semiconductor work function difference is important in determining the flat-band voltage and, therefore, affects the turn-on voltage of the transistor. Given in Figure 7 is a band diagram of p-type silicon showing the work function, ϕ_s, and its various constituent energy differences. The metal-semiconductor work function difference is simply given by $\phi_{MS} = \phi_M - \phi_S$. If ϕ_{MS} is specified at some temperature--usually 300 K for convenience--then $\phi_{MS}(T)$ can be found:

$$\phi_M - \chi = [\phi_{MS} + (\varepsilon_c - \varepsilon_i) + \psi_B]\Big|_{T=300°K}$$

so that

$$\phi_{MS}(T) = (\phi_M - \chi)\Big|_{T=300°K} - \frac{KT}{q}\,\ln\left(\frac{N_c}{n_i}\right) - \psi_B(T) ,$$

assuming that $\phi_M - \chi$ is essentially independent of temperature over the range of interest.

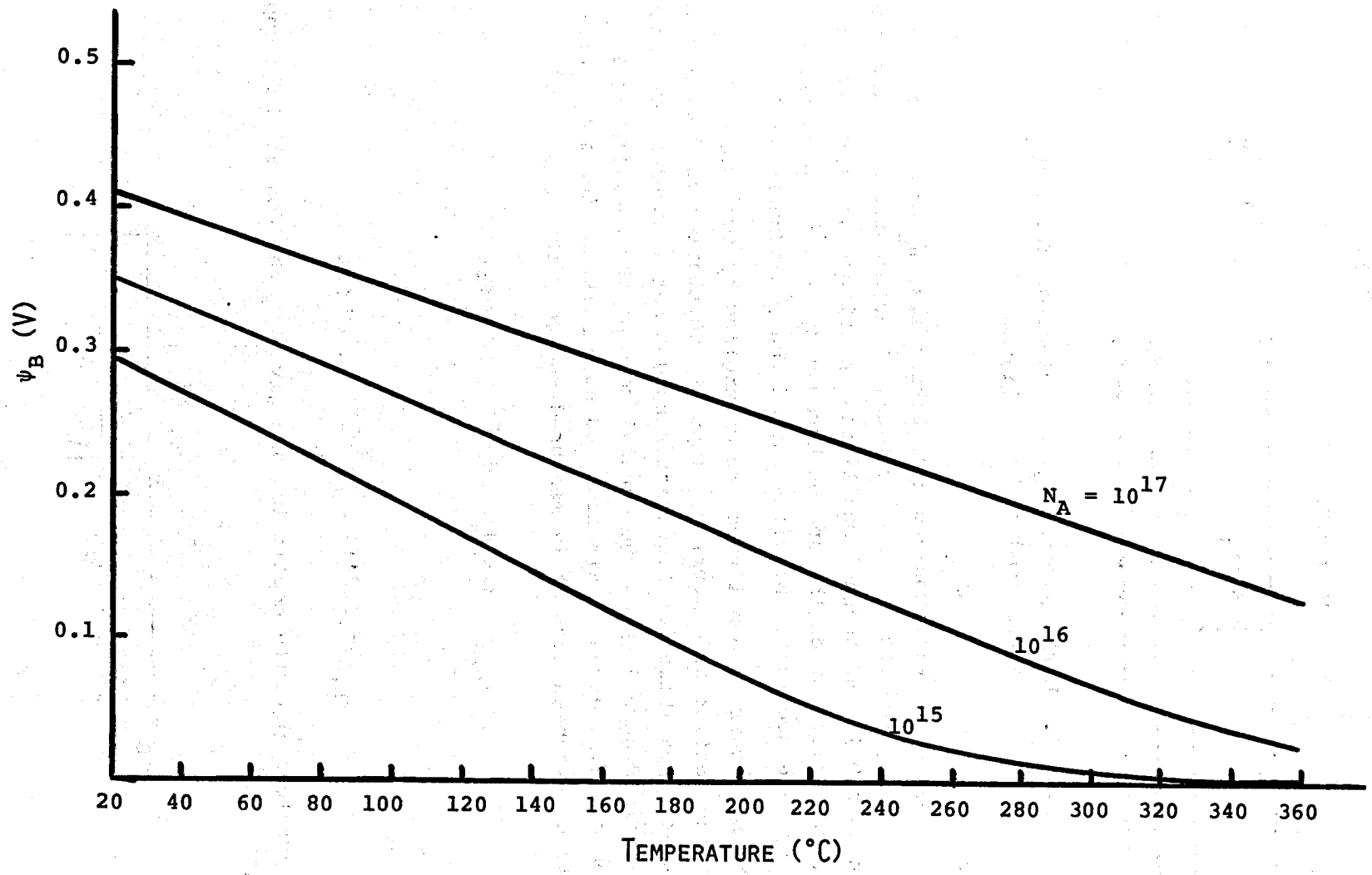
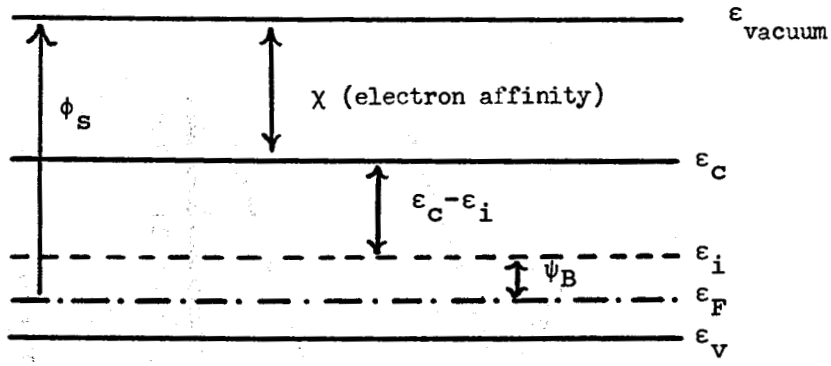


Fig. 6. The bulk fermi potential plotted as a function of temperature. Less percentage change occurs with highly doped silicon.



$$\frac{kT}{q}\ln\left(\frac{N_c}{n_i}\right) = \varepsilon_c-\varepsilon_i$$

Fig. 7. Work function ϕ_s, and electron affinity χ represented on band diagram.

Mobility

Expressing the electron and hole mobilities, μ_n and μ_p, in analytic form posed the greatest problem. Many measurements have been made on both bulk and channel mobilities in silicon as functions of temperature, field strength, and background doping.[7,8] However, no theory to date accurately predicts any of these dependencies.[8,9]

The bulk carrier mobilities are controlled by two types of scattering--lattice and impurity. Impurity scattering is dominant at low temperatures while lattice scattering dominates at high temperatures. The graph in Figure 8 shows the general form of the mobility as a function of temperature.[7] Electron and hole bulk lattice mobilities in silicon have been accurately measured and obey the equations[2]

$$\mu_{L,n} = 2.104 \times 10^5 T^{-2.5}\ M^2/V\ Sec$$

and

$$\mu_{L,p} = 2.3414 \times 10^5 T^{-2.7}\ M^2/V\ Sec\ .$$

The theoretical impurity mobilities are given by the Conwell-Weisskopf formula[10]

$$\mu_I = \frac{2^{7/2}\varepsilon_S^2 (KT)^{3/2}}{\pi^{3/2} C_B q^3 (M_c^*)^{1/2} \ln\left[\left(\frac{7\varepsilon_S KT}{2q^2 C_B^{1/3}}\right)^2 + 1\right]}$$

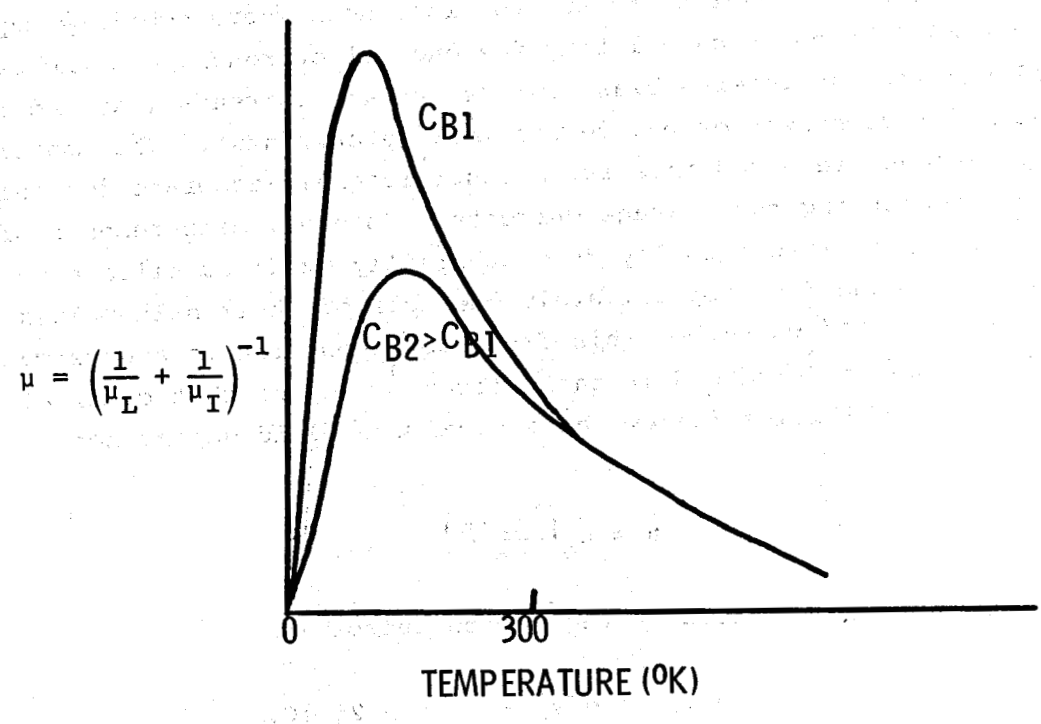


Fig. 8. Qualitative temperature dependence of carrier mobility. Two different bulk impurity concentrations, C_{B1} and C_{B2}, are used as the third parameter.

where C_B is the bulk impurity concentration and M_c^* is the conductivity effective mass for electrons or holes:

$$M_{n,c}^* = 3\left(\frac{2}{M_\perp^*} + \frac{1}{M_{||}^*}\right)^{-1} = 0.2598\ M_o$$

$$M_{p,c}^* = 3\left(\frac{1}{M_\ell^*} + \frac{1}{M_h^*} + \frac{1}{M_s^*}\right)^{-1} = 0.2425\ M_o\ .$$

The split-band effective mass for holes, M_s^*, should actually be included in the expression only for temperatures such that $\frac{KT}{q} > \Delta E_{split} = 0.035$ eV. However, its inclusion affects the expression very little at any temperature since $M_s^* = 0.245\ M_o$. The total bulk mobility of either charge carrier is then given by

$$\mu = \left(\frac{1}{\mu_L} + \frac{1}{\mu_I}\right)^{-1}\ .$$

In the MOS model there are two instances where mobility expressions are needed--once in calculating the channel currents, and the other in calculating the reverse bias drain/substrate currents (assumed to be the major component of the device leakage currents). The mobility expressions presented thus far are sufficiently accurate for calculations concerning the leakage currents. However, measurements of carrier mobilities in inversion layers on thermally oxidized silicon show that they are reduced to approximately one-half of their bulk values at fields up to 1.5×10^5 volts/cm, this field corresponding to approximately 10^{12} charges/cm^2 induced in the silicon.[8] Beyond that critical field value the mobilities follow the approximate field dependence of

$$\mu \approx \mu_o \left(\frac{E_{crit}}{E}\right)^{1/2} .$$

The total charge induced in the semiconductor is

$$Q_s(y) = -[V_G' - V(y) - 2\psi_B]C_i$$

where V_G' is the effective gate voltage, ψ_B is the bulk Fermi potential, C_i is the oxide capacitance, and $V(y)$ is the potential in the channel at a distance y from the source end. For a 1200 Å oxide thickness, C_i is 2.88×10^{-4} F/M^2. An induced charge of 10^{12} charges/cm^2 then corresponds to

$$\left|V_G' - V(y) - 2\psi_B\right| \leq 5.6 \text{ volts} .$$

Typically the devices are operated within the ranges

$$0 < 2\psi_B < 1 ,$$

$$0 \lesssim V_G' \lesssim 10 ,$$

and

$$0 \leq V(y) \leq 10 ,$$

so that

$$0 \lesssim \left|V_G' - 2\psi_B - V(y)\right| \lesssim 11 .$$

Therefore, only at the extremes of device operation will the critical field be exceeded, and even then by less than a factor of two. For that reason, the mobilities were assumed to be field independent for the purposes of this model.

The graph in Figure 9 shows electron mobility in the channel as a function of temperature. The theoretical values were computed by letting $\mu_{n,channel} = 0.45\ \mu_{bulk}$. The agreement with measured values is very good for doping concentrations within a factor of 2 of $6 \times 10^{15}\ cm^{-3}$, the range for common MOSFETs. No claim is being made that the physics of the inversion channel conduction process are explained by these mobility expressions. However, they do show good agreement with the experimental data, including the $T^{-3/2}$ temperature dependence in the range 25°C to 300°C.

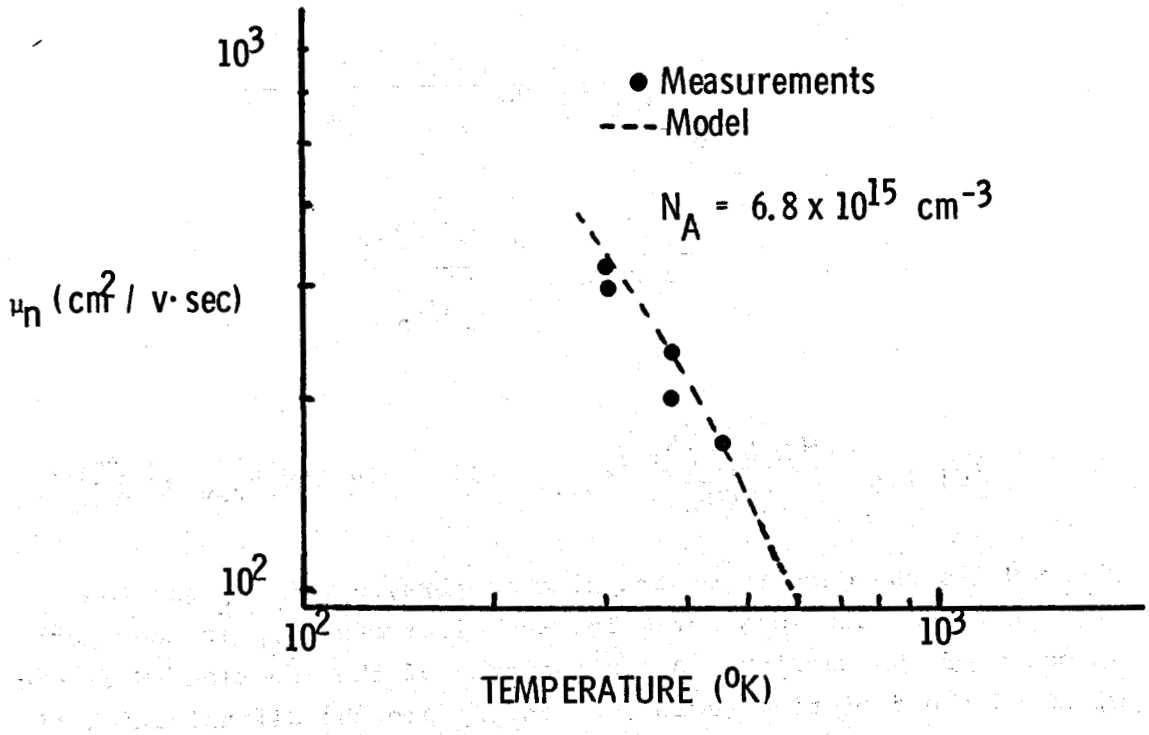


Fig. 9. Electron mobility in MOSFET channel as function of temperature. Model assumes $\mu_{n\text{-channel}} = 0.45\ \mu_{bulk}$.

Leakage Currents

For the purposes of this model it was assumed that the reverse biased drain/substrate junction is the source of all the device leakage currents. There are two types of reverse currents in p-n junctions which add together to form the total current--generation and diffusion current. The generation current component is due to electron-hole pairs thermally generated within the depletion region. The carriers are separated and swept across the region by the large electric field present. If electron-hole pairs are generated in neutral regions where there is no significant field present, they may move only by diffusion to the edge of the depletion region where they are then swept across the junction by the electric field. This component of the reverse current is called diffusion current.

The standard equations for each of the reverse current components are

$$I_{gen} = \frac{q\sigma_p\sigma_n v_{th} N_t n_i A_j W}{\sigma_n e^{(\varepsilon_t-\varepsilon_i)/KT} + \sigma_p e^{(\varepsilon_i-\varepsilon_t)/KT}}$$

$$I_{diff,n} = \frac{q\sqrt{D_n}\, n_i^2 A_j}{N_A\sqrt{\tau_n}}$$

and

$$I_{diff,p} = \frac{q\sqrt{D_p}\, n_i^2 A_j}{N_D\sqrt{\tau_p}} \quad \left(I_{diff} \text{ valid only for } V_{rev} >> \frac{KT}{q}\right)$$

where N_t is the density of trapping centers, σ_p and σ_n are the trapping cross sections for holes and electrons, v_{th} is the thermal velocity of the carriers, A_j is the area of the junction, W is the width of the depletion region, D_n and D_p are the diffusivities of electrons and holes, τ_n and τ_p are the effective lifetimes of electrons and holes, and $\varepsilon_t - \varepsilon_i$ is the energy difference between the trapping level and the intrinsic Fermi level. The diffusivities can be found from the bulk mobilities using Einstein's relationship,

$$D_{n,p} = \frac{KT}{q}\mu_{n,p} .$$

The effective lifetimes of electrons and holes are taken to be[5,6]

$$\tau_n = \frac{1}{\sigma_n v_{th} N_t} \text{ and } \tau_p = \frac{1}{\sigma_p v_{th} N_t} ,$$

respectively. σ_n and N_t refer to the electron trapping cross sections and density of traps in the p-type bulk. Similar adjustments must be made for the generation current equation. In the computer model the depletion region is considered as two different carrier generation rates determined by the trap characteristics on both sides of the junction.

The total width of the depletion region can be closely approximated by

$$W = \sqrt{\frac{2\varepsilon_s}{q} \frac{N_A + N_D}{N_A N_D} (\psi_B + \psi_D + V_{rev})} ,$$

and the width on the n and p sides of the junction are

$$W_n = W\left(\frac{N_A}{N_A + N_D}\right) , \quad W_p = W\left(\frac{N_D}{N_A + N_D}\right)$$

where N_A and N_D are the acceptor and donor concentrations in the substrate and drain, respectively; ψ_B and ψ_D are the Fermi potentials in the substrate and drain; and V_{rev} is the external reverse bias applied to the junction. If the substrate and source are tied to a common voltage as was assumed in this model, V_{rev} is equal to the drain-source voltage, V_{DS}. Note that the generation currents are bias dependent while the diffusion currents are not, provided $V_{rev} >> \frac{KT}{q}$.

At high temperatures the diffusion currents dominate the reverse current expressions. Because the drain/substrate junction is normally one-sided ($N_D >> N_A$ in n-channel devices), the electron diffusion current is usually much larger than that for holes, so that $I_{rev} \approx I_{diff,n}$ for temperatures above 200 C. Plotted in Figure 10 is the model output for a reverse biased n^+-p junction showing the bias and temperature dependencies to be expected.

Pinchoff Regime

Drain Saturation Voltage -- The onset of saturation--that region of the device characteristics where the drain current is nearly independent of drain voltage--occurs when the inversion layer

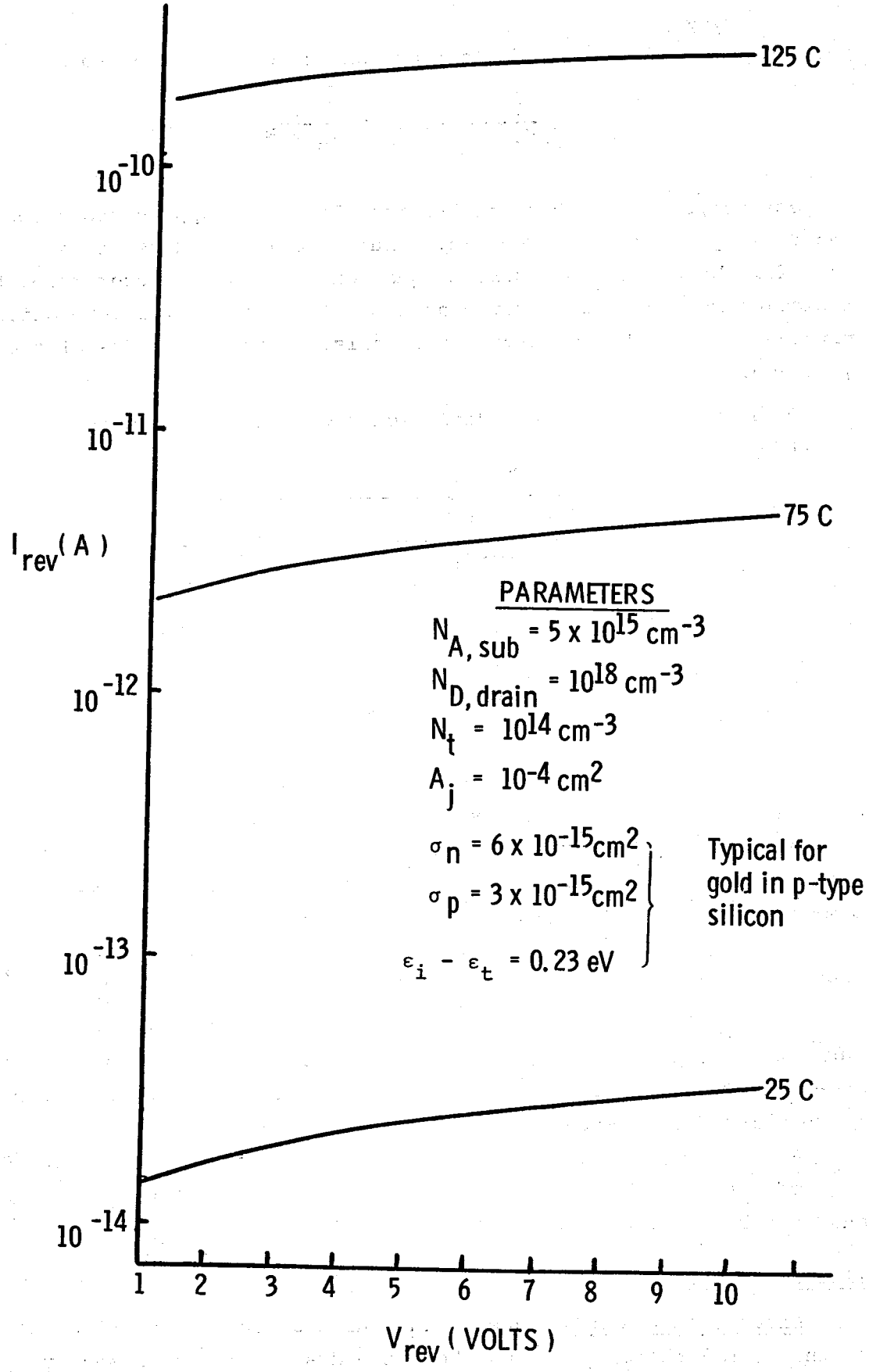


Fig. 10a. Model calculations for reverse current of a n^+-p junction.

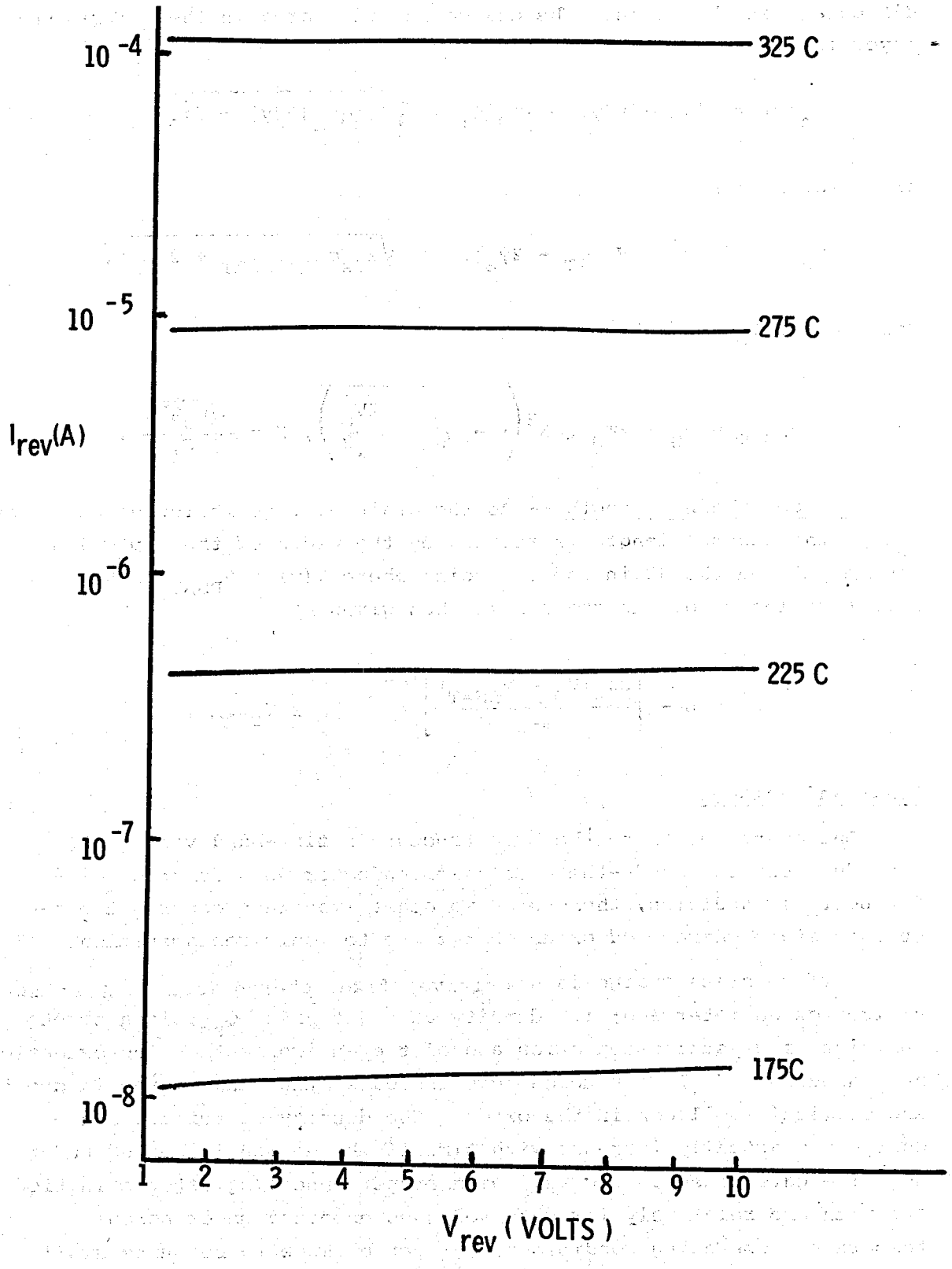

10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
I_{rev}(A)
325 C
275 C
225 C
175C
1
2
3
4
5
6
7
8
9
10
V_{rev} (VOLTS)

Fig. 10b

disappears at the drain. The charge per unit area in the inversion layer is given by

$$Q_n(y) = -[V_G' - V(y) - 2\psi_B]C_i + \sqrt{2\varepsilon_s q N_A [V(y) + 2\psi_B]} ,$$

or at saturation

$$Q_n(L) = -[V_G' - V_{DSAT} - 2\psi_B]C_i + \sqrt{2\varepsilon_s q N_A [V_{DSAT} + 2\psi_B]} .$$

Solving for V_{DSAT} yields

$$V_{DSAT} = V_G' - 2\psi_B + K^2\left(1 - \sqrt{1 - \frac{2V_G'}{K^2}}\right), \quad K = \frac{\sqrt{\varepsilon_s q N_A}}{C_i} .$$

Reduced Channel Length -- As the drain voltage is increased above V_{DSAT}, the channel length is reduced by the width of the depletion region between the drain and the point where $V(y) = V_{DSAT}$. The effective length of the channel is then given by

$$L' = L - \left[\frac{2\varepsilon_s (V_D - V_{DSAT})}{qN_A}\right]^{1/2} , \quad V_D \geq V_{DSAT} .$$

Flat-Band Voltage

One contribution to the MOS structure's flat-band voltage has already been discussed--the metal/semiconductor work function difference. In addition, there are two other important contributions--surface state charge and oxide charge due to ionic contamination.

Surface state charge is a positive, fixed charge located near the silicon/oxide interface; its density per unit area, Q_{ss}, is a strong function of crystal orientation and of the environment during oxidation and annealing.[11] Past studies have indicated that the charge is due to excess (ionic) silicon in the oxide. The density of surface state charge may actually increase with time if the device is heated under negative gate biases. However, with proper annealing after oxidation and with the relatively low gate voltages expected under normal temperature operating conditions, Q_{ss} can be made to be quite small and relatively time invariant.

Ionic contamination of the oxide can also contribute to the flat-band voltage. Unlike surface state charge, the ions may become very mobile at temperatures well below the 300 C level. This makes modelling somewhat more difficult unless it is assumed that the device is biased with either positive or negative gate voltage for long periods of time and that excursions to the opposite polarity are brief. In this way it can be assumed that the ions will be concentrated very near the metal/oxide or silicon/oxide interfaces.

The effective gate voltage can now be expressed as

$$V_G' = V_G - V_{FB}$$

$$= V_G - \Phi_{MS} + \frac{Q_{ss}}{C_i} + \frac{1}{C_i}\int_o^{x_d} \frac{x}{x_d}\,\rho(x)\,dx$$

where x_d is the oxide thickness, x is the distance from the metal/oxide interface, and $\rho(x)$ is the charge density within the oxide. Obviously, the effective gate voltage is made more positive by the presence of surface state charge or ionic charge within the oxide. The closer the ions are to the oxide/silicon interface the greater their effect is on V_{FB}.

Changes for the PMOS Model

As a general rule the NMOS equations could be adapted to PMOS devices by changing the signs of the terminal voltages and currents (V_G', V_{DS}, I_D, V_T, V_{DSAT}). One other change must be made: Since the substrate is n-type the metal semiconductor work function difference will be given by

$$\phi_{MS} = \phi_M - [\chi + (\varepsilon_c - \varepsilon_i) - \psi_B] \ .$$

An inspection of the terminal threshold voltage equations will show that the PMOS threshold is made up of three temperature dependent terms, all of the same sign and all decreasing in magnitude with increasing temperature. NMOS, on the other hand, has one negative and two positive terms, all decreasing in magnitude with increasing temperature. This means that the terminal threshold voltage in PMOS will have a slightly greater temperature dependence than in NMOS devices. Shown in Figure 11 is a plot of the computer model output of the threshold voltages as a function of temperature for two devices

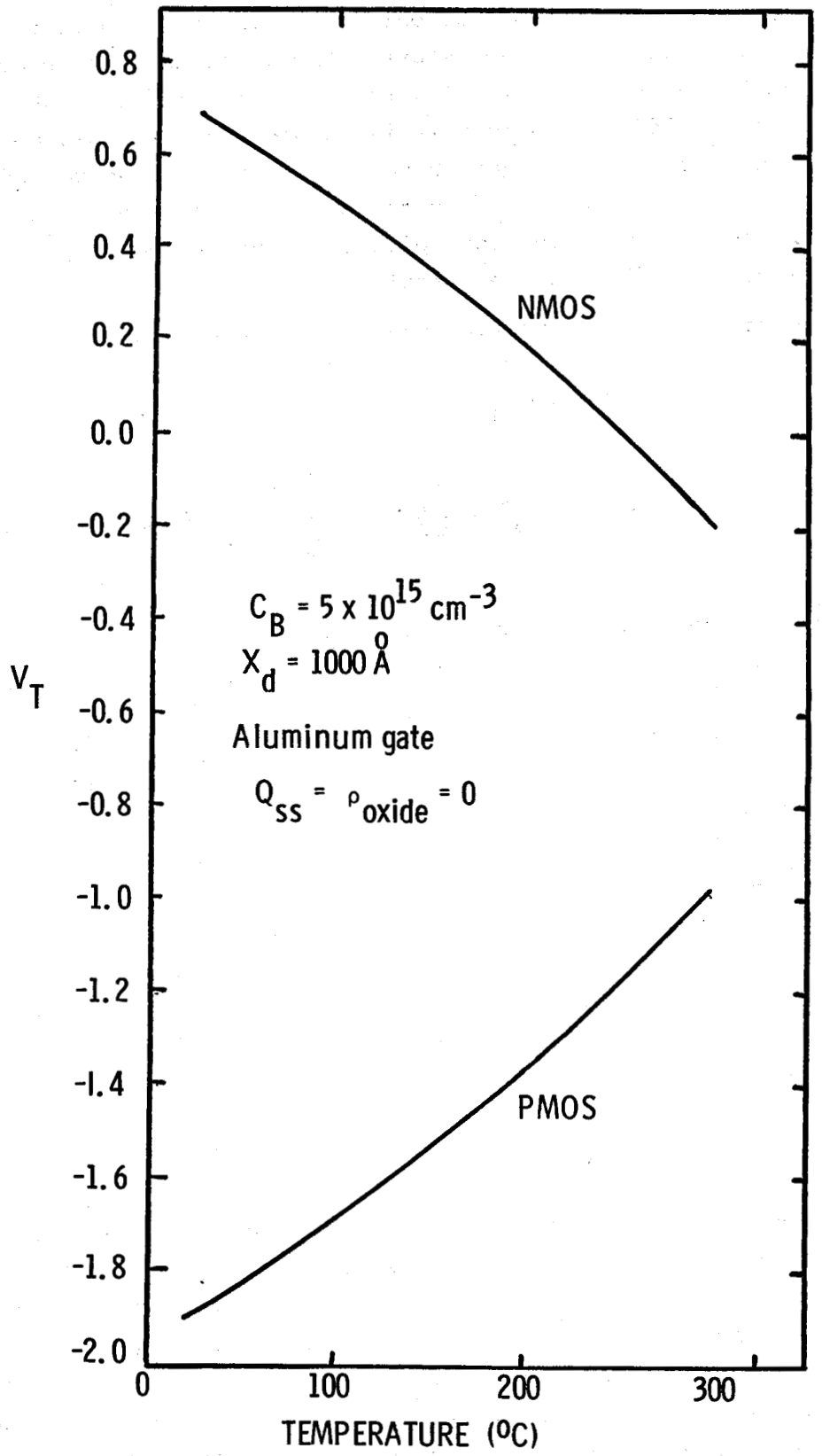


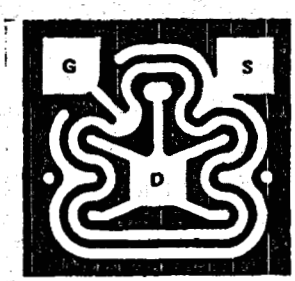
Fig. 11. Model generated temperature variations of threshold voltage for p and n-channel MOSFET.

identical in every respect except dopant type. The threshold voltage of the PMOS device shows slightly more variation with temperature than that of the NMOS device. In general, however, the PMOS threshold voltage will be less likely to change polarity as the temperature is increased since it is usually larger in magnitude. That is, a p-channel enhancement mode device is less likely to become a depletion mode device--a phenomena often observed.

MEASUREMENT VERSUS MODEL

Comparison

The Motorola MFE3001 n-channel MOSFET was chosen for high temperature reliability studies and for the purpose of comparing the model to experimental data. A diagram of the top surface of an MFE3001 chip is shown in Figure 12 below. In addition to the gate, source, and drain contacts on the top plane, there is a contact to the substrate on the back plane to enable substrate biasing and shifting of the turn-on voltage. For all of our studies the substrate was connected to the source.



CHIP 15 X 15 mils

SOURCE PAD 3.0 X 3.0 mils

GATE PAD 3.0 X 3.0 mils

DRAIN PAD 2.6 X 3.0 mils

Fig. 12. Electrode geometry for MFE3001 Motorola n-channel MOSFET.

The MFE3001 chip is 15 x 15 mils. The total channel width and length were estimated to be 1100 and 12 μm, respectively. The drain/substrate junction area is approximately 3×10^{-4} cm^2. From studies of the drain/substrate and source/substrate junction breakdown voltages when the gate was biased for flat-band conditions and from observations of the dependence of the turn-on voltage on temperature, the substrate doping concentration was found to be near $6 \times 10^{+15}$ cm^{-3}. The gate oxide thickness was estimated to be 1800 Å (fairly thick for this type of device). Aluminum is used for the top metallization giving a metal-semiconductor work function difference of approximately -1 volt at room temperature. Assuming ideal processing conditions, Q_{ss}/q is

1.8×10^{11} cm^{-2}. The concentration of ions in the gate oxide was taken to be 2×10^{17} e^{-2x/x_o} cm^{-3}, where x is measured from the metal/oxide interface and x_o is the oxide thickness.

The entire back plane of the device is covered with a gold film. It is not known at what point in the manufacturing process the gold is deposited, but subsequent heat treatments and device operation at 300 to 600°C could result in diffused gold concentrations of up to 10^{14} cm^{-3} in the bulk semiconductor. In p-type silicon gold introduces a state with an energy level 0.21 eV below the center of the gap. The trapping cross sections for electrons and holes for this state are 5×10^{-15} and 2×10^{-15} cm^2, respectively. In n-type silicon the gold trapping level is 0.02 eV above the center of the gap and the trapping cross sections are 3×10^{-16} and 4×10^{-15} cm^2 for electrons and holes, respectively.

It should be pointed out that many of the numbers presented above are only very rough estimates (the ion concentration in the oxide, for example). The unavailability of the details of the manufacturing processes and the lack of time to make good capacitance-voltage studies led to some device parameters being only approximately known. A better check of the computer model has been initiated by construction and testing a device of known design.

Experimental and theoretical transfer characteristics for the MFE3001 are shown in Figures 13 and 14. The agreement between the two is very good considering the uncertainties involved. Note the relatively large drain currents at $V_{GS} = -5$ and T = 275 C. In fact, these are the leakage currents that continued to flow after the transistor was well below cutoff. The model seems to confirm that these currents are due to the reverse saturation currents of the drain/substrate junction. At high positive gate voltages the measured transconductance is considerably less than that predicted by the model. This is probably due to a lowering of the channel mobility caused by the high surface field--a refinement to be added to the model in the near future.

A good indicator of the device sensitivity to temperature variations is the ratio of the transconductances at 275 C and 25 C ($V_{GS} = 2$):

$$R_{gm} = \frac{g_{m,275}}{g_{m,25}} .$$

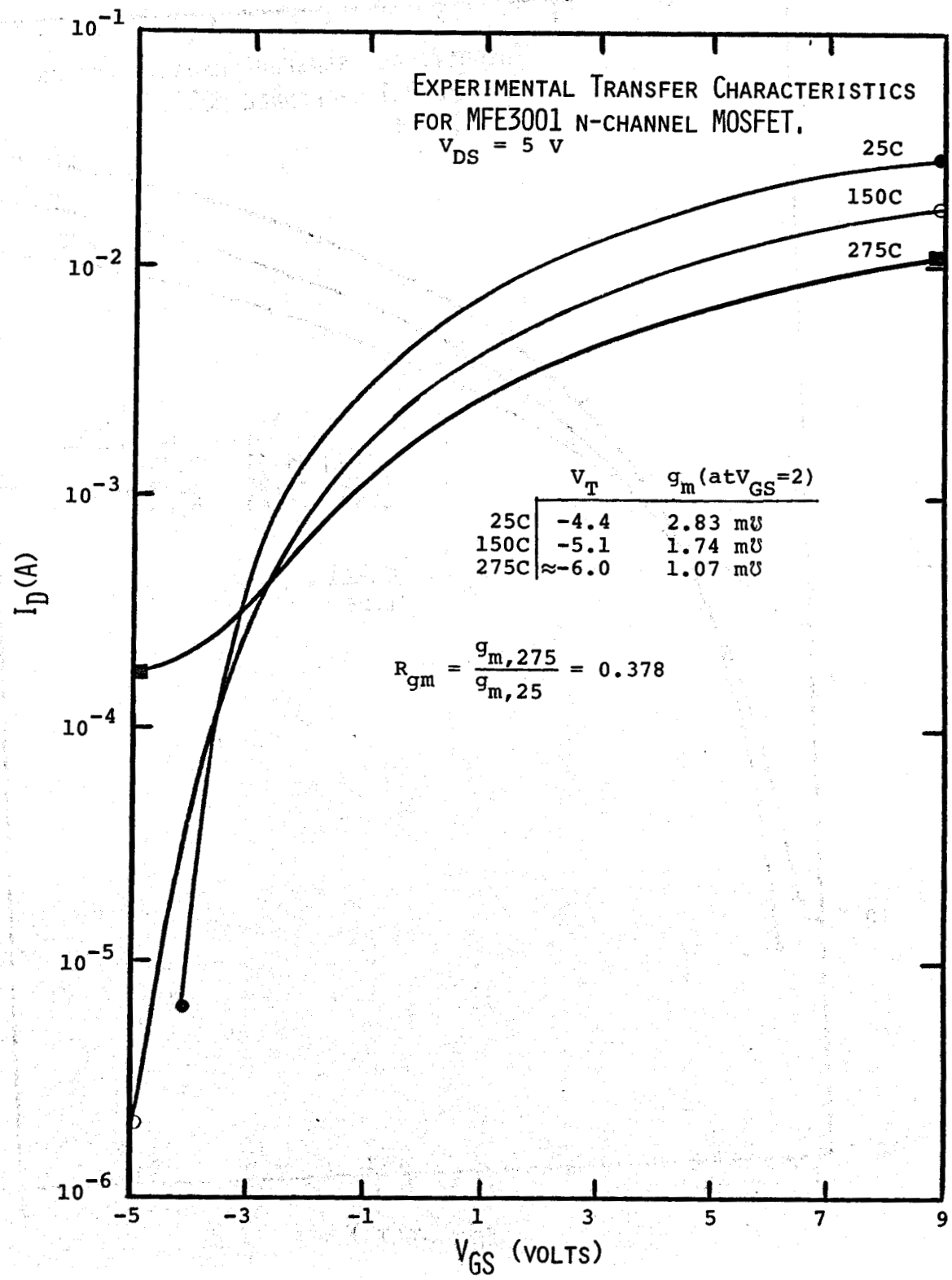

EXPERIMENTAL TRANSFER CHARACTERISTICS
FOR MFE3001 N-CHANNEL MOSFET.
V_{DS} = 5 V
25C
150C
275C
V_T g_m(atV_{GS}=2)
25C -4.4 2.83 m℧
150C -5.1 1.74 m℧
275C ≈-6.0 1.07 m℧
$R_{gm} = \frac{g_{m,275}}{g_{m,25}} = 0.378$
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
I_D(A)
-5
-3
-1
1
3
5
7
9
V_{GS} (VOLTS)

Fig. 13

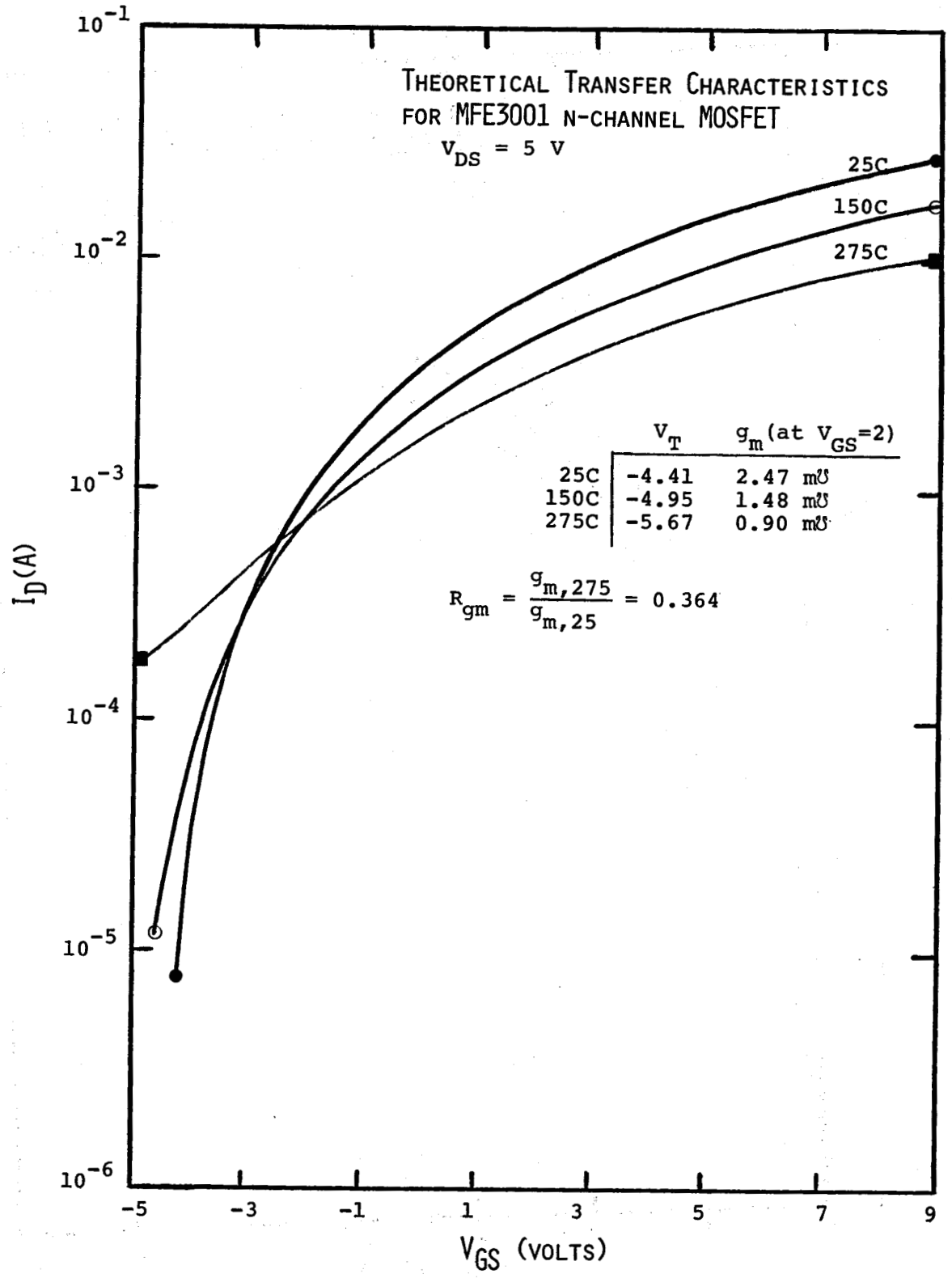

THEORETICAL TRANSFER CHARACTERISTICS
FOR MFE3001 N-CHANNEL MOSFET
V_{DS} = 5 V
25C
150C
275C
V_T g_m(at V_{GS}=2)
25C -4.41 2.47 m℧
150C -4.95 1.48 m℧
275C -5.67 0.90 m℧
$R_{gm} = \frac{g_{m,275}}{g_{m,25}} = 0.364$
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
I_D(A)
-5
-3
-1
1
3
5
7
9
V_{GS} (VOLTS)

Fig. 14

As shown in Figures 13 and 14 R_{gm} was found to be 0.378 experimentally and 0.364 theoretically--a close agreement. Therefore, with respect to transconductance the MFE3001 is performing at high temperatures as predicted from this computer model.

Redesign for High Temperatures

The computer model can be used to design devices to be less temperature sensitive. Figures 15, 16, and 17 show the transfer characteristics of a device equivalent to the MFE-3001 in all respects except that the substrate doping has been increased. Note that as N_A is increased from 6×10^{15} to 3×10^{16} cm^{-3}, R_{gm} increases from 0.364 to 0.672. This means that it should be possible to decrease the temperature sensitivity of the device by a considerable amount (increase R_{gm} 84.6%) simply by increasing the doping in the channel. However, caution must be used when considering these results. As was pointed out earlier, the expression used to calculate channel mobilities is only accurate for doping concentrations within a factor of 2 of 6×10^{15} cm^{-3}. In order to get a limit on just how much the temperature sensitivity could be decreased, a doping-independent channel mobility equation was substituted into the model:

$$\mu_{n,channel} = 203T^{-3/2} \ M^2/\text{sec-volt} \ .$$

This equation has been suggested by several studies of channel mobilities on p-type silicon. Using this equation the model then predicted an increase in R_{gm} of 20.4% when N_A was increased from 6×10^{15} to 3×10^{16} cm^{-3}. It is, therefore, safe to assume that if this device were to be built it would have an R_{gm} considerably higher than that of the MFE3001.

There are several problems with "improving" the device in this manner:

1. The threshold voltage varies more with temperatures as the doping is increased.
2. The zero temperature coefficient point, point on transfer curve independent of temperature, occurs at higher gate voltages and drain currents as the doping is increased. This may or may not be desirable from a circuit designer's viewpoint.
3. The overall transconductance of the device decreases rapidly as the doping is increased.

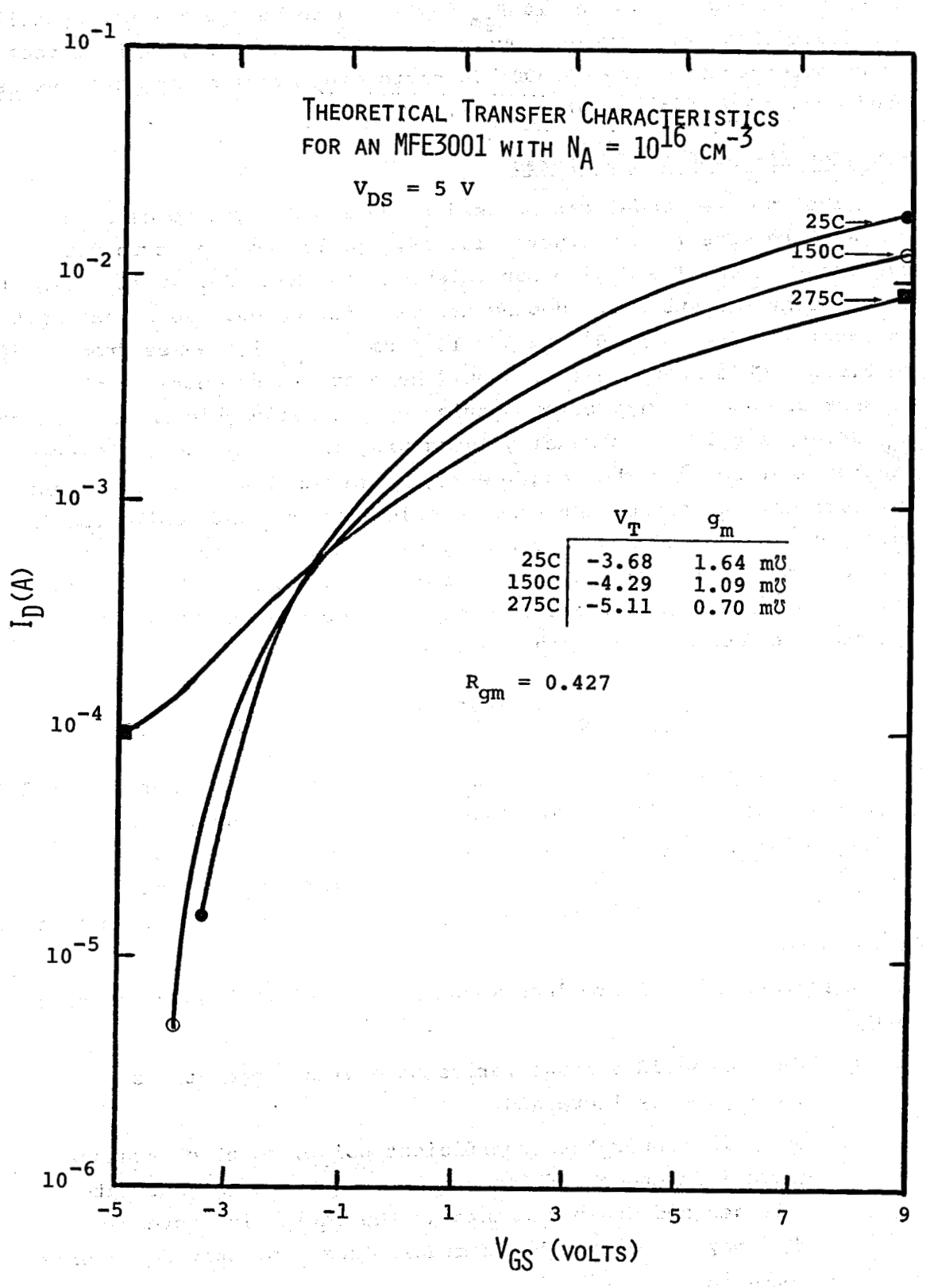

THEORETICAL TRANSFER CHARACTERISTICS
FOR AN MFE3001 WITH $N_A = 10^{16}$ CM^{-3}
V_{DS} = 5 V
25C
150C
275C
V_T g_m
25C -3.68 1.64 m℧
150C -4.29 1.09 m℧
275C -5.11 0.70 m℧
R_{gm} = 0.427
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
I_D(A)
-5
-3
-1
1
3
5
7
9
V_{GS} (VOLTS)

Fig. 15

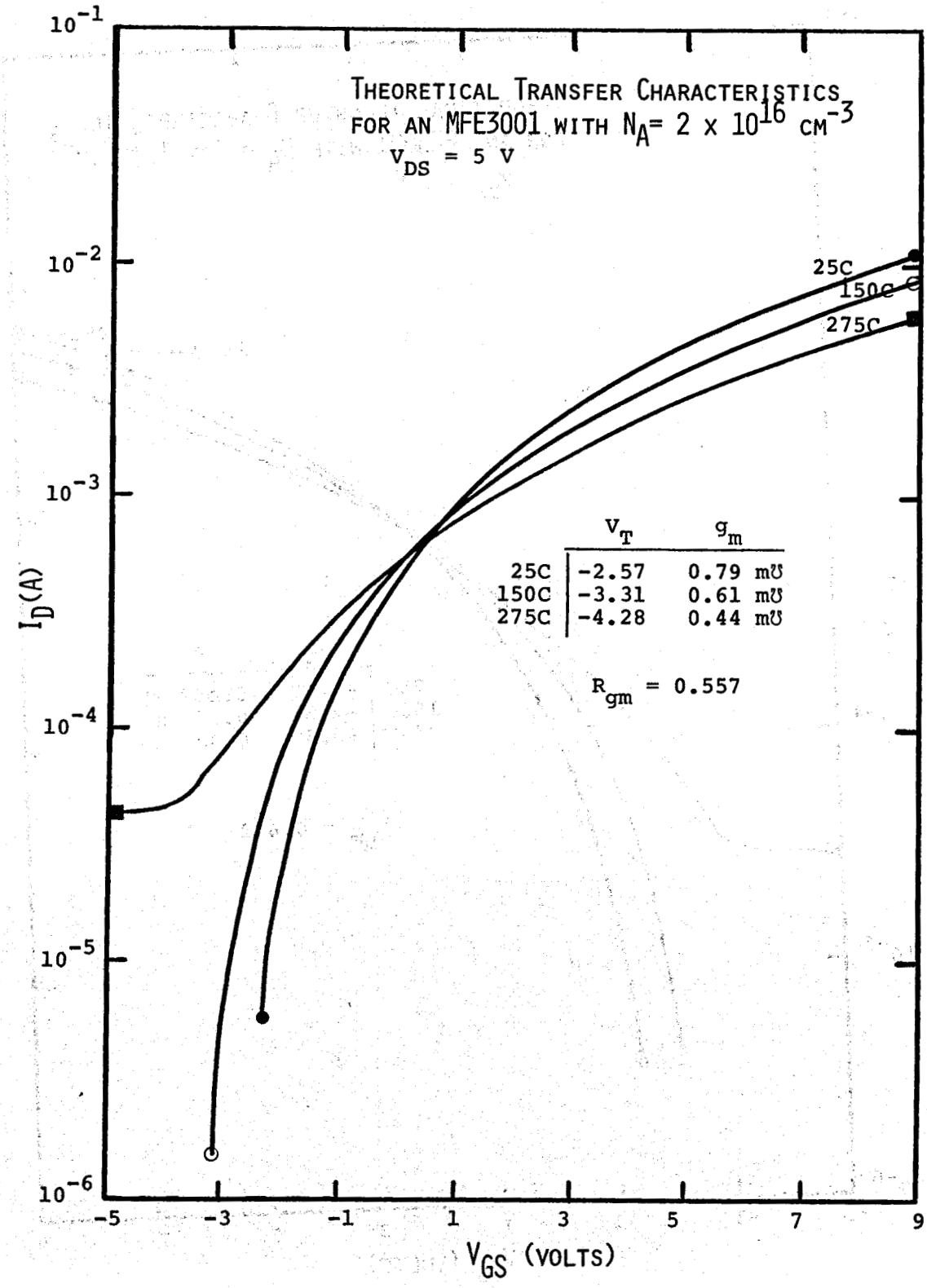

THEORETICAL TRANSFER CHARACTERISTICS
FOR AN MFE3001 WITH $N_A = 2 \times 10^{16}$ CM^{-3}
V_{DS} = 5 V
25C
150C
275C
V_T g_m
25C -2.57 0.79 m℧
150C -3.31 0.61 m℧
275C -4.28 0.44 m℧
R_{gm} = 0.557
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
I_D(A)
-5
-3
-1
1
3
5
7
9
V_{GS} (VOLTS)

Fig. 16

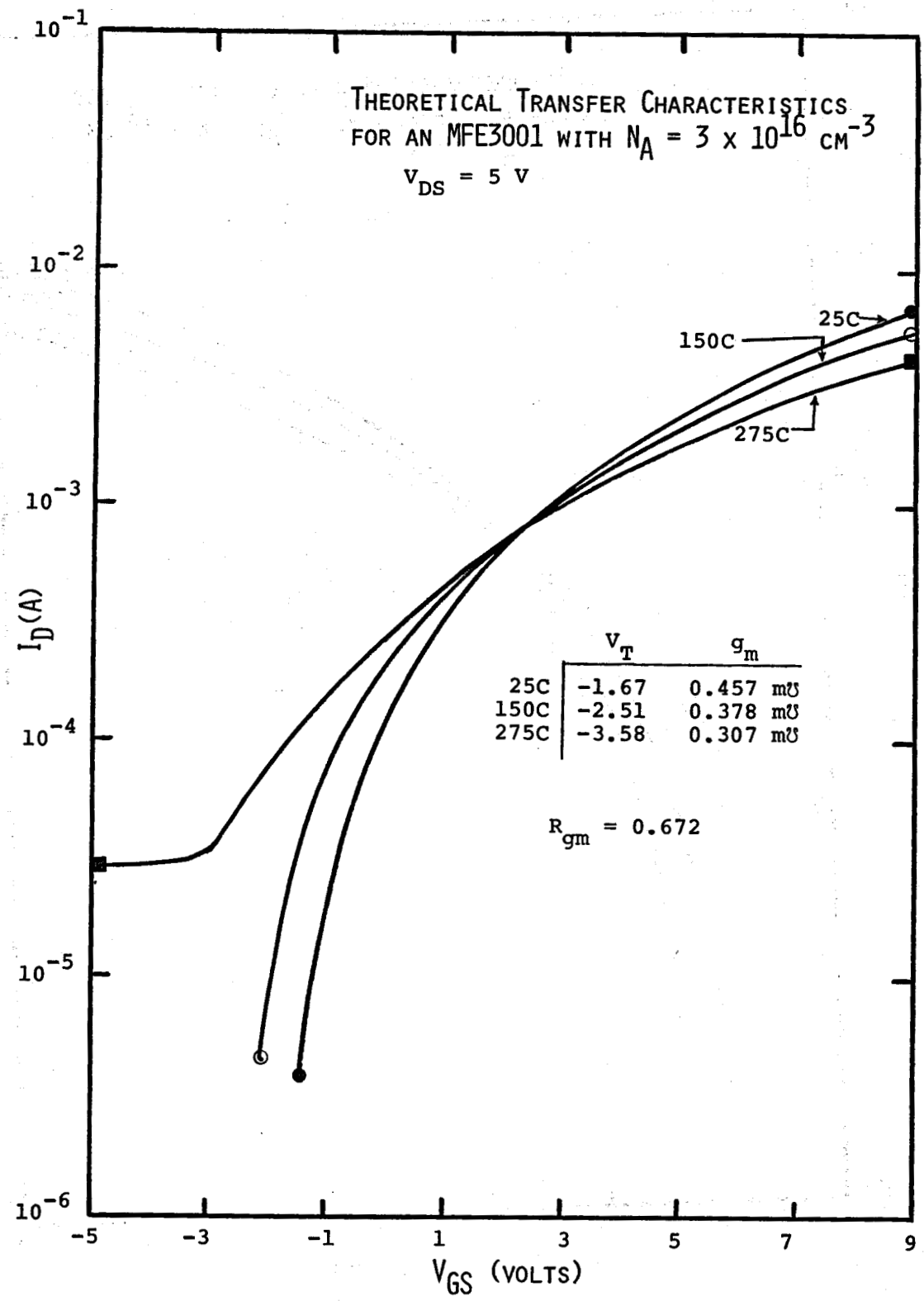

THEORETICAL TRANSFER CHARACTERISTICS
FOR AN MFE3001 WITH $N_A = 3 \times 10^{16}$ CM^{-3}
V_{DS} = 5 V
25C
150C
275C
V_T g_m
25C -1.67 0.457 m℧
150C -2.51 0.378 m℧
275C -3.58 0.307 m℧
R_{gm} = 0.672
I_D(A)
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
-5
-3
-1
1
3
5
7
9
V_{GS} (VOLTS)

Fig. 17

The zero temperature coefficient point may be moved to different voltages by changing any parameter influencing the flat band voltage (gate metallization, etc.). This computer model indicates that the device transconductance can be increased by thinning the oxide (Figure 18 shows this to have only a small effect), or by increasing the channel width to length ratio (Figure 19). On devices such as the MFE3001 the substrate may also be biased at a non-zero voltage with respect to the source. This shifts the transfer characteristics along the V_{GS} axis and it then becomes possible to change the voltage at which the zero temperature coefficient point occurs and/or to vary the transconductance at any given gate to source voltage. For example, shifting the transfer characteristics in Figure 18 by 4 volts would give $g_{m,25}$ = 1.97 mv as compared to 0.795 mv for the "normal" case.

The last remaining problem is the large leakage current at 275 C. Figure 20 shows the effect of decreasing the gold concentration by a factor of 10, presumably done by "cleaning up" the manufacturing process. This reduction of gold results in a factor of 3 diminution in leakage. However, other trapping centers besides gold may be present.

High Temperature Aging of MOSFETs

Aging Tests

The record of MOSFET high temperature aging is spotty. For this reason no MOS devices have been incorporated in field circuits to date. The problem should disappear as statistical confidence is built in the MOS device preselection procedure, and as hybrid bonding and hermetic packaging improve. Selection on the manufacturer level, lot level, and device level appear equally important.

High temperature aging runs were made on three different device types. All tests were run on manufacturer hermetically packaged devices (TO cans). The first test involved six MFE3001 under bias in an air oven at 275°C. Periodically drain characteristics were taken over 1100 hours. Only one catastrophic failure was observed during this period and it was later attributed to a poor connection at the drain bonding pad. During the test none of the six devices showed appreciable time variation in any of their characteristics. The second test involved five 2N4352 devices aged under bias at the zero temperature coefficient point at 300°C until failure. Failure in this case was characterized by an order of magnitude change in I_{DS} (see Fig. 21).

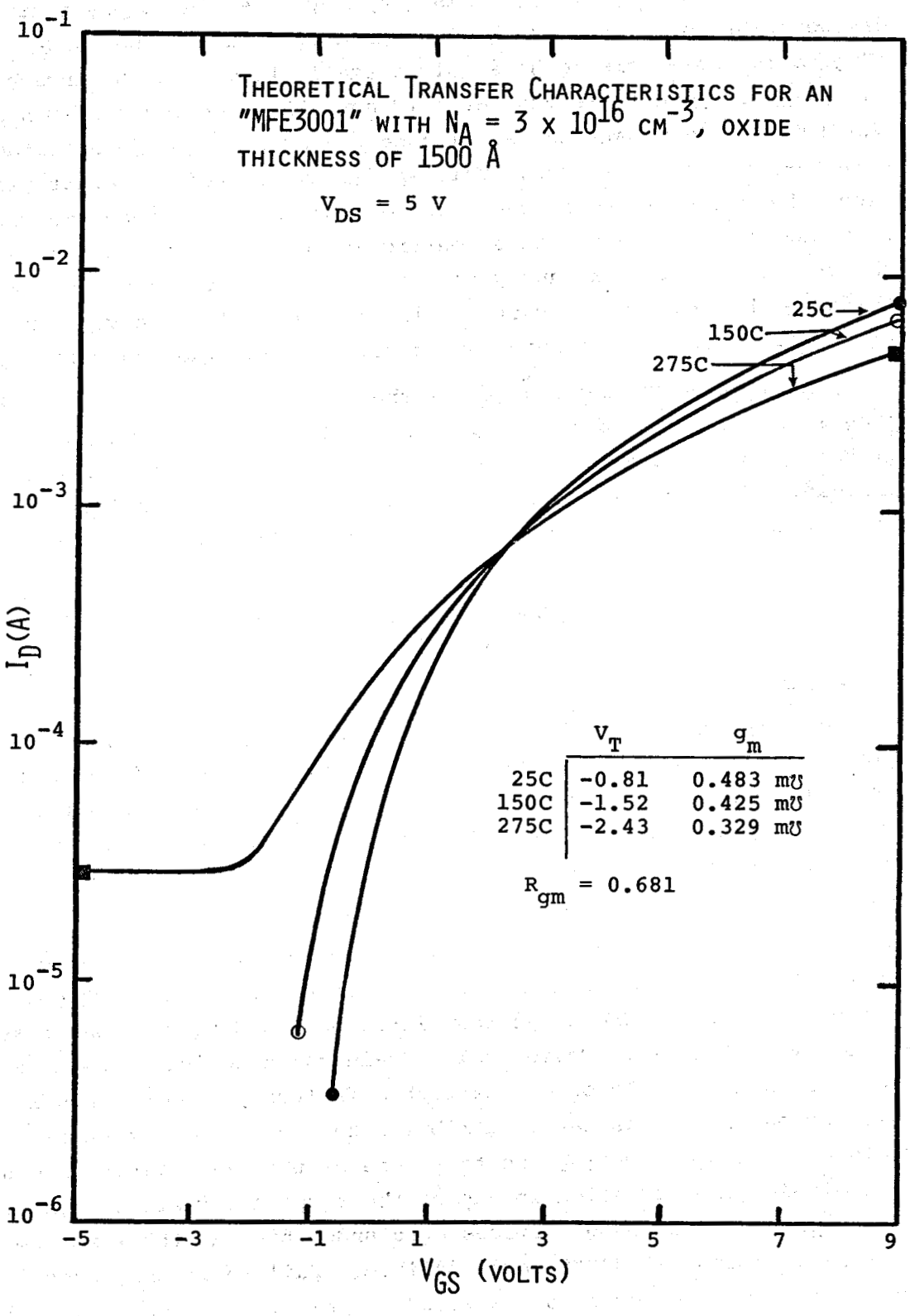

THEORETICAL TRANSFER CHARACTERISTICS FOR AN "MFE3001" WITH $N_A = 3 \times 10^{16}$ CM^{-3}, OXIDE THICKNESS OF 1500 Å
V_{DS} = 5 V
25C
150C
275C
V_T g_m
25C -0.81 0.483 m℧
150C -1.52 0.425 m℧
275C -2.43 0.329 m℧
R_{gm} = 0.681
I_D(A)
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
-5
-3
-1
1
3
5
7
9
V_{GS} (VOLTS)

Fig. 18

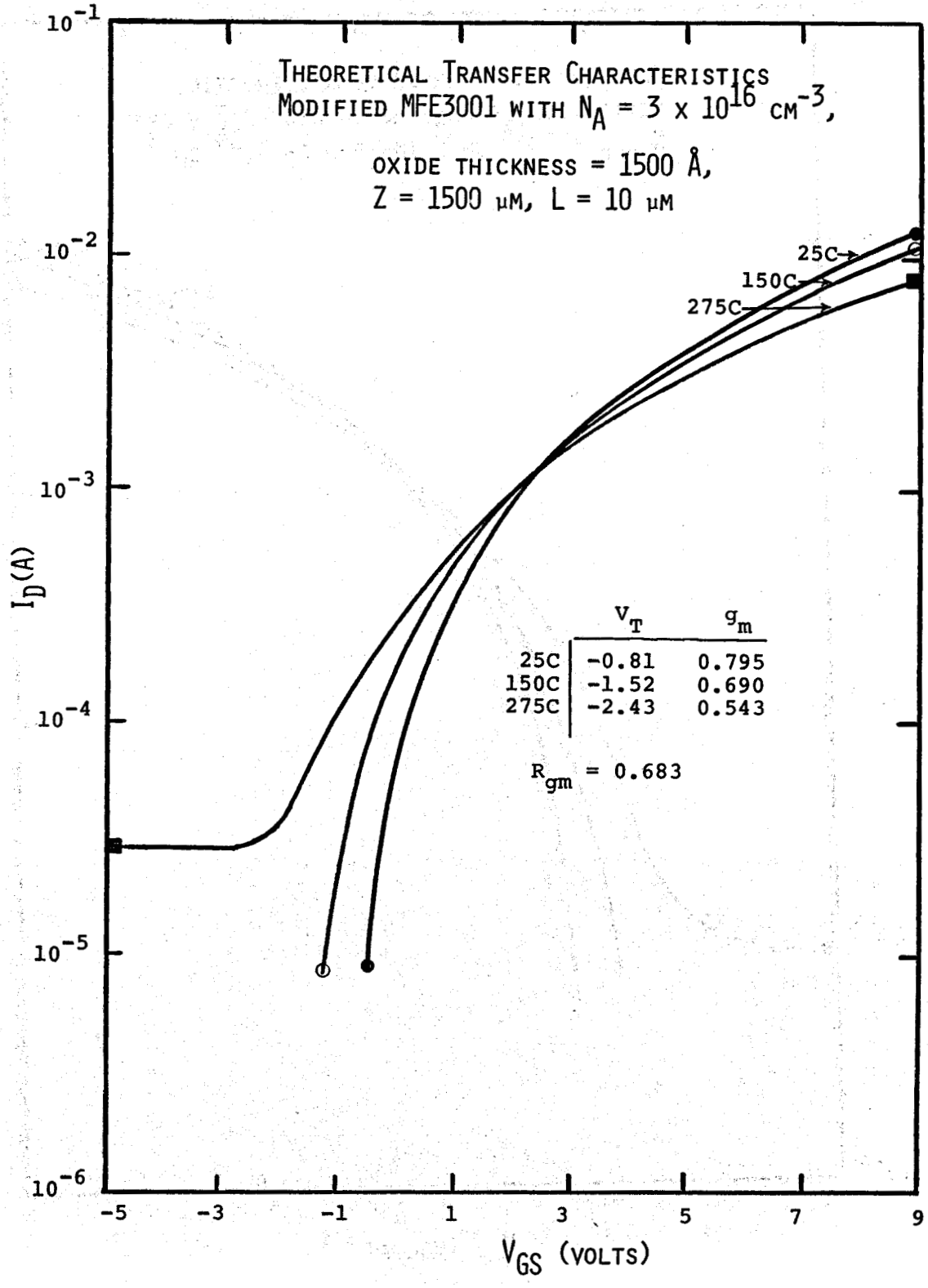

THEORETICAL TRANSFER CHARACTERISTICS
MODIFIED MFE3001 WITH $N_A = 3 \times 10^{16}$ CM^{-3},
OXIDE THICKNESS = 1500 Å,
Z = 1500 μM, L = 10 μM
25C
150C
275C
V_T g_m
25C -0.81 0.795
150C -1.52 0.690
275C -2.43 0.543
R_{gm} = 0.683
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
I_D(A)
-5
-3
-1
1
3
5
7
9
V_{GS} (VOLTS)

Fig. 19

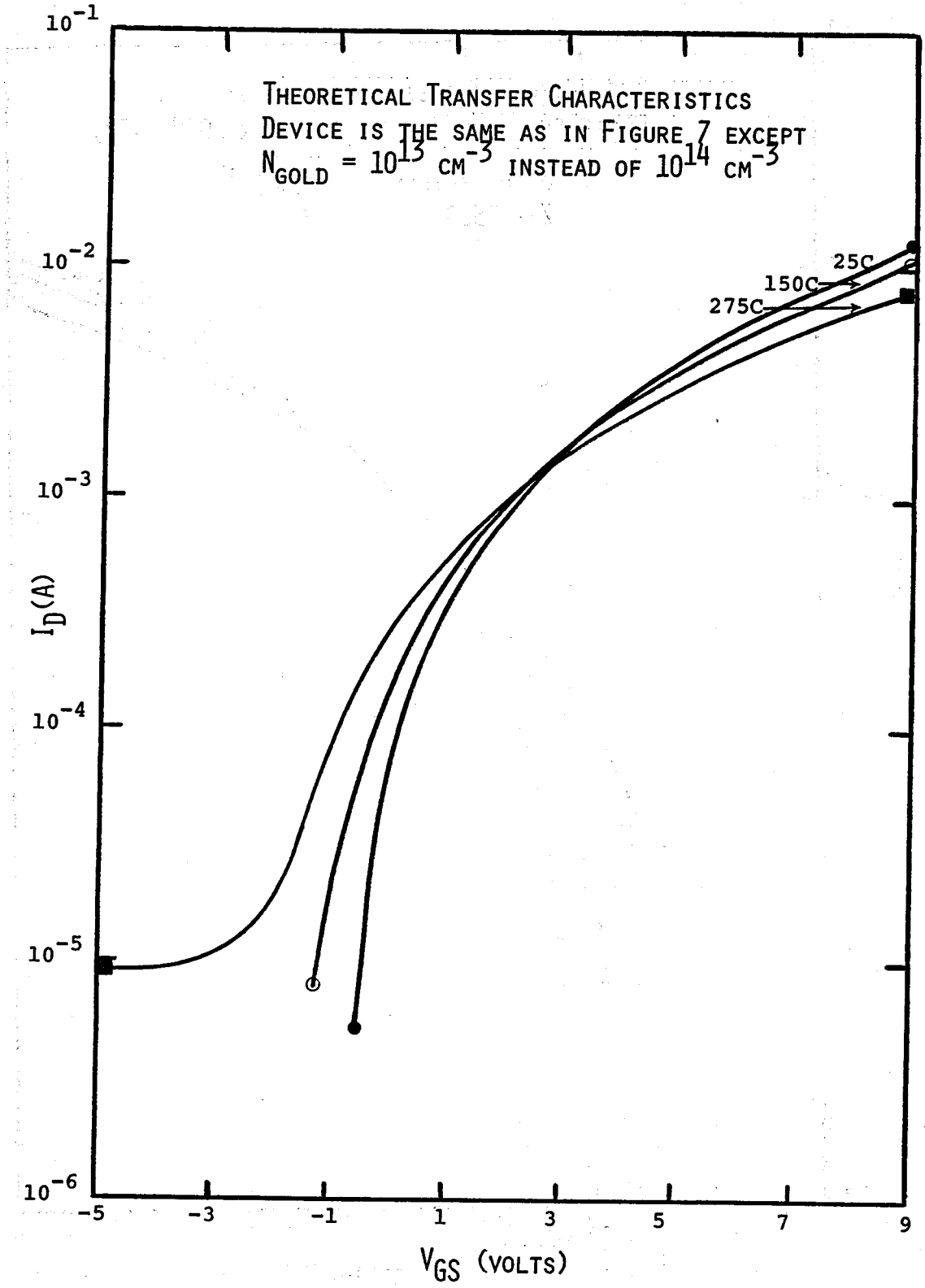

THEORETICAL TRANSFER CHARACTERISTICS
DEVICE IS THE SAME AS IN FIGURE 7 EXCEPT
$N_{GOLD} = 10^{13}$ CM^{-3} INSTEAD OF 10^{14} CM^{-3}
25C
150C
275C
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
I_D(A)
-5
-3
-1
1
3
5
7
9
V_{GS} (VOLTS)

Fig. 20

Unacceptable change in I_{DS} commenced at the beginning of aging for some transistors and after 400 hours for others. Several experienced open bonds before 1000 hours, but other drifts in characteristics had already ruled them unfit for linear circuits. The last test involved five 2N4351 devices aged at 300°C under a V_{DS} = 2 V bias. Again, I_{DS} showed unacceptably large change at 100 hours and bond opening occurred. During the last two tests abrupt changes in gate voltage led to one minute drifts in drain current, a symptom of mobile impurity ions in the gate oxide.

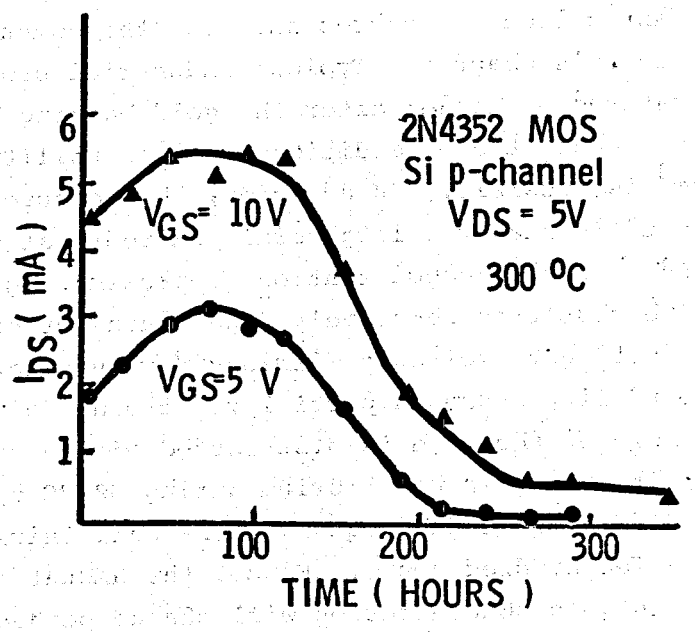


Fig. 21. High temperature aging produced changes in drain-source current with fixed bias.

Failure Modes

Three conditions were responsible for the failures seen during MOSFET aging tests: lead-to-package breaks, mobile impurity ions in gate oxide, and high concentration of gold ions in semiconductors. None of the functional or catastrophic failures seen in MOSFET high temperature aging appear fundamental; that is, changes in the standard fabrication technique should circumvent these failures.

The first indication of an open lead was an infinite resistance reading, usually to the drain pin. Careful package autopsy revealed an aluminum bonding wire lift at the gold drain pad of the package. As described in the chapter on bonding in this report, gold films exist which maintain bond pull strengths to aluminum wire under high temperature aging.

After hundreds of hours of aging at 300°C some devices exhibited several minutes of drain current drift whenever the dc gate voltage was abruptly changed. In addition, if all biasing on the device was removed for several hours, a recovery to "standard" characteristics would occur. These symptoms are associated with mobile impurity ions in the gate oxide; often sodium is the culprit. Since all device production lots tested did not develop this failure mode, it can be assumed that MOSFET devices can indeed be manufactured without the introduction of mobile gate impurity ions.

The presence of a high concentration of gold within the device silicon can be deduced from diffusion constants applied to typical industrial fabrication procedures and from the computer modelling comparisons in this chapter. Typical industrial processing involves 500°C temperatures or higher after the gold backing has been deposited on the wafer. Under these conditions gold solubility in silicon of 10^{14} ions/cm^3 is possible. In addition, the computer model generated the experimentally measured large drain currents at turn-off gate voltages only when gold concentrations approximating 10^{14} ions/cm^3 were included. The resulting relatively high drain current (leakage) even at normally "off" gate voltages eliminated many circuit designs. Thus, high gold solubility caused a partial functional failure for 300°C operation. However the gold is distributed within the transistor after fabrication; it is not in equilibrium during 300°C operation. At this temperature diffusion lengths equal to the chip thickness can be achieved in a few hundred hours. Hence, the amount of gold in solution or gradients in gold concentration will change perhaps by precipitation into particles or interfacial layers. Such an alteration would slowly change conductivities and the gate voltage effectiveness. Such drifts were seen during high temperature operation. Fortunately gold backing is not necessary in MOSFET processing as long as the gate, source, and drain contacts all appear as aluminum pads on the top of the die. Although gold impurities act as trapping centers, they are not the only possible cause of excessive high temperature drain current. The completion and testing of gold-free MOSFETs will help sort out the other causes.

Chapter 2 - Junction Field Effect Transistors

Introduction

Silicon junction field effect transistors (JFET) have become the backbone of Sandia's high temperature microcircuits. This utilization was justified by two test results. First, JFETs displayed drain characteristics with a zero temperature coefficient region, a gate voltage range for which the drain current varies little from 25 to 300°C. Secondly, 300°C aging under bias produced little drift in JFET characteristics over 1000 hours, in marked contrast with the substantial drift seen in MOSFET tests.

This chapter starts with a basic description of JFET operation and parameters incorporated by a computer model which is usable over the complete temperature range. The characteristics generated by the model are then compared with those taken in oven tests. Lastly, the aging test results for JFETs are described.

Computer Model

A simplified view of a typical n-channel Junction Field Effect Transistor (JFET) is given in Figure 22.

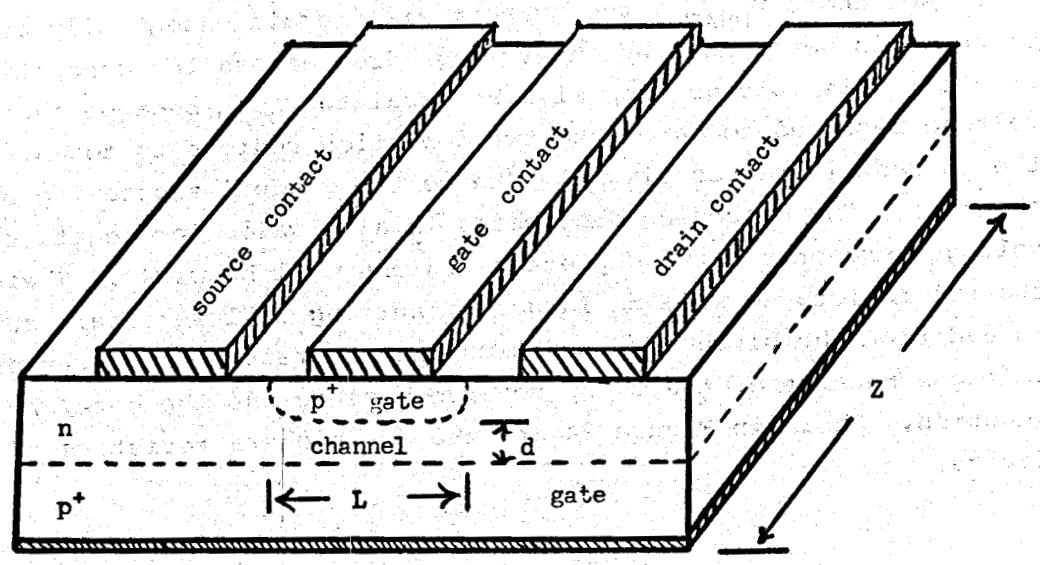
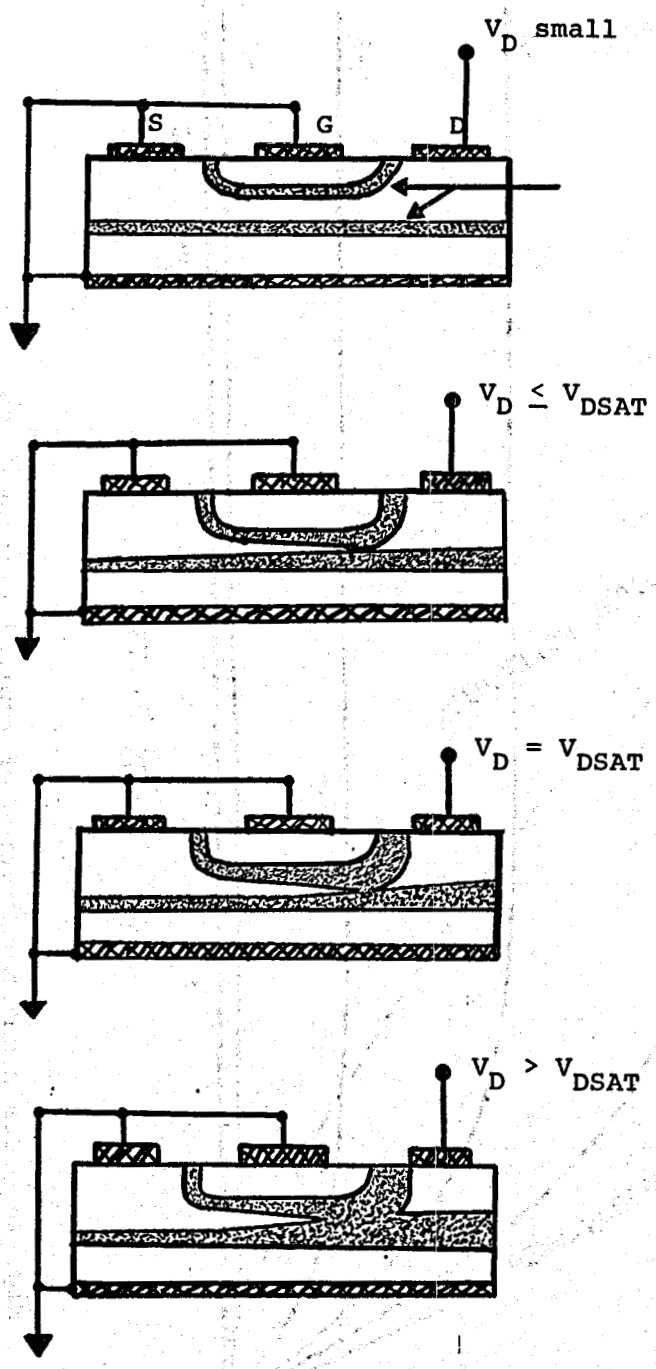


Fig. 22

The top and bottom gates may be electrically connected by a deep p^+ diffusion at the ends of the device. In that case no top metallization is required for the gate contact, simplifying the design and manufacturing processes.

The device operation for the case of zero gate and source voltages is illustrated in Figure 23. If a small, positive voltage is applied to the drain, electrons will flow from the source, through the channel between the two gates, to the drain. As long as the drain voltage remains small the channel acts like a fixed resistor, causing the I_D vs. V_D characteristics to be linear. However, as the drain voltage is increased the gate/channel junction depletion region near the drain widens, causing the cross-sectional area of the channel to decrease and, hence, the resistance of the channel to increase. If the drain voltage is increased to a sufficiently high value the two depletion regions touch, creating a condition called <u>pinch-off</u> or <u>saturation</u>: the voltage at which this occurs is V_{DSAT}. The source and drain electrodes are now completely separated by a reverse biased depletion region, a zone which would not normally conduct unless carriers were generated within or injected into it. In the case of a JFET in saturation the voltage drop between the source and the point in the channel where pinch-off occurs will remain constant and equal to V_{DSAT}. Therefore, the channel between those two points will carry current and the carriers arriving at the pinch-off point will be injected into the depletion region and drift to the drain contact. If the drain voltage is raised above V_{DSAT}, the current will remain essentially constant since it is determined by the voltage drop across the conducting channel; this voltage drop will be equal to V_{DSAT} because that is the voltage required to cause the two depletion regions to touch. (Actually the current increases slightly due to the gradual shortening of the channel). The preceding discussion is also valid for negative gate voltages except the two depletion regions will be wider. Therefore, the channel resistance will be larger, resulting in lower drain currents. In addition the pinch-off condition will be reached at lower drain voltages because of the added reverse bias across the gate/channel junction. Shown in Figure 24 are the drain characteristics of a typical device.



A. LINEAR OPERATING REGION

B. CHANNEL RESISTANCE INCREASES AS THE DRAIN VOLTAGE IS INCREASED

C. PINCH-OFF

D. DEVICE OPERATING IN THE SATURATION REGION

OPERATION OF AN N-CHANNEL JFET WITH $V_G = V_S = 0$

Fig. 23

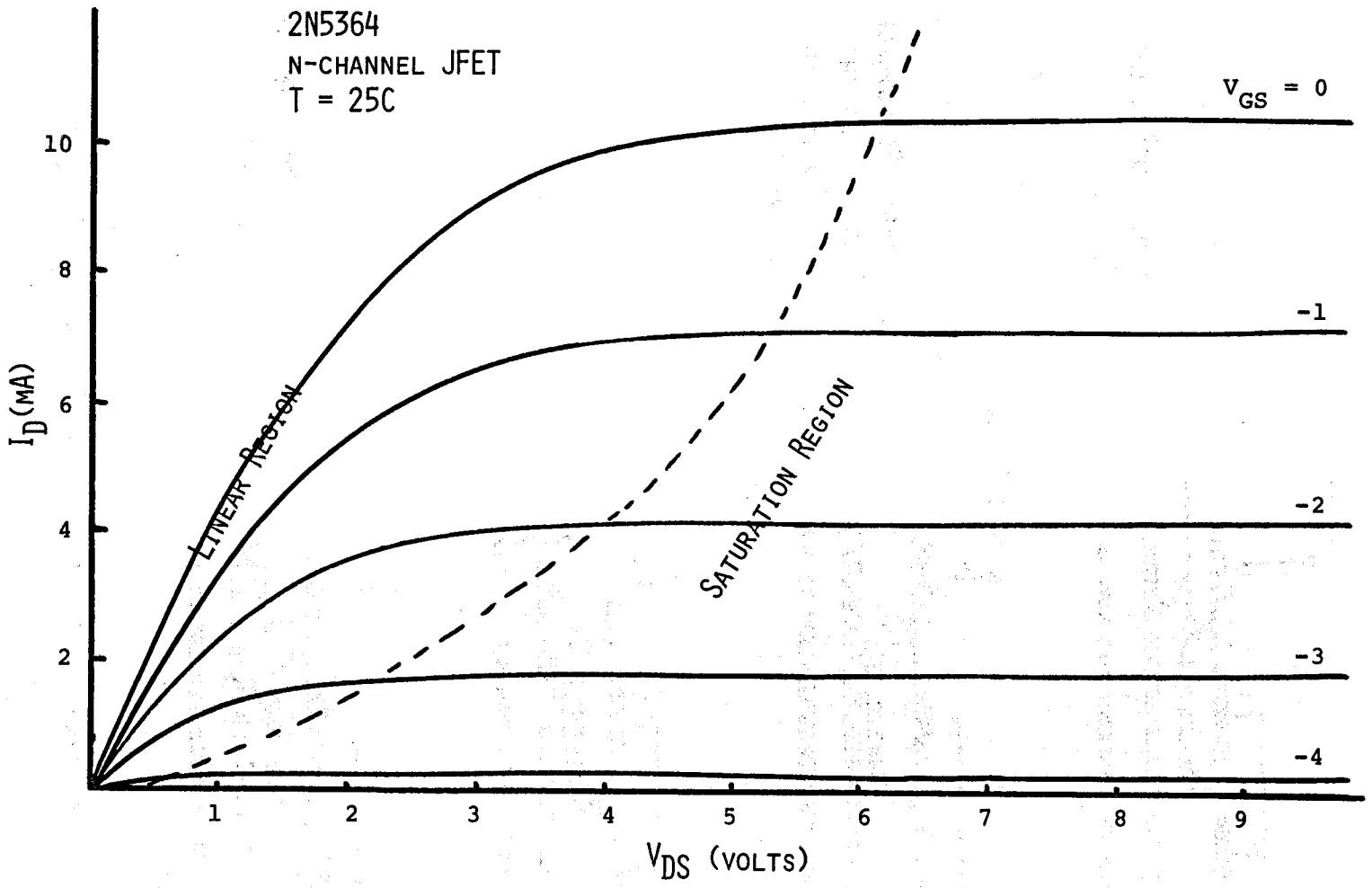


Fig. 24. Drain characteristics of typical n-channel JFET. As with the MOSFETs both a linear and saturation region exist.

Drain Current

The standard equation relating the gate and drain voltages to the drain current in an ideal n-channel JFET is[13]

$$I_D = \frac{zq\mu_n N_D d}{L}\left\{V_{DS} - \frac{4}{3d}\sqrt{\frac{2\varepsilon_s}{qN_D}}\left[(V_{DS} + V_{bi} - V_{GS})^{3/2} - (V_{bi} - V_{GS})^{3/2}\right]\right\} ,$$

$$V_{DS} \leq V_{DSAT} \ , \ V_{GS} \geq V_T \text{ (Turn-off Voltage) } ;$$

V_{bi} is the built-in voltage of the gate/channel junction and N_D is the donor doping concentration in the channel. Unlike the MOS transistor, the JFET has regions near the source and drain whose resistances are not under gate control. As can be seen in Figure 25, the existence of these zones causes the voltages at the beginning and end of the channel to be different than the terminal voltages.

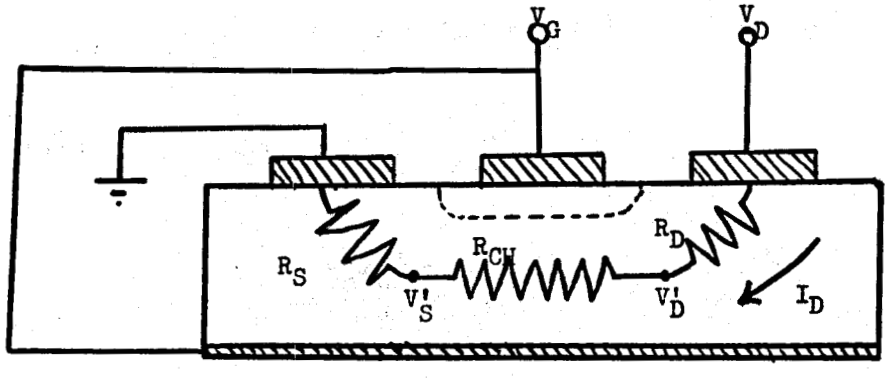


Fig. 25. Schematic illustration of resistances inherent in JFETs.

$$V_S' = I_D R_S \ , \ V_D' = V_D - I_D R_D$$

so that

$$V_{GS}' = V_G - V_S' = V_G - I_D R_S$$

and

$$V_{DS}' = V_D' - V_S' = V_D - I_D(R_S + R_D) \ .$$

The expression for the drain current may now be rewritten as

$$I_D = \frac{zq\mu_n N_D d}{L}\left\{V_D - I_D(R_S + R_D) - \frac{4}{3d}\sqrt{\frac{2\varepsilon_s}{qN_D}}\left[(V_D - I_D(R_S + R_D) + V_{bi} - V_G + I_D R_S)^{3/2} - (V_{bi} - V_G + I_D R_S)^{3/2}\right]\right\}$$

or

$$I_D = \frac{zq\mu_n N_D d}{L}\left\{V_D - I_D(R_S + R_D) - \frac{4}{3d}\sqrt{\frac{2\varepsilon_s}{qN_D}}\left[(V_D - I_D R_D + V_{bi} - V_G)^{3/2} - (V_{bi} - V_G + I_D R_S)^{3/2}\right]\right\} .$$

In order to evaluate this expression, an iteration scheme using the Newton-Rapheson method was set up to find the zero of the function

$$G(I_D) = I_D - C_1\left\{V_D - I_D(R_S + R_D) - C_2\left[(V_D - I_D R_D + V_{bi} - V_G)^{3/2} - (V_{bi} - V_G + I_D R_S)^{3/2}\right]\right\} ,$$

where

$$C_1 = \frac{zq\mu_n N_D d}{L}$$

and

$$C_2 = \frac{4}{3d}\sqrt{\frac{2\varepsilon_s}{qN_D}} .$$

The slope of G at any point is given by

$$S \equiv \frac{\partial G}{\partial I_D} = 1 - C_1\left\{- (R_S + R_D) + \frac{3C_2}{2}\left[R_D(V_D - I_D R_D + V_{bi} - V_G)^{1/2} + R_S(V_{bi} - V_G + I_D R_S)^{1/2}\right]\right\} .$$

Given V_D, V_G, and a first guess for I_D, the next approximation to the root is

$$I_{D(2)} = I_{D(1)} - \frac{G\left(I_{D(1)}\right)}{S\left(I_{D(1)}\right)} .$$

The cycle can be repeated until the desired accuracy is obtained. In the computer model the iteration was terminated when $G\left(I_{D(n)}\right)$ was less than 5×10^{-8}.

At this point it should be pointed out that these equations apply exactly only for the case of a step junction at the gate and uniform doping in the channel. However, it has been shown[14,15] that the device characteristics are nearly independent of the doping profiles.

Saturation Region

The equation for the width of the depletion region of a one-sided step junction is

$$W = \sqrt{\frac{2\varepsilon_S}{qN_D}\,(V_{bi} + V_{rev})} ,$$

where V_{rev} is the reverse bias across the junction. The channel is pinched off when each depletion region extends halfway into the channel:

$$\frac{d}{2} = \sqrt{\frac{2\varepsilon_S}{qN_D}\,(V_{bi} + V_D' - V_G)} = \sqrt{\frac{2\varepsilon_S}{qN_D}\,(V_{bi} + V_D - I_D R_D - V_G)} .$$

Solving for $V_D = V_{DSAT}$ yields

$$V_{DSAT} = \frac{d^2 qN_D}{8\varepsilon_S} + V_G + I_D R_D - V_{bi} .$$

Substituting the value $V_{DS}' = \frac{d^2 qN_D}{8\varepsilon_S} + V_G - V_{bi} - I_D R_S$ back into the expression for I_D gives the saturation current

$$I_{DSAT} = \frac{zq\mu_n N_D d}{L}\left\{\left[\frac{4}{3d}\sqrt{\frac{2\varepsilon_S (V_{bi} - V_G + I_D R_S)}{qN_D}} - 1\right](V_{bi} - V_G + I_D R_S) + \frac{qN_D d^2}{24\varepsilon_S}\right\} .$$

This equation was also evaluated using the Newton-Rapheson iteration scheme.

$$G(I_D) = I_D - C_1\left\{\left[C_2\sqrt{V_{bi} - V_G + I_D R_S} - 1\right](V_{bi} - V_G + I_D R_S) + C_3\right\}$$

where

$$C_1 = \frac{zq\mu_n N_D d}{L}, \quad C_2 = \frac{4}{3d}\sqrt{\frac{2\varepsilon_s}{qN_D}} \text{ and } C_3 = \frac{qN_D d^2}{24\varepsilon_s}.$$

$$S(I_D) \equiv \frac{\partial G}{\partial I_D} = 1 - C_1 R_S\left[\frac{3C_2}{2}(V_{bi} - V_G + I_D R_S)^{1/2} - 1\right].$$

Then

$$I_{D(n)} = I_{D(n-1)} - \frac{G\left(I_{D(n-1)}\right)}{S\left(I_{D(n-1)}\right)}.$$

Turn-Off

It is possible to cause the entire channel to become depleted if a large enough negative bias is applied to the gate. This voltage is called the turn-off voltage, V_T. By using the equation for the width of the depletion region of a one-sided step junction, V_T can be calculated to be

$$V_T = V_{bi} - \frac{qN_D d^2}{8\varepsilon_S}.$$

Drain and Source Resistances

The resistance of an n-type semiconductor sample is

$$R = \frac{L}{q\mu_n nA},$$

where L and A are the length and cross-sectional area of the sample, respectively, and n is the electron concentration. If the source and drain resistances are specified at room temperature (300°K), then the resistances at any temperature can be found from

$$R_{S,D}(T) = R_{S,D,300}\,\frac{\mu_{n,300}N_D}{\mu_{n,T}(N_D + n_i)}.$$

The factor $N_D/(N_D + n_i)$ arises from the fact that at room temperature nearly all of the donors are ionized and $n_i << N_D$. At elevated temperatures, however, the intrinsic carrier concentration may not be negligible compared to the doping concentration so that $n = N_D + n_i$.

Junction Built-In Voltage, V_{bi}

Shown in Figure 26 is a simplified band diagram of a p^+n junction under equilibrium conditions.

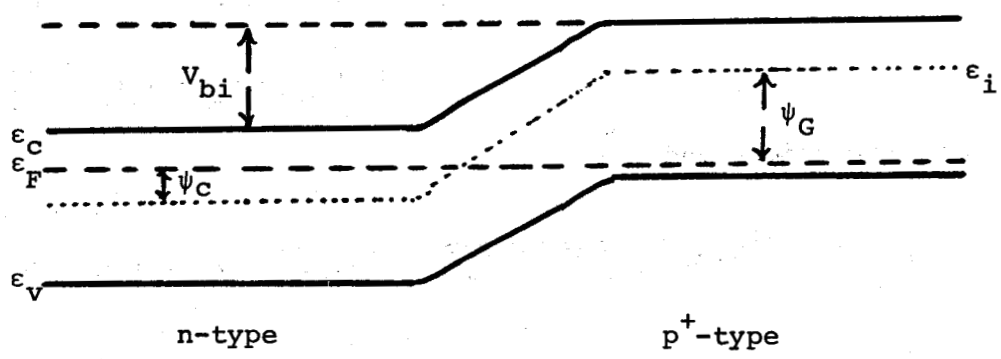


Fig. 26. Band diagram illustrating built-in voltage, V_{bi}.

ψ_c and ψ_G are the Fermi potentials in the channel and gate regions, respectively. Following the equations set forth in the MOSFET section of this report, the Fermi potentials are

$$\psi_c = \frac{KT}{q} \ln\left\{\frac{N_D + \sqrt{N_D^2 + 4n_i^2}}{2n_i}\right\},$$

$$\psi_G = \frac{KT}{q} \ln\left\{\frac{N_A + \sqrt{N_A^2 + 4n_i^2}}{2n_i}\right\},$$

and $V_{bi} = \psi_c + \psi_G$, where N_D and N_A are the donor and acceptor concentrations in the channel and gate regions, respectively. A plot of Fermi potential versus temperature is given in the MOSFET section.

Mobility and Other Temperature Dependent Terms

The bulk mobility expressions presented in the MOSFET section of this paper were used to describe the channel mobilities in the JFET. Equations for the intrinsic carrier concentration and band gap shrinkage were also used without modification.

P-Channel JFETs

The equations for the p-channel device characteristics are very similar to those of the n-channel JFET. In normal operation the p-channel JFET has positive gate voltages and negative drain voltages. The charge carriers are holes, hence the device conducts in the opposite direction. However, if the current is defined as positive when the carriers (holes) flow from source to drain, then

$$I_D = C_1\left\{-V_D - I_D(R_S + R_D) - C_2\left[(-V_D - I_DR_D + V_{bi} + V_G)^{3/2} - (V_{bi} + V_G + I_DR_S)^{3/2}\right]\right\}$$

below saturation, and

$$I_{DSAT} = C_1\left\{\left[C_2\sqrt{V_{bi} + V_G + I_DR_S} - 1\right](V_{bi} + V_G + I_DR_S + C_3)\right\},$$

where C_1, C_2, and C_3 have the same meanings as before. The saturation and turn-off voltages are given by

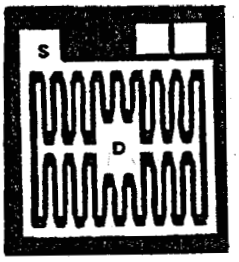
$$V_{DSAT} = -\frac{qN_Ad^2}{8\varepsilon_s} + V_{bi} + V_G - I_DR_D$$

and

$$V_T = \frac{qN_Ad^2}{8\varepsilon_s} - V_{bi}\ .$$

Comparison of Measurement to Model

The 2N4391 n-channel JFET was selected for the purpose of comparing the model to experimental data. Shown in Figure 27 is a diagram of the top surface of a 2N4391 chip.[16] Connection to the gate is made to the back plane.



S = 2.6 x 2.6 mils

D = 3.2 x 2.7 mils

G = substrate

Fig. 27. Electrode geometry for Motorola 2N4391 geometry.

The chip dimensions are 19 by 19 mils. The gap between the source and drain fingers is 10.6 μm in all cases. Allowing 2 μm between the drain/source regions and the gate diffusion leaves approximately 6 μm for the channel length. The total width, z, of the channel found by summing the lengths of all of the fingers is 3206 μm.

The gate junction breakdown voltage was found to be 62 volts. Doping concentrations can be directly related to breakdown fields.[17,18] If the radius of curvature at the ends of the gate region is assumed to be 3 μm (typical for this type of device with these dimensions), then a breakdown voltage of 62 V corresponds to a doping concentration of 5×10^{15} cm^{-3}. The turn-off voltage at room temperature was measured to be -5.6 volts. Knowing V_T and N_D, the channel depth can now be calculated.

$$V_T = \frac{-qN_D d^2}{8\varepsilon_s} + V_{bi}$$

or

$$d = \sqrt{\frac{(V_{bi} - V_T)\,8\varepsilon_s}{qN_D}} = 2.577\ \mu m\ .$$

The only remaining device parameters are the source and drain resistances. Recall that for a given gate voltage the I_D vs. V_D characteristics are linear for small drain voltages. The reciprocal of the slope in the linear region corresponds to the total resistance of the device. For the 2N4391

$$I_D = 13.1\ mA \text{ at } V_{GS} = 0.00\ V,\ V_{DS} = 0.50\ V\ .$$

(Linear region operation was verified by an inspection of the drain characteristics.) This implies a device resistance of 38.2 Ω. The channel conductance in the linear region for $V_G = 0$ is

$$g = \frac{zq\mu_n N_D d}{L}\left[1 - \sqrt{\frac{8\varepsilon_s V_{bi}}{qN_D d^2}}\right] = 9.215 \times 10^{-2}\ \mho\ .$$

The 2N4391 is a symmetrical device (the source and drain leads may be interchanged) so that

$$R_S = R_D = \frac{38.2\Omega - 1/g}{2} = 14\ .$$

The device parameters are summarized below.

Parameter	Symbol	Value
Channel length	L	6 μm
Channel width	z	3206 μm
Channel depth	d	2.577 μm
Source Resistance	R_S	14 Ω
Drain Resistance	R_D	14 Ω

Theoretical and experimental results are given on the following pages. Model agreement with the measured data is very good: the model follows the observed temperature dependence of drain current and threshold voltage quite well (see Fig. 28). The zero temperature coefficient (zTC) point is quite evident on the graphs. If the device is biased with gate voltage less negative, thermal runaway is impossible. A rise in temperature caused by internal power dissipation causes a reduction in drain current. This, in turn, brings about a reduction in the power dissipation and eliminates the possibility of any further increase in temperature. On the other hand, a device biased with gate voltage more negative may be unstable. Heating of the device caused by internal power dissipation would effect an <u>increase</u> in drain current and more internal heating.

From the comparison of model to measurement, it is obvious that the 2N4391 is performing according to its design at elevated temperatures. Figures 29 and 30 show the theoretical model results of using the 2N4391 geometry, but changing the channel doping concentration slightly. In all three cases the zero temperature coefficient point occurs at a drain current of approximately 1 mA but at different gate voltages. As a rule, the zero temperature coefficient point should occur at more negative gate voltages as the channel doping concentration is increased; obviously the same is true of the turnoff voltage. The magnitude of the change in current with increasing temperature is less for the device with low doping; however, the 0.40 ratio of peak current at 275°C to peak current at room temperature is approximately the same for all three doping levels.

For comparison purposes the theoretical transfer characteristics for a p-channel version of the 2N4391 are given in Figure 31. Because of the lower mobilities involved the drain currents are lower and the internal resistances are higher. The currents in the p-channel device also show a larger temperature dependence.

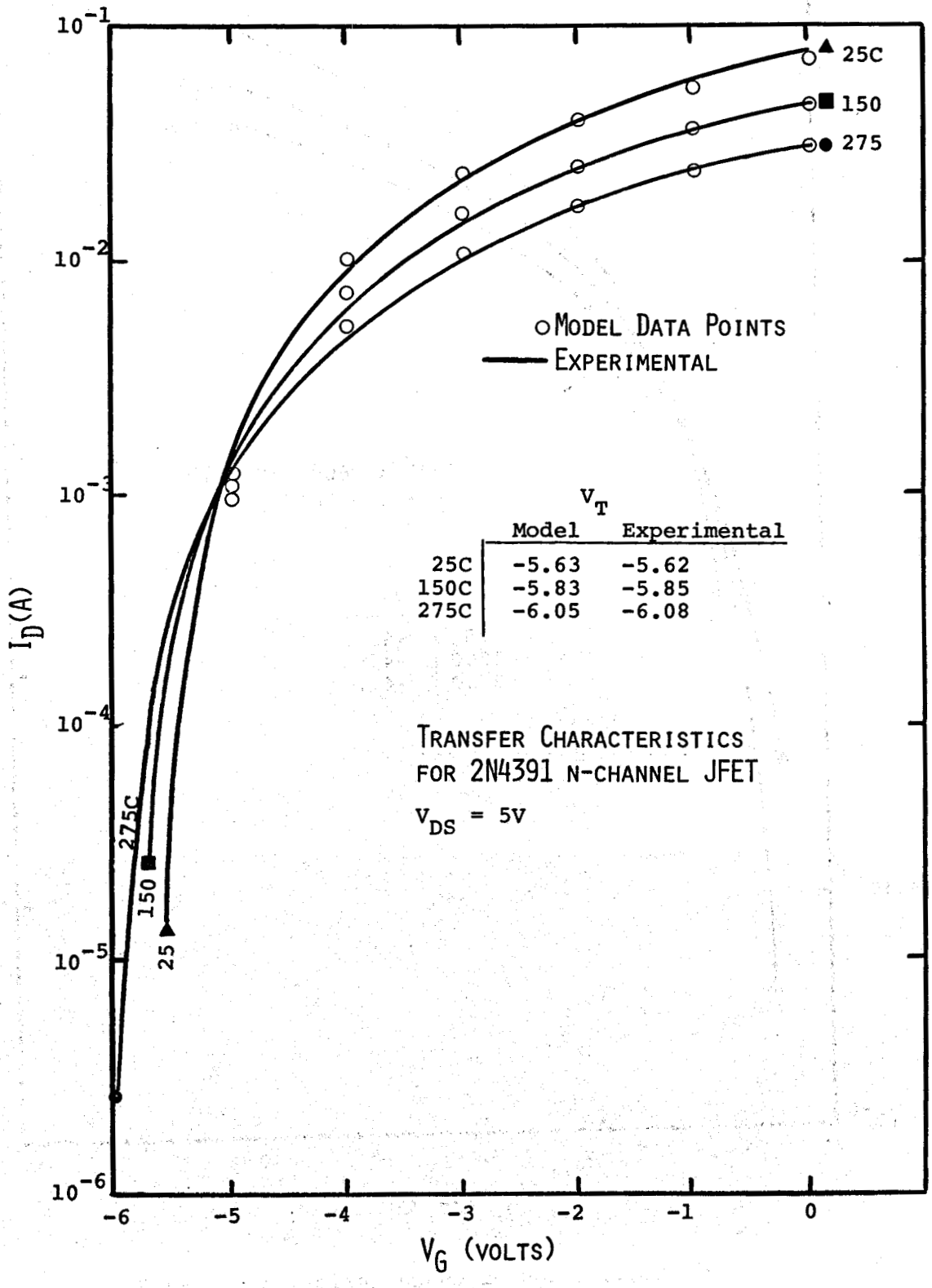


Fig. 28. Comparison of model and experimental transfer characteristics.

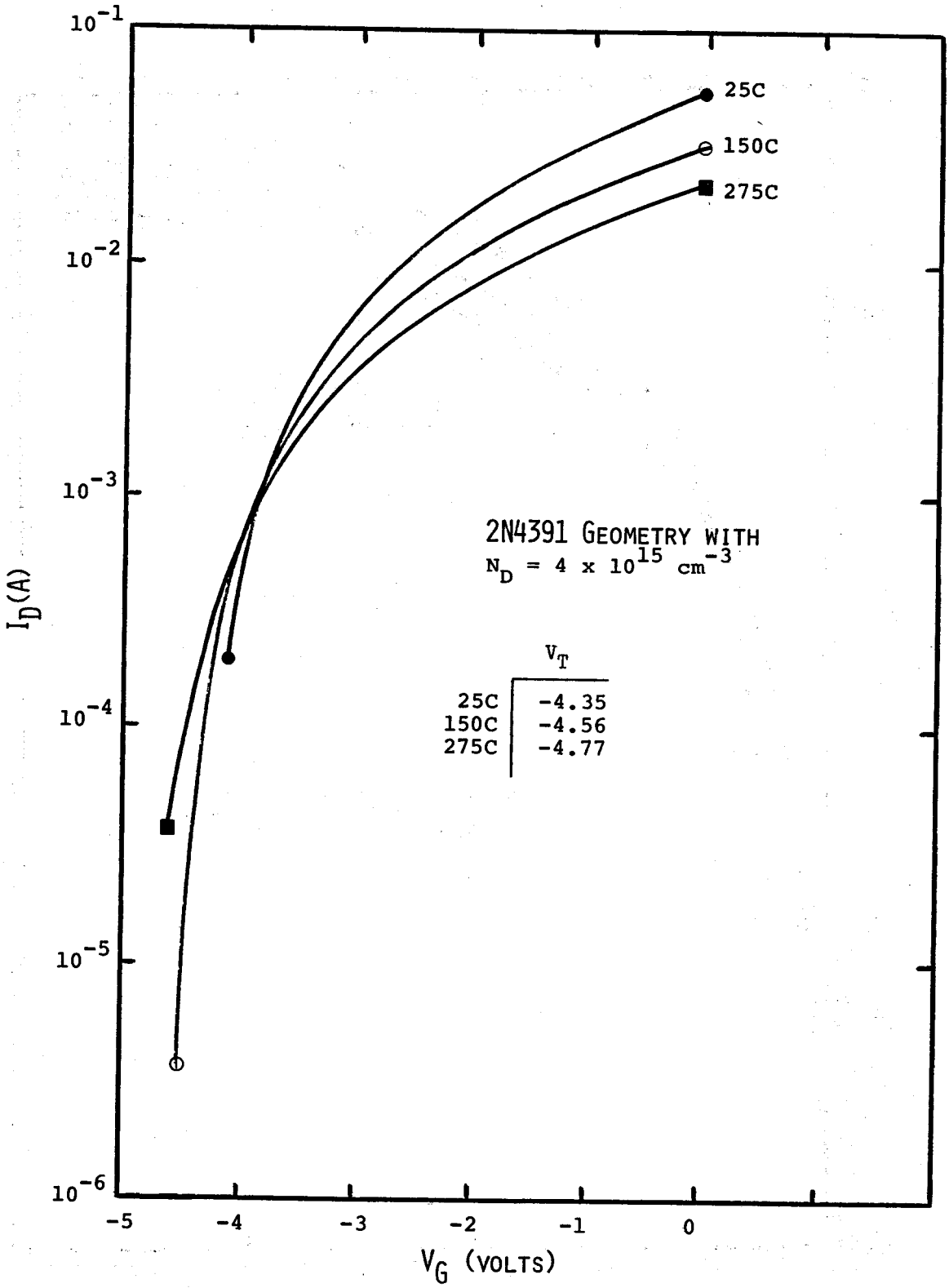


Fig. 29. Theoretical transfer characteristics of 2N4391 with $N_D = 4 \times 10^{15}$ cm^{-3}.

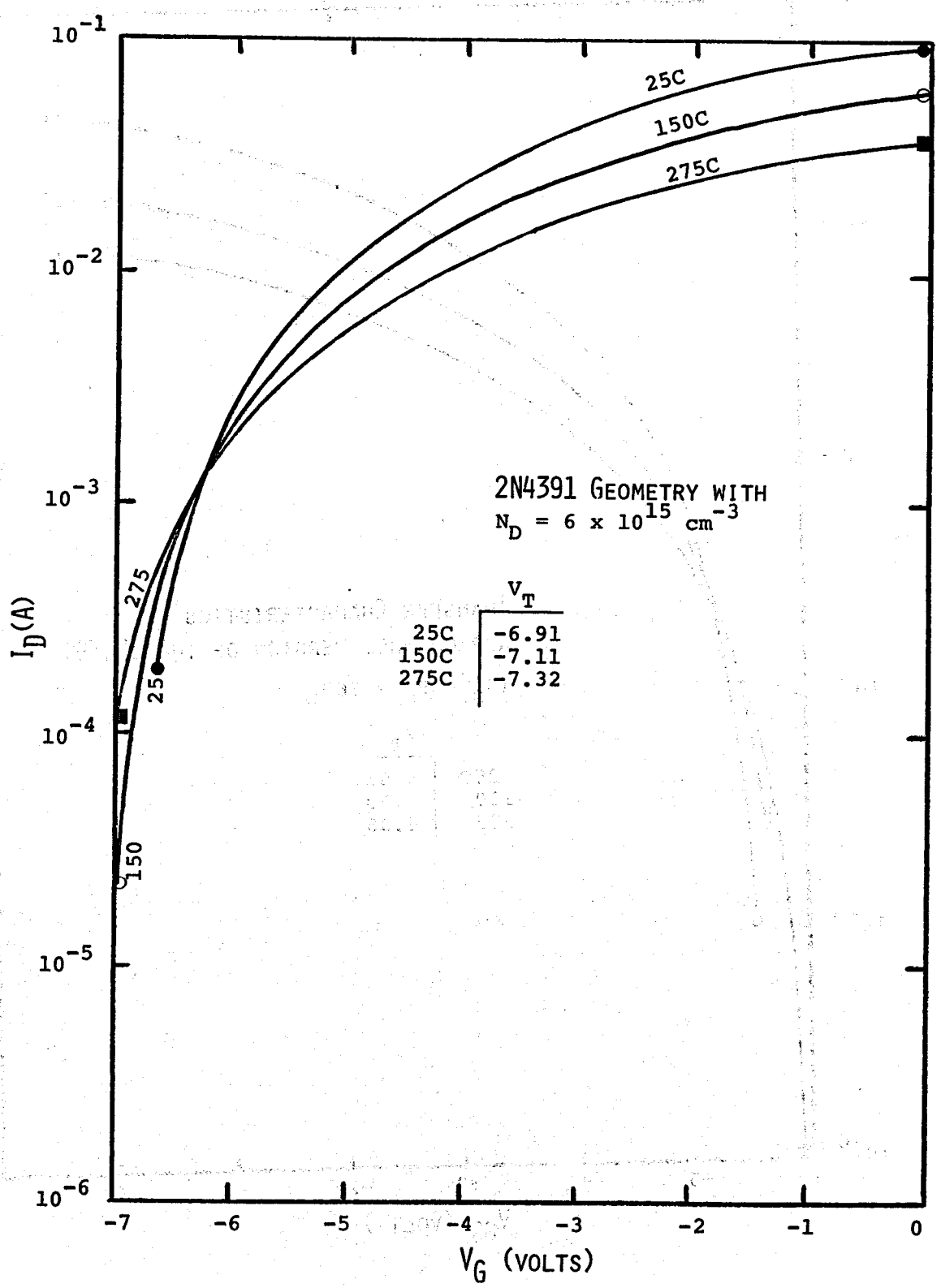


Fig. 30. Theoretical transfer characteristics of 2N4391 with $N_D = 6 \times 10^{15}$ cm^{-3}.

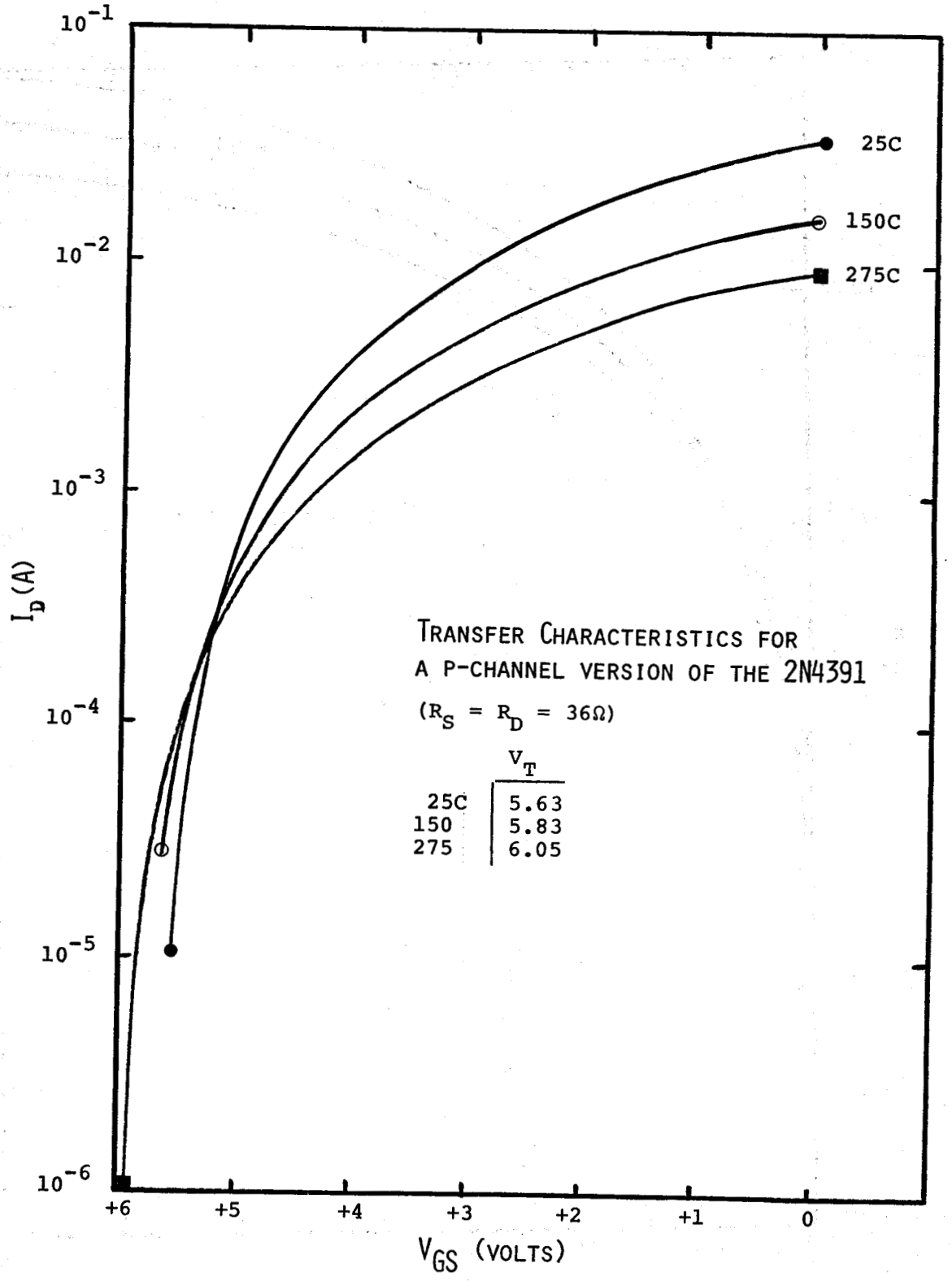


Fig. 31. Theoretical transfer characteristics of p-channel version of 2N4391.

Figure 32 shows the model output for an n-channel JFET of a different design:

$$N_D = 10^{16}\ cm^{-3}$$

$$L = 6\ \mu m$$

$$z = 1000\ \mu m$$

$$d = 2\ \mu m$$

$$R_S = R_D = 5\ \Omega$$

The zero temperature coefficient point for this device occurs at a lower drain current than in the 2N4391 (this could be a disadvantage in some amplifier circuits). However, the variation of drain current with temperature is lower for this device. A range of compromise is available for designing devices for wide temperature range use.

High Temperature Aging of JFETs

The drift of electrical parameters with high temperature aging of JFET silicon devices was small enough to allow extended operation of analog circuits. The results of five p-channel JFET 2N5270s placed under a 5-volt bias during 300°C aging in a forced air oven are typical. Characteristics were taken at 24-hour intervals for 1000 hours. The aging and test circuits are shown in Figure 33. For gate voltages from 0 to 5 V there was at most a few percent drift in I_{DS} during this test. No device failures occurred.

Other aging tests were run on 2N4856 and 2N4220 n-channel devices. Again, no catastrophic failures were noted, but one set of tests run at Clemson University[19] detected a substantial increase in pinchoff current during a few hundred hours of the 1000-hour test. No physical cause of this intermittent change is known.

The Sandia high temperature circuit for the platinum thermometer logging tool involves 25 JFETs. To date four such complete circuits have been fabricated and exposed to 300°C oven and field tests. In addition, numerous circuit subsystems (voltage regulators, line drivers) have been assembled to undergo oven cycle and aging tests in order to ascertain circuit reliability. Therefore, a total of several hundred circuit-committed JFETs have each operated for 200+ hours at 300°C under bias without device failure or significant drift. Rigorous inspection and electrical high temperature prescreening, as described in Chapter 6 of this report, certainly contributed to this performance record. To

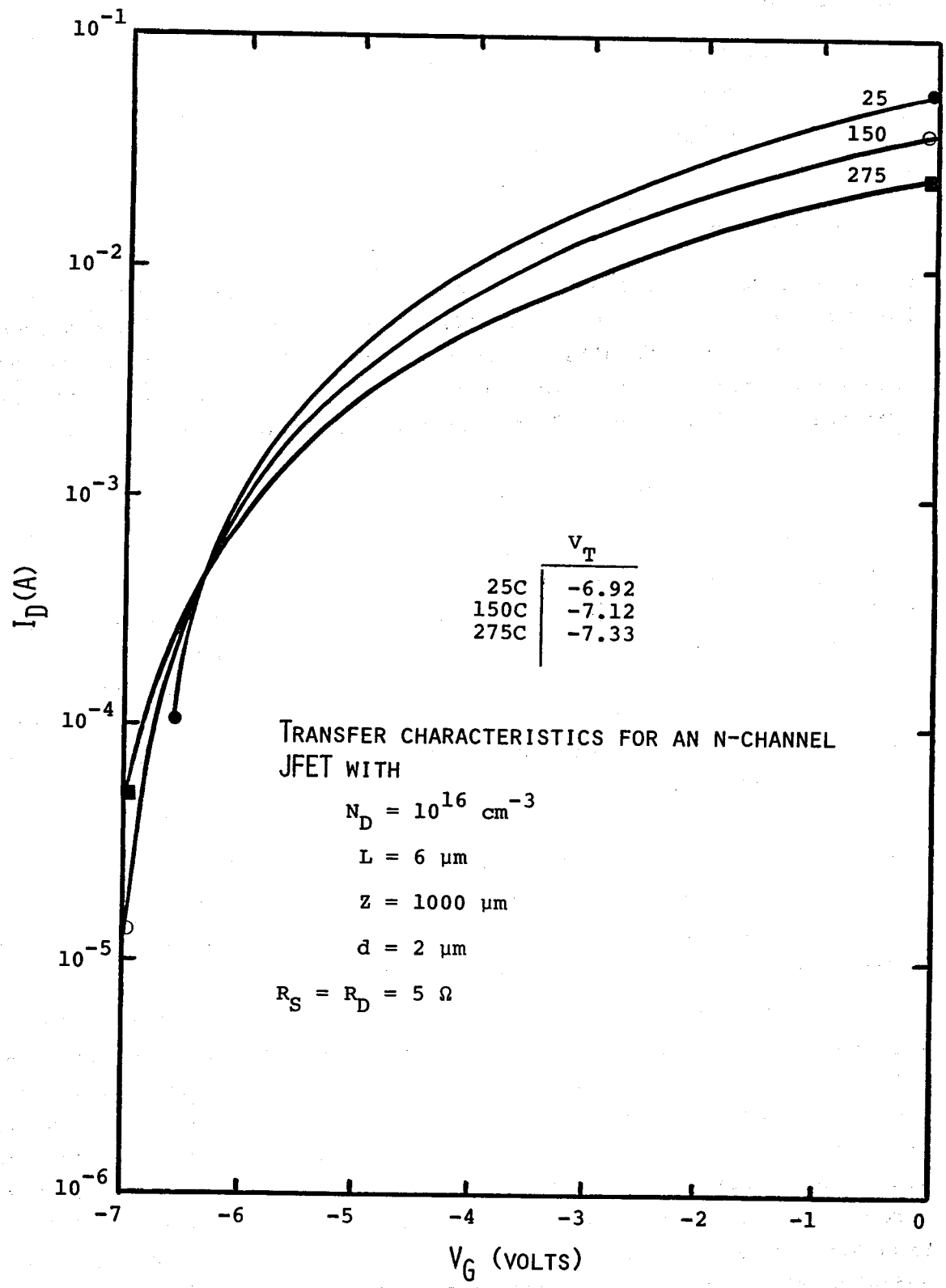


Fig. 32. Theoretical transfer characteristics of redesigned JFET.

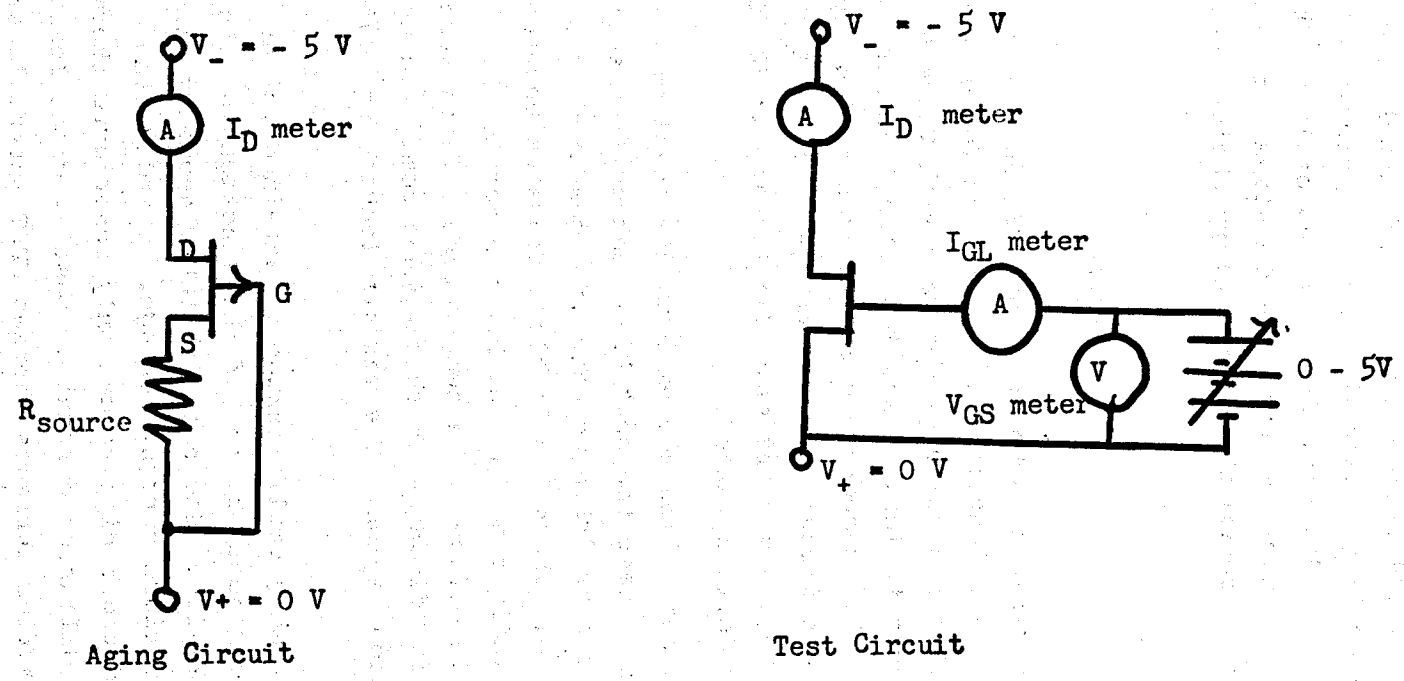


Fig. 33. Circuits used to age and monitor JFETs under bias conditions.

date, devices used in circuits and reliability tests are: 2N4220, 2N4391, 2N3994, 2N5270, BT4856, 2N3823, and U403.

Due to some initial reliability problems with chips from several manufacturers, all devices now used are supplied by Motorola. Their product reliability during this hybrid microcircuit development has been excellent. However, the use of Motorola product should not be interpreted as resulting from an exhaustive search of manufacturers, but rather as a continuing satisfactory choice based on little initial data.

LEAKAGE

The test circuit shown in Figure 33 was used to measure the gate to drain leakage as a function of temperature for n-channel JFETs 2N4391 and MMF-2. The bias voltages were set with $V_{GS} = 0$ and $V_D = +2.5$. In both cases the gate leakage was less than 1 μA for temperatures below 200°C. Above this temperature the leakage scaled approximately as a standard silicon diode; that is, with a slope of $E_g/2k$ showing domination by depletion region generation. The leakage at 300°C was between 27 and 55 μA for the devices tested.

A second set of leakage experiments involved the n-channel JFET 2N4220. In this case the back bias leakage from source to gate, drain to gate, and source-drain to gate were measured as a function of voltage and temperature. There was little difference between these three measurements indicating that either contact to the n-region addressed the total np interface. The temperature effects were again similar to ordinary silicon diodes with the leakage dominated by thermal generation in the depletion region. The maximum leakage at 300°C (5V bias) was 8 μA.

This extremely small leakage is attained for at least four reasons. First, the cross section area of the junction is rather small, 30 square mils for the 2N4220. Secondly, the JFET geometry eliminates most opportunities for surface current leakage. Thirdly, the channel material is fully depleted under bias so can only contribute thermal generation currents--not diffusion currents. Lastly, diode leakage current depends on minority carrier currents whereas JFET materials are purposely fabricated to facilitate majority, not minority, carrier currents.

CHAPTER 3 - BIPOLAR DEVICES

Introduction

When first contemplating 300°C electronics, it was hoped that bipolar silicon devices could be utilized. These devices would be advantageous for the following reasons: most diodes used in solid state circuits are bipolar; bipolar transistors are available for high frequency and high power operation; bipolar devices are available as chips, hermetic cans, and gold beam leaded format; bipolar devices are ubiquitous in integrated chips as electrostatic input protection diodes, as junction isolation regions and as circuit devices; and lastly, many standard circuit designs already exist in bipolar dress.

There was expectation for high temperature performance of silicon bipolar devices for several reasons. First, manufacturer specifications showed continuous operational junction temperatures of 200°C for many bipolar device types; much closer to geothermal temperature limits than most other components. Secondly, standard bipolar geometries involve little temperature dependent surface states or troublesome thin oxide layers. In contrast, there existed good reason to suspect loss of functionality at high temperature; the Shockley bipolar diode equation has an exponential dependence on temperature of the leakage current, a clear impediment to circuit design. In this chapter we will briefly present the formulas describing the operation of bipolar diodes and transistors and compare these to experimental measurements made up to 300°C. Results of the high temperature aging tests will also be discussed. Despite the drastic temperature dependences, several modes of bipolar device utilization will be presented.

Bipolar Diodes

The standard formula for the current density in a bipolar diode is

$$J = J_s(e^{qV/kT} - 1)$$

where $J_s = qD_p p_{no}/L_p + qD_n n_{po}/L_n$. In this expression, D is the carrier diffusion coefficient, L is the carrier diffusion length, and p_{no} is the hole concentration in the n-type semiconductor in thermal equilibrium. Unfortunately, D, L, and p(n) are temperature dependent:

$$p_{no} \sim T^3 \exp(-E_g/kT)$$

$$D = (kT/q)\mu \sim T^{-0.6} .$$

L has a small but complicated dependence which in general is experimentally rather than theoretically determined. In this derivation, L is taken as increasing in temperature. With these dependences the current equation becomes

$$J_s = T^n \exp(-E_g/kT), \quad n < 4 .$$

It is clear that the extent of temperature dependence is almost entirely determined by the size of the energy gap. Thus, design changes in geometry or doping profiles will do little to ameliorate the extreme temperature dependence of bipolar diodes as compared with a change of the basic semiconducting material to one of larger energy gaps (such as GaAs). Essentially, for reverse bias, the current increases as $\exp(-E_g/kT)$ with temperature, and in the forward direction one gets approximately an $\exp[-(E_g - qV)/kT]$ dependence. In Figure 34 the measured diode leakage currents are plotted versus 1/T to compare the slope of the data with $-E_g/k$. For silicon diodes the results compare best with an analytic slope of $E_g/2k$. In silicon diodes the reverse saturation current is often due to generation current in the depletion layer. As shown in Chapter 1, this current varies only as the first power of n_i or $\exp[E_g/2kT]$.

Given this large but predictable temperature dependence, diodes can still be used in some circuits. For example, silicon diodes have been used in circuits as rectifiers up to 300°C, albeit with much leakage. A series connected positive coefficient thermistor can be used to help temperature stabilize a silicon rectifier. As another application, the forward biased characteristics of diodes have been utilized as linear temperature transducers (see Fig. 35). Thirdly, despite the change in breakdown voltage and some loss in breakdown voltage distinctness over the temperature range, voltage regulation by zeners is possible up to 300°C. The breakdown voltage for zener diodes undergoes a 10% change from 25 to 300°C. Some zener types (Raytheon beam leaded BZ821) have built-in temperature compensation which is of some help for extended temperature operation. This compensation is achieved by using back-to-back diodes so that the change in forward characteristics with temperature compensate the change in reverse breakdown (see Figs. 34, 36).

Once the circuit has been made tolerant to the diode temperature dependences, the next most important consideration becomes the aging properties of the diode. For the most part, high temperature aging depends on the diode packaging. Discrete high voltage, high power diodes are packaged with extreme junction temperature operation in mind.

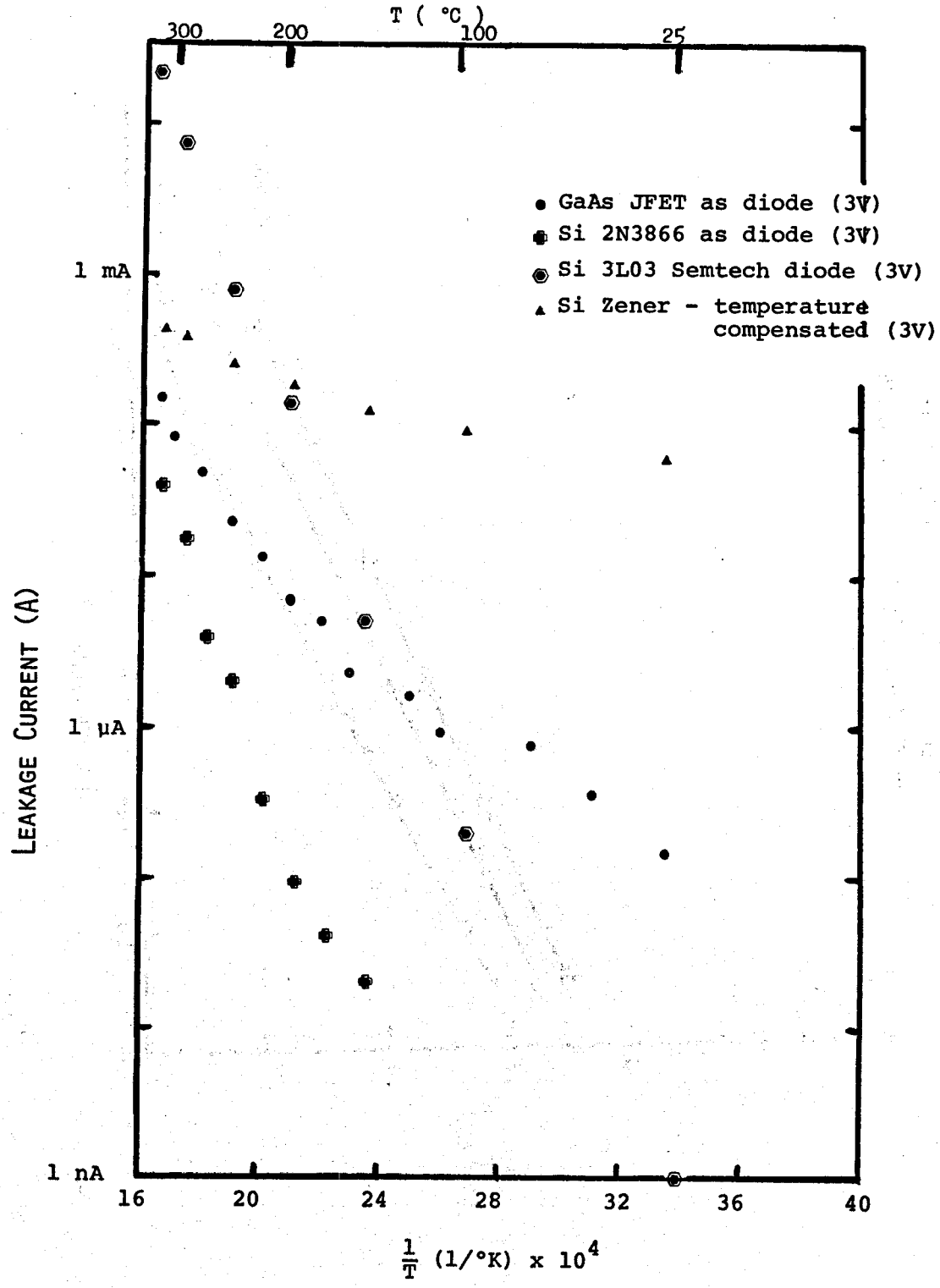


Fig. 34. Reverse saturation current measured at 3 Vdc is plotted as 1/T for various diodes.

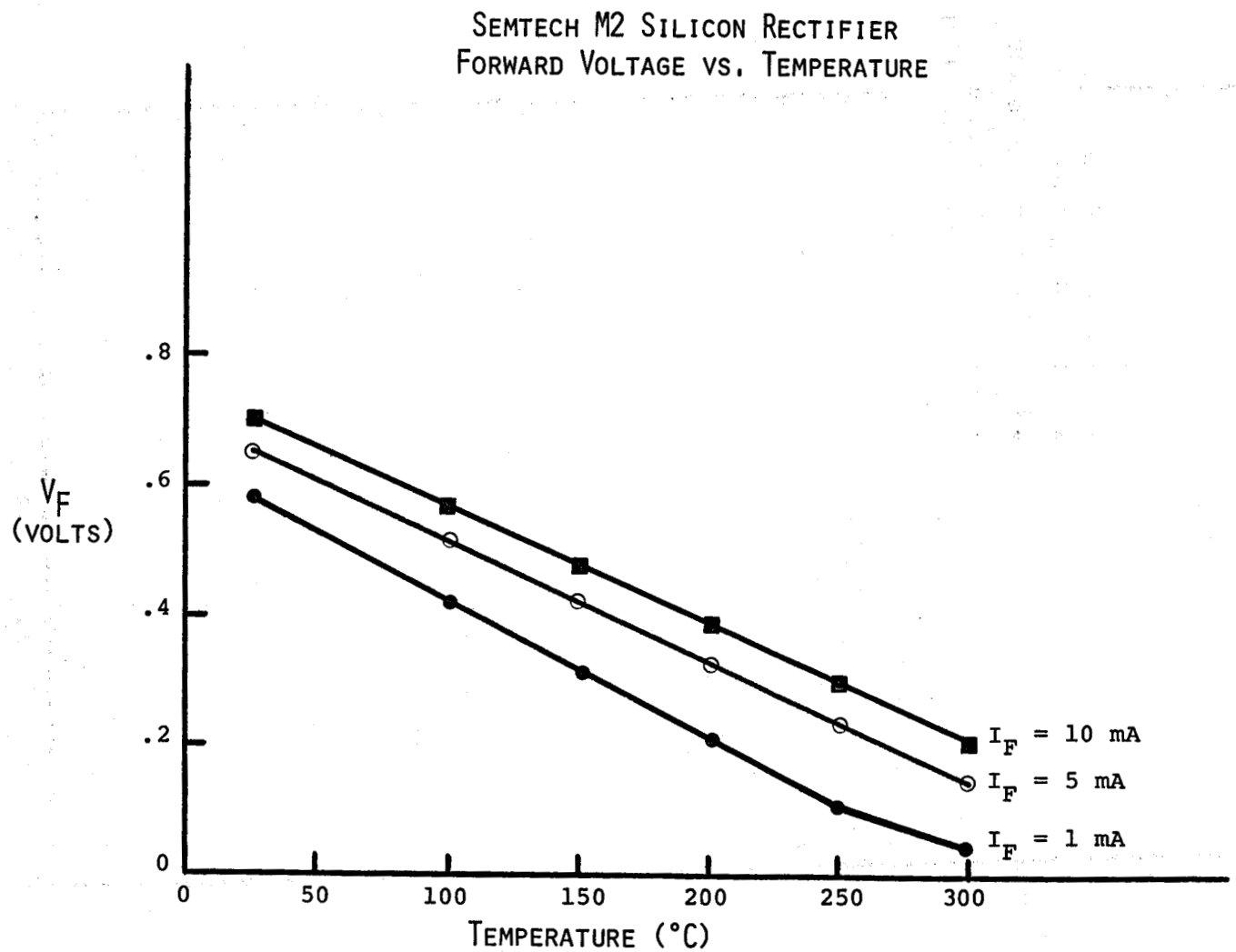


Fig. 35. At constant current there is a linear decrease in diode forward voltage with increasing temperature.

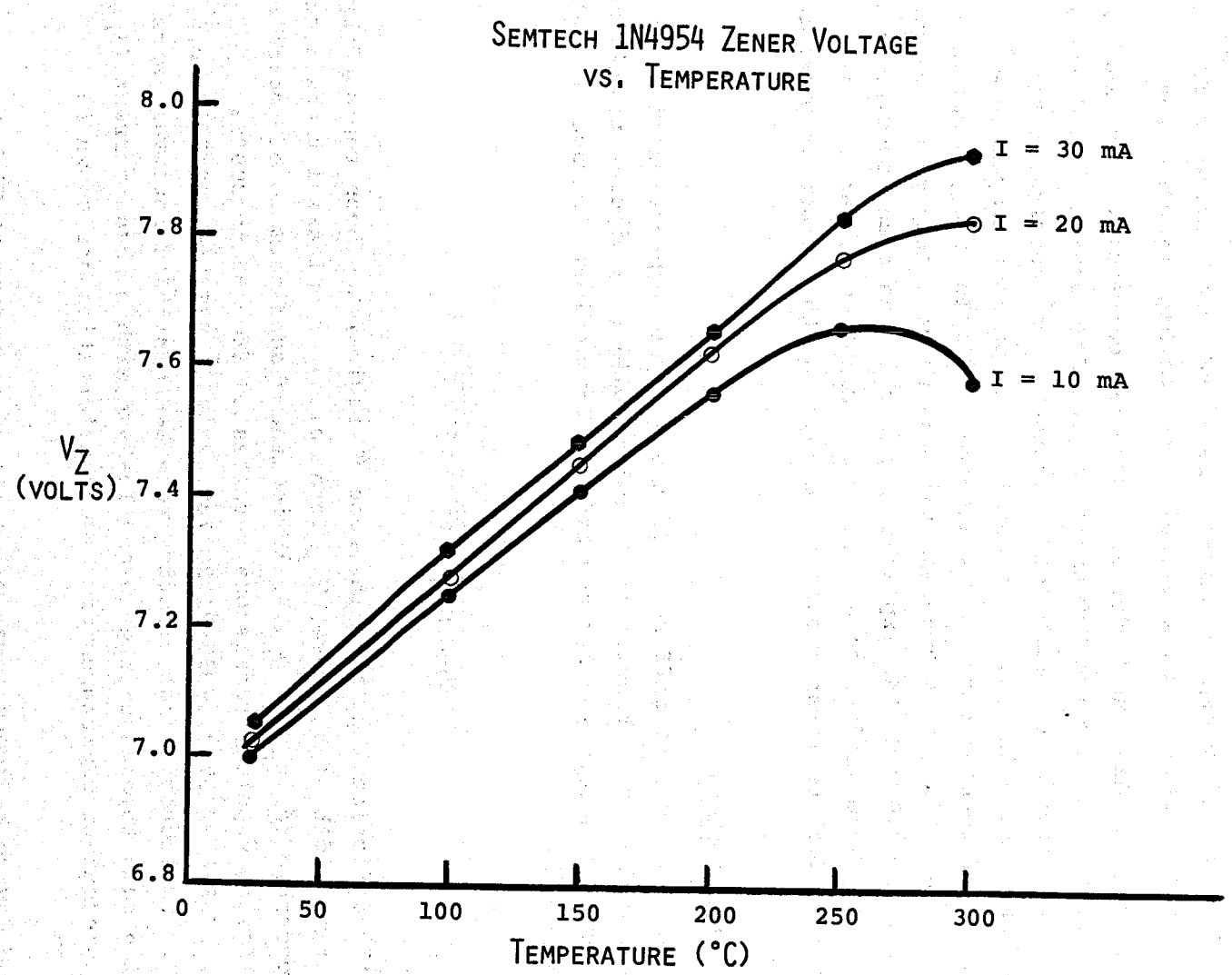


Fig. 36. Measured increase in zener voltage breakdown with temperature.

For example, operation of Semtech high voltage diodes for 1000 hours at 300°C produced typical leakage current changes of 10% at a fixed 5-volt back bias. However, about 1/4 of the devices tested showed extreme drifts (X5), but this did not create a threat for circuit fabrication since large degradation behavior could be predicted by changes in the first 100 hours of aging. Similarly, beam leaded and hermetic TO can packaged diodes have been successfully aged at high temperatures.

Although no GaAs pn diodes are currently commercially available, it was possible to use the McDonnell Douglas JFET device as a diode by shorting the source and drain leads together. The results of this approach are shown in Fig. 34, a considerably smaller temperature dependence of leakage current was detected. Simple theory predicts a slope of -16,595°K ($-E_g/k$) whereas the measurements only gave a slope of -1,000 to -3,000°K. No explanation for this has been found, but the leakage for these diodes was extremely dependent on voltage. This suggests a shunt resistance exists, perhaps due to surface or package leakage.

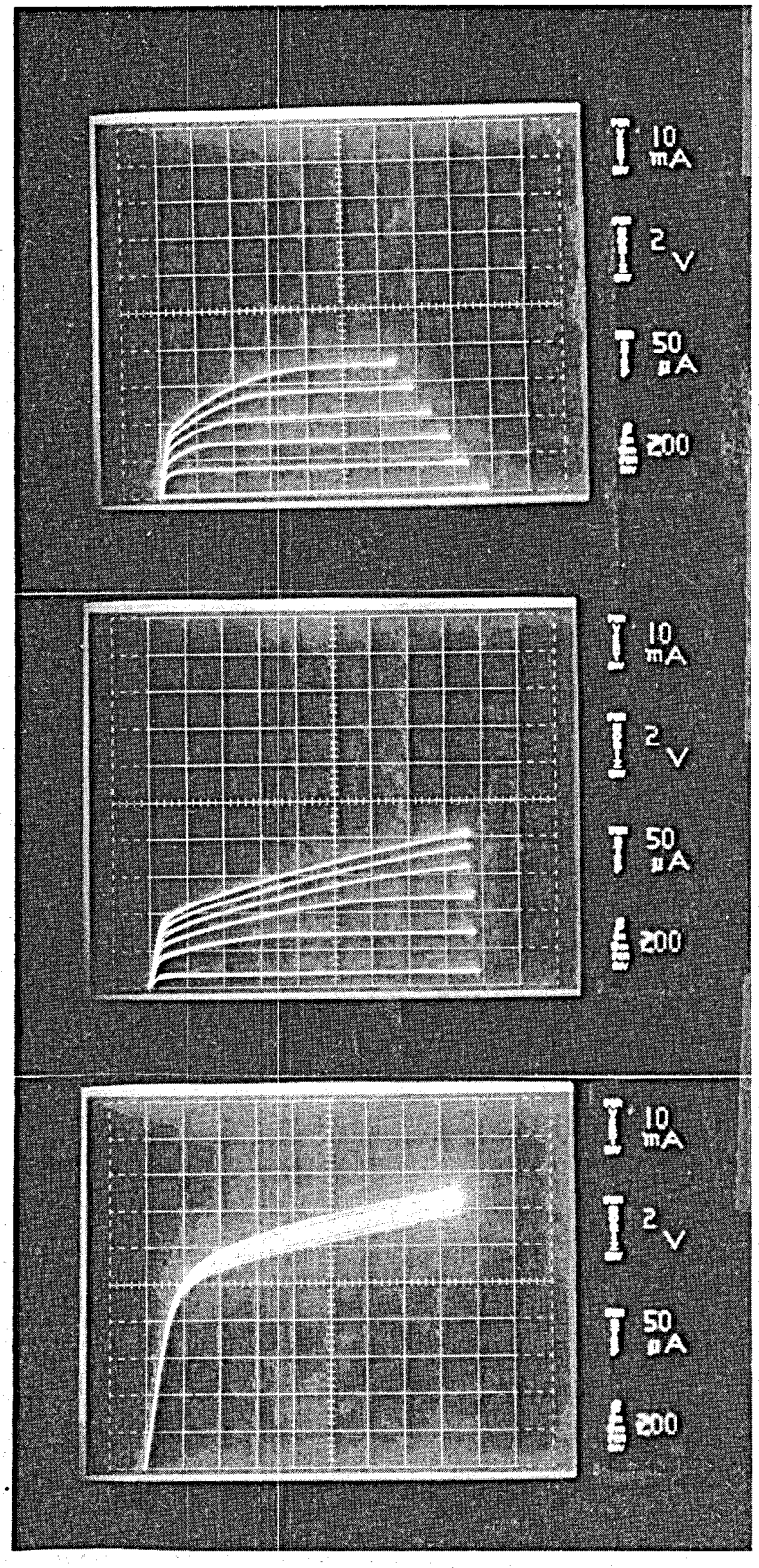
Bipolar Transistors

There is a slight difference in the analytic expressions for the expected leakage of a bipolar diode and a diode in a bipolar transistor. For example, the formulas for the base-collector diode leakage in a PNP transistor is

$$J_{(B-C)S} \propto \frac{D_B P_{BO}}{W} + \frac{D_C n_{co}}{L_C}$$

where the diffusion length in the base (N region) has been replaced by the shorter width of the base, W. In an alloy or epitaxial transistor it is possible for $n_{co} << p_{BO}$, allowing the second term to be neglected. The following bipolar transistors were tested from 25 to 300°C: 2N3771, 2N3866, 2N3743, 2N3742, 2N3728, 2N3964, B2T3965, B2T2222, and B2T2907. Collector characteristics were taken at 50°C intervals with attention paid to change in gain and leakage with no base current (I_{CEO}). Some representative pictures of the characteristics are shown in Figure 37.

One device had considerably less leakage current at high temperature. Figure 34 illustrates the base-collector leakage current as a function of temperature for a 2N3866 silicon NPN transistor.[20] Notice the slope is similar to that of an ordinary silicon diode. This base leakage must



2N3742

30 °C

200 °C

300 °C

Fig. 37. Representative collector characteristics for bipolar transistors (2N3742) over temperature range. Horizontal is collector-emitter voltage; vertical is collector current, base current is parameter.

essentially be multiplied by the static common-emitter current gain β to obtain the emitter-collector leakage. Collector characteristics for this device are shown in Figure 38. The 2 mA of emitter-collector leakage for zero base current at 300°C was found to be excessive for most circuit applications, although circuits meant to operate in a narrow temperature range around 300°C (for example, in a thermostatically controlled oven environment) could have compensation for the large but constant leakage. All other bipolar transistors tested had emitter-collector leakages of 10-200 mA at 300°C.

For a transistor of fixed current cross section the leakage can be minimized by use of high doping. For example, using the simplest analytic expressions for semiconductor diode conduction we find the leakage

$$J_s \propto \frac{D_p}{L_c} \propto \frac{1}{(N_o)^{2.3}} ,$$

where N_o is the doping concentration of the lightly doped diode region.

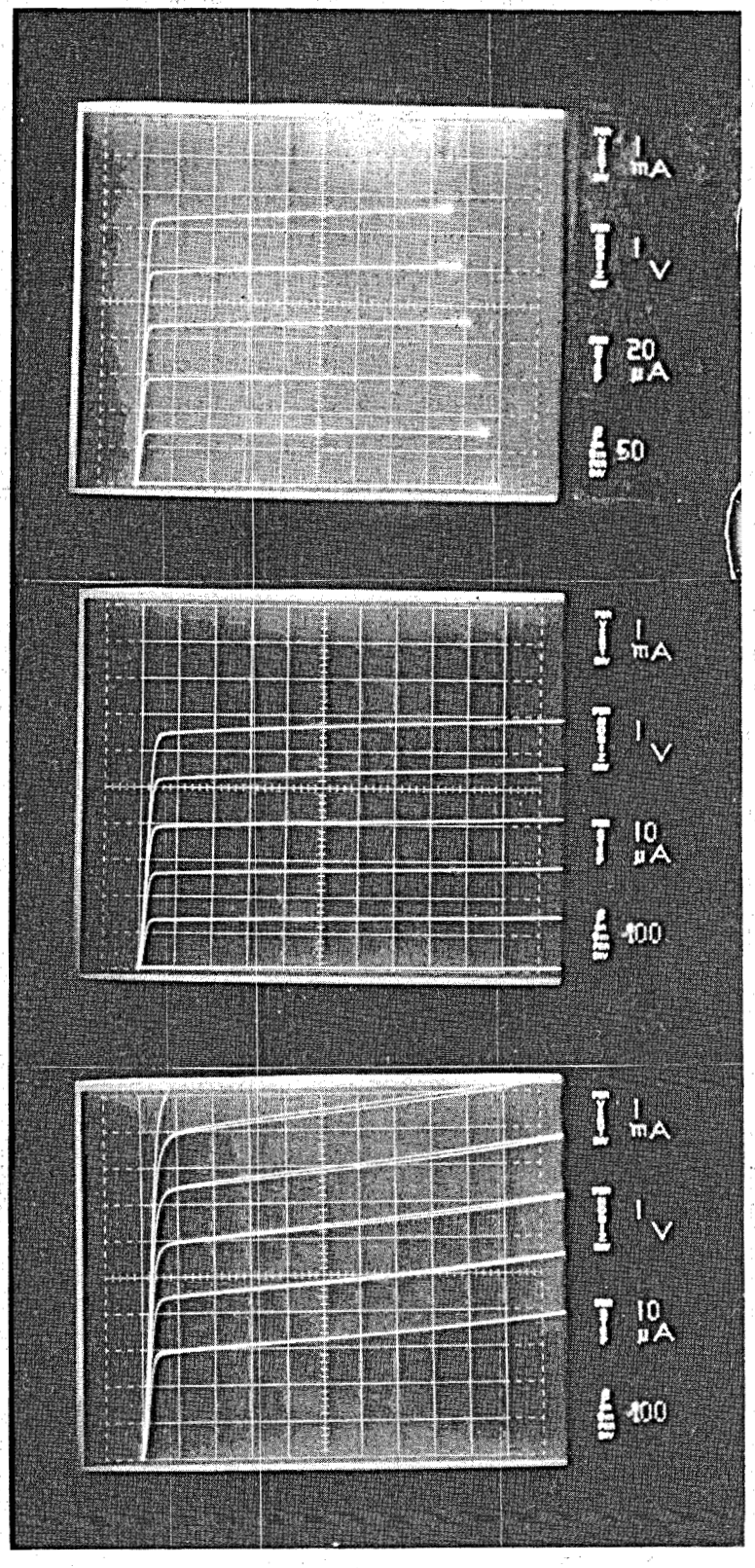
Thus, for a fixed unit cross section the leakage can be minimized. However, two qualifications must be made: first for a fixed forward voltage the current flow is reduced proportionately to the leakage, and secondly, other transistor parameters such as the gain and breakdown voltages are also affected by doping changes. Significantly, the one bipolar transistor type found with low leakage (3866) also had higher base doping than the others. The doping was calculated from the diode breakdown voltages.

Designing bipolar transistors for extremely low leakage does not appear possible, but the fact that at least one device type outperforms others by a factor of ten is promising. As an example of the flexibility for improvement, but complexity of the task, consider the static forward current transfer ratio

$$\alpha = \gamma\beta\alpha^*$$

where γ is the emitter injection efficiency, β is the base transport factor, and α^* is the collector-body multiplication ratio. Each of these factors have temperature dependences that are sharply dependent on geometry and doping.

2N3866



25 °C

200 °C

300 °C

Fig. 38. Low leakage bipolar transistor 2N3866.

CHAPTER 4 - GaAs FIELD EFFECT DEVICES

Introduction

Silicon field effect devices appear to be reaching their usable temperature limit at 300°C. The exact limit is determined by metallization and doping level choices. A fundamental limitation between 300-350°C is built into the silicon. The thermally induced carrier density increases exponentially with temperature. This rate depends on the band gap of the material, $\exp(-E_g/kT)$. Silicon has a gap of 1.12 eV and reaches a point where thermally generated carriers are about as dense as doped carriers at about 300°C. Gallium Arsenide (GaAs) with a larger energy gap (1.4 eV) does not reach this point until considerably higher temperatures, hence the interest in GaAs for high temperature application.

First the general theory of intrinsic cutoff temperature, temperature dependence of gain, and leakage current of a Schottky barrier on GaAs will be discussed. Then some data on commercial GaAs devices will be presented and discussed. The existing devices are of two types, metal semiconductor field effect transistors (MESFETs) and junction field effect transistors (JFETs). Finally a discussion of the future of GaAs for high temperature work will be presented.

Intrinsic Cutoff Point for GaAs

The following equation is derived from standard semiconductor theory found in any of many texts on this subject.[5,6]

$$\ln N_i = \ln 2 + \frac{3}{4} \ln \frac{2\pi m_n^* K}{h^2} + \frac{3}{4} \frac{2\pi m_p^* K}{h^2} + \frac{3}{2} \ln T - \frac{E_g}{2kT}$$

where N_D is the carrier density, m^* is an effective mass, and E_g is the electron band gap. For GaAs the numbers are

$$m_n^*/m_o = 0.068$$

$$m_p^*/m_o = 0.5$$

$$E_g = 1.43 - (4.3 \times 10^{-4})(T - 300) \quad \text{eV} .$$

Thus, the intrinsic carrier density becomes

$$n_i = N_{Dmin} = \exp\left[\frac{3}{2}\,\ell n\ T - \frac{1.43 - (4.3 \times 10^{-4})(T - 300)}{T(1.725 \times 10^{-4})} + 47.3912\right].$$

Figure 39 is a plot of this carrier density as a function of temperature both for GaAs and Si. The doped carrier density (extrinsic carrier density) will typically be in the range of 10^{15} - 10^{17} for either silicon or gallium arsenide devices. In order for the differences in doping intensity to create the action of an active device the doped carrier density of at least one of the device regions must exceed the intrinsic carrier density. For example, in a simple p-n diode the current in either direction will be equal and dominantly produced by intrinsic carriers unless the doped carrier density in at least one region exceeds the intrinsic carrier density. The degree to which the doped carrier density must exceed the intrinsic density will be arbitrarily taken as 10, a factor that in practice depends on the circuit. With this rule of thumb, Figure 39 shows 300-350°C as the cutoff range of useful active silicon devices. Similarly, gallium arsenide should be useful up to at least 500°C.

Gain in GaAs Devices with Temperature

The transconductance for GaAs field effect devices is higher than for silicon at room temperature. This is due to the higher carrier mobility since $g_m \sim \mu_n$ and $\frac{\mu_{n-GaAs}}{\mu_{n-si}} = 4.73$. Furthermore, the mobility in gallium arsenide devices decreases as inverse temperature (T^{-1}) compared to the sharper decrease in silicon ($T^{-2.3}$). Both the high initial transconductance and the slower decrease in transconductance with temperature enhance the interest in gallium arsenide for high temperature work.

Gate Leakage Current

Operation below the intrinsic cutoff temperature and within a constant gain temperature range is not enough; the gate leakage of a field effect device must remain small for operation. A MESFET device is a field effect transistor where the gate function is supplied by a metal semiconductor junction, with no oxide separation. Most

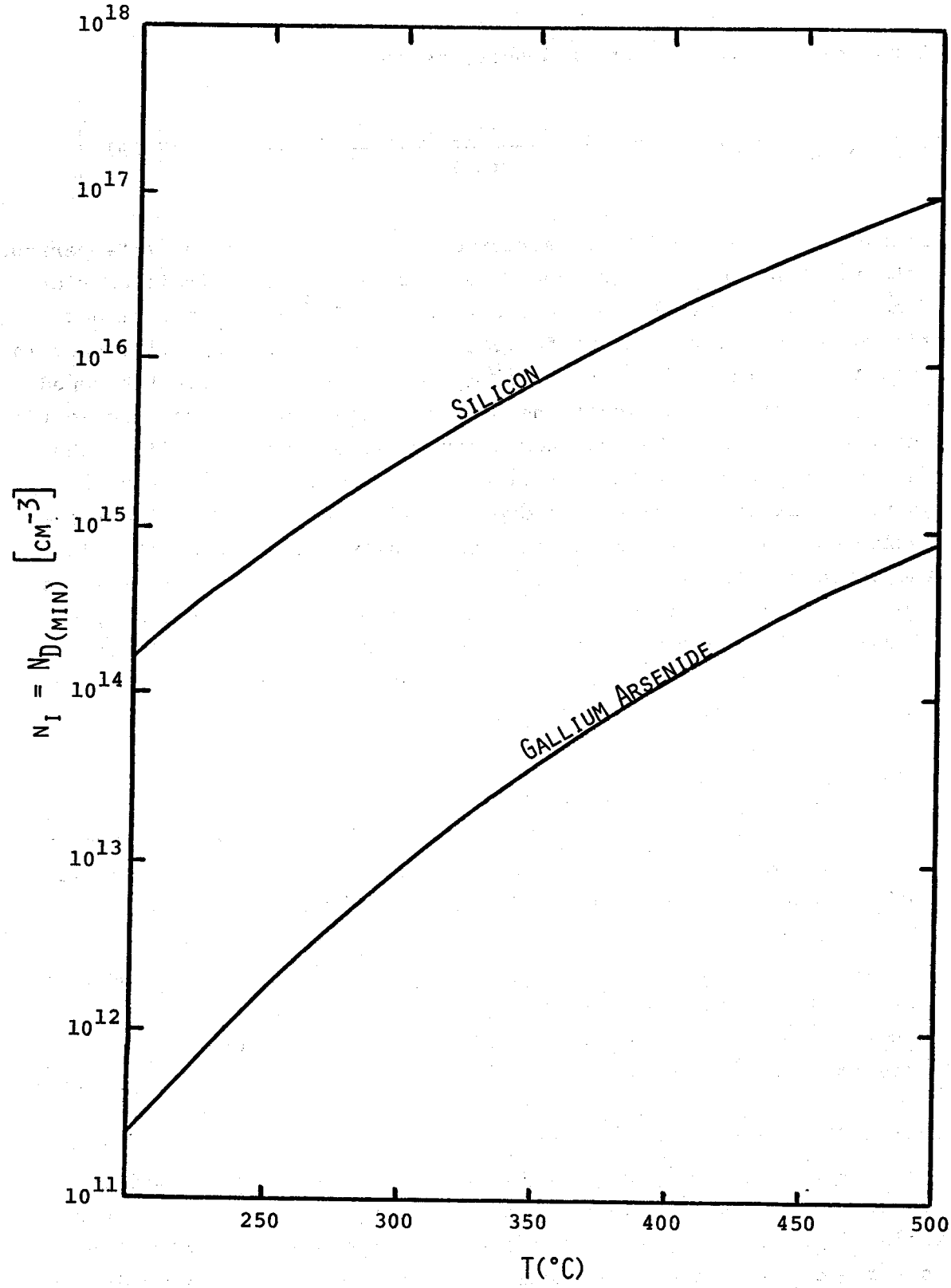


Fig. 39. Intrinsic carrier density as function of temperature for silicon and gallium arsenide. For standard doping silicon devices remain extrinsic up to 300-350°C, gallium arsenide to 500°C.

metals form a contact with GaAs that has a boundary energy barrier of 2/3 of the energy gap of GaAs. In essence it is this smaller barrier height (∿0.8 eV) which results in large gate leakage at elevated temperatures. The semiconductor-metal barrier model to be used can be found in Reference 5.

Thermionic Emission Component of Leakage -- The metal-semiconductor barrier height can be calculated with the formula

$$\phi_{BH} = C_2\phi_m + C_3 ,$$

where for GaAs $C_2 = 0.07$ and $C_3 = 0.49$. Assuming a Au/Al metallization, the work function for conduction electrons is $q\phi_m \cong 4.5$ eV. Thus, $\phi_{BH} = .805$ eV. The thermionic current density can then be written from diode theory as

$$J_{rs} = AT^2 \exp(-q\phi_{BH}/kT)[\exp(qV/kT) - 1] ,$$

where A is the Richardson constant. In device operation the reverse bias (-V) is large enough so that $\exp(-qV/kT) << 1$. Thus, we can simplify the expression for J_{rs}

$$J_{rs} = -100T^2 \exp\left(\frac{-9333}{T}\right) \quad \text{amp/cm}^2 .$$

This is plotted in Figure 40.

Diffusion Component of Leakage -- For the same metal-semiconductor system the diffusion current density of leakage can be written as follows.

$$J_{rs} = q\mu N_c \left[\frac{q(V_{bi} - V)8\pi N_d}{\varepsilon_{si}}\right]^{1/2} \exp\left(\frac{-q\phi_{BH}}{kT}\right)$$

where $\varepsilon_{si} = 11.7\ \varepsilon_o$

$$N_c = 2\left[\frac{2\pi m_r^* kT}{h^2}\right]^{3/2} = 8.55 \times 10^{19}\ T^{3/2}$$

$$N_D = 10^{14}\ \text{cm}^{-3}$$

$$V_{bi} = 1.5\ \text{V}$$

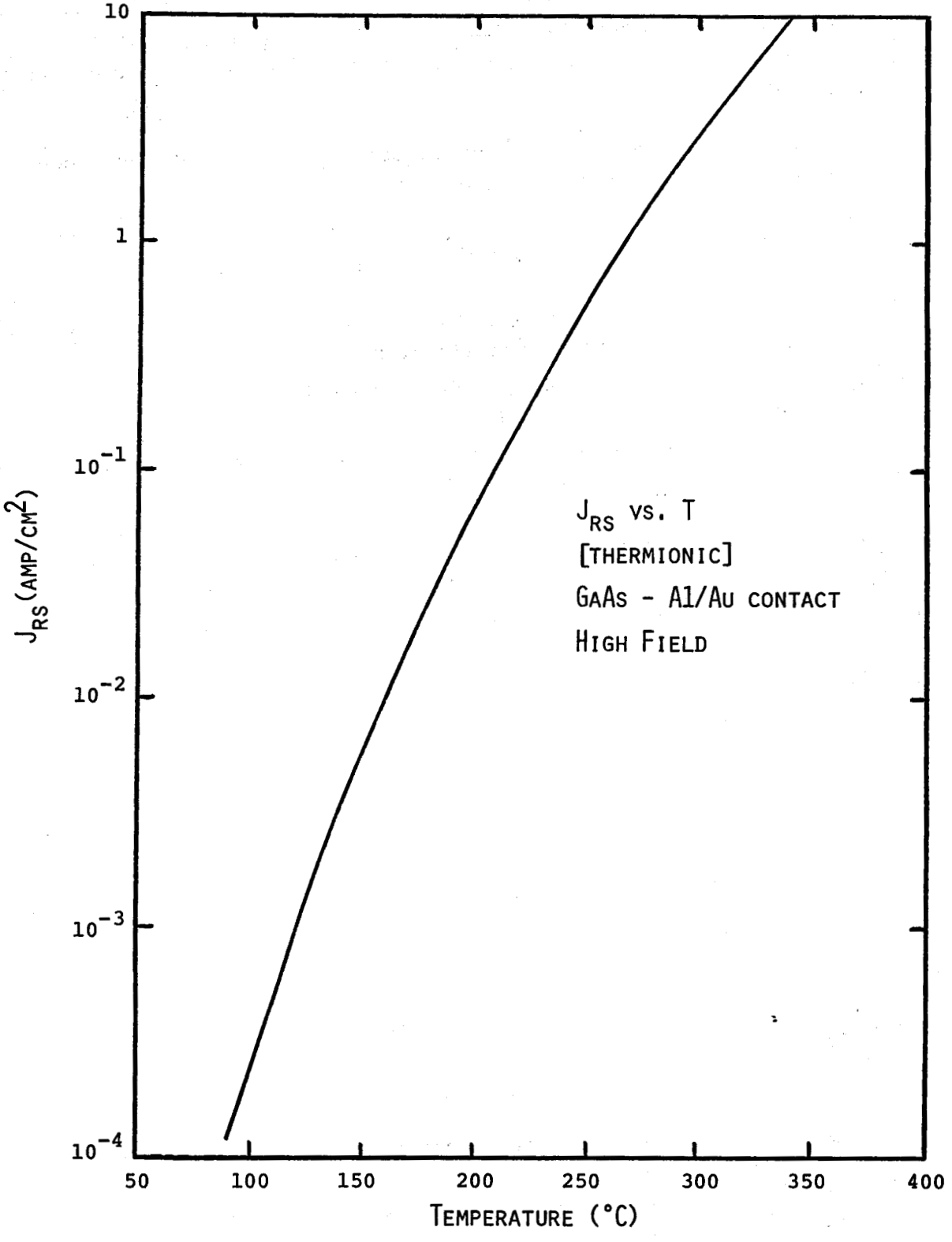


Fig. 40. Thermionic emission component of leakage as a function of temperature for Al/Au contact on GaAs.

$\phi_{BH} = .805$ eV

$\mu \sim m^{*3/2} T^{-1}$ at T = 300°C

$\mu = 7 \times 10^3$ (measured)

Thus, $\mu = 2.1 \times 10^{-6}\ T^{-1}\ cm^2/V$ sec or $210\ T^{-1}\ m^2/V$ sec. Even though ϕ_{BH} decreases slightly with increasing temperature, the variation is small compared to T^{-1}. Inserting these values gives

$$J_{rs} \cong 5.347 \times 10^9 T^{1/2} (1.5 + V_{rev})^{1/2} \exp\left[\frac{-9333.33}{T}\right] \quad Amp/m^2 .$$

Figure 41 uses this equation to plot leakage current versus reverse voltage with temperature as the parameter. Figure 42 exhibits the leakage current versus the temperature at various reverse biases.

The thermionic emission and diffusion components of leakage are additive. It is clear that the gate leakage for GaAs MESFETs are too large at high temperatures to be useful. For example, the leakage of a GaAs/Al-Au contact of area $10^{-4}\ cm^2$ at $V_{rev} = 4$ volts at 300°C is .5 mA. The combined theory of leakage in a metal-semiconductor junction (as in Sze[6]) gives a similar result.

The gate leakage in GaAs JFETs was also calculated and found to increase with increasing temperature. However, this leakage wasn't found to be so high as to exclude JFETs from effective use at high temperatures. This smaller leakage is essentially due to the larger "barrier height" that exists between n and p GaAs as compared to that between GaAs and a metal. These leakage calculations followed Grove,[5] page 178.

Evaluation of Commercial Devices

There are many GaAs device types presently available from many suppliers: Plessey Optoelectronics and Microwave, McDonnell Douglas, Texas Instruments, Hewlett Packard, and Dexcel. The GaAs MESFET devices found in the market today are made for microwave frequencies and therefore are n channel (to utilize the higher mobility of electrons). Being n channel a negative gate voltage is needed for operation and the drain source current is maximum at zero gate voltage. The fact that commercial devices are designed for microwave operation encourages internal device microwave oscillation when dc bias is applied. Throughout these tests ferrite beads were placed on the device leads to suppress such oscillation.

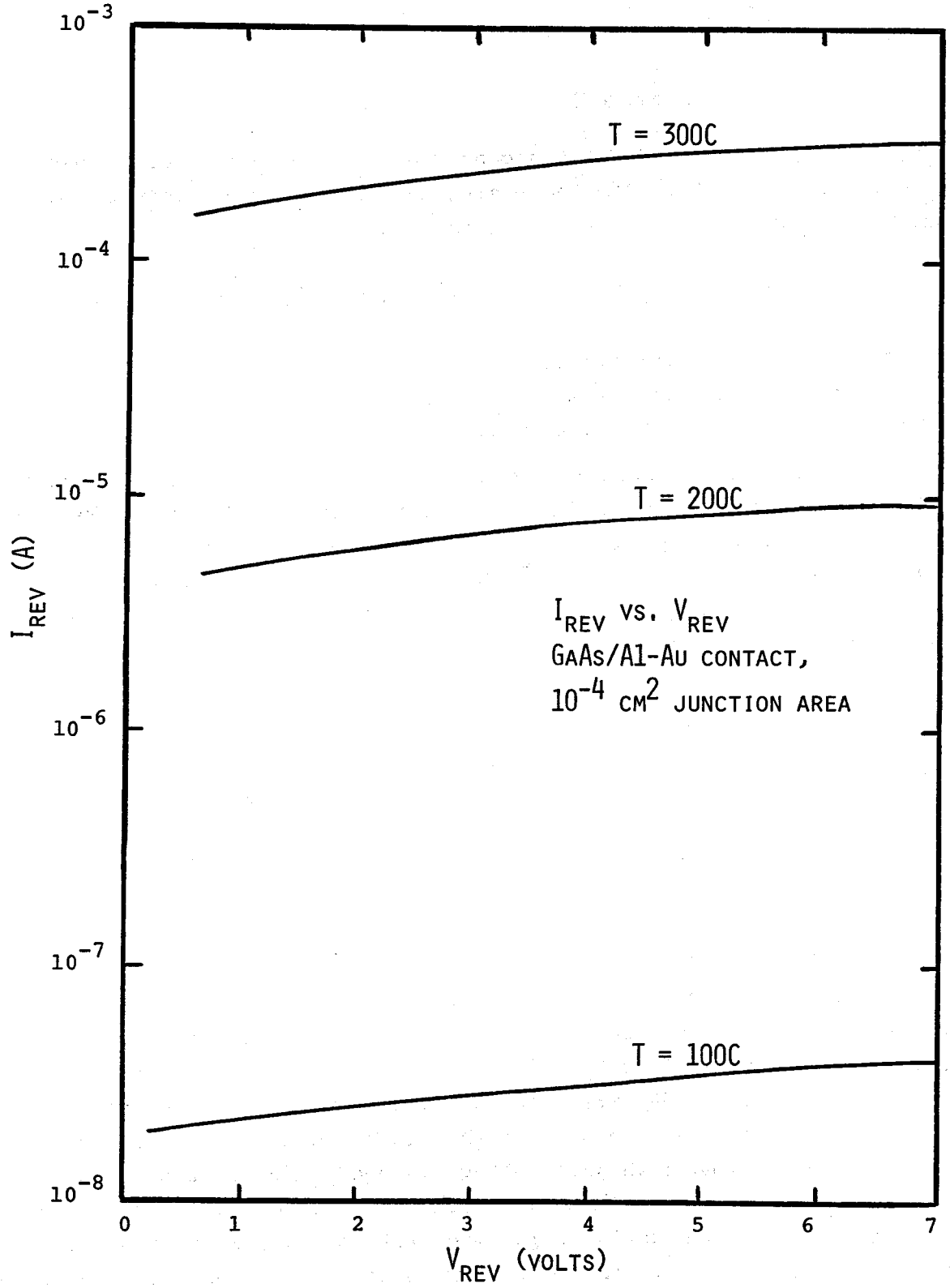


Fig. 41. Reverse leakage versus voltage for an Al/Au contact on GaAs.

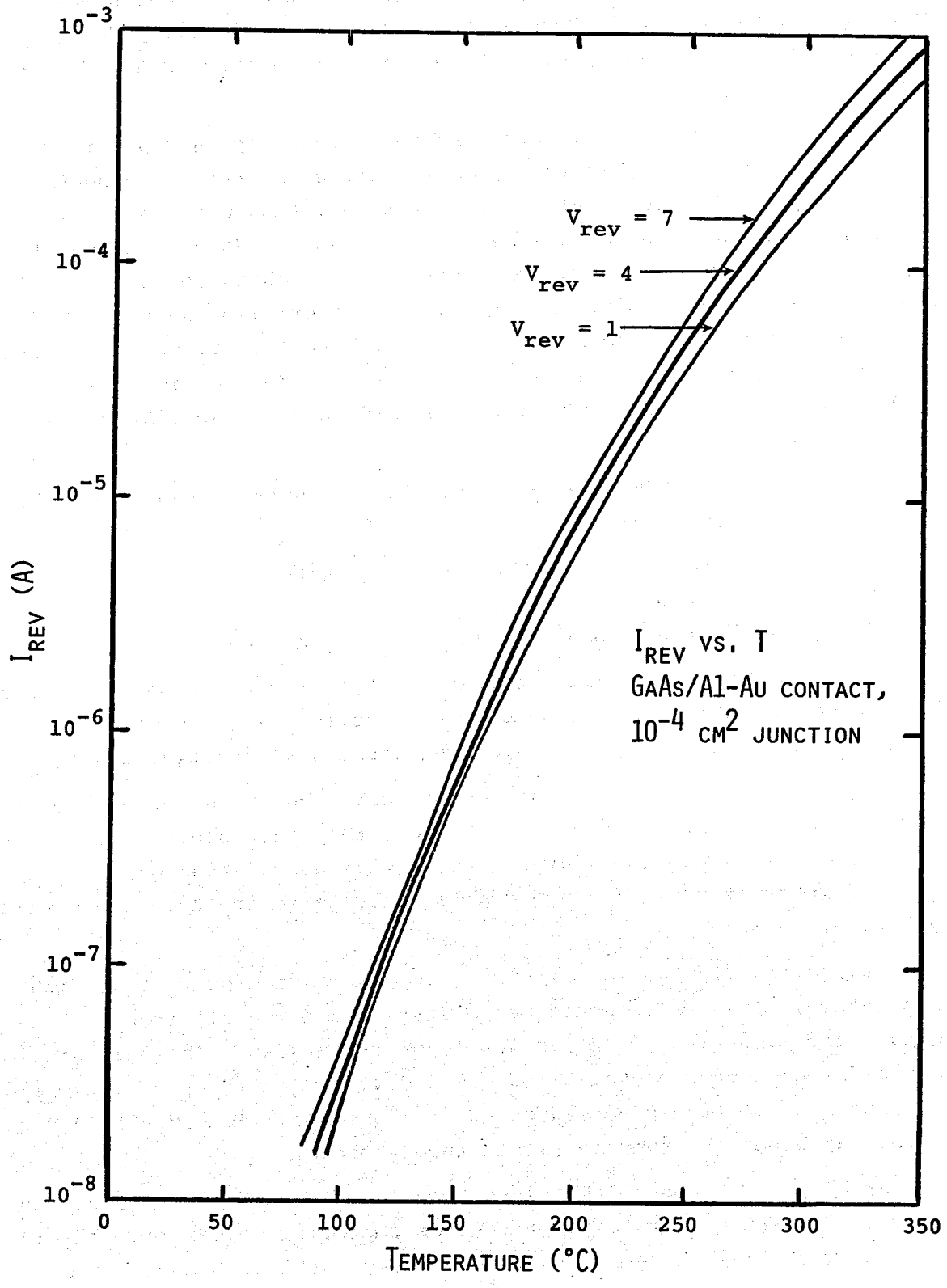


Fig. 42. Reverse leakage versus temperature for an Al/Au contact on GaAs.

In this report we will describe in detail several samples of a Plessey Optoelectronic and Microwave MESFET, the GAT 1, and several prototypes of a McDonnell Douglas JFET which was originally designed for high radiation tolerance. All devices were subjected to identical test procedures.

Test -- Devices were mounted inside a high temperature forced air oven. Wires were attached to the device leads and run to connectors on the outside of the oven. All drain characteristics were taken with dc biasing, no pulse measurements were made. The standard sequence of tests were: characterized at room temperature, characterized at 150°C, soak at 150°C at full bias for 65 hours, characterized again, 275°C characteristics taken, soak at 275°C under bias for 191 hours, return to room temperature for last characterization. In addition, temperature cycling was done to test for structural endurance. The test circuit used is shown in Figure 43.

Plessey GAT 1 MESFET -- The metallization system used on the GAT 1 GaAs FETs is as follows:

1. Gold/indium/germanium for ohmic contacts
2. Aluminum gate
3. 0.001 inch gold bonding wire in P101 package

Figures 44 to 47 show detailed characteristics for two samples of this device, No. 2 and No. 3. These characteristics are quite different for two of the same device type, indicating perhaps a sensitive design.

Device No. 3 displayed drain characteristics which could be used in circuits operated up to 300°C; however, the drain source leakage at high temperatures was excessive. This device showed high gain (g_m = 12 mmhos at T = 25°C) and stable characteristics under temperature cycling and aging.

Device No. 2 showed a maximum of 165 μA leakage current at high temperature. This value could be tolerated in a useful circuit. The aging drift of device No. 2 was small but measurable. The only significant difference between No. 2 and other devices tested at room temperature was its low transconductance, g_m = 5.6 mmhos. This device did not perform as expected from the simple theory above.

JFET -- The McDonnell Douglas JFETs functioned well at temperatures below 225°C. At higher temperatures the characteristics irreversibly degraded with time, becoming extremely leaky within 100 hours at 277°C (see Figures 48, 49). In reference to the characteristic plots of these JFETs it should be noted that leakage current was measured by

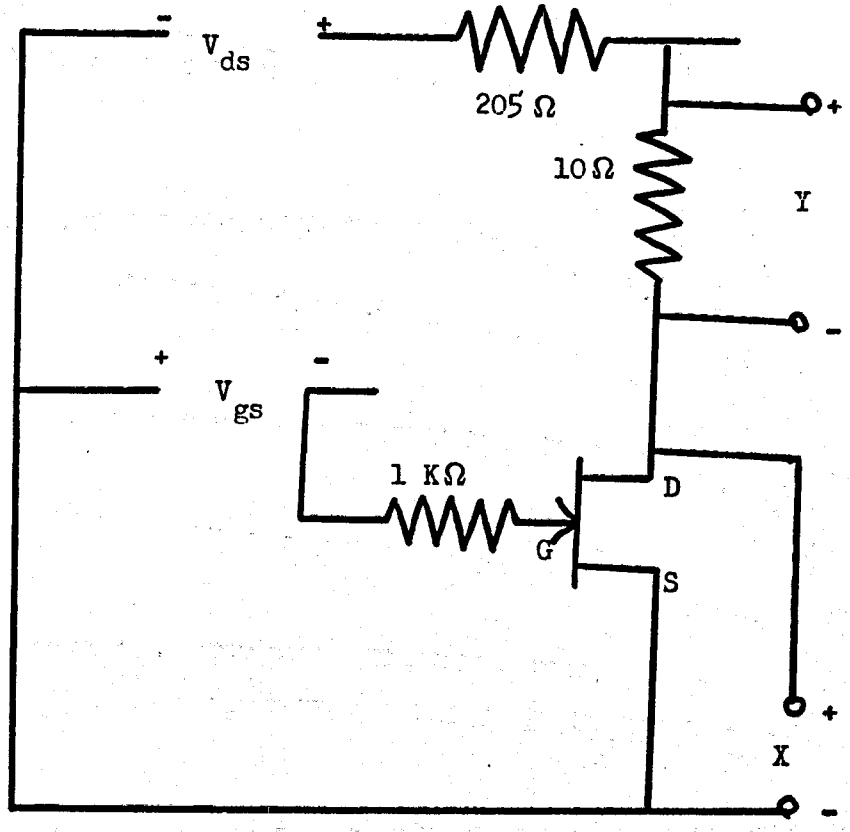


Fig. 43. Test circuit for characterization of GaAs devices.

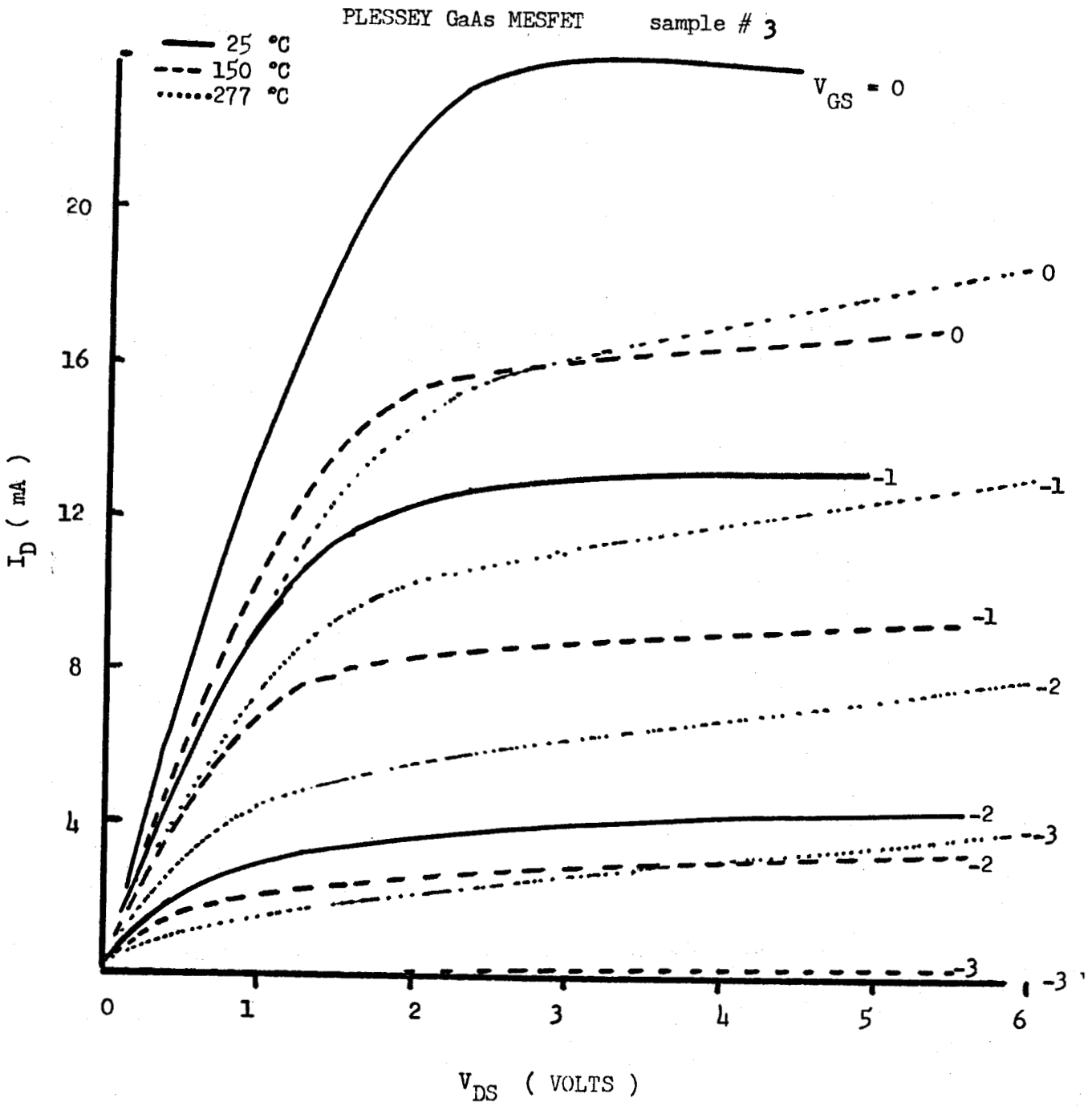


Fig. 44. Temperature variation of drain characteristics of Plessey GAT ⊥ sample #3.

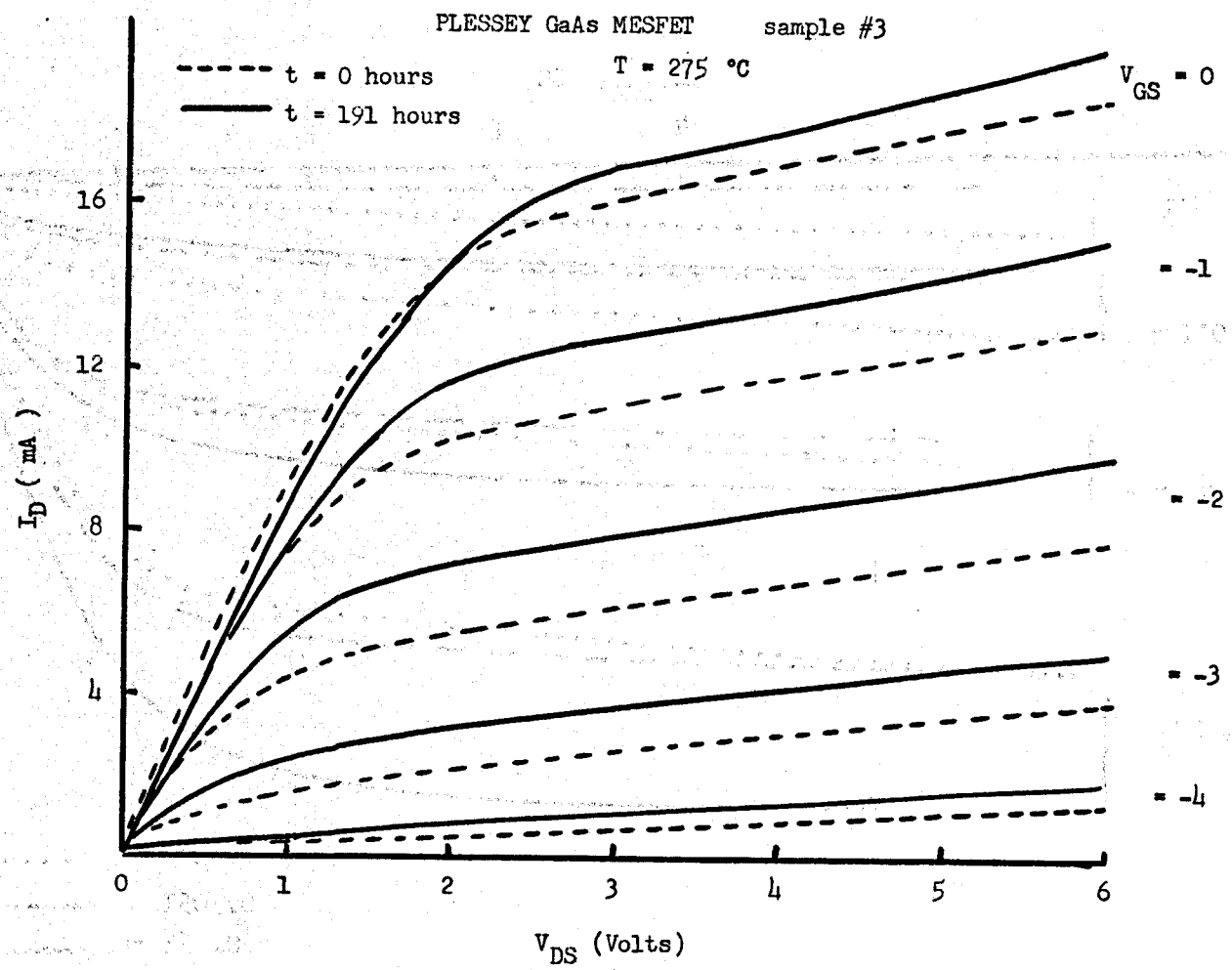


Fig. 45. Time variation at 275°C of drain characteristics of Plessey GAT ⊥ sample #3.

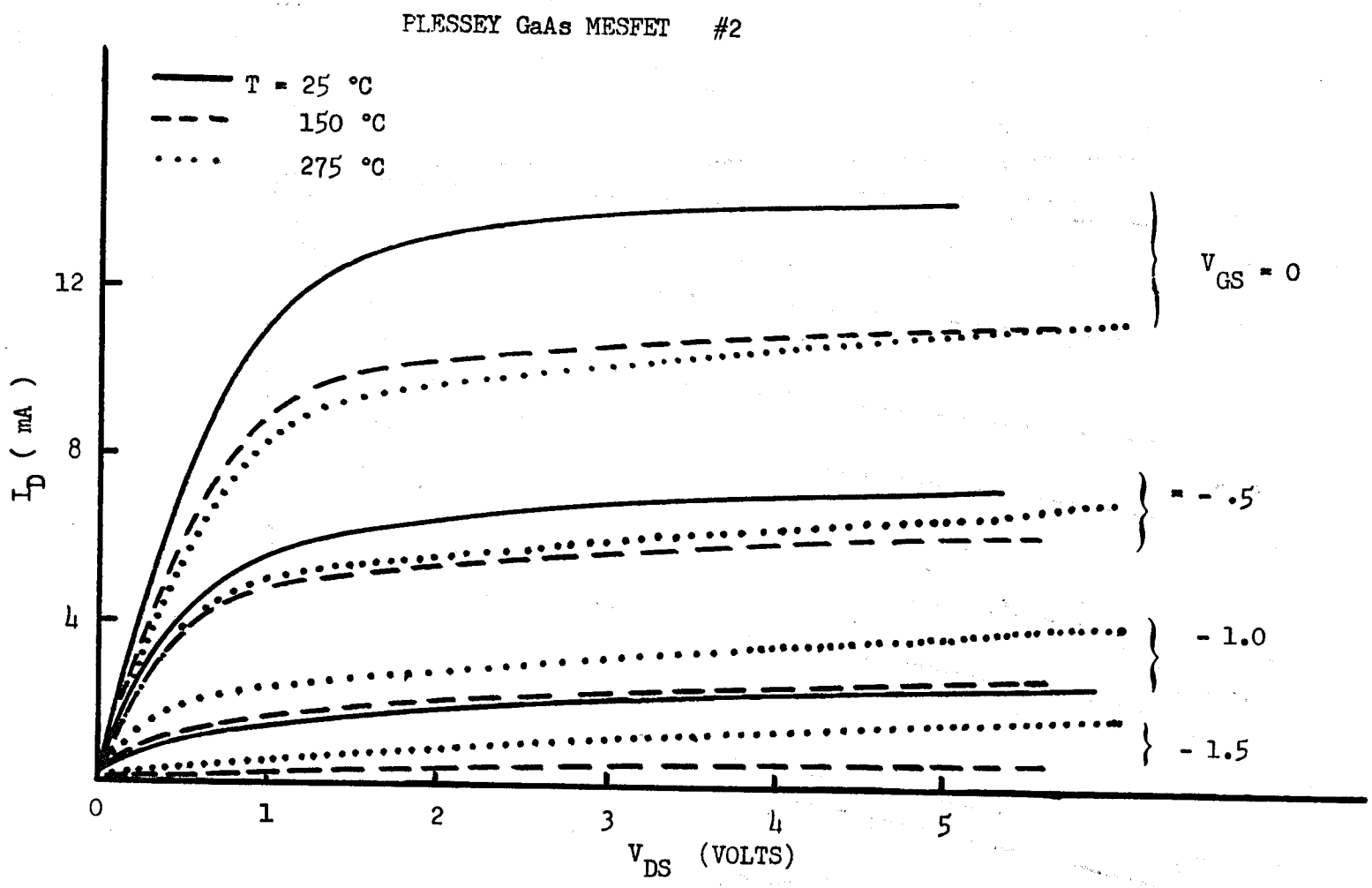


Fig. 46. Temperature variations of drain characteristics of Plessey GAT ⊥ sample #2.

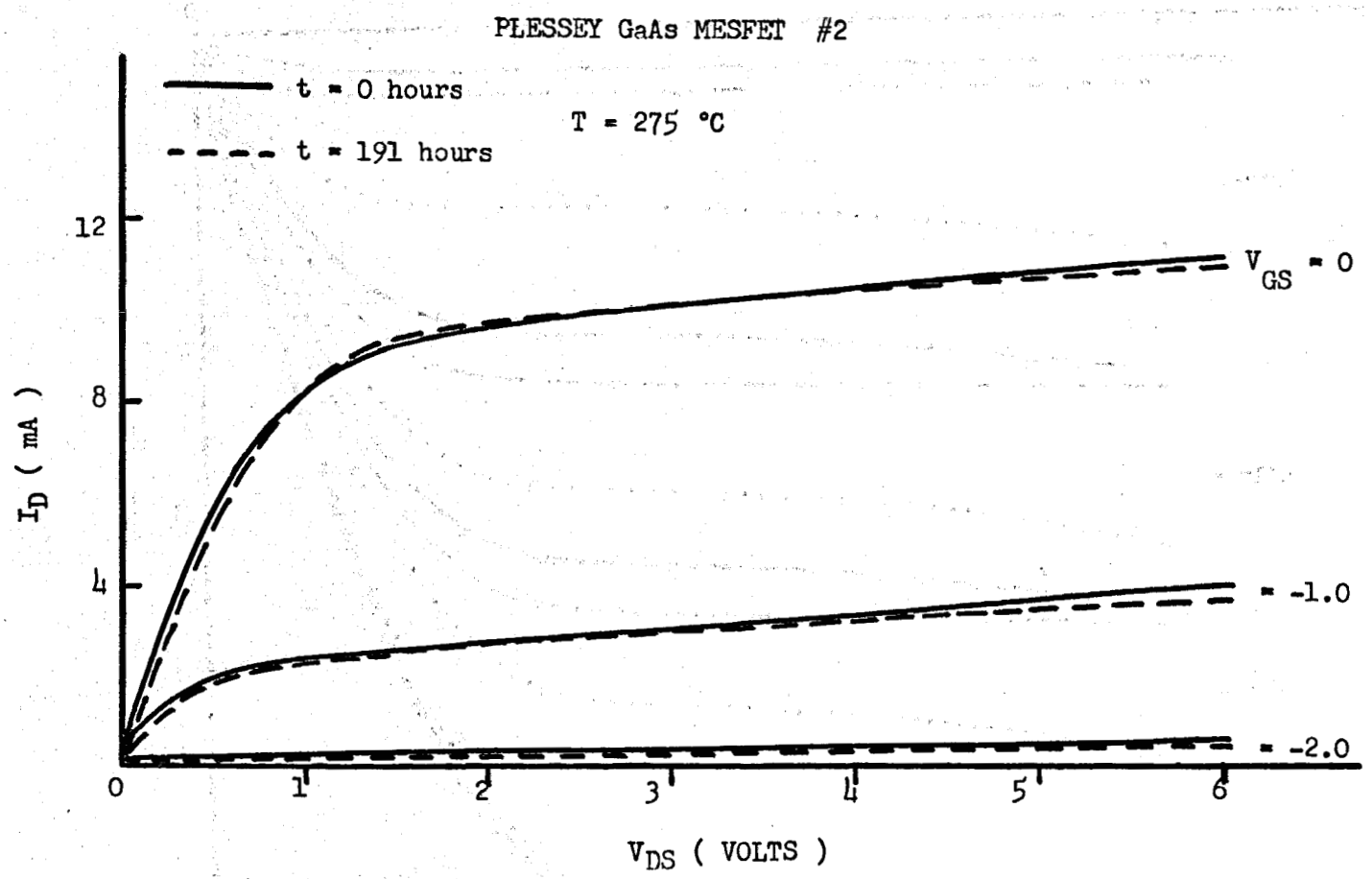


Fig. 47. Time variations at 275°C of drain characteristics of Plessey GAT ⊥ sample #2.

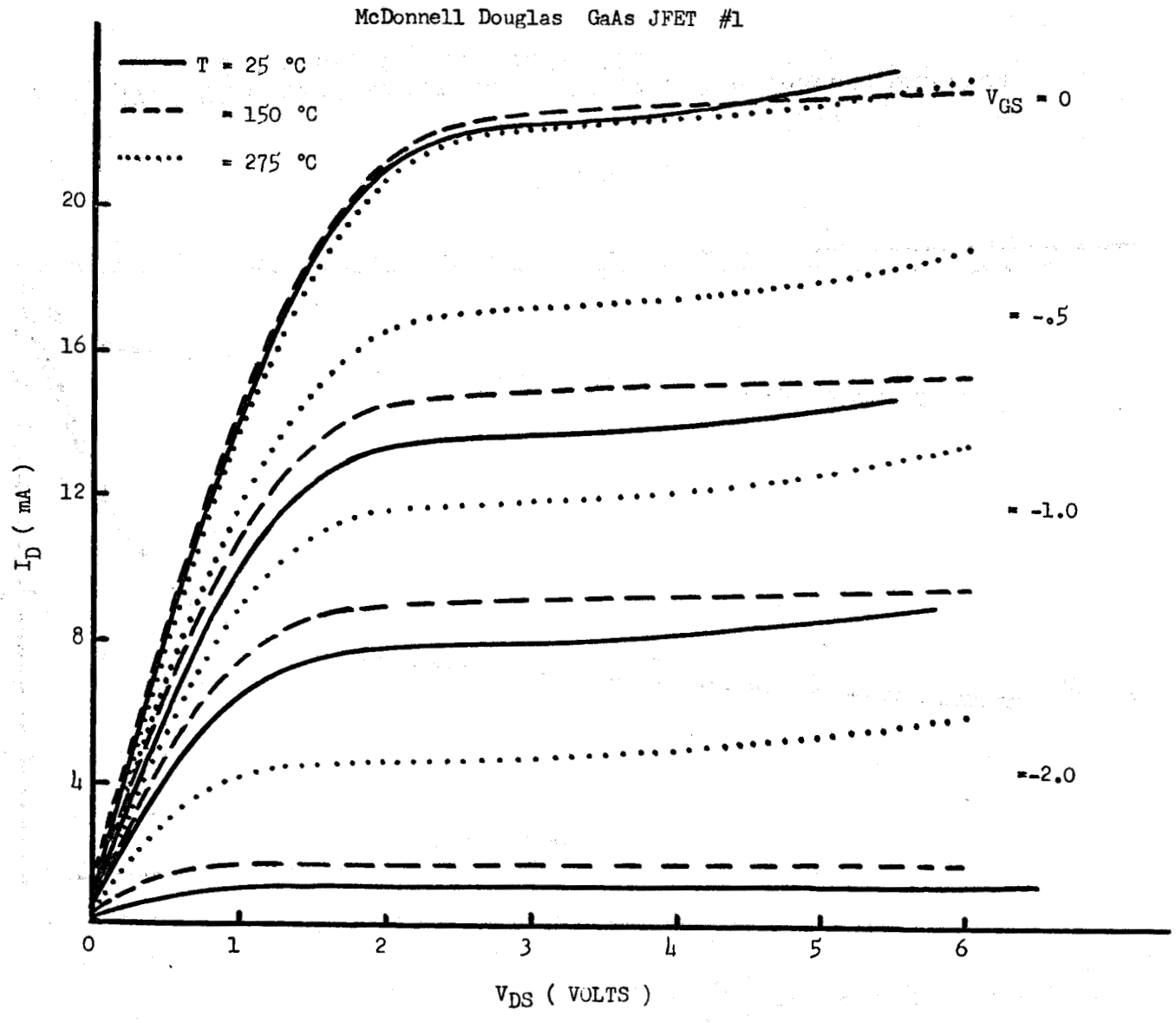


Fig. 48. Temperature variations of drain characteristics of McDonnell Douglas GaAs JFET.

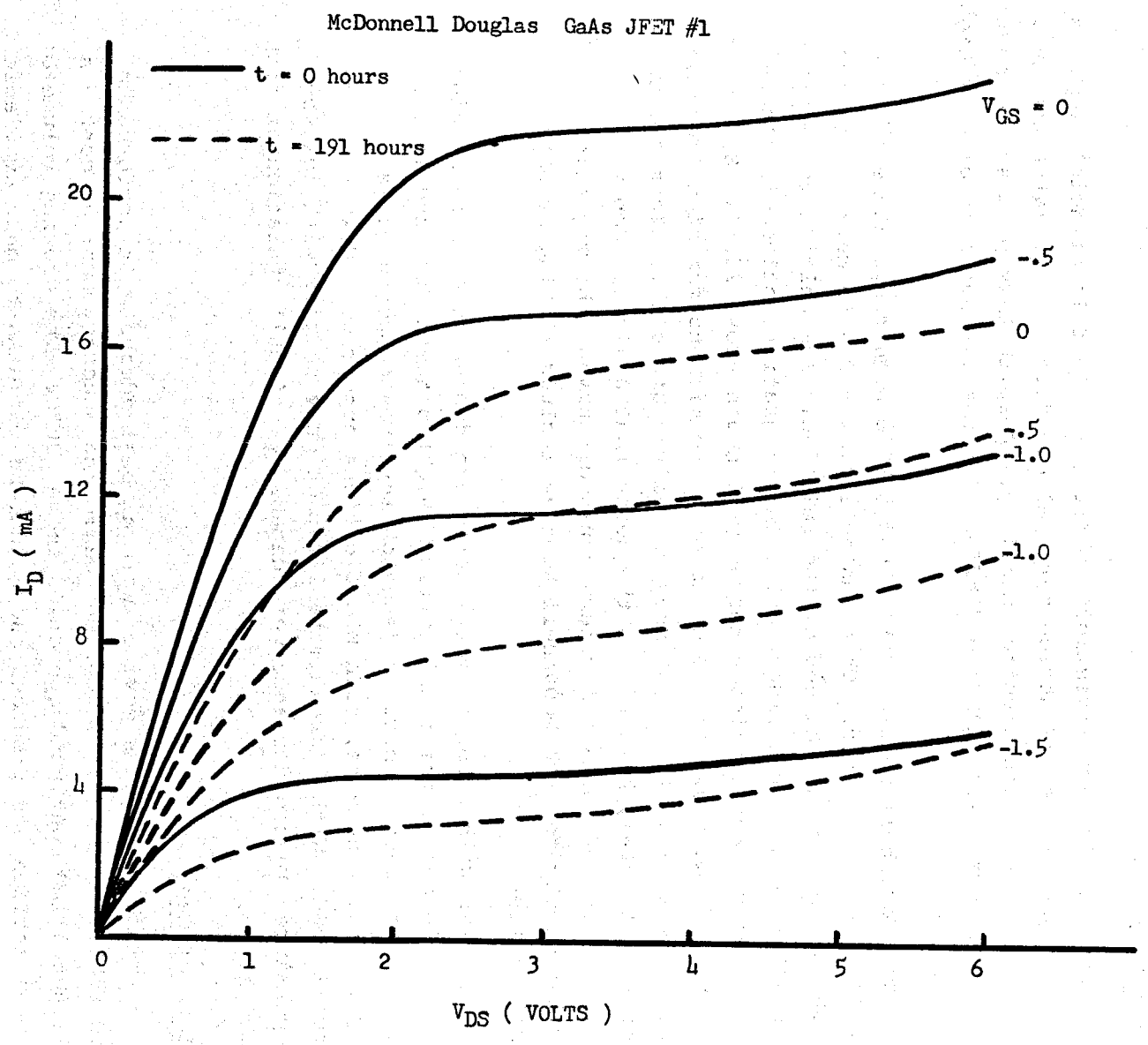


Fig. 49. Time variation of drain characteristics of McDonnell Douglas GaAs JFET.

taking voltage measurements across the 1 kΩ resistor. Thus, the voltage across the gate was different from that recorded on the chart recorder by the voltage drop across the 1 kΩ resistor. This accounts for the increase in slope as V_{DS} was increased.

Conclusion

This preliminary investigation indicated that in principle GaAs is a good high-temperature device material due first to its large gap and, secondly, to the high electron mobility. Despite this promise, presently available commercial GaAs field effect devices are not suitable for high temperature use.

The McDonnell Douglas JFET would handle high temperature if aging stability were achieved. This instability was due to metal migration on the device surface caused by the relatively low melting temperature gold alloy used in the electrodes. This migration noticeably altered the device characteristics after only 10 hours above 250°C. Since the electrode details are on the order of a few microns for high frequency GaAs devices, migration distances to failure are small. This failure mode is not fatal, however, in the sense that a higher temperature metallization or surface barriers could circumvent the migration. Current contracts with McDonnell Douglas include looking at both possibilities.

MESFETs with standard metal gates are doomed to failure at high temperature due to the small barrier height between GaAs and metal. Recent GaAs Schottky barrier research involves compound gates with larger barrier heights; such modifications appear well down the commercial road. With current metallization only samples with low room temperature transconductance were capable of circuit operation at high temperature.

Future of GaAs

Commercial rf GaAs devices were at best adequate in performance when tested up to 300°C. Current ohmic and Schottky barrier contacts will not allow continued operation above 300°C. The growing volume of rf GaAs devices has produced enough demand for GaAs to make available low impurity, low surface state density wafers; the first necessary step for any semiconductor design. Device fabrication technology has also expanded[21] leading to better ways of etching, metallizing, and passivating.[22] For example, current Schottky barrier gates are limited in temperature operation by the barrier height being only 2/3 of the

GaAs band gap, but the study of high electronegativity contacts may lead to usable, larger barriers.[23] In addition, investigations of compatible oxide surface layer deposition will lead to insulated gate field effect devices. Lastly, higher temperature metallization, surface passivation, and larger spaced contact geometry will improve the basic McDonnell Douglas junction field effect device, enabling higher temperature performance.

Although the electronic houses are not headed for high temperature, low frequency, solid-state devices, the general trends in GaAs material, fabrication, and design technology are making such device development simpler. A small effort on design and metallization study over a few years should prepare the way for commercial prototype device runs. The high temperature possibility inherent in the large band gap of GaAs has not yet been tested.

CHAPTER 5 - BONDING

Most attachment techniques used for hybrids which operate in standard temperature ranges are not able to withstand 300°C without failure. In particular, active devices with aluminum metallization present metallurgical problems when bonded into a Au based conductor circuit. Fortunately, some active device types are available with gold metallization (such as the beam leaded format of the silicon junction field effect transistor 2BT4856), but most devices are available only in aluminum metallized chip formats. Indeed, beam leaded devices were routinely thermocompression bonded to fritless gold thick films which were then successfully aged at 300°C. Unfortunately, gold wire could not be used to bond aluminum metallized chips because of well known Au-Al interface reactions discovered in thin film hybrid investigations.[24] Thus, Al wire was used with three new techniques being investigated for the necessary bonding of the aluminum wire to the Au-based thick film: (1) aluminum wire ultrasonically bonded directly from the chip to a special gold thick film, (2) aluminum wire from the chip to a diffusion barrier pad which, in turn, was thermocompression bonded to the gold film, and (3) copper beams with gold plating and nickel bumps in a tape carrier format.

A. DIRECT BONDING

In response to aging degradation of Al-Au interfaces, several thick film manufacturers have produced modified Au thick films which inhibit the formation of Au-Al intermetallics.[25] One of these modified materials was compared to three standard conductors in high temperature bond aging studies; the modified DuPont 9910 fritless Au was compared to Cermalloy fritless Au 4399, Cermalloy fritless Pt-Au 4121, and DuPont fritless Au 9791. All tests were made with a thick film dot test pattern (see Fig. 50), placing aluminum wires from pad to pad to form 70 bonds in electrical series on each sample. Three mil Al wire was used for the general survey and 1 mil Al with 1% Si wire was used for the extensive test of DuPont 9910. Air oven aging was performed at 250, 300, and 350°C with periodic resistance measurements being taken. Pull strength tests were performed before and after and in some cases during the aging. Although many different test runs were performed, the results can be collated into three studies.

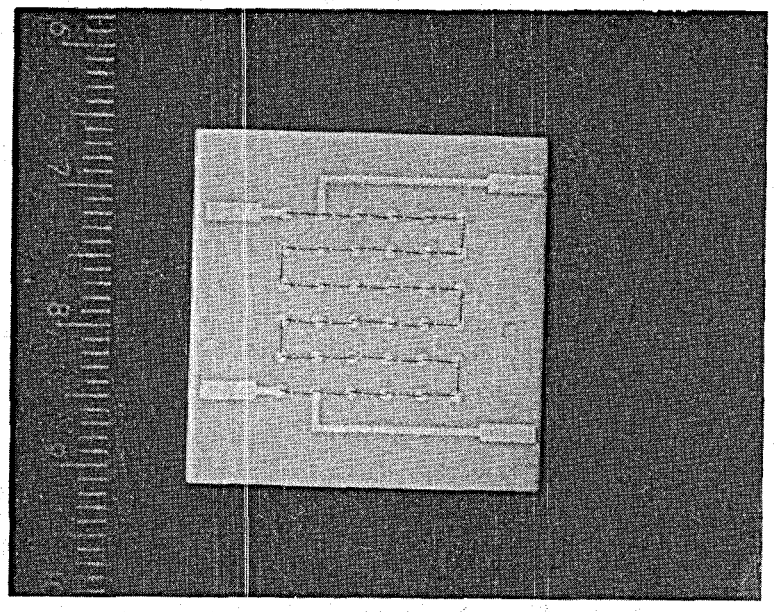


Fig. 50. Bonding dot test pattern. 70 bonds in electrical series allow interface resistance measurement during aging.

Test 1, Comparison of Thick Film Materials -- Comparison bonding tests were made among the following thick film materials: Cermalloy 4121 and 4399, DuPont 9791 and 9910. Only fritless thick films were used due to initial work done with Cermalloy fritted Pt-Au 8653 which indicated bond adhesion difficulties on a fritted surface. Three mil aluminum wire was bonded to the standard thick film dot patterns; four samples of each ink were prepared. A Kulicke & Soffa 484 Al wire ultrasonic bonder was used.

One sample of each ink was pull-tested immediately after bonding; the other three were placed in air ovens of temperature 250, 300, and 350°C. Periodic resistance measurements were taken of the series bonds by momentarily cooling the substrate to room temperature. At the end of the 1000-hour aging period pull tests were performed with all samples.

For comparison of materials the 300°C aging data was typical. The two fritless Au inks had excessive resistance increase with time (see Fig. 51). Pull strengths also decreased catastrophically after 500 hours of aging: (from 38 to 1.1 grams) for 4399, and (from 34 to 1.3 grams) for 9791. In consequence, neither of these systems qualified for high temperature circuits, presumably due to the rapid intermetallic formation along the Al-Au interface.

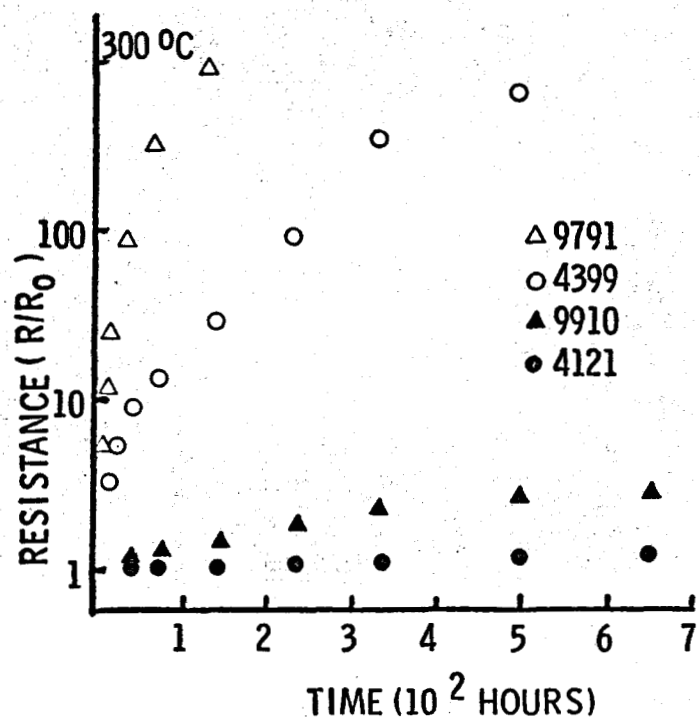


Fig. 51. Rates of bond resistance increase at 300°C vary enormously among thick film conductor compositions. Three mil pure aluminum wire was used for bonds.

Test 2, Temperature Effect on Aging -- The sensitivity of the bond degradation with temperature is illustrated by the results at 250, 300, and 350°C in Figure 52. Comparing the aging of aluminum wire bonds to DuPont 9910 at 250 and 350°C shows a 165 times faster resistance increase at the higher temperature.

The simplest model for such bond degradation would be formation of a single intermetallic at the interface, rate limited by a diffusion process. The standard diffusion coefficient equation for such a simple process is

$$D = A \exp(-E_a/kT) \ ,$$

where A is called the frequency factor, and E_a is the activation energy. Both A and E_a can be considered temperature independent. Since the highly resistive intermetallic is forming 165 times faster at 350 than 250°C, it is possible to use the above formula to derive the activation energy, E_a = 1.43 eV/atom. Looking at the data for the other Au thick films (4399, 9791), the same activation energy is found over at least the first 50 hours at temperature. However, the frequency factor A is much larger in the ordinary Au thick films than in the modified 9910.

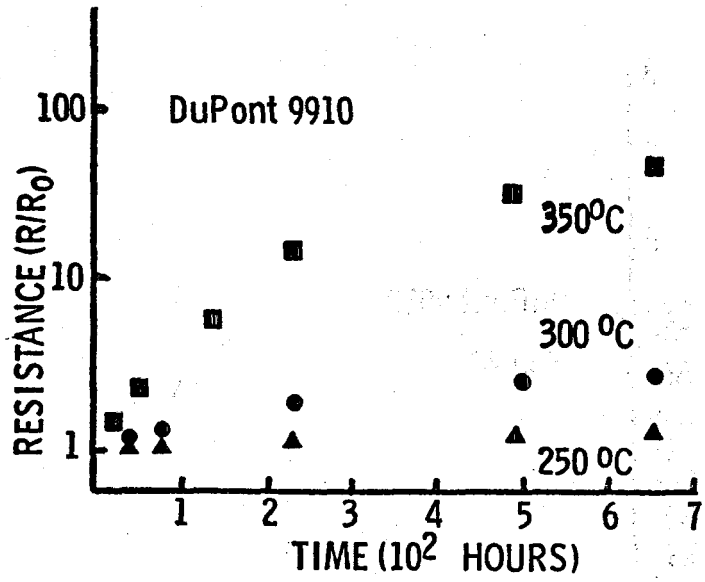


Fig. 52. Rate of bond resistance increase is highly temperature dependent. Three mil pure aluminum wire was used for bonds.

Thus, the same physical process is leading to bond degradation in all the Al wire--Au thick film systems. However, the Pt-Au 4121 thick film exhibited an activation energy of only .18 eV with an extremely small frequency factor. Thus, a different degradation process is involved in this system. These activation energy values are not out of line with past work done with Au-Al diffusion systems.[26]

Test 3, 1 mil Al Wire on 9910 -- After the first two tests had indicated the relative advantage of DuPont 9910 for Al wire bonding (see Fig. 51), additional tests using 1-mil wire (99% Al - 1% Si) were performed. A Kulicke & Soffa 484 ultrasonic bonder was again used to make bonds to 12 dot patterned substrates. All bonds were formed at one sitting to ensure consistency.

Initial resistance readings were taken on all samples, and one substrate had all bonds pulled for strength measurements. The other samples were placed in a 300°C air oven. Periodically the samples were cooled to room temperature for resistance readings. At each reading one of the remaining samples was pull-tested. Figures 53 and 54 show the results of these tests. The resistance growth was approximately linear with time. The pull strengths showed a definite minimum. One possible interpretation for these results would be (1) the initial decrease in pull strengths resulted from an annealing of the Al wire which was originally highly cold worked, and (2) the subsequent increase in pull strength results from the mechanically stronger intermetallic regions growing throughout the bonding region. The majority of bond

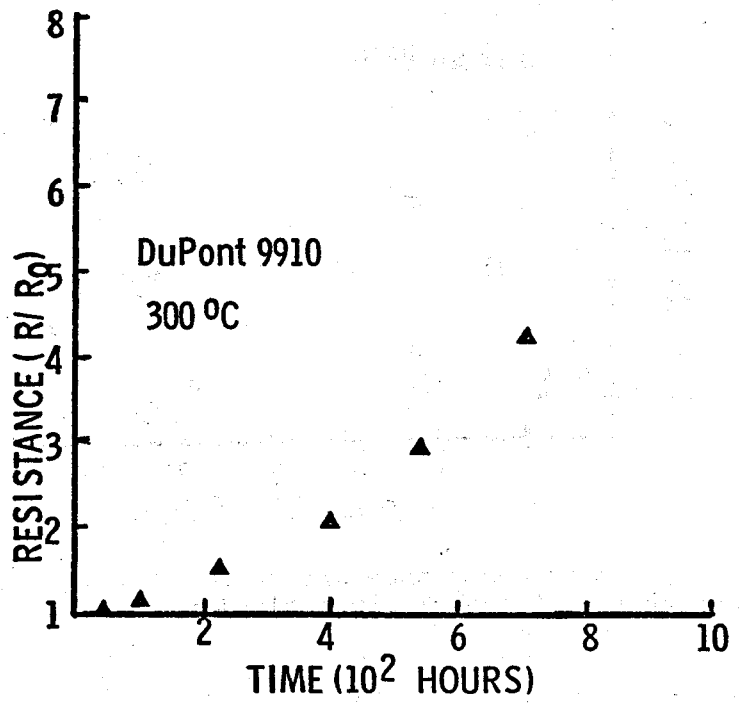


Fig. 53. Resistance increase with time of DuPont 9910 modified gold composition bonds with aluminum 1 mil wire (1% silicon added).

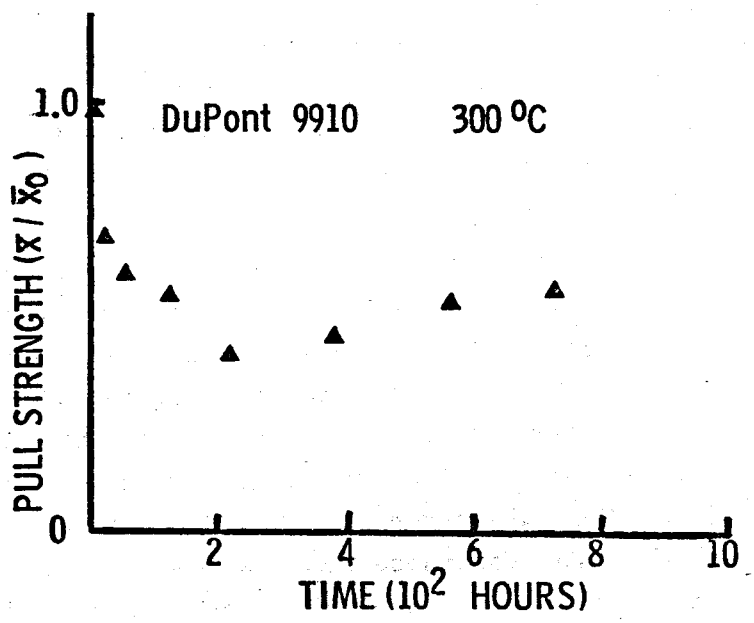


Fig. 54. Pull strength of bonds during 300°C aging. One mil aluminum wire (1% silicon added) was bonded to DuPont 9910 modified gold composition.

failures occurred at the thinned heel of the bond, the hard surface of the thick film resulted in more wire deformation than occurs on evaporated thin film hybrids. Typically the initial average bond strengths were 6-8 g with a standard deviation of 0.8 g. DuPont 9910 metallization has proved reliable and adequate for Al wire bonding.

Some general conclusions can be made from this work. First, there exist large diffusion rate differences between different thick films used in bonding even when they all are mostly Au. Second, all thick films have hard surfaces which cause excessive wire deformation upon bond formation. Third, aluminum wire annealing causes initial loss in bond strength regardless of thick film. Fourth, bond degradation rates depend strongly on the temperature.

B. Diffusion Barrier Pad Interconnections

Higher bond strengths and slower bond degradation are possible by placing a diffusion barrier pad between the Al wire and the thick film. Figure 55 shows schematics of such pads that were tested. Although many different materials could be used for pads, the most natural choice for a pad is a diffusion proof wafer with Au on one side and Al on the other. In this way the Au can be thermocompression bonded to the Au thick film and the Al surface will accept Al wire bonds. Since the wafer itself blocks diffusion there is no Al-Au intermetallic problem. Nickel, kovar, and silicon have been used as diffusion barrier wafers. The metal wafers were 1 mil thick and 30 mils in diameter. Care was taken in annealing to obtain large grains so that the slower bulk diffusion was dominant over the faster grain boundary diffusion. The Au and Al were evaporated onto the foil which was then punched out as disks. To make silicon buffer pads, a standard highly doped 5-mil wafer had Au and Al vapor deposited and then was diamond sawed to produce 30-mil square pads. The pads were eutectically attached to the thick film rather than thermocompression bonded. These silicon bonding pads promise to be at least as long lived as the active devices themselves since the gold and aluminum diffusion distances are the same. This bond pad system has the advantage of being easily fabricated in any semiconductor shop.

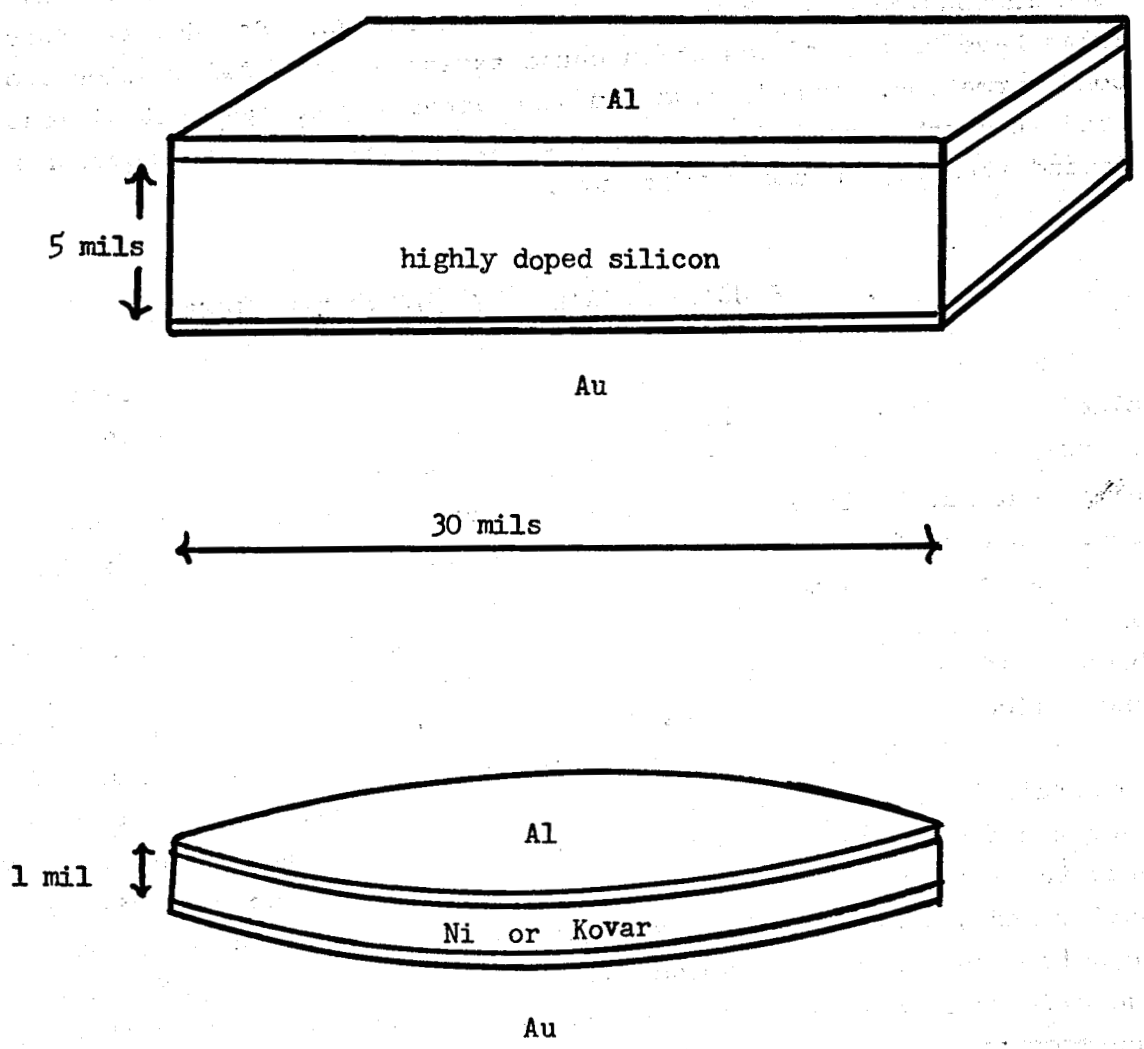


Fig. 55. Schematics of diffusion barrier pads. Gold and aluminum films were evaporated onto pads.

It was found that bonds could be directly made to the nickel wafer without need of the Al film. This simplified pad fabrication but presented a harder surface to the wire. Thus, standard Al wire was excessively deformed. A harder wire, say a more highly cold worked wire, with only 0.5% elongation could be used to be more compatible with the nickel.

Tests -- The most exhaustive tests to date have been performed on the Au-coated nickel disks. The Au surface was thermocompression bonded with a wobble bonder to the standard dot pattern samples made of four different thick films: 9910, 4121, 9791, and 4399. Al wire loops were formed between adjacent pads forming 70 bonds in electrical series. One sample of each was pull-tested immediately and the rest were aged at 250, 300, and 350°C with regular resistance monitoring and a final bond pull test after 1000 hours of aging. Only a slight (5%) bond resistance change was noticed during the test. Pull strengths decreased due to the annealing of the Al wire. No failure of adhesion between pad and thick film was noticed, nor any degradation at the Al-Ni interface.

There are some obvious drawbacks to the use of diffusion barrier pads. First, more substrate area is required for the 30-mil diameter pads than for a simple bond; second, labor is required to secure the pads to the substrate; third, the number of bond interfaces is doubled introducing more chance of failures; fourth, the pads add expense to the circuit (10¢ a pad). However, the complete lack of bond resistance degradation and retention of pull strengths mark diffusion barrier pads as a high reliability, high temperature system.

C. Tape Carrier

Tape carrier technology is a new technology being introduced for easier mass production of microcircuits. Usually the carrier consists of a tape of plastic film (not unlike a movie reel) with many identical sets of metal leads etched on it (see Figure 56). The chips are attached to the leads on the film, then the film is positioned over the circuit, and, last, all the chip leads are fastened to the circuit breaking the chip and leads off the plastic film in one step.

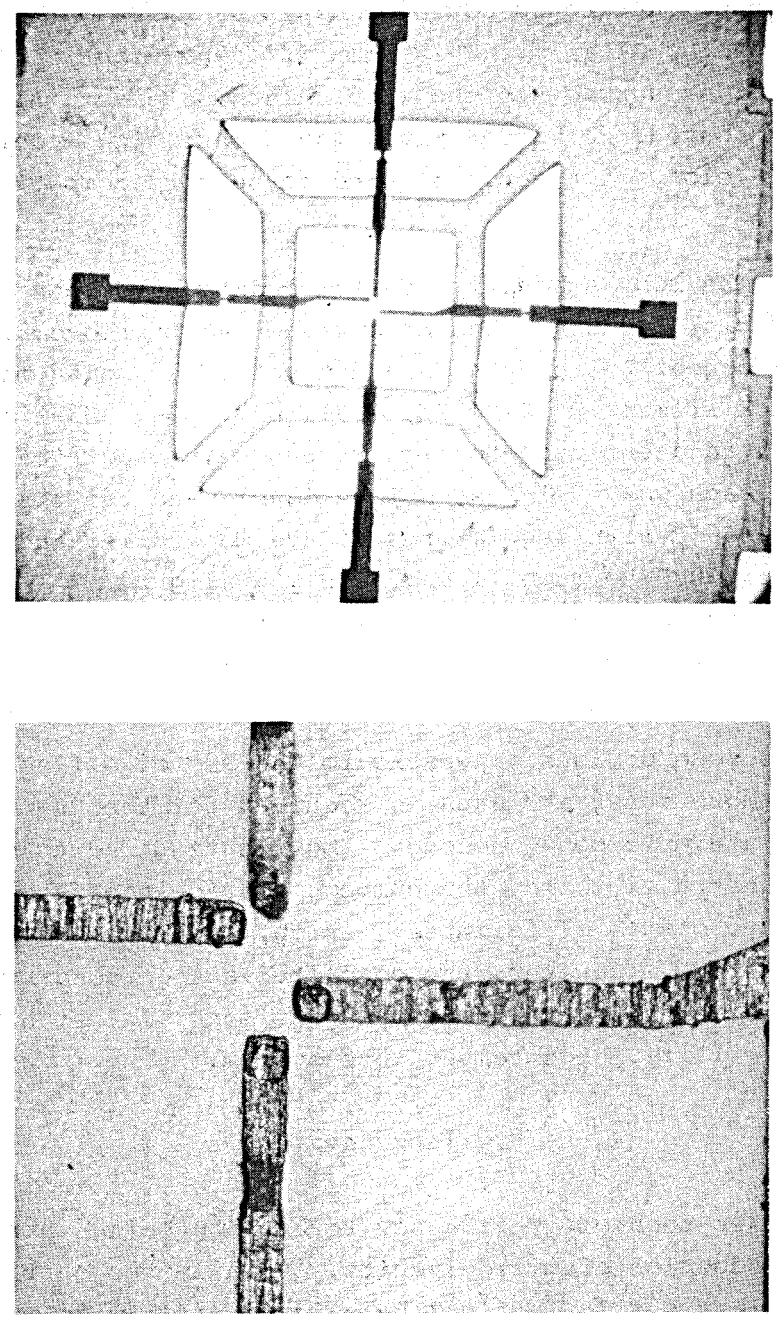


Fig. 56. Microscopic views of high temperature tape carrier. (Top) Four copper beams are supported by polyimide tape. Each beam has a breakaway neck for final attachment to hybrid. (Bottom) Close view of 2-mil wide beams show nickel bumps used to bond to aluminum pads on silicon die.

Special modified tape carriers were made for high temperature bonding.[28] The copper beams were bumped with nickel at the ends, each bump being 2 mils in diameter to fit within the standard chip bonding pad. The bumps were then coated with a 2 μm film of aluminum to facilitate the bump-pad ultrasonic bond. The reverse side of the beam was gold plated so that the beam could be thermocompression bonded to the thick film. Initial tests have proved feasibility but have not revealed reliability or lifetime.

D. Au-Ge Solder

Gold-Germanium eutectic solder (M.P. 356°C) has been used to attach active devices in TO cans to printed circuit boards and also small discrete components directly to hybrid substrates (rectifiers). Success has been found with DuPont Formon 8513 thick film Au-Ge solder ink paste. Reflow is created with a hotplate set slightly below the flow temperature and a small torch or hot iron to cause reflow one connection at a time. It is also possible to solely use an iron or torch.

CHAPTER 6 - PRESCREENING ACTIVE DEVICES

Introduction

Within a specific lot of a device type, there exists large electrical characteristic differences at elevated temperatures. Thus, the normal reasons for pretesting a device before commitment to a particular circuit are more imperative for high temperature circuitry. In circuit fabrication to date, four needs for prescreening have developed: (1) rejection of devices that have excessive temperature dependence, (2) tailoring of the hybrid to fit the exact device characteristics, (3) matching devices, and (4) eliminating infant mortality.

The spread of characteristics due to temperature dependence can be large even within a given device lot. Circuit design and calibration are greatly simplified by eliminating any device showing above average temperature change in characteristics by prescreening.

In most cases when a device is needed for a linear function, it is necessary to bias the device at its zero temperature coefficient point (see Figure 28, for example). Since the bias current or voltage to achieve this zero point differ significantly within a lot, each device must be characterized from 25 to 300°C and then the resistor biasing network in a particular hybrid must be custom trimmed for that particular device.

A more exacting reason for pretesting devices was to find matched devices for inputs in a differential amplifier. Not only must the characteristics match at room temperature, but up to 300°C for all working biases.

The most common prescreening motive in standard circuitry is to enhance reliability. In any lot of devices there are a few which are initially impaired, although this cannot be detected from standard characterization. For example, a die may have a crack in the passivation layer. Such a crack can severely shorten the operational lifetime since corrosives can reach the active surface of the semiconductor; however, initial test would reveal no fault because no corrosion has occurred yet. However, a burn-in, operation under bias and perhaps elevated temperature, for a hundred hours will cause precipitous failure (infant mortality) for the defective parts. In contrast such a test will hardly shorten the expected lifetime for the perfect devices (10,000-100,000 hours).

Three methods of prescreening have been investigated during this study; device attachment to a ceramic chip carrier, segregation of the device within the hybrid, and device attachment to polyimide film chip carrier tapes.

Ceramic Chip Carriers

A common method of prescreening devices in hybrid fabrication is the ceramic chip carrier. A small wafer of ceramic, perhaps 150 by 150 mils, has a metallization pattern allowing device mounting and external lead connection (see Figure 57). In a typical use long gold ribbon was welded on the outer pads of the ceramic chips. One device was then eutectically attached to each chip. Aluminum wires connected the device pads to the ceramic chip pads. The device-ceramic carrier unit was placed in the oven with the ribbon connected to binding posts. After characterization over the complete temperature range and high temperature aging the unit was ready for a circuit. The ceramic chip was attached to the hybrid substrate either with ceramic cement[29] or with gold-germanium solder. The chip must have gold backing for the use of solder. The device is now electrically connected to the circuit by welding the shortened gold ribbons to the conductor pads on the hybrid substrate.

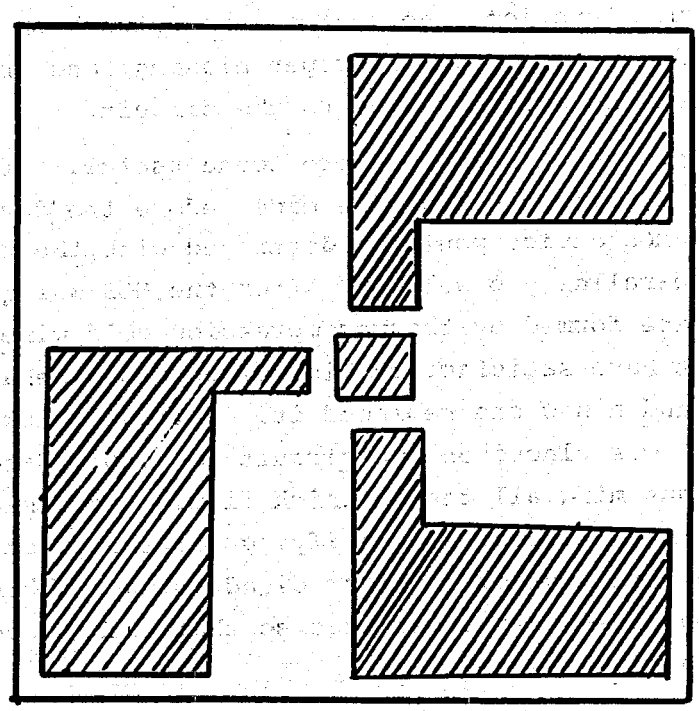


Fig. 57. Ceramic chip carrier for die mounting and pretesting at high temperatures.

This pretesting method involves much attachment and fairly large substrate area compared to the device chip area; however, in its favor no devices other than the faulty need be wasted. That is, for any given device characteristics a hybrid can be tailored or a matching device can be found. A standard temperature version of this method of device handling has been around for at least 10 years (chip-in channels) and has been made highly reliable.

Device Segregation

To date in this project pretesting by device segregation has proved the most convenient method. When the artwork for the conductor pattern was made, the bonding pads for the active device were made large enough to accommodate a Au ribbon in addition to the aluminum wire from the die. In addition, these conductor pads were isolated from the rest of the circuit by breaks in the conductor which were ribbon bridged once the active device had been characterized at temperature.

The testing procedure was straightforward: First, the active device was eutectically died down and the wire bonds were made. Next, gold ribbon was connected between these pads and the oven testing terminal. Now characteristics were taken over the complete temperature range of interest and aging tests were accomplished. If the device was acceptable for this circuit function, the rest of the network on the circuit was adjusted (resistors trimmed for proper biasing) and bridging ribbons were used to connect the active device to the circuit.

Several points of practice were found useful. If MOS rather than JFETs were used, ribbon welds were made before the device die down. Otherwise the MOS device would be destroyed with the nearby current pulse of the parallel gap welder. After the MOS was qualified, bridging connections were formed by thermocompression gold wire bonding. If a device did not have satisfactory high temperature behavior, it was scrubbed off and a new one replaced it. A large thick film patch (50 x 50 mils) was placed on the circuit to accommodate several different die without consuming all the Au thick film. One disadvantage of this approach was that devices not qualifying for the exact spot they were first located were wasted. Another disadvantage was the need to make the circuit on bite-sized substrates so that each piece had only one or two critical active devices.

Polyimide Tape Carriers

To date the most promising but least tested system is the polyimide tape carrier system (see Figure 56). Various forms of this technology have been introduced in commercial high volume production over the last 5 years, but no predominant variation yet reigns supreme. For operation at high temperature several special considerations must exist: The tape material must age well and the beam metallization must be compatible with the common aluminum pads on the chips. For these reasons a polyimide tape was chosen and the standard copper leads were modified by plating gold on the region to be bonded to the gold hybrid conductor and forming nickel bumps (2-mil diameter) on the beam end intended for bonding to the aluminum pad on the die. Either the nickel bump is directly bonded to the aluminum pad or a thin film of aluminum is evaporated on the nickel before bonding. Aging tests have not been performed to compare these two approaches.

The advantage of this prescreening system is that it can also solve the bonding problem by a careful choice of metallization. The penalty is the need for special bonding equipment and expertise. If the tape carrier system eventually settled on by industry has high temperature capability, then the availability and consequent lower cost of polyimide tape carriers should greatly simplify high temperature hybridization.

CONCLUSION

Four active device types have been investigated for use in microcircuits operated from 25 to 300°C. (1) The most promising device has been the silicon junction field effect transistor (JFET). Both n and p-channel types have functioned up to 325°C and have been used in circuits up to 300°C. These devices show little aging during a 300°C 1000-hour test. Commercial JFETs perform closely to standard model predictions. These models indicate fabrication parameter changes which would lessen JFET temperature dependence. (2) Silicon insulated gate field effect transistors (MOSFET) function well up to 300°C. Significant aging changes sometimes occur after about 100 hours at high temperatures, thereby limiting circuit use. Model comparisons indicate possible improvement in temperature stability. (3) Silicon bipolar devices experience eight orders of magnitude change in leakage current over the temperature range 25 to 300°C, thus making them impractical in most circuit design. (4) GaAs devices have promise in theory. Existing MESFET and JFET types tested showed more temperature dependence and thermal aging than their silicon counterparts. Two high temperature device redesign rules were found: First, elimination of gold in the semiconductor would significantly reduce high temperature leakage, and, secondly, higher doping concentrations produce less behavior variation with temperature.

Modification of commercial bonding procedures was necessary to attach active devices for high temperature operation. Special thick film conductor was used to allow ultrasonic aluminum wire bonds which would survive 300°C aging. In addition, diffusion barrier pads were developed to serve as the go-between from Au thick films to aluminum wire bonds. Beam leaded transistors were used where possible since their gold leads formed a high temperature bond with the thick film. Tape carrier systems showed promise for solving bonding and prescreening processes. Discrete devices were soldered on with Au/Ge eutectic solder.

Because of the large temperature range of operation active devices were pretested at high temperature. This pretest allowed elimination of infant mortality, rejection of extremely temperature dependent devices, tailoring of hybrids to specific chips, and matching of chips. Three systems were used to achieve pretesting at high temperatures: (1) ceramic chip carriers, (2) polyimide chip carriers, and (3) isolated pads on the hybrid itself.

To date several different hybrid microcircuits and printed circuit boards have been tested from 25 to 300°C. Life tests have been run from 150 to 1000 hours with no active device failures or significant drift.

APPENDIX

The following four programs model silicon MOSFETs and JFETs. The program format serves Sandia's "NOS" system, and can be easily adapted to any standard time sharing computer system.

NMOS

PROGRAM NMOS2

```
00005 REM CORRECTED VERSION
00100 READ H,K,Q1,D1,M1,M2,D3
00110 DATA 6.6262E-34,1.38062E-23,1.60219E-19
00120 DATA 1.03594E-10,5.283545E-31,9.656134E-31
00130 DATA 3.453132E-11
00132 FOR X=1 TO 2
00134 PRINT
00136 IF X=1 GO TO 00139
00137 PRINT "FOR THE DRAIN REGION:"
00138 GO TO 00140
00139 PRINT "FOR THE BULK (SUBSTRATE):"
00140 PRINT"ENTER THE DENSITY OF TRAPPING CENTERS PER CUBIC"
00150 PRINT"CENTIMETER, TRAPPING CROSS SECTION FOR ELECTRONS"
00160 PRINT"AND TRAPPING CROSS SECTION FOR HOLES IN SQUARE"
00170 PRINT"CENTIMETERS, AND THE HEIGHT OF THE TRAPPING"
00180 PRINT"LEVEL ABOVE THE CENTER OF THE GAP (IN EV)."
00190 F=1
00200 INPUT N4(X),A2(X),A3(X),E1(X)
00210 N4(X)=N4(X)*E6
00220 A2(X)=A2(X)*1E-4
00230 A3(X)=A3(X)*1E-4
00235 NEXT X
00240 PRINT
00250 PRINT"ENTER THE ACCEPTOR CONCENTRATION IN THE"
00260 PRINT"BULK AND THE DONAR CONCENTRATION FOR THE"
00270 PRINT"DRAIN (PER CUBIC CENTIMETER)."
00280 INPUT N2,N3
00290 PRINT
00300 PRINT"ENTER THE LENGTH AND WIDTH OF THE CHANNEL"
00310 PRINT"IN MICRONS AND THE OXIDE THICKNESS IN ANGSTROMS."
00320 INPUT L1,Z,D2
00330 PRINT
00340 PRINT"ENTER THE AREA OF THE DRAIN/SUBSTRATE"
00350 PRINT"JUNCTION IN SQUARE CENTIMETERS."
00360 INPUT A1
00370 N2=N2*1E6
00380 N3=N3*1E6
00390 L1=L1*1E-6
00400 Z=Z*1E-6
00410 A1=A1*1E-4
00420 D2=D2*1E-10
00430 PRINT
00440 PRINT"ENTER THE METAL-SEMICONDUCTOR WORK FUNCTION"
00450 PRINT"DIFFERENCE AT ROOM TEMPERATURE (EV) AND THE"
00460 PRINT"DENSITY OF SURFACE STATE CHARGE (NUMBER OF "
00470 PRINT"STATES PER SQUARE CENTIMETER THAT CONTAIN CHARGE)."
00480 INPUT P1,Q2
00490 Q2=Q2*Q1*10000
00500 T=300
```

```
00510 GOSUB 00630
00520 A8=P1+V7*LOG(N5/N1)+P2
00530 PRINT
00540 PRINT"ENTER THE STARTING AND ENDING TEMPERATURES"
00550 PRINT"IN DEGREES CENTIGRADE, FOLLOWED BY THE"
00560 PRINT"TEMPERATURE INCREMENT TO BE USED."
00570 INPUT T1,T2,T3
00580 T1=T1+273
00590 T2=T2+273
00600 FOR T=T1 TO T2 STEP T3
00610 GOSUB 00630
00620 GOTO 00710
00630 V7=K*T/Q1
00640 E2=1.12-(T-300)*2.4E-4
00650 N5=12*(2*3.14159*M1*K*T/H**2)**1.5
00660 N6=2*(2*3.14159*M2*K*T/H**2)**1.5
00670 N1=SQR(N5*N6)*EXP(-E2/(2*V7))
00680 P2=V7*LOG((N2+SQR(N2*N2+4*N1*N1))/(2*N1))
00690 P3=V7*LOG((N3+SQR(N3*N3+4*N1*N1))/(2*N1))
00700 RETURN
00710 C=D3/D2
00720 V8=2*P2+(2/C)*SQR(D1*Q1*N2*P2)
00730 V6=3.5746E17*N2**(-.71717)
00740 M3=5.5905E17*T**1.5
00750 M3=M3/(N2*LOG((195006.3*T/N2**(1/3))**2+1))
00760 M3=1/(1/M3+1/(2.104E5*T**(-2.5)))
00770 M4=5.78678E17*T**1.5
00780 M4=M4/(N3*LOG((195006.3*T/N3**(1/3))**2+1))
00790 M4=1/(1/M4+1/(2.3414E5*T**(-2.7)))
00800 REM FNA IS THE CHARGE DISTRIBUTION IN PARTICLES/CC
00810 DEF FNA(X)=Q*X
00820 DEF FNB(X)=Q1*FNA(X)
00830 REM FNC(X) IS THE INTEGRAND
00840 Y=0
00850 DEF FNC(X)=X*FNB(X)/D2
00860 FOR X=0 TO D2-D2/1000 STEP D2/1000
00870 Y=((FNC(X)+FNC(X+D2/1000))/2)*D2/1000 +Y
00880 NEXT X
00890 P1=A8-V7*LOG(N5/N1)-P2
00900 V5=P1-Q2/C-Y/C
00910 V4=SQR(3*K*T/9.10956E-31)
00920 IF F=0 GOTO 01000
00930 PRINT
00940 PRINT"THE TURN ON VOLTAGE AT";T-273;"C IS";V8+V5;"V"
00950 PRINT"DRAIN BREAKDOWN VOLTAGE=";V6
00960 PRINT"ENTER THE LOWER AND UPPER LIMITS AND"
00970 PRINT"THE STEP SIZE FOR THE GATE AND"
00980 PRINT"DRAIN VOLTAGES"
00990 INPUT V1(1),V1(2),V1(3),V2(1),V2(2),V2(3)
01000 FOR X=1 TO 4
01010 PRINT
01020 NEXT X
01030 PRINT"************************"
01040 PRINT "TEMPERATURE=";T-273;"C"
01050 PRINT"TURN ON VOLTAGE=";V8+V5
01060 PRINT
01070 PRINT
01080 PRINT" VGS     VDS       IDS    **";
01090 PRINT" VGS     VDS       IDS"
01100 X1=1
```

13

```
01110 FOR V1=V1(1) TO V1(2) STEP V1(3)
01120 FOR V2=V2(1) TO V2(2) STEP V2(3)
01130 J=V2
01140 V9=V1-V5
01150 K1=(SQR(D1*Q1*N2))/C
01160 I1=0
01170 I2=0
01180 I3=0
01190 REM START LEAKAGE CURRENTS
01200 IF V2=0 GOTO 01400
01210 W=SQR(2*D1*(N2+N3)/(N2*N3*Q1))
01220 W=W*SQR(V2+P2+P3)
01222 X(1)=W/(N2/N3+1)
01224 X(2)=W-X(1)
01226 FOR S=1 TO 2
01230 I(S)=(Q1*N4(S))*(A3(S)*N1*A1)*(A2(S)*V4*X(S))
01240 I(S)=I(S)/(A2(S)*EXP(E1(S)/V7)+A3(S)*EXP(-E1(S)/V7))
01242 NEXT S
01244 I=I(1)+I(2)
01250 IF V2<3*V7 GOTO 01290
01260 I2=Q1*N1*N1*A1*SQR(V7)
01270 T4(1)=1/(A2(1)*V4*N4(1))
01272 T4(2)=1/(A3(2)*V4*N4(2))
01280 I2=I2*(SQR(M3)/(N2*SQR(T4(1)))+SQR(M4)/(N3*SQR(T4(2))))
01290 IF V9>V8 GOTO 01310
01300 GOTO 01400
01310 V3=V9-2*P2+K1*K1*(1-SQR(1+2*V9/(K1*K1)))
01320 IF V2>V3 GOTO 01350
01330 L2=L1
01340 GOTO 01370
01350 L2=L1-SQR(2*D1*(V2-V3)/(Q1*N2))
01360 V2=V3
01370 I3=V2*(V9-2*P2-V2/2)
01380 I3=I3-(2*SQR(2)*K1/3)*((V2+2*P2)**1.5-(2*P2)**1.5)
01390 I3=I3*Z*M3*C*.45/L2
01400 I4=I1+I2+I3
01410 V2=J
01420 PRINT USING"##.#",V1;
01430 PRINT"    ";
01440 PRINT USING"##.#",V2;
01450 PRINT"    ";
01460 PRINT USING "#.##^^^^",I4;
01470 PRINT" **";
01480 IF X1=1 GOTO 01520
01490 PRINT" "
01500 X1=1
01510 GOTO 01530
01520 X1=2
01530 NEXT V2
01540 NEXT V1
01550 F=0
01560 NEXT T
01570 END
READY.
```

PROGRAM PMOS2

```
00005 REM CORRECTED VERSION
00100 READ H,K,Q1,D1,M1,M2,D3
00110 DATA 6.6262E-34,1.38062E-23,1.60219E-19
00120 DATA 1.03594E-10,5.283545E-31,9.656134E-31
00130 DATA 3.453132E-11
00132 FOR X=1 TO 2
00134 PRINT
00136 IF X=1 GO TO 00139
00137 PRINT "FOR THE DRAIN REGION:"
00138 GO TO 00140
00139 PRINT "FOR THE BULK (SUBSTRATE):"
00140 PRINT"ENTER THE DENSITY OF TRAPPING CENTERS PER CUBIC"
00150 PRINT"CENTIMETER, TRAPPING CROSS SECTION FOR ELECTRONS"
00160 PRINT"AND TRAPPING CROSS SECTION FOR HOLES IN SQUARE"
00170 PRINT"CENTIMETERS, AND THE HEIGHT OF THE TRAPPING"
00180 PRINT"LEVEL ABOVE THE CENTER OF THE GAP (IN EV)"
00190 F=1
00200 INPUT N4(X),A2(X),A3(X),E1(X)
00210 N4(X)=N4(X)*1E6
00220 A2(X)=A2(X)*1E-4
00230 A3(X)=A3(X)*1E-4
00235 NEXT X
00240 PRINT
00250 PRINT"ENTER THE DONAR CONCENTRATION IN THE"
00260 PRINT"BULK AND THE ACCEPTOR CONCENTRATION FOR THE "
00270 PRINT"DRAIN (PER CUBIC CENTIMETER)."
00280 INPUT N3,N2
00290 PRINT
00300 PRINT"ENTER THE LENGTH AND WIDTH OF THE CHANNEL"
00310 PRINT"IN MICRONS AND THE OXIDE THICKNESS IN ANGSTROMS."
00320 INPUT L1,Z,D2
00330 PRINT
00340 PRINT"ENTER THE AREA OF THE DRAIN/SUBSTRATE"
00350 PRINT"JUNCTION IN SQUARE CENTIMETERS."
00360 INPUT A1
00370 N2=N2*1E6
00380 N3=N3*1E6
00390 L1=L1*1E-6
00400 Z=Z*1E-6
00410 A1=A1*1E-4
00420 D2=D2*1E-10
00430 PRINT
00440 PRINT"ENTER THE METAL-SEMICONDUCTOR WORK FUNCTION"
00450 PRINT"DIFFERENCE AT ROOM TEMPERATURE (EV) AND THE "
00460 PRINT"DENSITY OF SURFACE STATE CHARGE (NUMBER OF"
00470 PRINT"STATES PER SQUARE CENTIMETER THAT CONTAIN CHARGE)."
00480 INPUT P1,Q2
00490 Q2=Q2*Q1*10000
00500 T=300
00510 GOSUB 00630
00520 A8=P1+V7*LOG(N5/N1)-P2
00530 PRINT
00540 PRINT"ENTER THE STARTING AND ENDING TEMPERATURES"
00550 PRINT"IN DEGREES CENTIGRADE, FOLLOWED BY THE"
00560 PRINT"TEMPERATURE INCREMENT TO BE USED."
00570 INPUT T1,T2,T3
00580 T1=T1+273
00590 T2=T2+273
```

```
00600 FOR T=T1 TO T2 STEP T3
00610 GOSUB 00630
00620 GOTO 00710
00630 V7=K*T/Q1
00640 E2=1.12-(T-300)*2.4E-4
00650 N5=12*(2*3.14159*M1*K*T/H**2)**1.5
00660 N6=2*(2*3.14159*M2*K*T/H**2)**1.5
00670 N1=SQR(N5*N6)*EXP(-E2/(2*V7))
00680 P2=V7*LOG((N3+SQR(N3*N3+4*N1*N1))/(2*N1))
00690 P3=V7*LOG((N2+SQR(N2*N2+4*N1*N1))/(2*N1))
00700 RETURN
00710 C=D3/D2
00720 V8=-2*P2-(2/C)*SQR(D1*Q1*N3*P2)
00730 V6=3.5746E17*N3**(-.71717)
00740 M4=5.78678E17*T**1.5
00750 M4=M4/(N3*LOG((195006.3*T/N3**(1/3))**2+1))
00760 M4=1/(1/M4+1/(2.3414E5*T**(-2.7)))
00770 M3=5.5905E17*T**1.5
00780 M3=M3/(N2*LOG((195006.3*T/N2**(1/3))**2+1))
00790 M3=1/(1/M3+1/(2.104E5*T**(-2.5)))
00800 REM FNA IS THE CHARGE DISTRIBUTION IN PARTICLES/CC
00810 DEF FNA(X)=0*X
00820 DEF FNB(X)=Q1*FNA(X)
00830 REM FNC(X) IS THE INTEGRAND
00840 Y=0
00850 DEF FNC(X)=X*FNB(X)/D2
00860 FOR X=0 TO D2-D2/1000 STEP D2/1000
00970 Y=((FNC(X)+FNC(X+D2/1000))/2)*D2/1000+Y
00880 NEXT X
00890 P1=A8-V7*LOG(N5/N1)+P2
00900 V5=P1-Q2/C-Y/C
00910 V4=SQR(3*K*T/9.10956E-31)
00920 IF F=0 GOTO 01000
00930 PRINT
00940 PRINT"THE TURN ON VOLTAGE AT";T-273;"C IS";V8+V5;"V"
00950 PRINT"DRAIN BREAKDOWN VOLTAGE=";V6;"V"
00960 PRINT"ENTER THE LOWER AND UPPER LIMITS AND"
00970 PRINT"THE STEP SIZE FOR THE GATE AND"
00980 PRINT"DRAIN VOLTAGES (INCLUDE THE SIGNS)."
00990 INPUT V1(1),V1(2),V1(3),V2(1),V2(2),V2(3)
01000 FOR X=1 TO 4
01010 PRINT
01020 NEXT X
01030 PRINT"*********************"
01040 PRINT"TEMPERATURE=";T-273;"C"
01050 PRINT"TURN ON VOLTAGE=";V8+V5
01060 PRINT
01070 PRINT
01080 PRINT"  VGS      VDS        IDS    **";
01090 PRINT"  VGS      VDS        IDS"
01100 X1=1
01110 FOR V1=V1(1) TO V1(2) STEP V1(3)
01120 FOR V2=V2(1) TO V2(2) STEP V2(3)
01130 J=V2
01140 V9=V1-V5
01150 K1=(SQR(D1*Q1*N3))/C
01160 I1=0
01170 I2=0
01180 I3=0
```

```
01190 REM START LEAKAGE CURRENTS
01200 IF V2=0 GOTO 01400
01210 W=SQR(2*D1*(N2+N3)/(N2*N3*Q1))
01220 W=W*SQR(-V2+P2+P3)
01222 X(1)=W/(N2/N3+1)
01224 X(2)=W-X(1)
01226 FOR S=1 TO 2
01230 I(S)=(Q1*N4(S))*(A3(S)*N1*A1)*(A2(S)*V4*X(S))
01240 I(S)=I(S)/(A2(S)*EXP(E1(S)/V7)+A3(S)*EXP(-E1(S)/V7))
01242 NEXT S
01244 I=I(1)+I(2)
01250 IF -V2<3*V7 GOTO 01290
01260 I2=Q1*N1*N1*A1*SQR(V7)
01270 T4(1)=1/(A2(1)*V4*N4(1))
01272 T4(2)=1/(A3(2)*V4*N4(2))
01280 I2=I2*(SQR(M3)/(N2*SQR(T4(1)))+SQR(M4)/(N3*SQR(T4(2))))
01290 IF V9<V8 GOTO 01310
01300 GOTO 01400
01310 V3=V9+2*P2-K1*K1*(1-SQR(1-2*V9/(K1*K1)))
01320 IF V2<V3 GOTO 01350
01330 L2=L1
01340 GOTO 01370
01350 L2=L1-SQR(2*D1*(V3-V2)/(Q1*N3))
01360 V2=V3
01370 I3=V2*(V9+2*P2-V2/2)
01380 I3=I3-(2*SQR(2)*K1/3)*((-V2+2*P2)**1.5-(2*P2)**1.5)
01390 I3=I3*Z*M4*.45*C/L2
01400 I4=-(I1+I2+I3)
01410 V2=J
01420 PRINT USING"###.#",V1;
01430 PRINT"    ";
01440 PRINT USING"###.#",V2;
01450 PRINT"    ";
01460 PRINT USING"##.##^^^^",I4;
01470 PRINT" **";
01480 IF X1=1 GOTO 01520
01490 PRINT" "
01500 X1=1
01510 GOTO 01530
01520 X1=2
01530 NEXT V2
01540 NEXT V1
01550 F=0
01560 NEXT T
01570 END
READY.
```

PROGRAM NJFET

```
00100 READ H,K,Q1,D1,M1,M2
00110 DATA 6.6262E-34,1.38062E-23,1.60219E-19
00120 DATA 1.03594E-10,5.28345E-31,9.656134E-31
00130 PRINT"ENTER THE DONAR CONCENTRATION IN THE"
00140 PRINT"CHANNEL AND THE ACCEPTOR CONCENTRATION IN THE"
00150 PRINT"GATE (PER CUBIC CENTIMETER)."
00160 INPUT N1,N2
00170 IF N2>=50*N1 GOTO 00210
00180 PRINT"WARNING: THIS PROGRAM ASSUMES A ONE-SIDED "
00190 PRINT"JUNCTION AT THE GATE."
00200 GOTO 00130
00210 PRINT
00220 PRINT"ENTER THE LENGTH, WIDTH, AND DEPTH (JUNCTION"
00230 PRINT"TO JUNCTION) OF THE CHANNEL IN MICRONS."
00240 INPUT L1,Z,D2
00250 PRINT
00260 PRINT"ENTER THE STARTING AND ENDING TEMPERATURES"
00270 PRINT"IN DEGREES CENTIGRADE, FOLLOWED BY THE"
00280 PRINT"TEMPERATURE INCREMENT TO BE USED."
00290 INPUT T1,T2,T3
00300 PRINT
00310 PRINT"INPUT THE SOURCE AND DRAIN RESISTANCES."
00320 INPUT R1,R2
00330 N1=N1*1E6
00340 N2=N2*1E6
00350 L1=L1*1E-6
00360 Z=Z*1E-6
00370 D2=D2*1E-6
00380 T1=T1+273
00390 T2=T2+273
00400 T=300
00410 GOSUB 00690
00420 R3=R1*M3
00430 R4=R2*M3
00440 C2=4*SQR(2*D1/(Q1*N1))/(3*D2)
00450 C3=Q1*N1*D2*D2/(24*D1)
00460 PRINT
00470 PRINT"ENTER THE LOWER AND UPPER LIMITS AND "
00480 PRINT"THE STEP SIZE FOR THE GATE AND DRAIN"
00490 PRINT"VOLTAGES (INCLUDE THE SIGNS)."
00500 INPUT V2(1),V2(2),V2(3),V3(1),V3(2),V3(3)
00510 FOR T=T1 TO T2 STEP T3
00520 FOR X=1 TO 4
00530 PRINT
00540 NEXT X
00550 PRINT"*****************"
00560 PRINT"TEMPERATURE=";T-273;"C"
00570 V7=K*T/Q1
00580 E2=1.12-(T-300)*2.4E-4
00590 N5=12*(2*3.14159*M1*K*T/H**2)**1.5
00600 N6=2*(2*3.14159*M2*K*T/H**2)**1.5
00610 N3=SQR(N5*N6)*EXP(-E2/(2*V7))
00620 P1=V7*LOG((N1+SQR(N1*N1+4*N3*N3))/(2*N3))
00630 P2=V7*LOG((N2+SQR(N2*N2+4*N3*N3))/(2*N3))
00640 V1=P1+P2
00650 V9=V1-Q1*N1*D2*D2/(8*D1)
00660 PRINT"TURN OFF VOLTAGE=";V9;"V"
```

```
00670 GOSUB 00690
00680 GOTO 00730
00690 M3=5.5905E17*T**1.5
00700 M3=M3/(N1*LOG((195006.3*T/N1**(1/3))**2+1))
00710 M3=1/(1/M3+1/(2.104E5*T**(-2.5)))
00720 RETURN
00730 C1=Z*Q1*M3*N1*D2/L1
00740 R1=R3/M3
00750 R2=R4/M3
00760 PRINT
00770 PRINT
00780 PRINT" VGS     VDS       IDS    **";
00790 PRINT" VGS     VDS       IDS"
00800 F=1
00810 FOR V2=V2(1) TO V2(2) STEP V2(3)
00820 IF V2<V9 GOTO 01220
00830 I3=0
00840 REM IDSAT ITERATION
00850 I1=0
00860 G=C2*SQR(V1-V2+I1*R1)-1
00870 G=I1-C1*(G*(V1-V2+I1*R1)+C3)
00880 IF ROF(G,7)=0 GOTO 00920
00890 S=1-C1*R1*(1.5*C2*SQR(V1-V2+I1*R1)-1)
00900 I1=I1-G/S
00910 GOTO 00860
00920 REM END IDSAT ITERATION WITH IDSAT=I1
00930 FOR V3=V3(1) TO V3(2) STEP V3(3)
00940 IF V3=0 GOTO 01090
00950 V5=3*C3-V1+V2
00960 IF V3<V5+I1*R2 GOTO 00990
00970 I3=I1
00980 GOTO 01090
00990 REM START ID ITERATION
01000 I3=I1/2
01010 G=C2*((V3-I3*R2-V2+V1)**1.5-(V1-V2+I3*R1)**1.5)
01020 G=I3-C1*(V3-I3*(R1+R2)-G)
01030 IF ROF(G,7)=0 GOTO 01080
01040 S=1.5*R1*SQR(V1-V2+I3*R1)+1.5*R2*SQR(V3-I3*R2-V2+V1)
01050 S=1-C1*(-(R1+R2)+C2*S)
01060 I3=I3-G/S
01070 GOTO 01010
01080 REM END ID ITERATION WITH ID=I3
01090 PRINT USING"##.#",V2;
01100 PRINT"    ";
01110 PRINT USING"##.#",V3;
01120 PRINT"    ";
01130 PRINT USING"#.##^^^^",I3;
01140 PRINT" **";
01150 IF F=1 GOTO 01190
01160 PRINT
01170 F=1
01180 GOTO 01200
01190 F=2
01200 NEXT V3
01210 NEXT V2
01220 NEXT T
01230 END
READY.
```

PROGRAM PJFET

```
00100 READ H,K,Q1,D1,M1,M2
00110 DATA 6.6262E-34,1.38062E-23,1.60219E-19
00120 DATA 1.03594E-10,5.28345E-31,9.656134E-31
00130 PRINT"ENTER THE ACCEPTOR CONCENTRATION IN THE"
00140 PRINT"CHANNEL AND THE DONAR CONCENTRATION IN THE"
00150 PRINT"GATE (PER CUBIC CENTIMETER)."
00160 INPUT N1,N2
00170 IF N2>=50*N1 GOTO 00210
00180 PRINT"WARNING: THIS PROGRAM ASSUMES A ONE-SIDED "
00190 PRINT"JUNCTION AT THE GATE."
00200 GOTO 00130
00210 PRINT
00220 PRINT"ENTER THE LENGTH, WIDTH, AND DEPTH (JUNCTION"
00230 PRINT"TO JUNCTION) OF THE CHANNEL IN MICRONS."
00240 INPUT L1,Z,D2
00250 PRINT
00260 PRINT"ENTER THE STARTING AND ENDING TEMPERATURES"
00270 PRINT"IN DEGREES CENTIGRADE, FOLLOWED BY THE"
00280 PRINT"TEMPERATURE INCREMENT TO BE USED."
00290 INPUT T1,T2,T3
00300 PRINT
00310 PRINT"INPUT THE SOURCE AND DRAIN RESISTANCES AT ROOM TEMPERATURE."
00320 INPUT R1,R2
00330 N1=N1*1E6
00340 N2=N2*1E6
00350 L1=L1*1E-6
00360 Z=Z*1E-6
00370 D2=D2*1E-6
00380 T1=T1+273
00390 T2=T2+273
00400 T=300
00410 GOSUB 00690
00420 R3=R1*M3
00430 R4=R2*M3
00440 C2=4*SQR(2*D1/(Q1*N1))/(3*D2)
00450 C3=Q1*N1*D2*D2/(24*D1)
00460 PRINT
00470 PRINT"ENTER THE LOWER AND UPPER LIMITS AND "
00480 PRINT"THE STEP SIZE FOR THE GATE AND DRAIN"
00490 PRINT"VOLTAGES (INCLUDE THE SIGNS)."
00500 INPUT V2(1),V2(2),V2(3),V3(1),V3(2),V3(3)
00510 FOR T=T1 TO T2 STEP T3
00520 FOR X=1 TO 4
00530 PRINT
00540 NEXT X
00550 PRINT"**********************"
00560 PRINT"TEMPERATURE=";T-273;"C"
00570 V7=K*T/Q1
00580 E2=1.12-(T-300)*2.4E-4
00590 N5=12*(2*3.14159*M1*K*T/H**2)**1.5
00600 N6=2*(2*3.14159*M2*K*T/H**2)**1.5
00610 N3=SQR(N5*N6)*EXP(-E2/(2*V7))
00620 P1=V7*LOG((N1+SQR(N1*N1+4*N3*N3))/(2*N3))
00630 P2=V7*LOG((N2+SQR(N2*N2+4*N3*N3))/(2*N3))
00640 V1=P1+P2
00650 V9=-V1+Q1*N1*D2*D2/(8*D1)
00660 PRINT"TURN OFF VOLTAGE=";V9;"V"
00670 GOSUB 00690
```

```
00680 GOTO 00730
00690 M3=5.78678E17*T**1.5
00700 M3=M3/(N1*LOG((195006.3*T/N1**(1/3))**2+1))
00710 M3=1/(1/M3+1/(2.3414E5*T**(-2.7)))
00720 RETURN
00730 C1=Z*Q1*M3*N1*D2/L1
00740 R1=R3*N1/(M3*(N1+N3))
00750 R2=R4*N1/(M3*(N1+N3))
00760 PRINT
00770 PRINT
00780 PRINT" VGS     VDS       IDS    **";
00790 PRINT" VGS     VDS       IDS"
00800 F=1
00810 FOR V2=V2(1) TO V2(2) STEP V2(3)
00820 IF V2>V9 GOTO 01220
00830 I3=0
0040 REM IDSAT ITERATION
00850 I1=0
00860 G=(V1+V2+I1*R1)*(C2*SQR(V1+V2+I1*R1)-1)
00870 G=I1-C1*(G+C3)
00880 IF ROF(G,7)=0 GOTO 00920
00890 S=1-C1*R1*(1.5*C2*SQR(V1+V2+I1*R1)-1)
00900 I1=I1-G/S
00910 GOTO 00860
00920 REM END IDSAT ITERATION WITH IDSAT=I1
00930 FOR V3=V3(1) TO V3(2) STEP V3(3)
00940 IF V3=0 GOTO 01090
00950 V5=-3*C3+V1+V2
00960 IF V3>V5-I1*R2 GOTO 00990
00970 I3=I1
00980 GOTO 01090
00990 REM START ID ITERATION
01000 I3=I1/2
01010 G=(-V3-I3*R2+V1+V2)**1.5-(V1+V2+I3*R1)**1.5
01020 G=I3-C1*(-V3-I3*(R1+R2)-C2*G)
01030 IF ROF(G,7)=0 GOTO 01080
01040 S=R2*SQR(-V3-I3*R2+V1+V2)+R1*SQR(V1+V2+I3*R1)
01050 S=1-C1*(-(R1+R2)+1.5*C2*S)
01060 I3=I1-G/S
01070 GOTO 01010
01080 REM END ID ITERATION WITH ID=I3
01090 PRINT USING"##.#",V2;
01100 PRINT"    ";
01110 PRINT USING"##.#",V3;
01120 PRINT"    ";
01130 PRINT USING"#.##^^^^",I3;
01140 PRINT" **";
01150 IF F=1 GOTO 01190
01160 PRINT
01170 F=1
01180 GOTO 01200
01190 F=2
01200 NEXT V3
01210 NEXT V2
01220 NEXT T
01230 END
READY.
```

REFERENCES

1. SAND75-0608, "Report of the Geophysical Measurements in Geothermal Wells Workshop," L. E. Baker, R. P. Baker, R. L. Hughen (Eds.), available through NTIS.

2. Wolf, H. F., Silicon Semiconductor Data, 1969.

3. LA-6339-MS, "A New Electronic Gain Device for High-Temperature Applications," J. B. McCormick, S. W. Depp, D. J. Hamilton, W. J. Kerwin, Los Alamos, 1976.

4. SAND76-0611, "275°C Microcircuitry: Resistor, Capacitors, Conductor, Substrates, and Bonding," D. W. Palmer, G. L. Knauss, 1976, available through NTIS.

5. Grove, A. S., Physics and Technology of Semiconductor Devices, John Wiley, 1967.

6. Sze, S. M., Physics of Semiconductor Devices, Wiley-Interscience, 1969, p. 518.

7. Pearson, G. L. and J. Bardeen, "Electrical Properties of Pure Silicon and Silicon Alloys Containing Boron and Phosphorus," Phys. Rev. 75, 865 (1949).

8. Leistiko, O., A. S. Grove, and C. T. Sah, "Electron and Hole Mobilities in Inversion Layers on Thermally Oxidized Silicon Surfaces," IEEE Trans. on Electron Devices, May 1965, p. 248.

9. Schrieffer, "Effective Carrier Mobility in Surface-Space Charge Layers," Phys. Rev. 97, 641 (1955).

10. Bullis, W. M., "Properties of Gold in Silicon," Solid-State Electronics, 9, 143 (1966).

11. Deal, B. E., M. Sklas, A. S. Grove, and E. H. Snow, "Characteristics of the Surface State Charge (Q_{ss}) of Thermally Oxidized Silicon," J. Electrochemical Society 114, 266 (1967).

12. Semiconductor Data Library - Chips, Motorola Inc., 1976, p. 3-27.

13. Shockley, W., "A Unipolar 'Field Effect' Transistor," Proc. IRE 40, 1365 (1952).

14. Richer, I., "Basic Limits on the Properties of Field Effect Transistors," Solid State Electronics, 6, 539 (1963).

15. Middlebrook, R. D. and I. Richer, "Limits on the Power Law Exponent for Field Effect Transistor Transfer Characteristics," Solid State Electronics, 6, 542 (1963).

16. Semiconductor Data Library/Chips, Motorola Inc., 1976, p. 3-29.

17. Sze, S. M., G. Gibbons, "Effect of Junction Curvature on Breakdown Voltage in Semiconductors," Solid State Electronics, 9 (1966).

18. Leistiko, O., Jr. and A. S. Grove, "Breakdown of Planar Silicon Junctions," Solid State Electronics, 9, 847 (1966).

19. Prince, J. L., Final report Sandia Contract 06-4336, "Investigation of the Performance of Semiconductor Devices at Elevated Temperatures," 1977.

20. This transistor was first brought to our attention by Allan MacPherson of Naval Research Lab.

21. Colliver, D. J., Compound Semiconductor Technology, Artech House, 1976.

22. "Double-Oxide-Layer Process to Make GaAs More Useful," News item in Electronic Design, 13, June 21, 1977, p. 111.

23. McCaldin, J. O., T. C. McGill, and C. A. Mead, "Correlation for III-V and II-Vl Semiconductors of the Au Schottky Barrier Energy with Anion Electronegativity," Phys. Rev. Let., 36, No. 1, Jan. 5, 1976, p. 56-58.

24. Bushmire, D. W., "Gold Aluminum Interconnect Stability on Thin Film Hybrid Microcircuit Substrates," SAND76-0306, 1976, available through NTIS.

25. In particular, modified fritless gold, DuPont 9910, AVX 3520, and Thick Film Systems A328.

26. Campisano, S. U., et.al., "Kinetics of Phase Formation in Au-Al Thin Film, Philosophy Magazine, 33, p. 914.

27. The final design for the metal diffusion pads were created by F. P. Ganyard and F. G. Yost, Sandia. Design for the silicon pad came from D. W. Palmer. All of Div. 2151, Sandia Labs.

28. Pactel Corporation, Unit K, 755 Lakefield Rd., West Lake Village, CA 91361.

29. For example, Kelox refractory cement by International Materials Inc.

Acknowledgments

This report would not have been possible without the technical advice of Helen Finley and Floyd Ganyard, the graphics of Peggy Bonn, and the manuscripting of Barbra Ford.

DISTRIBUTION:

Dr. William Brigham, Jr.
Stanford University
Petroleum Engineering Dept.
Stanford, CA 94305

Donald A. Campbell
Republic Geothermal, Inc.
11823 E. Slauson Ave., Suite 1
Santa Fe Springs, CA 90670

Lyman M. Edwards
Petroleum & Minerals Group
Dresser Industries, Inc.
601 Jefferson/Dresser Tower
P. O. Box 6504
Houston, TX 77005

Donald G. Hill
Chevron Oil Field Research Co.
P. O. Box 446
La Habra, CA 90631

Dr. George V. Keller
Colorado School of Mines
Golden, CO 80401

Dr. W. E. Kenyon
Schlumberger-Doll Research Center
P. O. Box 307
Ridgefield, CT 06877

W. Scott Keys
Geological Survey
Building 25
Denver Federal Center
Denver, CO 80225

Jack H. Howard
Lawrence Berkeley Laboratory
One Cyclotron Road
Building 90, Room 2071
Berkeley, CA 94720

Mark Matthews
Mail Stop 573
Los Alamos Scientific Lab
Los Alamos, NM 87544

Robert C. Ransom
Union Oil Research Center
P. O. Box 76
Brea, CA 92621

John Rowley
Mail Stop 573
Los Alamos Scientific Lab
Los Alamos, NM 87544

Werner Schwartz
Lawrence Berkeley Lab
One Cyclotron Road
Building 90, Room 2071
Berkeley, CA 94720

Wally Sowder
Phillips Petroleum
Natural Resources Division
P. O. Box 752
Delmar, CA 92014

Dr. D. Roger Wall
Geothermal Resources Division
Aminoil USA, Inc.
1250 Coddingtown Center
P. O. Box 11239
Santa Rosa, CA 95406

B. F. Wilson
Research & Engineering
Dresser Atlas
P. O. Box 1407
Houston, TX 77001

Carl Zimmerman
Halliburton Services
P. O. Box 1431
Duncan, OK 73533

Larry Ball
ERDA
Division of Geothermal Energy
Washington, D. C. 20545

Mel Spitz
Circuit Technology
160 Smith Street
Farmingdale, NY 11735

Jack Burgen
Gearhart-Owen International
P. O. Box 1258
Fort Worth, Texas 76101

Cliff Carwile
ERDA
Division of Geothermal Energy
Washington, D. C. 20545

Carl Gatlin
Petroleum Engineering Dept.
Stanford University
Stanford, CA 94305

Mike Lamers
Measurement Analysis Corporation
36 Melaga Cove Plaza
Palos Verdes Estates, CA 90274

Bruce Draper (10)
228A Marshall St.
Princeton, NJ 08540

R. G. McCain
Geotechnical Division
Stone & Webster Engineering Corp.
Greenwood Plaza
Box 5406
Denver, CO 80217

R. K. Kirschman
Jet Propulsion Laboratory
157-507
4800 Oak Grove Dr.
Pasadena, CA 91103

John Jones
Hewlett Packard
1501 Page Mill Road
Palo Alto, CA 94304

Ed Basham
Gearhart Owens Industries, Inc.
P. O. Box 1936
Fort Worth, TX 76101

Steve Decker
E44/015
IBM
Monterey and Cottle Roads
San Jose, CA 95193

Harris Notarys
63-37
Caltech
Pasadena, CA 91125

R. D. Kelly
SDC - Mechanics Research Inc.
2500 Colorado Avenue
Santa Monica, CA 90406

Charles P. Morse
SDC - Mechanics Research Inc.
2500 Colorado Avenue
Santa Monica, CA 90406

J. C. Robertson
Raytheon Co.
430 Boston Post Road
Wayland, MA 01778

Morris Eisenberg
Electro-Chimica
2485 Charleston Rd.
Mt. View, CA 94040

Phillip Martin
P. O. Box 1635
Whittier, CA 90609

R. H. Mastin
Seismic Engineering Co.
1133 Empire Central
P. O. Box 47045
Dallas, TX 75247

James C. Wood
Seismic Engineering Co.
1133 Empire Central
P. O. Box 47045
Dallas, TX 75247

P. M. Woodley
Micropac Industries, Inc.
905 E. Walnut St.
Garland, TX 75040

Dr. Bill Kent
Sperry Research Center
North Road
Sudbury, MA 01776

Prof. W. M. Portnoy
Dept. of Electrical Engineering
Texas Tech University
Lubbock, TX

Jan L. Arps
Arps Consultants
Meadows Building
Dallas, TX 75206

R. C. Kilpatrick
Haskell Shapiro, Consulting Engineers
3500 East Coast Highway
Corona Del Mar, CA 92625

G. Boesen
Borg-Warner Corporation
Roy C. Ingersoll Research Center
Wolf and Algonquin Roads
Des Plaines, Illinois

Allan MacPherson
5210.2
Naval Research Lab
Washington, DC 20930

Sam Horowitz
E. I. DuPont
Electronic Materials Division
Niagara Falls, NY 14302

J. T. DeLorenzo
Oak Ridge National Lab
P. O. Box X
Oak Ridge, TN 37830

Daniel L. deKock
Physics and Engineering Lab
DSIP
Private Bag, Lower Hutt, New Zealand

B. Laughlin
Los Alamos Scientific Lab
Los Alamos, NM 87544

Salvadore V. Caruso
EC42 Building 4487
NASA
Marshall Space Flight Center
Alabama 35812

C. W. Millis
Dresser Atlas Division
601 Jefferson
Dresser Tower, 30th Floor
P. O. Box 6504
Houston, TX 77005

R. Mink
ERDA
Division of Geothermal Energy
Washington, D. C. 20545

E. D. Percifield
Schlumberger-Doll Research Center
P. O. Box 307
Ridgefield, Connecticut 06877

Dr. John L. Prince
Department of ECE
Clemson University
Clemson, South Carolina 29631

Prof. H. J. Ramey, Jr.
Petroleum Engineering Dept.
Stanford University
Stanford, CA 94305

Charles Swift
Chevron Resources
P. O. Box 3722
San Francisco, CA 94119

Mr. A. H. Youmans
Dresser Atlas Division
Dresser Industries, Inc.
P. O. Box 1407
Houston, TX 77001

Mr. G. L. Marquis
Dresser Atlas Division
Dresser Industries, Inc.
P. O. Box 1407
Houston, TX 77001

Dr. J. P. Hauser
Geophysical Instrumentation Sys.
Westinghouse Electric Corp.
5441 Western Ave.
Boulder, CO 80301

Dr. D. K. Steinman
Mineral Exploration Technology
RT Corporation
7650 Convoy Court
Box 80817
San Diego, CA 92138

Mr. James W. Wonn
Sonic Technology
Westinghouse Electric Corporation
Pittsburgh, PA 15235

Mr. R. F. Kehrman
Geophysical Instrumentation Sys.
Westinghouse Electric Corporation
Boulder, CO 80301

Dr. Robert Kratz
Systems Science and Software
P. O. Box 1620
La Jolla, CA 92037

Mr. R. K. Swanson
Southwest Research Institute
8500 Culebra Road
P. O. Box 28510
San Antonio, TX 78284

Mr. H. F. Poppendiek
Geoscience Ltd.
410 South Sedros Avenue
Solana Beach, CA 92075

Mr. J. D. Starnes
Gearhart-Owen Industries, Inc.
P. O. Box 1936
Fort Worth, Texas

Dr. Ali Daneshy
Fracturing Section
Halliburton Services Res. Center
Duncan, OK 73553

Mr. G. J. Crawford
Birdwell, Div. of Seismograph
Services Corp.
6200 E. 41st Street
Tulsa, OK 74102

Mr. Ron Anderson
Schlumberger Well Services
5000 Gulf Freeway
Houston, TX

Mr. John M. Jones
Schlumberger Well Services
5000 Gulf Freeway
Houston, TX

Bob Cowan
E-2
Los Alamos Labs
Los Alamos, NM 87544

R. A. Nelson
Radio Physics Lab
SRI International
333 Ravenswood Ave.
Menlo Park, CA 94025

F. L. Johnson
Electrocube
1710 South Del Mar Ave.
San Gabriel, CA 91776

Howard Imhoff
Cermalloy Bala Electronic Corp.
W. Conshohocken, PA 19428

Prof. Raymond
Electronic Engineering Lab
University of Arizona
Tucson, Arizona 85721

W. J. Kerwin
Electronic Engineering Lab
University of Arizona
Tucson, Arizona 85721

Run Han Wang
MS 429
Los Alamos Scientific Lab
Los Alamos, NM 87544

Del Wilde
MS 429
Los Alamos Scientific Lab
Los Alamos, NM 87545

Jack Nachamkin
MS 429
Los Alamos Scientific Lab
Los Alamos, NM 87545

J. Waggoner
Schlumberger Well Services
5000 Gulf Freeway
P. O. Box 2175
Houston, TX 77001

Al Hess
U. S. Geological Survey
Box 25046
Denver Federal Center
Denver, CO 80225

Jim Licare
MC: DF03
Electronic Device Div.
3370 Mira Loma Ave.
Anaheim, CA 92803

D. J. Hamilton
University of Arizona
Tucson, Arizona 85721

Alan Adler
Acurex
485 Clyde Ave.
Mt. View, CA 94042

J. B. McCormick
MS 429
Los Alamos Scientific Lab
Los Alamos, NM 87544

Mr. Ed Day
Systems Science and Software
P. O. Box 1620
La Jolla, CA 92037

Jim Leftwich
Geophysical Communications
410 S. Glendora Ave.
Glendora, CA 91740

Leonard Jaffe
MS 183-501
Jet Propulsion Labs
California Institute of Technology
4800 Oak Grove Dr.
Pasadena, CA 91103

2151	R. C. Heckman	(44)
2151	D. W. Palmer	(10)
2151	K. R. White	(10)
2155	J. D. McBrayer	(10)
5736	A. F. Veneruso	(100)
8266	E. A. Aas	(1)
3141	Tech. Library	(5)
3151	W. L. Garner	(3)
DOE/TIC	(R. P. Campbell, 3172-3)	(25)